Quantime - A miniature cesium atomic clock using CPT technique for telecom applications

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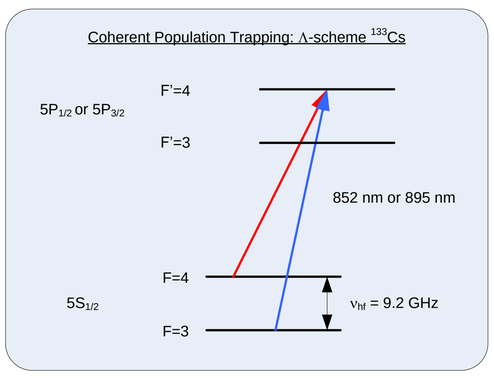
Abstract – the Quantime project aims at developing a miniature atomic clock suited for the telecom market, requiring a wide operating temperature range (from -40 to +85°C), and a low production cost. The CPT (Coherent Population Trapping) technique for atomic interrogation is used for miniaturization and low power consumption. In the first phase of the project, the clock architecture was chosen, and the main sub-systems were developed. A clock breadboarding demonstrator was assembled and the measured Allan deviation of $1E^{-11}$ at 400 s confirms the operation of all the sub-systems.

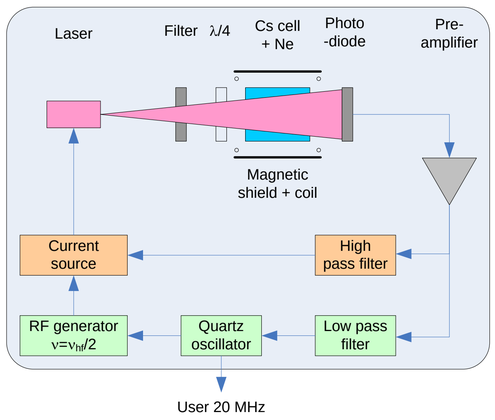
Clock Architecture & Specs

Physical operation mode



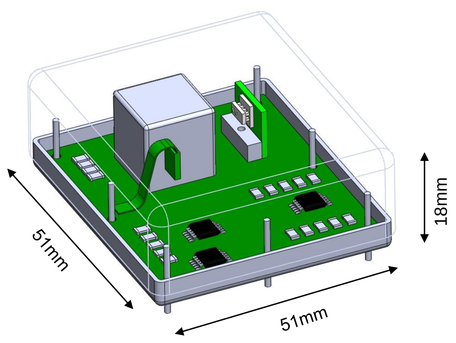
- 3-level system with 2 phase-coherent laser frequencies obtained by modulating a single laser at 4.6 GHz.
- The resulting atomic dark state produces a measurable light absorption drop.

Implementation



Main regulation loops:
- Laser thermal stability
- Cs cell thermal stability
- Laser optical frequency stability
- Quartz oscillator frequency stability

Realization

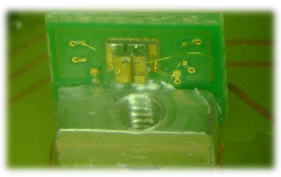


Standard case used in OCXO

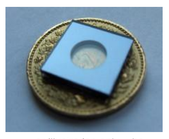
Product specifications

- Time stability: 1 µs/day
- Power consumption: 2W
- Operating temperature range: -40 to +85°C
- Supply: single 3.3 Volt
- Size: 51x51x18 mm

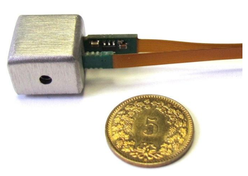
Developed sub-systems



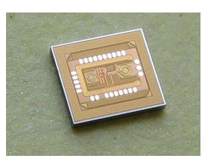
Laser Assembly
- VCSEL
- TEC
- 4.6 GHz RF transmission

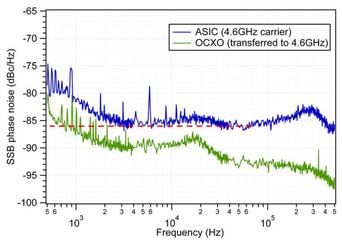


For illustration only. The project cell is confidential and cannot be displayed here

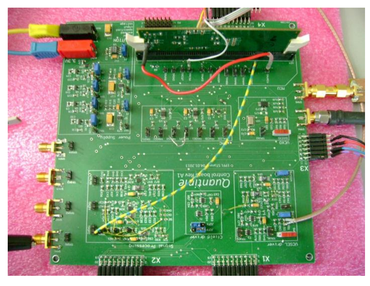


Cell Assembly
- Cs micromachined cell
- Photodetector
- C-field coil
- Magnetic Shielding





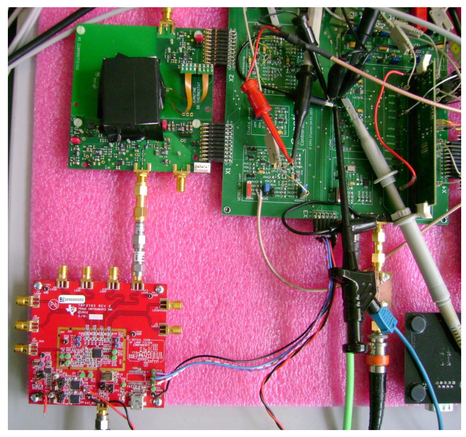
RF synthesizer ASIC
- PN: -86 dBc/Hz @ 5 kHz
- Rel. Freq. Resolution: 10^{-12}
- Single-chip, 15 mW



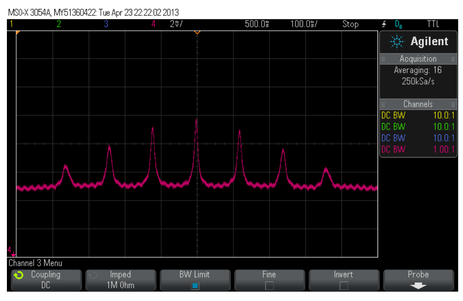
Control electronics
- Commercial components
- All digital control loops
- Debugging capabilities

Thermal control
- Digitally controlled laser and cell temperature controllers.
- Support for physics

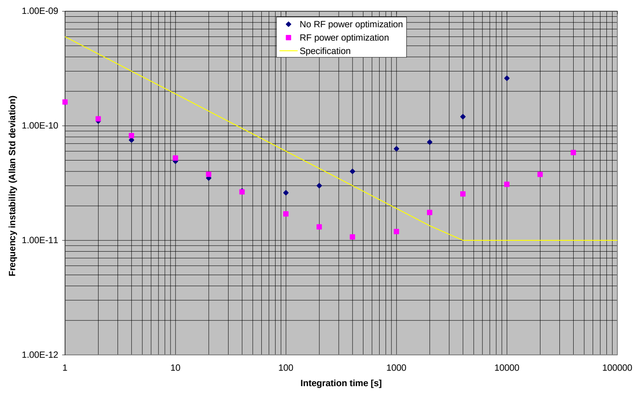
Prototype and test results



Breadboarding demonstrator
- Commercial single-chip RF synthesizer used.
- Full system parameter control and monitoring via PC



Typical CPT signals
- 7 Zeeman levels
- Excellent shape & SNR



Measured frequency stability at 20 MHz out
- Excellent short-term stability of 1.6^{E-10} at 1 s.
- Down to 1^{E-11} at 400 s.
- Long-term to be improved by better thermal and laser operation.

Conclusion and perspectives

The first phase of the project (10 months) allowed to design, fabricate and test all the clock sub-systems. A complete clock was assembled and successfully tested, meeting the specifications.
During the coming phase 2 (8 months), the clock will be down-sized to its targeted dimensions and will be packaged in the final case.