An Energy Efficient Power Converter for Zero Power Wearable Devices

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PAR

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ای برادر تو همان اندیشه‌ای ما بقی تو استخوان و ریشه‌ای

-مولانا

Oh brother, you are nothing but your thoughts
The rest of you is merely skin and bones

-Rumi 1207-1273, translated by B. Gooch

تقدیم به مادر و پدر عزیزم مهرخ زکیخانی و ابوالفضل عطائی آشتیانی

To my beloved mother, Mahrokh, and my beloved father, Abolfazl

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Neuchâtel, 21 October 2017 Milad Ataei Ashtiani

Abstract

Early diagnosis of Alzheimer's and epilepsy requires monitoring a subject's development of symptoms through electroencephalography (EEG) signals over long periods. Wearable devices enable convenient monitoring of biosignals, unlike complex and costly hospital equipment. The key to achieving a fit and forgettable wearable device is to increase its operating cycle and decrease its size and weight. Instead of batteries, which limit the life cycle of electronic devices and set their form factor, ambient energy can be employed as an alternative energy source. Body heat and environmental light can power wearable devices through energy-scavenging technologies. The energy available to harvest is limited, and therefore the harvester transducers should be tailored according to on the application and the sensor placement. This leaves a wide variety of transducers with an extensive range of impedances and voltages.

To realize an autonomous wearable device, the power converter energy harvester, which is responsible for transferring the transducer's low-voltage energy and providing it as a high-potential-energy source, has to be very efficient and maintain its efficiency despite potential transducer replacement or variations in environmental conditions. This thesis presents a detailed design of an efficient integrated power converter for use in an autonomous wearable device. The design is based on the examination of both power losses and power transfer in the power converter. The efficiency bound of the converter is derived from the specifications of its transducer. The inflexible converter parameters are optimized and fixed with regard to the worst-case efficiency scenario. The tuning ranges for the reconfigurable parameters are extracted to keep the converter efficient with variations in the transducer specifications. With the efficient design and the manual tuning of the reconfigurable parameters, the converter can work optimally with different types of transducers, and keeps its efficiency in the conversion of low voltages from the harvesters. Measurements of the designed converter demonstrate an efficiency of higher than 50%

and 70% with two different transducers having an open-circuit voltage as low as 20 mV and 100 mV, respectively.

The power converter should be able to reconfigure itself without manual tunings to keep its efficiency despite changes in the harvesters' specifications. The second portion of this dissertation addresses this issue with a proposed design methodology to implement a control section. The control section adjusts the converter's reconfigurable parameters by examining the power transfer and loss and through concurrent closed loops. The reconfigurable parameters here are the converter's switching durations. The concurrent loops working together raise a serious concern regarding stability. The system is designed and analyzed in the time domain with the state-space averaging (SSA) model to address the stability issue. The ultra-low-power control section obtained from the SSA model estimates the power and loss with a reasonable accuracy, and adjusts the timings in a stable manner. The entire control section consumes only 30 nW dynamic power at 10 kHz. The control section tunes the converter's speed or its working frequency depending on the available power. The frequency clocks the entire architecture, which is designed asynchronously; therefore, the power consumption of the system depends on the power available from the transducer. Low-power circuits and techniques are introduced and employed in the sub-circuits to realize the ultra-low-power converter. The system is implemented using 0.18 μm CMOS technology. For an input as low as 7 mV, the converter is not only functional but also has an efficiency of more than 40%. The efficiency can reach 70% with an input voltage of 50 mV. The system operates in a range of just a few of millivolts to half a volt with ample efficiencies. It can work at an optimal point with different transducers and environmental conditions. This work does not focus on the cold start, and it is assumed that the output energy storage has some initial charge during start-up. The prior-art has addressed the low-voltage start-up issue using different methods.

Keywords: Analog design, application specific, autonomous system, chopper, CMOS, DC-DC converter, digital control oscillator, dynamic loss, efficiency, energy harvester, energy scavenging, frequency tuning, inductor-based, integrated circuit, low-power, low-voltage, medical device, mixed-signal, phase tuning, photovoltaic cell, power converter, power electronics, power transfer, reconfigurable, solar cell, state space, static loss, thermoelectric generator, ultra-low-power, ultra-low-voltage, wearable device, zero-power

Résumé

Le diagnostic précoce de la maladie d'Alzheimer et de l'épilepsie nécessite une surveillance sur de longues périodes du développement des symptômes par électroencéphalographie (EEG). L'utilisation de dispositifs de mesures portables permet la surveillance de signaux biologiques en libérant le patient d'une hospitalisation et de l'utilisation d'équipements complexes et coûteux. Les clés du succès sont l'augmentation des cycles d'opération, la miniaturisation et la diminution du poids. Au lieu de batteries, qui limitent la durée de vie et influencent grandement la taille du dispositif, l'énergie ambiante peut être utilisée comme source. Grâce aux technologies de récupération d'énergie, il est envisageable d'utiliser la chaleur corporelle et la lumière ambiante pour alimenter de tels dispositifs. L'énergie à disposition étant limitée, sa production doit être adaptée au positionnement des capteurs et à l'application visée. Le choix des générateurs d'énergie est tel qu'il débouche sur une grande gamme d'impédances et de tensions différentes.

Pour réaliser un dispositif portable autonome, il faut un convertisseur de puissance chargé de transformer l'énergie produite à basse tension par un générateur en une source d'énergie utilisable par une électronique. Ce convertisseur de puissance doit être efficace et en mesure de maintenir son efficacité pour différents types de générateurs et pour des variations de conditions environnementales. Cette thèse présente la conception d'un tel convertisseur intégré. Cette conception se base sur l'examen des pertes et de l'efficacité du transfert de puissance. La limite d'efficacité est dérivée des spécifications du générateur. Les paramètres du convertisseur sont optimisés et fixés en fonction du scénario d'efficacité le plus défavorable. Les plages de régulation du convertisseur ont été définies de manière à en assurer la plus haute efficacité. En optimisant l'efficacité et l'utilisation de paramètres de configuration externes, le convertisseur peut fonctionner de manière optimale avec différents types de générateurs tout en maintenant son efficacité même en présence de basses tensions. Les mesures du convertisseur montrent que des efficacités supérieures à 50%

et 70% sont obtenues avec deux générateurs différents dont la tension en circuit ouvert sont respectivement de 20 mV et 100 mV.

Pour maintenir son efficacité malgré le changement de spécifications des générateurs, un convertisseur de puissance doit pouvoir s'auto configurer, c'est-à-dire ne pas avoir recours à des réglages externes. La deuxième partie de cette thèse traite de cette question en proposant une méthodologie de conception visant à mettre en œuvre une régulation automatique. Cette régulation ajuste les paramètres reconfigurables en surveillant le transfert et la perte de puissance au travers de boucles concurrentes de contrôle. Les paramètres réglables sont les durées de commutation. Les boucles de contrôles concurrentes posent. Pour répondre à cette préoccupation, le système est conçu et analysé dans le domaine temporel avec un modèle de moyennes d'espace-état (state-space averaging SSA). La régulation obtenue grâce à ce modèle (SSA) fonctionne à très faible consommation en estimant la puissance et les pertes avec une précision raisonnable et ajuste le diagramme temporel d'une manière stable. Le circuit de régulation obtenu ne consomme que 30 nW à 10 kHz. Il régule la vitesse du convertisseur, c'est-à-dire sa fréquence de travail en fonction de la puissance disponible. Celle-ci cadence toute l'architecture qui fonctionne de manière asynchrone. La consommation du système dépend donc de la puissance disponible fournie par le générateur. Des circuits faible consommation et des techniques particulières sont introduits et utilisés dans les sous-circuits afin d'atteindre une consommation ultra-basse. Le système a été implémenté en utilisant une technologie CMOS à 0.18 µm. Avec une tension d'entrée de seulement 7 mV, le convertisseur est fonctionnel avec un rendement de plus de 40%. Le rendement peut atteindre 70% avec une tension d'entrée de 50 mV. Le circuit fonctionne à partir de quelques millivolts jusqu'à un demi-volt. Il adapte son fonctionnement de façon optimal pour différents générateurs et pour des conditions environnementales qui varient. Pour démarrer, le circuit a besoin d'une charge initiale à la sortie. L'art antérieur abordant déjà la problématique du « démarrage à froid », ce travail n'en traite pas.

Mots-clés: Conception analogique, application spécifique, système autonome, découpage, CMOS, convertisseur DC-DC, oscillateur numérique, pertes dynamiques, rendement, récupérateur d'énergie, récupération d'énergie, accord de fréquence, à base d'inductance, circuit intégré, basse consommation, faible tension, dispositif médical, signal mixte, accord de phase, cellule photovoltaïque, convertisseur de puissance, électronique de puissance, transfert de puissance, reconfigurable, cellule solaire, espace-état, pertes statiques, générateur thermoélectrique, ultra-basse puissance, ultra-basse tension, dispositif portable, zéro puissance.zero-power

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1 Introduction

From the emergence of mainframes in the late 1950s, which belonged to the central computing processing class, to the present day's internet of things (IoT) or distributed computing class, semiconductor technology has advanced and evolved in two directions: device performance has been continuously enhanced inside a computing class while costs have been kept constant as, at the same time, devices have evolved from one class to another every decade with reduced costs and an unchanged performance. The former advancement was predicted by Moore's Law[1] [1, 2], the latter by Bell's Law [3]. Figure 1-1 illustrates the semiconductor industry's advancement according to Moore and Bell's Laws [4-6]. Central computing systems like mainframes have evolved in recent decades, but their market share has shrunk. The demand for small, high-volume, and cheap devices has gradually shifted the semiconductor industry from improving integration and complexity towards the development of lower-cost sensor nodes by keeping or even decreasing device performance. The exponential trends of Moore's Law are slowing down [7], and the semiconductor industry is pushing to develop small form-factor and low-cost devices more than ever before.

Wearable sensors, wireless sensors, and implantable devices aimed at medical monitoring [8-10] and environmental monitoring [11-13] of hazardous environments [14], automotive [15], and smart buildings [16, 17] are the main emerging applications of the new computing class. Wearable sensors can significantly benefit the long-term monitoring of biosignals. However, today's sensors invade the user's normal life as their platforms require removal, replacement, or recharging of the battery. This can be detrimental to medical applications, since clinicians need to monitor the psychological state of patients without any interruption. Moreover, the size of the sensors should be miniaturized to millimeter scales and their weight should

[1] Gordon Moore predicated exponential improvements in complexity and cost per component in his first paper.

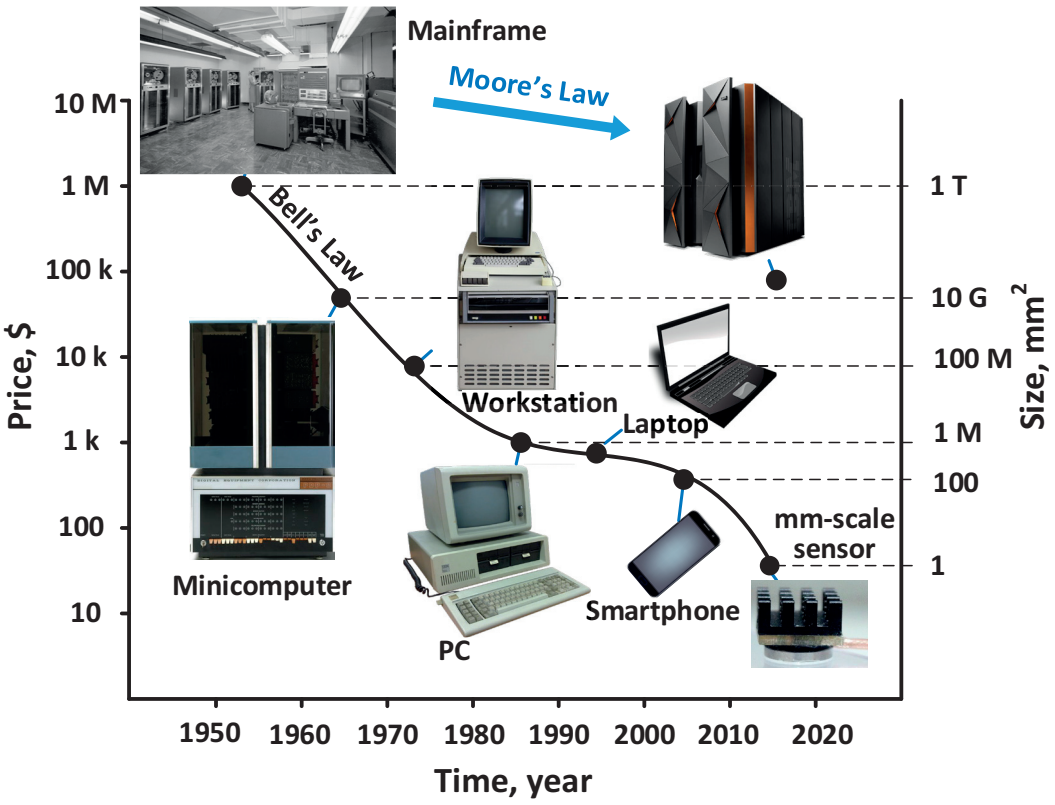
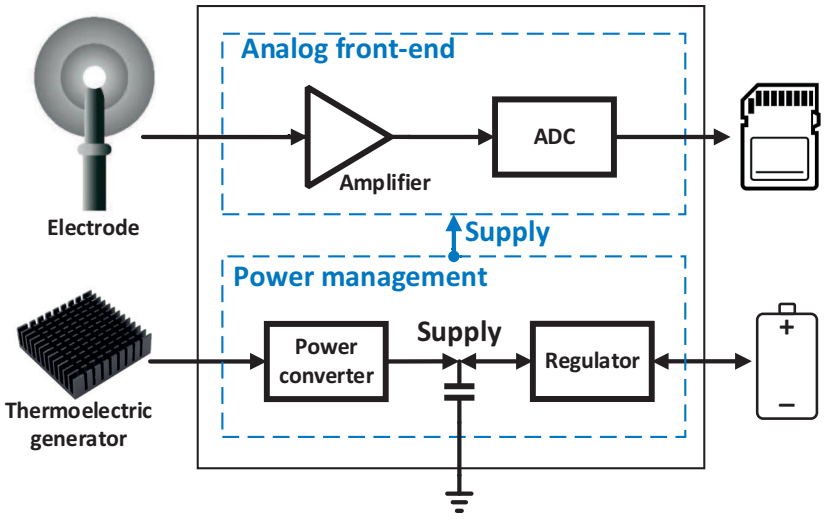


Figure 1-1: Evolution of computing devices [4-6] from mainframes to millimeter-scale sensors.

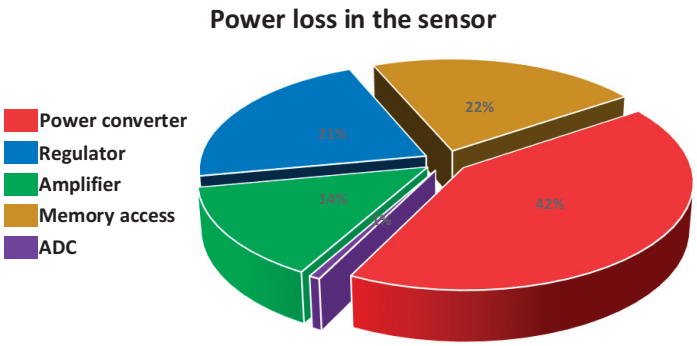
be reduced to lower costs and make the device more user-friendly. However, the size of integrated electronic systems is often limited and set by their batteries.

To address these issues, the autonomy of the systems has to be increased while smaller form-factor batteries are used in the systems. This may not be possible unless ultra-low-power circuits are employed in the devices. Low-power circuit design has made great progress in recent years. The power consumption of electronic building blocks is steadily decreasing by reducing unnecessary performance for their intended applications. Recent innovative advances include a 0.24 μW Bluetooth low-energy wake-up receiver [18], 600 μW ultra-wideband transceiver [19], 0.7 μW amplifier [20], 2.8 μW chopper amplifier [21], 0.5 μW analog to digital converter (ADC) [22], and 2.7 μW microcontroller [23]. The development of these low-power integrated circuits benefits wearable sensors by making them more convenient for long-term monitoring.

When battery replacement is not an option or is too costly, it becomes necessary to look for alternative sources of energy. One solution is to power blocks by harvesting environmental energy or ambient energy through energy-scavenging technologies. Energy harvesting is an emerging research area in integrated systems.



a)



b)

Figure 1-2: a) Block diagram of a medical wearable sensor node with a low-voltage TEG harvester, and b) the normalized power loss of each block in the node with the harvester.

Since energy harvesters can provide a lifetime of energy even under unyielding constraints, they are useful for applications such as medical devices that demand a relatively small amount of power for a long time. The 'zero power' medical devices approach can improve human parameters monitoring thanks to new circuits and architectures that will drastically lower power needs; their small needed energy can then be harvested directly from natural sources. This makes it possible to implement low-cost systems that minimize their impact on the everyday life of patients.

Body heat can be a source for energy harvesting when autonomous medical devices are placed directly on human skin. In this case, miniaturized thermoelectric generators (TEGs) are used as transducers. Small-scale photovoltaic cells (PV) can

be used when a wearable device is exposed to sufficient environmental light intensity. The output voltages of these transducers change according to their environmental conditions and have been shown to be very small [24, 25]. The power converter is then responsible for transferring such infinite but unreliable low potential energy from the harvesters and providing it as a high-potential-energy and reliable power source for the application.

A system-level schematic of a medical sensor node supplied by a low-voltage energy harvester is shown in Figure 1-2 a). Two main sections can shape the sensor node: the analog front-end, which is responsible for conditioning and digitizing biosignals to prepare them to be stored in or transferred from the sensor node, and the power management unit, which provides a regulated supply for the sensor node. In the power management section, the power converter transfers energy from the transducer to a high-potential-energy storage element as the supply node. The switching regulator transfers extra charges from the supply to a small rechargeable battery to regulate the supply and to store additional energy. When there is not sufficient energy available from the harvest, or during a system cold-start when the supply storage is empty, the switching regulator has to charge the storage from the battery. The normalized estimated power consumption or power loss of each block is illustrated in the pie chart in Figure 1-2 b). The data were extracted from the recent literature and the practical results obtained in this work. One of the main bottlenecks in the sensor node is the power loss of the energy harvesting power converter. Therefore, the sources of this loss have to be identified, and a solution has to be proposed to mitigate this bottleneck and enhance the power converter efficiency.

1.1 Thesis goal

To find the sources of the power converter's losses and the factors limiting the power transfer, the constraints imposed by the sensor node have to be quantified. Therefore, the sensor node should be designed at the system level to observe its power-consumption requirements. The power converter loss must later be studied to understand the challenges in improving the converter's efficiency. Then, it is possible to propose methods to confront those challenges to optimize the converter. After that, since the harvester can be replaced due to sensor placement, the converter should be designed to with different types of harvesters without any manual adjustment. Therefore, the converter should tune and configure itself to keep its optimum point despite changes in the transducer specifications. To address these goals, this thesis is organized into chapters as follows.

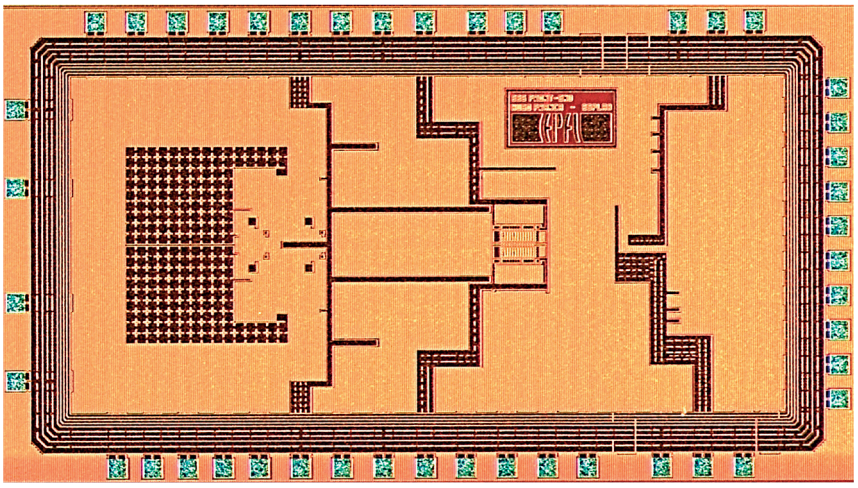


Figure 1-3: Microchip of the analog front-end.

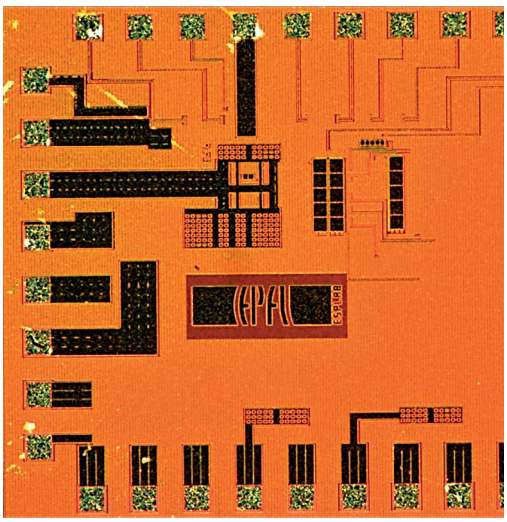
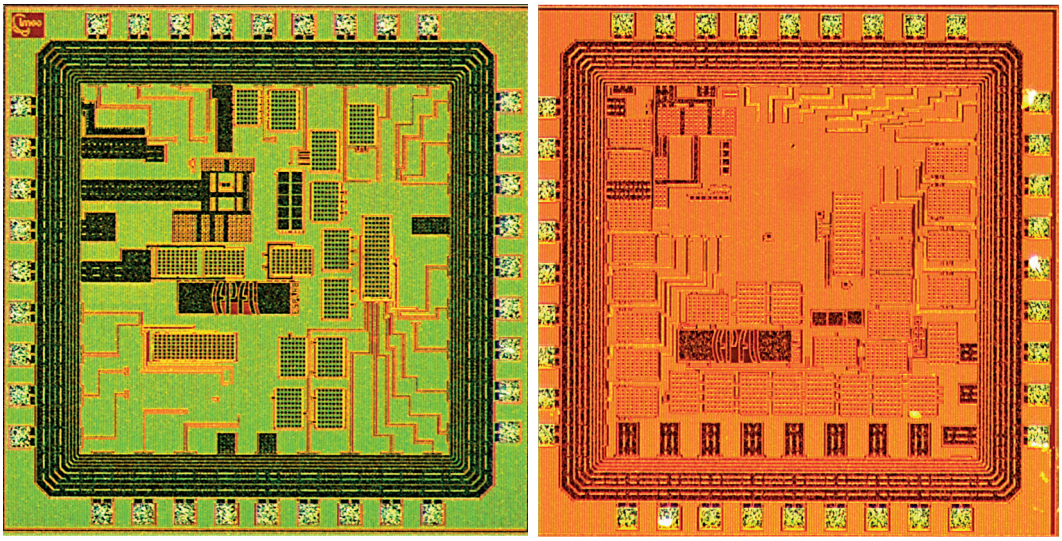


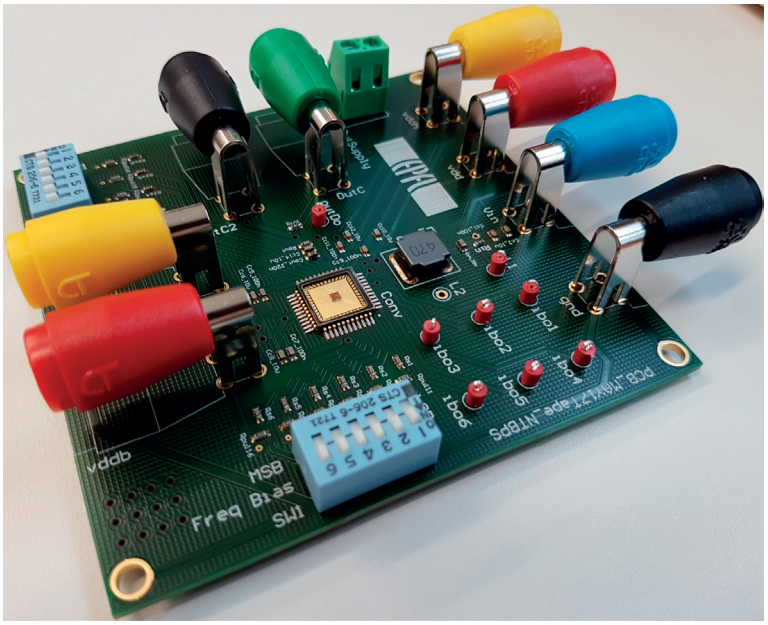
Figure 1-4: Microchip of the designed efficient converter.

Chapter two

In this chapter, the targeted application of the wearable sensor node is introduced. The building blocks of the node are presented. Its analog front-end is designed to study the feasibility of the sensor. A microchip of the fabricated front-end is shown in Figure 1-3. The actual requirements of the power converter are obtained with the measurements of the designed front-end. Then, the literature related to converters with similar requirements is reviewed to examine the state of the art in designing an efficient converter.



a) b)



c)

Figure 1-5: Microchips of the self-reconfigurable converters with a) a low-complexity and b) a moderate-complexity control system, and c) the converters' test board.

Chapter three

The losses and limitations in the power transfer in a converter are examined in this chapter. A design approach based on this examination is suggested to implement an optimal integrated power converter. Inflexible converter parameters are

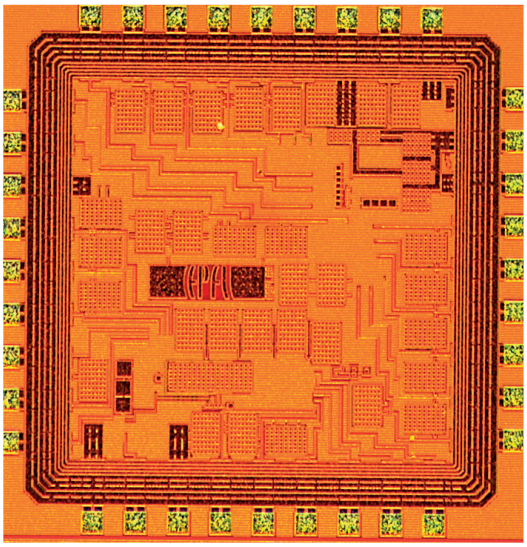


Figure 1-6: Microchip of the stand-alone converters' main blocks.

designed and fixed, and the tuning ranges for the converter's timings are suggested. The fabricated microchip of this converter is shown in Figure 1-4. The converter is measured and the results illustrate that it can efficiently transfer power from different low-voltage transducers.

Chapter four

In this chapter, a closed-loop design is proposed to tune and configure the converter's timings to decrease losses and increase the power transfer. This allows the converter to maintain its efficiency, regardless changes in the transducer's characteristics. A time-domain state-space averaging model is used to design the closed-loop system. Based on this approach, two architectures are suggested and implemented in 0.18 µm CMOS technology. The microchips of these self-reconfigurable converters are shown in Figure 1-5 a) and b). The converters are measured with the test board shown Figure 1-5 c). The results illustrate that the converters can harvest from different types of transducers. One of the converters is designed with a more elaborate control system without any significant overhead on the power consumption and the area. This converter can efficiently harvest energy from millimeter-scale transducers with available power of a few tens of microwatts to larger transducers with available power of several hundred microwatts. The entire system of the converters is implemented with low-power and sufficiently precise, custom building blocks. To characterize these blocks, some of them are implemented separately on a chip shown in Figure 1-6. This chip provides the possibly to control the converter by an external control system if necessary.

2 Designing a zero-power wearable medical device

In a wide range of diseases, clinicians are looking for solutions to provide an early diagnosis. For early diagnosis of neurological disorders such as Alzheimer's and epilepsy, physicians monitor a subject's physiology and development of symptoms through body signals over long periods without interruption. These examinations such as electroencephalography (EEG) and electrocardiography (ECG), which are carried out with sophisticated devices, are currently costly. Furthermore, they disturb the ordinary life of patients because they have to be performed in a hospital environment.

Long-term monitoring of body signals is not convenient unless a lightweight fit and forgettable[1] wearable sensor is used. A lightweight, low-power EEG or ECG sensor can have an acceptable precision if its signal conditioning blocks are placed right next to the electrodes. If these blocks are supplied by a battery, the signal recording may be interrupted for charging or replacement of the battery, which is not acceptable for clinicians. To supply the device without interruption and a large battery, an autonomous active electrode is the proposed solution. It consists of an EEG or ECG electrode, a harvester, a power converter and an amplifier with the size of one electrode. Harvester types here will be TEGs and PV cells, based on sensor placement.

This chapter examines the realization of the autonomous wearable device and the requirements of its energy harvesting power converter. Section 1 introduces the device at the system level. The design and characterization of the electronic subsystems of the device are discussed in section 2. Finally, the requirements of the

[1] The device has to be comfortable to the point that a user would forget after a while that he/she was wearing the device.

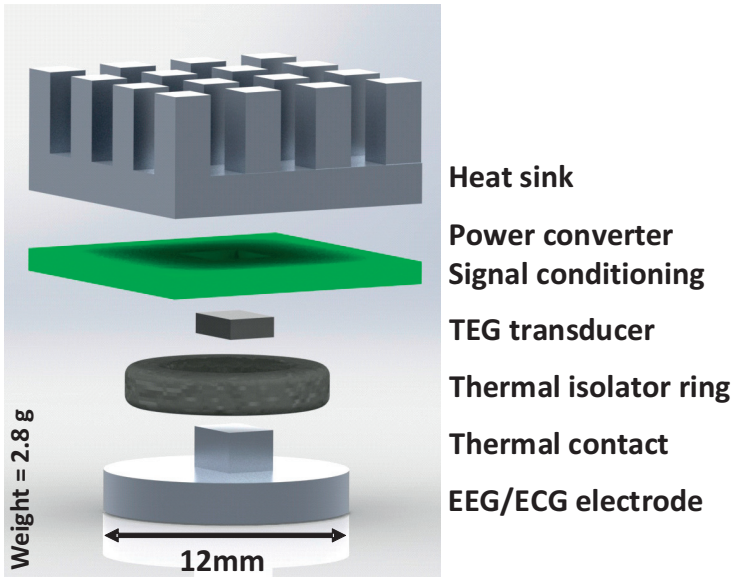


Figure 2-1: Exploded view of the zero-power active electrode [24].

energy harvesting power converter are investigated in detail in section 3. The power converter challenges, the state-of-the-art solutions, and the remaining open questions are introduced in this section as well.

2.1 A wearable device for early diagnosis of Alzheimer's and epilepsy

Long-term EEG or ECG signal monitoring devices must be convenient while maintaining precision. Accordingly, readout electrodes and electronic components must be small and lightweight. They must deliver a high signal-to-noise ratio (SNR) and a low distortion signal at their output. EEG signals are weak and are accompanied by substantial interferences. To achieve a high SNR and low distortion signal aimed at processing, it is mandatory to amplify the signal and reject interferences immediately after acquiring the signal from the electrodes. Introducing an analog front-end responsible for amplifying and digitalizing the signal right next to the electrodes can be solution. However, active components increase the energy budget, and they limit the system runtime for a medical device that employs a tiny lightweight battery as an energy storage element.

An autonomous active EEG electrode [24] based on a TEG harvester or PV cells as a solution are suggested in a multidisciplinary project called BodyPoweredSenSE [26]. Seven academic partners including two university hospitals have collaboration

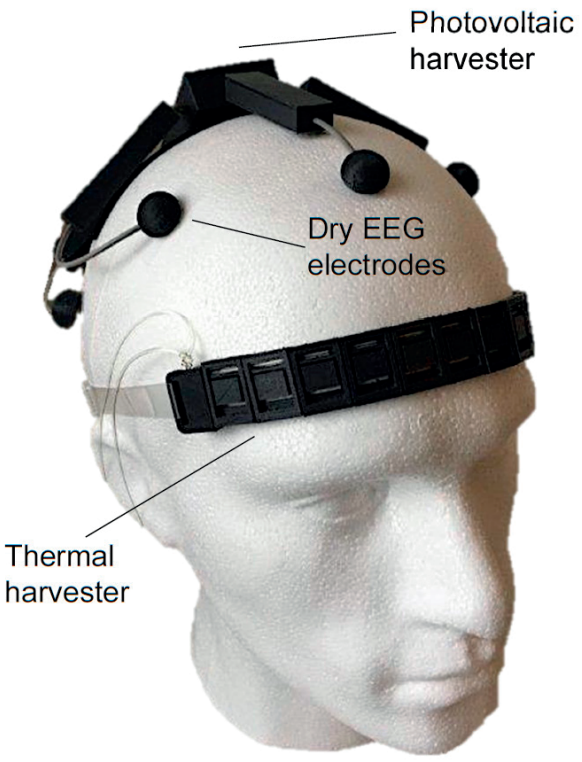


Figure 2-2: Wearable device scheme in BodyPoweredSenSE project, courtesy of Dennis Majoe from ETHZ, Laboratory for Software Technology.

in this project. Figure 2-1 illustrates the mm-scale of the BodyPoweredSenSE wearable sensor scheme. The sensor can be placed on the forehead or on the chest for EEG and ECG signal recording. A sufficient area of skin and an adequate source of body heat is expected to be available there. A metallic plate is placed at the bottom of the sensor to serve the function of the electrode and at the same time as a thermal contact to transfer body heat to a TEG. The body heat is transferred to the TEG transducer through a thermal isolator ring. Ultra-low-power electronics responsible for EEG signal conditioning and TEG power conversion are placed on the top of the TEG. A small heat sink is used at the top of the sensor to have a better heat flux from the body to the environment.

The size of the entire system should be the same as one electrode (12×12 mm^2 here). A printed circuit board (PCB) of the electronic circuits should be less than 12×12 mm^2. This implies a hard limit form-factor for the electronic circuits. Besides area constraints, the analog front-end has to be ultra-low power, and the power converter must have enough efficiency to provide adequate power for the EEG amplifier. Due to the form-factor and power efficiency constraints, the use of an ultra-low-power integrated circuit will be an inevitable choice for electronic parts.

If the sensor is placed on the scalp and in middle of the hair, a different type of a dry electrode should be employed. The electrodes are fabricated by silver chloride (AgCl) pins, which are matched relatively well with scalp skin. They can penetrate well between hairs to establish a better electrical contact with the skin. Since there is not enough thermal connection here, the mm-scale TEG cannot be an apt candidate for energy harvesting. The electrodes are connected to a central part as is shown in Figure 2-2. PV cells and a small battery are placed in the central part to supply the analog front-end. A TEG with the broader area located on the forehead provides energy in this case. This structure can be assembled on a sun hat to shape a wearable device.

The system-level schematic of the wearable sensors which was shown in Figure 1-2 is depicted in detail in Figure 2-3. The power converter processes the energy extracted from the harvesters. The energy has to be efficiently transferred to an energy storage element which can be capacitor bank or a supercapacitor. The potential level of this energy storage element should be almost constant to supply the analog front-end. Therefore, the excess charge on the energy storage element is transferred by a converter to a small battery that is located in the central section of the system. In the signal path, the EEG or ECG signals acquired by the electrodes are delivered to a low-power amplifier that is placed right next to the electrode. It amplifies the signal to a level suitable for ADC while reducing the level of common-mode interferences and noises. The digitized data is recorded on a secure digital (SD) memory card. The raw data is analyzed later by clinicians, or processed by a higher level algorithms to extract the features aimed at early diagnosis of Alzheimer's and epilepsy. As stated before, the mm-scale TEG transducer, power converter, electrode, and the analog front-end are part of the active electrode. The rechargeable battery and its converter, the memory, PV cell, and the broader area TEG belong to the wearable device.

Our medical partner has reported that low-frequency components (mainly alpha waves) of the EEG signal should be studied to monitor progression Alzheimer's [27] and epilepsy in their early stages. A bandwidth of less than 100 Hz is needed to record these low-frequency components. The performance of the EEG activity recording system depends on its "spatial" and "detection" resolutions. To achieve high spatial resolution, a large number of closely placed electrodes are required, and to reach a high detection resolution, a low-noise analog front-end is necessary. The EEG signal is typically extracted from 128 or 64 electrodes. However, in this project, a low-density EEG signal recording has been tried with just 32 electrodes to have a more convenient wearable device.

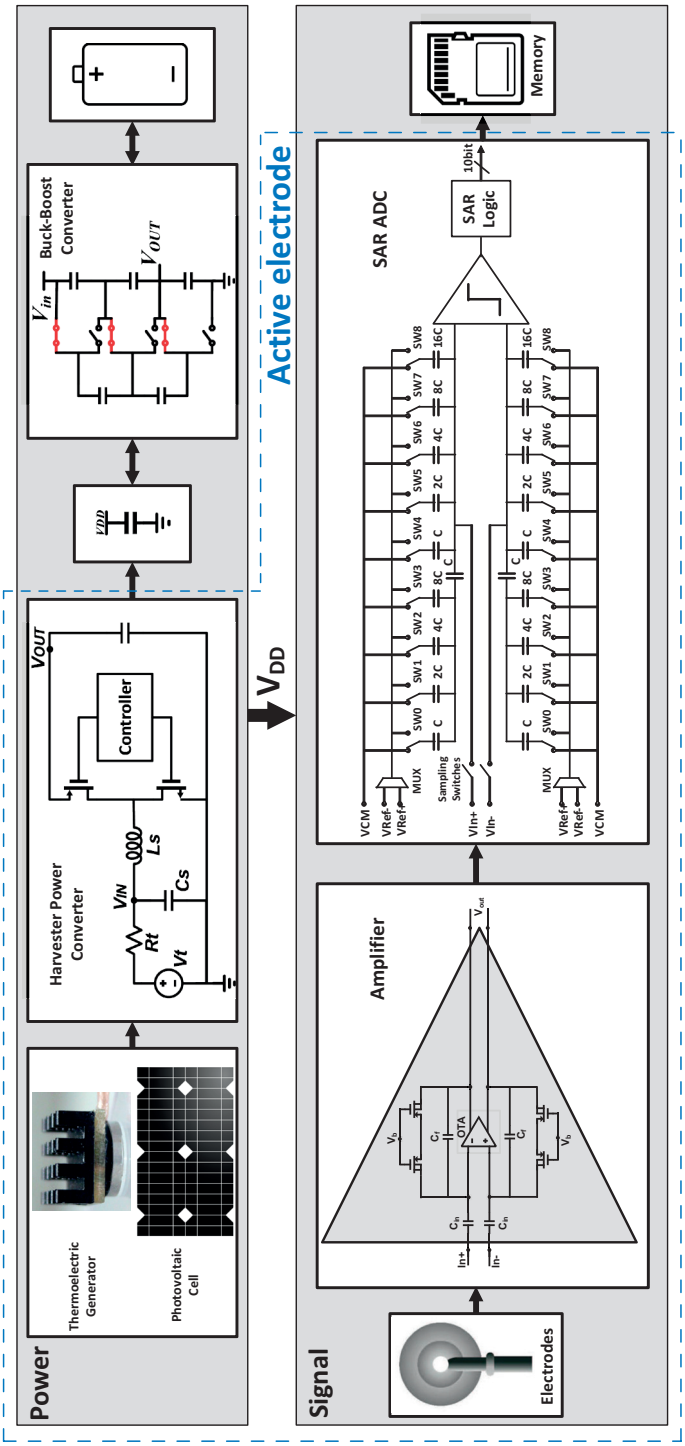


Figure 2-3: The BodyPoweredSenSE project system implementation.

Table 2-1: Power consumption and data generation in the different configurations of the EEG sensor.

# of electrodes	32	64	128
# of microcontrollers	1	2	4
Required BW, Hz	100	100	100
ADC # of bits	12	12	12
Data flow, kbps	38.4	76.8	153.6
Raw data size in 24 h, GB	0.4	0.8	1.6
SD card size, GB	16	16	16
Power consumption, µW	400	800	1600

The generated electrode raw data is recorded on the SD card memory. A low-power microcontroller manages the memory. An MSP430 microcontroller [28] which has a ferroelectric random-access memory (FRAM) is used here to transfer the data to the SD card. The FRAM is a nonvolatile memory that is faster and consumes much lower write power than traditional flash memories. Therefore, a microcontroller with FRAM can save data internally with lower power, before formatting and transferring it to the SD card. The data from each of 32 electrodes is transferred to the SD card by one microcontroller. The microcontroller is interrupted with the rate of the data flow to wake up and save the output of the ADC into its FRAM. Once the FRAM is filled, the data is transferred in blocks to the SD card as the file allocation table (FAT) format dictates. A 16 GB SD card flash memory, which provides the best trade-off between power consumption and capacity, is used here. This setup has been measured over fifteen hours, and the results show that it consumes 400 µW on average. Table 2-1 summarizes the data generation flow and power consumption of the different EEG sensor configurations.

2.2 Analog front-end

Monitoring the EEG signals produced by the neural cells as a means of observing brain activity requires signal conditioning circuits. The general block diagram of such a system is illustrated in the lower part of Figure 2-3. The electrodes are used to pick up EEG signals, which are an average of action potentials of a large number of neurons located in the area below the electrode. The signal picked up by each electrode is then amplified by a dedicated EEG amplifier with suitable gain and

bandwidth. These amplified signals are then delivered to the sampling/processing domain. The sampling/processing circuitry, employing an ADC, samples the amplified signal with an adequate sampling rate dictated by the frequency content of the target EEG signal. The sampled data can then be either recorded in memory as in this project or transmitted using an active/passive wireless telemetry link [29] or a simple wired serial connection.

Since every electrode is associated with its dedicated EEG analog front-end, the total number of front-ends is equal to the number of electrodes employed. Considering the very limited available harvested power, it is crucial that the system have ultra-low-power consumption. In addition to the power consumption constraint, the front-end is required to have adequate gain and sensitivity to capture the weak and noisy EEG signals. The input-referred noise of the system should be kept below the minimum required input detectable signal. The EEG signal amplitude can be as low as 5 µV [30-32]. With dry electrodes, a value of even less than 5 µV is expected here. This minimum EEG detectable signal imposes very severe constraints on front-end noise and dynamic range, and consequently on its power consumption. Commercial products like a TI ADS1299 [33], or an AD AD82224 [34] amplifier with an AD AD7768 [35] ADC, which have an input-referred noise of less than the mentioned detectable signal, consume about 5 mW and 1 mW, respectively. State-of-the-art solutions consume in a range of 80 µW to 1 mW [36-38] which is more than the available power from mm-scale harvesters as well. Therefore, it is impossible to utilize commercial products or to redesign the prior-arts in this work.

To realize the wearable device, the front-end should be then implemented as a custom integrated circuit (IC) for this application. Thanks to the expertise of our medical partners, the analog front-end requirements can be more relaxed than a general EEG acquisition device. As mentioned in section 2.1, extracting of all the EEG rhythmic components is not necessary. Just the alpha component, which has a minimum amplitude about 20 µV [32], is needed here. Considering a possible reduction in the signal level due to an unmatched connection between the dry electrodes and the skin, the front-end should have an input-referred noise of less than 15 µV, which is much more relaxed in comparison to the general scenario. The EEG signal can reach an amplitude of ±500 µV [30] at its maximum point. The EEG processing algorithms can tolerate 1% harmonic distortion. The entire frequency content of an EEG signal ranges from 0.5 Hz to 150 Hz [31]. In this work, though, it is sufficient to detect only a part of this bandwidth up to 30 Hz.

Table 2-2: EEG signal specification.

	Minimum	Maximum
EEG signal on scalp, µV	5	500
The desired EEG signal on scalp, µV	20	200
EEG frequency content, Hz	0.5	150
Acceptable harmonic distortion, %	-	1
DC offset at the amplifier input, V	-	0.3
Common-mode 50 Hz signal at the electrode, V	-	1.5
Front-end input-referred noise, µV	-	15

A DC offset of about ±300 mV, which is related to the quality of the connection between the electrode and the skin, is produced at the input of the amplifier. Additionally, the power-line noise can create a significant common-mode signal with an amplitude of 1.5 V [39] around 50 Hz on electrodes. The common-mode noises impose a hard constraint on the system power consumption. However, if a bandwidth smaller than 50 Hz is selected, the front-end can be more relaxed. The front-end specifications are summarized in Table 2-2. The ECG sensor front-end in this application is even more relaxed than that of the EEG. The maximum ECG signal can reach 5 mV [39], and its minimum detectable signal level is much higher than EEG. Therefore, a reduced gain EEG front-end can be employed for the ECG conditioning as well.

In this section, based on the above application-specific requirements, a low-power custom IC front-end is designed to demonstrate that the autonomous mm-scale sensor is feasible. The section is organized as follows. First, a design methodology of the amplifier and its core operational transconductance amplifier (OTA) is discussed. After that, the ADC topology and its implementation are described. The measurement results of both circuits are presented in the final part of this section. Given that the design is not solely the author's [40][2] and that it is not the main direction of this thesis, the design steps are not discussed in great detail.

[2] The author contributed the architecture and system design and about 20% of the circuit design.

2.2.1 EEG amplifier

Since the EEG amplifier is the first stage in the signal's path, it is required to have an adequate gain and sensitivity to capture the weak and noisy target signal and to satisfy the specifications in Table 2-2. The noisy supply voltage provided by the harvester and the required linearity from Table 2-2 impose severe constraints on the tolerable common-mode rejection ratio (CMRR), power supply rejection ratio (PSSR), and total harmonic distortion (THD). The requirements prohibit the front-end from employing high-gain open-loop [41] architectures.

The amplifier must also be able to reject the DC offset voltage at the electrode-electrolyte interface. In [42], a low-frequency feedback was employed to reject the DC offset along with the low-frequency noise. This approach, however, requires an additional OTA for the integrator block, thus consuming more power. Moreover, the open-loop operation of the system as seen by the signal results in an amplifier gain that is sensitive to process and temperature variations. The PSRR and THD parameters are also degraded as a result of this open-loop operation. Another method, used in [43], is to attenuate the DC offset using a resistive voltage divider and a high-value (pseudo-)resistor (HVR). Nevertheless, the variation in the pseudo-resistor and the DC offset values results in a different offset from one electrode to another and a system that cannot be fully symmetric.

The most common approach to eliminate the offset of biosensor amplifiers is to employ an AC-coupled architecture [44-46]. Despite the required large-area-consuming capacitors, this method is superior regarding power consumption, noise, and robustness. Therefore, the AC-coupled capacitive-feedback architecture is adopted in this work. The topology of the EEG amplifier is shown in Figure 2-3. The gain of the closed-loop amplifier is approximately equal to the inverse of the gain of the feedback.

$$A_m = v_{out}/v_{in} \approx -C_{in}/C_f \,, \tag{2-1}$$

where C_{in} and C_f are the input and feedback capacitors, respectively. The gain should be limited to the value that the output amplitude reaches in its full range for the maximum in-band single-ended signal. The amplitude full range is less than the amplifier's supply voltage by just a few transistors' overdrive voltages. Considering a supply voltage near to 1.2 V and the maximum in-band voltage from Table 2-2, the amplifier (closed-loop) gain should be around 55 dB.

Capacitor C_f with a parallel resistor, R_p creates the amplifier closed-loop high-pass corner around 0.5 Hz. This high-pass filtering rejects strong low-frequency

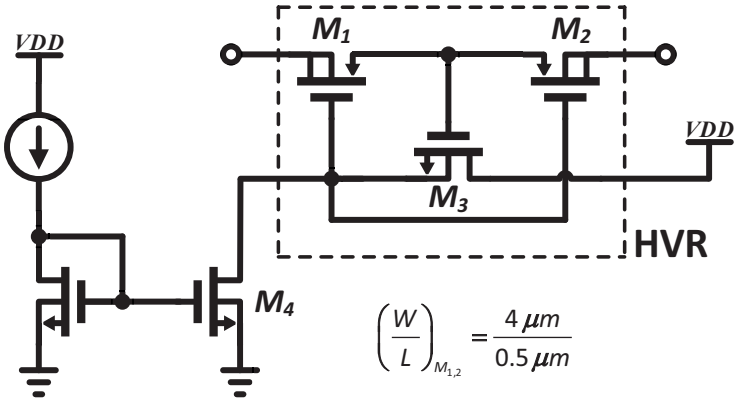


Figure 2-4: Schematic of the tunable high-value resistor.

noises around DC. To avoid a sizeable passive capacitor as C_f, and as a result from equation (2-1) a significant C_{in}, an HVR is employed as R_p. Two PMOS transistors biased in the subthreshold region can create the HVR as shown in Figure 2-4. The gate-source voltages of the transistors $M_{1,2}$ are kept by M_3 in which the current mirror M_4 forces the current. The HVR value changes with its gate-source voltage; therefore, it can be adjusted by tuning the current mirror as [47] suggested.

Four HVRs are connected in series to create resistance as large as possible with a sufficient bandwidth for the application. The values of the HVRs are susceptible to their gate-source voltages. The HVRs' source voltages are changed when the amplifier output sweeps. The M_3 non-idealities and mismatches with M_4 do not allow the gate of M_3 to perfectly follow its source. This results in nonlinearity in the amplifier, particularly at low frequencies. NMOS transistors have to be initiated on the substrate of CMOS technology. Therefore, the cascode transistor M_3 has a different substrate-source voltage than M_4 and their threshold voltages cannot be matched. The CMOS technology employed here provides the option to place NMOS transistors in an isolated P-well. Then, M_3 is placed in the P-well, and its bulk connection is tied to its source similar to M_4 to have a better matching and higher linearity.

The amplifier should have flat gain in the desired EEG bandwidth, and it has rigorous linearity requirements as mentioned. The high-density MOS capacitor cannot be used as C_{in} or C_f. The lower density metal-insulator-metal (MIM) capacitors are used here. These capacitors should be big enough to satisfy the gain and the high-pass corner requirements while having a reasonable area. With the designed HVR, a C_f equal to 1 pF is selected. Then with the schematic shown in Figure 2-4, the high-pass corner in the frequency response of the amplifier can be tuned in the

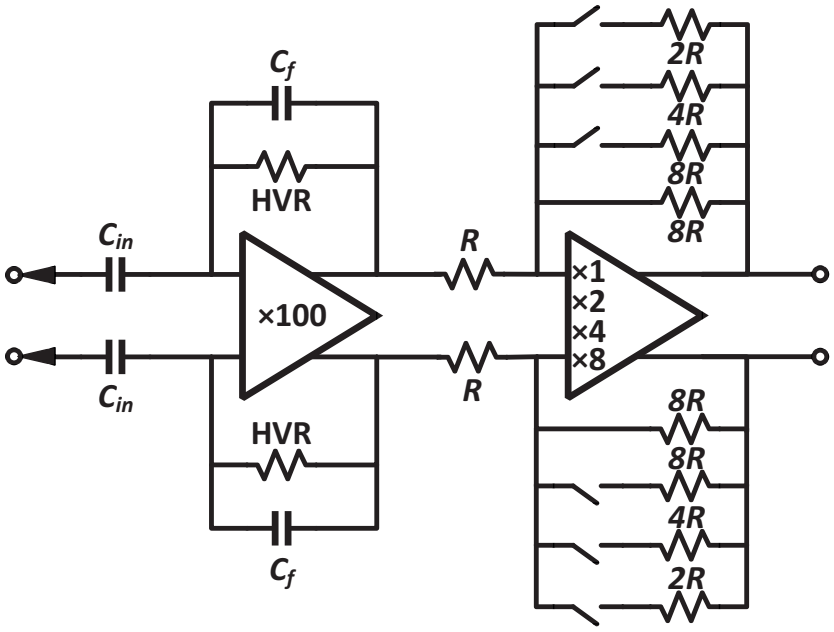


Figure 2-5: Overall architecture of the EEG amplifier.

range of 0.1 Hz to 2 Hz. This is sufficient to create a high-pass corner at 0.5 Hz with given set of the technology process and temperature variations. The maximum C_{in} that can be fit in a given area of about 0.2 mm^2 is 200 pF (differentially), which results in a 40 dB gain. To achieve the recommended gain in section 2.2, the amplifier is cascaded in two stages. The same core as in the first stage is employed in the second stage for simplicity. The second stage is designed to have a variable gain as shown Figure 2-5. The variable gain enables the front-end to be employed in the ECG sensor as well.

The amplifier has to drive an off-chip low-pass filter to reject unwanted signal and noise, especially power-line noise at 50 Hz. The core OTA is designed with a two-stage architecture [48] in which the second stage can provide current for the external load. Therefore, it is possible to use the resistor feedback instead of the capacitive network in the cascade stage to provide a small signal gain and input DC biasing at the same time.

2.2.1.1 OTA design

The common-mode signal levels from Table 2-2 leave strict requirements for the CMRR of the amplifier. The common-mode signal should be attenuated at the output of the amplifier below the level of the amplified minimum detectable signal $V_{n,amp}$. The DC common mode is expected to be attenuated enough with the selected AC-coupled architecture. As for the power-line noise, a CMRR on the order

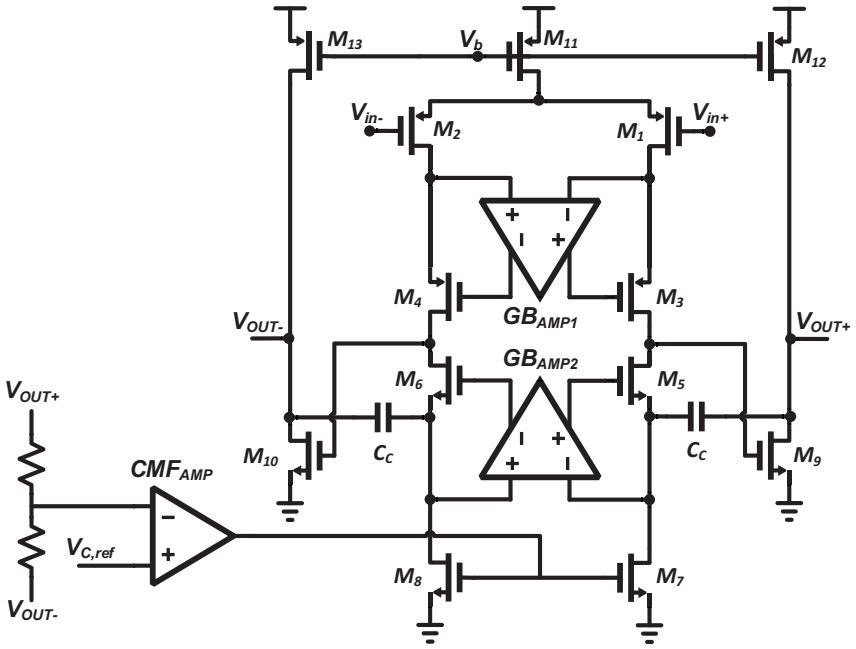


Figure 2-6: The two-stage gain-boosting amplifier with its common-mode feedback.

of 80 dB is recommended for a more general EEG signal conditioning circuit with dry electrodes [36, 49]. Since the 50 Hz noise is partially filtered after the first stage and the minimum detectable signal has a higher level than the general case, a CMRR of more than 65 dB is expected to be required for the amplifier with 40 dB gain. The core of the amplifier is designed to be entirely symmetric for the severe CMRR requirement. Thus, a common-mode feedback (CMF) is adopted, as depicted in the schematic of Figure 2-6.

To maximize the OTA gain, the transistors $M_{1,2}$, $M_{3,4}$, $M_{5,6}$, $M_{9,10}$ are placed in the weak inversion operating region where their transconductance to drain current g_m/I_D is maximized. The choice of the aspect ratio of transistors is made with regard to the gain and noise characteristics of the OTA. The second stage of the OTA has a limited gain. Therefore, the gain of the first stage is enhanced by GB_{AMP1} and GB_{AMP2} gain-boosting OTAs. A single-stage common source is employed as the gain-boosting amplifier. The limited gain of $GB_{AMP1,2}$ cannot change the dominated poles and zeros of the OTA, and it does not deteriorate the OTA phase margin.

C_C is a compensation capacitor to stabilize the OTA. However, it creates an unwanted right-hand-side zero in the frequency response. The common gate M_5 moves the zero to the left side of the response. The zero shapes the noise response of the M_9 as well. This noise contributes to the output with a differentiator response.

Therefore, considering the limited bandwidth of the amplifier, the main noise contributors are the transistors at the first stage.

The noise of the tail current source M_{11} does not appear at the OTA output due to the symmetry in the circuit topology. The equivalent noise voltage source at the gate of the cascode transistors $M_{3,4}$, $M_{5,6}$ encounters a large degeneration impedance which can attenuate their input-referred noise voltage. The input transistors $M_{1,2}$ are the major contributor to the noise of the OTA. The input-referred noise contribution of these transistors is proportional to the inverse of their g_m. As stated before, $M_{1,2}$ are placed in the weak inversion to maximize gm/I_D. This reduces the $M_{1,2}$ noise contribution as well. Furthermore, to minimize their low-frequency flicker noise, PMOS transistors are employed as the input stage, and a large width and length are chosen to increase $W\times L$.

$M_{7,8}s'$ noise is not attenuated due to degeneration impedance or symmetry, and it contributes to the output of the OTA by the $g_{m7,8}/g_{m1,2}$ ratio. Therefore, their noise contribution is desired to be suppressed by minimizing their g_m. It is better to place these transistors in the strong inversion operating region with a small width-to-length aspect ratio (W/L). Moreover, to minimize their flicker noise, a large $W\times L$ must be selected. Reducing these transistors' g_m does not affect the gain of the OTA. Besides, increasing $L_{7,8}$ maximizes the mirror matching and the output resistance of the first stage and boosts the OTA gain. However, $M_{7,8}$ with the CMF_{AMP} create a two-stage amplifier. A low $g_{m7,8}$ and a large $W_{7,8}$ or $L_{7,8}$ push the second pole of this amplifier close to its first pole and can make the CMF unstable. To sum up, a small W/L ratio with large values for $W_{7,8}$ and $L_{7,8}$ is desired up to the point that the CMF stays stable.

2.2.2 ADC design

The ADC described in this section [40] is based on the successive approximation (SAR) architecture, as it is the most suitable for the mentioned requirement of the analog front-end. The resolution of the ADC is set by the system minimum detectable signal $V_{n,system}$, the amplifier input-referred noise $V_{n,amp}$, and amplifier gain A_m. In the worst-case scenario, when the available power noise from the output of the amplifier is transferred to the ADC input, the minimum detectable ADC signal or its the least significant bit LSB can be written as:

$$LSB = \sqrt{\left(V_{n,system}{}^2 - V_{n,amp}{}^2\right) \times A_m{}^2}\ . \tag{2-2}$$

Then, the required ADC number of bits can be written as:

$$N = \log_2 \frac{\text{Full scale}}{LSB}. \tag{2-3}$$

From equation (2-2) and equation (2-3), it can be approximated that the full dynamic range of an EEG signal can be covered with an 8-bit ADC. EEG acquisition systems employ ADCs with a vast range of resolutions, between 8 bits and 24 bits [33, 50, 51]. The reason for this large variety is related to the power budget of the system (portable or stationary) and the coupling strategy between the ADCs and the EEG signal amplifiers. Here to achieve an ultra-low-power system and still leave some margin for low-frequency interferences, an ADC with 10 bits of resolution has been implemented. The ADC was designed to operate at 400 S/s, a sufficiently high frequency for acquiring the full spectrum of EEG signals.

The block diagram of the SAR differential ADC described in this section is shown in Figure 2-3. This circuit is power-efficient and does not require any complicated high-performance analog blocks. Therefore, it can operate with a low supply voltage. The ADC operates as follows. In the first phase, the sampling switches are closed, connecting one side of the capacitors to the input voltages V_{In+} and V_{In-}. The other side of the capacitors is connected to the common-mode voltage V_{CM}. Then, the sampling switches open, and the comparator is triggered a small instant afterward. The result of the comparison is used to select which reference voltage connects to the capacitor bank by using two multiplexers. The capacitors are switched sequentially between V_{CM} and V_{Ref+} or V_{Ref-}. After each comparison, the most significant indeterminate output bit is resolved, and the voltage difference at the inputs of the comparator is reduced proportionally.

SAR ADCs require one clock cycle per bit resolved. However, if the minimum clock frequency of 4 kHz for a 10-bit 400 S/s ADC is used, the time available for tracking the input signal is only half a clock period. This creates a difficulty for the sampling switches, which will be in an open state during most of the time, and closed during only a small instant. As the time available for tracking the input is very small, the on-resistance of the switches should be very low. Conversely, the charge leakage is proportional to the duration that the switches are open. Therefore, the off-resistance of the switches should be very high to limit the contamination of the sample when it is being processed.

The double-sampling scheme used by [52] mitigates this issue but requires additional hardware and introduces a tone at half of the sampling frequency. It can result in charge injection mismatches for the odd and even samples. The technique used here to address the issue increases the ratio of the tracking time to the hold time by employing a higher clock frequency. Here, a clock frequency 8 times higher

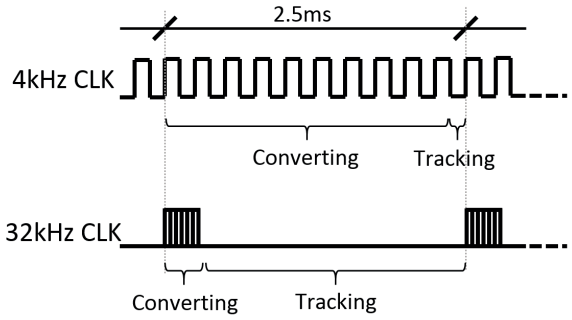


Figure 2-7: The clocking scheme of the designed ADC.

is used, and the ADC conversion proceeds during just 1/8th of the available time. The ADC is disabled during the rest of the period. This principle, which requires a 32 kHz clock signal, is illustrated in Figure 2-7. When the ADC was using the minimum clock frequency, the switches were closed for 5% and opened for 95% of the time, whereas with the 8-times-faster clock, they are closed for 88% and opened for only 12% of the time.

This operating method is also advantageous regarding the static power consumption of the ADC. A buffer with a static consumption interfaces the comparator's input with the capacitor's bank. This block is now disabled during 7/8ths of the clock period, which enables considerable power saving. On the other hand, both the dynamic power consumption and the area stay almost unchanged, since the effective switching clock frequency of the ADC remains 4 kHz and the added circuits have a negligible area and power consumption. The main disadvantage of this technique is the requirement of a higher frequency clock; however, this can be a minor issue given the low-speed operation requirement for this application.

2.2.2.1 Sampling Switches

The switches used for sampling the analog input signals are the transmission gate type. The distortion introduced by the sampling switches should be small in comparison to the resolution of the ADC. This distortion is caused mainly by the nonlinear on-resistance of the switches. The harmonic distortion introduced by the switches has been simulated for a 200 Hz full-swing sine wave input signal, for a given set of process and temperature corners. The result indicates that the highest harmonics are at about -79 dB and -83 dB for the slow-slow-cold and the fast-slow-cold corners. These levels of harmonic distortion are well below the requirements for an ADC with a resolution of 10 bits, and it is not necessary to introduce bootstrapping or an OTA-based method for the sampling switches.

2.2.2.2 Comparator and buffer

The comparator used in this design is a dynamic latch, as presented in [53]. The simulation results have shown that the comparator has 50 μV of input-referred noise, which is much smaller than the ADC's LSB. The comparator's offset distribution has been extracted from Monte Carlo simulations. It has a standard deviation of 6.4 mV, which is tolerable for this ADC. The comparator's input transistors have been designed to be relatively large to reduce its offset and noise. However, the large transistors can intensify the kickback noise. This noise affects the voltage level that is going to be processed and can degrade the linearity of the ADC significantly. To attenuate the kickback noise to a tolerable value, a buffer circuit has interfaced the capacitor bank with the comparator. This circuit increases the offset to 9.4 mV (standard deviation) and the noise to 250 μV. The new values of both the offset and the noise are still acceptable for the application. The offset corresponds to 0.6% of the comparator's input range, and the noise accounts for only 16% of the LSB.

2.2.2.3 Capacitor bank

For a 10-bit SAR ADC, the ratio of the smallest capacitor to the biggest one in the bank goes up to 256. Assuming that the smallest capacitor consists of multiples of a unit capacitor, which is essential for matching, a bank of 1022 unit capacitors would be required. It would be impractical to route such a large number of components, and the parasitic capacitances from the routing would very likely degrade the overall matching. For these reasons, the well-known split capacitor technique has been applied here. In this method, a series capacitor is used to attenuate the values of the capacitors placed after it, as shown in the schematic of the ADC in Figure 2-3. This allowed reducing the total number of capacitors to 94. The unit capacitor used is a 25 μm^2 MIM device with 26.5 fF. The total sampling capacitance is 846 fF for each input. The resulting sampling noise is about 100 μV, which is an acceptable value that corresponds to 6.4% of the LSB amplitude.

2.2.3 Characterization of the analog front-end

Both the EEG amplifier and the SAR ADC are designed in UMC 0.18 μm CMOS technology. A chip microphotograph of these circuits is shown in Figure 2-8. The core area of the amplifier and ADC are 0.53 mm2 and 0.13 mm2, respectively. The amplifier consumes 9 μW from a 1.2 V voltage supply. An Agilent 34411A Digital multimeter device is used to measure the power consumption of the circuit. The gain can be set to 40 dB, 46 dB, or 58 dB. The measurements show that the amplifier high pass corner frequency can be set 0.5 Hz. The input-referred noise voltage

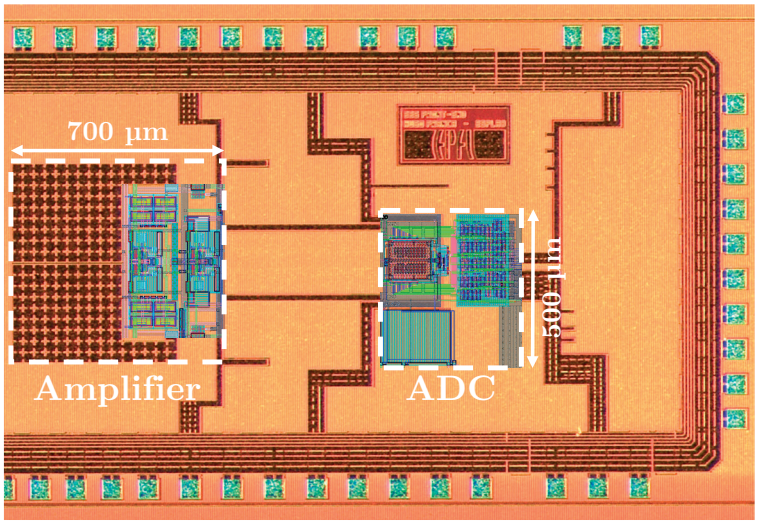


Figure 2-8: The analog front-end microchip designed in 0.18 µm CMOS.

Table 2-3: Performance summary of this EEG amplifier.

	Requirements	This work
Gain, dB	40, 55	40, 46, 52, 58
Power consumption, µW	<10	9
Supply voltage, V	<1.6	1.2
Input-referred noise, μV_{rms}	15	6[a]
CMRR	65	72[a]
Process, µm	0.18	0.18
High-frequency corner, Hz	0.5	0.5
Configuration	Closed loop	Closed loop
DC rejection	AC coupling	AC coupling

[a] simulations

of the amplifier is calculated by integrating the output noise density spectrum up to 150 Hz from the simulation[3] and dividing it by the gain at 10 Hz frequency. The value of the input-referred noise voltage is found to be 6 µVrms. The amplifier simulation and measurement results are summarized in Table 2-3 and compared with the requirements for this application-specific circuit.

[3] The amplifier has not been fully characterized with measurements at the time of the submission of the manuscript.

Table 2-4: SAR ADC performance summary.

DNL	0.93
INL	1.46
ENOB	9.02
Analog power consumption, nW	22.8
Digital power consumption, nW	45.6
I/O power consumption, nW	32.4
Total power consumption, nW	101
Area, mm^2	0.13

The ADC consumes just 0.1 µW from a 1.2 V voltage supply. The ADC both the differential and the integral nonlinearities (DNL and INL) were measured by testing the prototype using the code density histogram technique [54]. The maximum values for the DNL and INL are 0.93 LSB and 1.46 LSB, respectively. The measurement results show that the ADC has a relatively stable effective number of bits (ENOB) of 9.02 for the full input frequency range from simulations. The figure of merit of the ADC is at 490 fJ/conv. The characteristics of the ADC are summarized in Table 2-4.

2.3 Low-voltage power conversion for energy harvesters

Temperature difference and light are the two main sources selected to harvest energy in this study. To extract power from the thermoelectric effect, two materials with different Seebeck effects should be merged. Each material is called a thermoleg, and the combination a thermocouple. TEGs are formed by connecting the thermocouples electrically in series. Microscopic- or macroscopic-scale thermolegs can be used in TEG fabrication. A TEG with microscopic thermolegs (µTEG) has more thermocouples, and as a result, its open-circuit (OC) voltage and its output impedance are higher than a TEG with macroscopic thermolegs (mTEG).

Table 2-5 summarizes the average experimental specifications of the primary transducers used in the wearable device. The transducers are three different types of TEG (named TEG1, TEG2, and TEG3) [24, 25] and a monocrystalline PV cell [55]. The monocrystalline PV cell was chosen because it has a higher efficiency even in low light intensity conditions. The TEGs and their heatsinks are optimized for harvesting from body warmth to have an efficient output power with a low weight and small form-factor. The TEGs were designed not to create an unpleasant cold

Table 2-5: TEG body harvester and PV cell electrical characteristics at 24 °C ambient temperature.

	TEG1	TEG2	TEG3	PV cell	
Fabrication	mTEG	µTEG	mTEG	Monocrystalline	
Size	15 × 15 × 11 mm^3	15 × 15 × 17 mm^3	130 × 15 × 11 mm^3	57 × 35 × 1 mm^3	
Impedance type	Constant	Constant	Constant	Variable	
Condition	On skin 37 °C	On skin 37 °C	On skin 37 °C	Indoor 300 lux	Outdoor 1500 lux
Available power	40 µW	23.5 µW	320 µW	92 µW	286 µW
OC voltage	~20 mV	~130 mV	~160 mV	450 mV	450 mV
Voltage type	DC	DC	DC	DC	DC
Output impedance	2.5 Ω	180 Ω	20 Ω	550 Ω	177 Ω

feeling on the skin. Data from the mm-scale TEG1 and TEG2 were recorded from a person's forehead with a 37 °C temperature when the average ambient temperature was 24 °C. TEG3 is fabricated with a combination of TEG1 cells and can be used as a headband as shown in Figure 2-2 or even as a bracelet.

Energy has to be supplied to the analog front-end and the microcontroller in the wearable device shown in Figure 2-2. In the mm-scale active electrode, on the other hand, energy has to be provided only to the analog front-end. The central part of the wearable device is responsible for storing the active electrode's data. The power consumption of the sensor's blocks which were discussed in this chapter is summarized in Table 2-6. Given the power consumption and the available power from the transducers, the active electrode implementation can be feasible if the harvesting power converter has an efficiency higher than 25% and 42% for TEG1 and TEG2, respectively.

The EEG wearable device with 32 electrodes has TEG3 as the primary transducer. TEG3 is placed on the forehead where body heat can be continuously harvested. Additionally, the device can be supplied by a small (20 × 11 × 3 mm^3) lithium-ion rechargeable battery and a PV cell as described in Table 2-5. The battery [56] provides 95 mWh of energy with 80% depth of discharge and 80% efficiency of its buck converter. This is sufficient for about five days' autonomy. A converter efficiency of 70% with TEG3 extends the system autonomy more than one week which can be necessary to study epilepsy in children in some cases [57].

Table 2-6: Power consumption of the different blocks in the EEG wearable sensor.

# of electrodes	1 (active)	32
Amplifier, µW	10	320
ADC, µW	0.1	3.2
Analog front-end, µW	10.1	323
Memory access, µW	-	400
Total, µW	10.1	725

Table 2-7: Converter efficiency required in different scenarios.

	Battery	Autonomy	η-TEG1	η-TEG2	η-TEG3
Active electrode	No	Full	25%	42%	-
32 electrodes	Yes	7 days	-	-	70%

Moreover, sufficient environmental light can even lead to a fully autonomous system. The efficiencies needed for the converter are summarized in Table 2-7.

The converter needed for this application has to work with different types of harvesters with different characteristics. It should keep its efficiency in the extensive range of impedances, voltages, and available powers. A converter architecture that does not have a limit for satisfying the demanding requirements has to be selected. Two main architectures have been used in the literature to implement low-power energy harvesting converters: fully integrated switched capacitor (SC) converters and inductor-based converters.

2.3.1 Fully integrated switched capacitor power converters

An SC architecture employs flying capacitors and switches to transfer charges from the input to an output storage capacitor. The switches configure connectivity of the flying capacitors to be charged by the input in one phase and transfer the charges to the output with a different voltage level in the other phase. The most straightforward structure of an SC is a charge pump that has one flying capacitor. In the first phase, the flying capacitor is placed between the input and ground by the switches and is charged by the input, whereas in the second phase, the capacitor is reconfigured to be placed between the input and the output to create an output

voltage two times higher than the input. The SC architectures offer full integration and low power consumption [58]. A non-overlapping clock generator and a level shifter control the switches. In [59], an SC converter was presented that consumes just 3 nW by combining the clock generator and the level shifter in the switch network. It can have 75% efficiency in doubling voltage level. Another work [60] presented a harvester with a conversion ratio of three (higher than the previous work), by a maximum efficiency of 58% while the converter just consumes 3 µW.

SCs deliver charges with a fixed ratio [61]; if a different ratio is needed, the SC topology has to be configured. SC conversion ratio step sizes are large, and it is challenging to have a non-integer up-conversion ratio. Parasitic capacitance limits their efficiency. In low-voltage applications, in which a considerable conversion ratio is needed, a large number of switches and capacitors have to be employed and accordingly the parasitic capacitance increases. Their efficiency can be very low inherently for a high conversion ratio. On the other hand, because of a large number of switches and capacitors in the structure, their input range is limited by the switches' driving strength and leakages, with respectively a higher and a lower input power than the SC is designed for.

The SC architecture is a perfect candidate when the input range is almost constant, and is a small integer fraction of the output. In this case, a fully integrated SC converter can be employed with very high efficiency and low power consumption. The system shown in Figure 2-3 has a constant supply voltage whose extra charges have to be transferred to the battery with a voltage level about two times bigger than the supply. If the supply level decreases, it has to be charged and regulated. An SC converter can be employed here as the switching regulator. This converter can be implemented with a design adapted from [62] which can provide 75% efficiency in a similar condition. The converter stays idle until it detects a voltage drop on the supply level with a comparator and an internal reference, then the converter is activated and charged the supply. Therefore, since such converters have been implemented with high efficiencies and with the same requirements as needed here, it is assumed that their design can be repeatable. That is to say, the design of the switching regulator has not been a focus of this study.

However, as shown in Table 2-5 and Table 2-7, the energy harvesting converter has to convert a wide range of the input[4] from 10 mV to 220 mV with a conversion ratio that has to reach 150. The converter has to maintain its efficiency for this extensive range of the transducers, voltages, and available power. Therefore, the

[4] The converter input is half of the TEG transducer's OC voltage in an impedance-matched situation.

inherent limitation of the SC architecture to have a wide range of inputs and high variable conversion ratios, eliminates this fully integrated converter from consideration for use as the architecture for the energy harvesting converter in this work.

2.3.2 Low-voltage inductor-based power converters

Power converters aimed at small-scale medical monitoring sensors should have a high efficiency, a high conversion ratio, and limited power consumption. Since inductor-based power converters do not encounter the inherent parasitic capacitance challenge faced by SC converters, they may be a suitable architecture for medical monitoring. The input range of the inductor-based converters can be more extensive, and they can harvest with ample efficiency when their transducer's voltage changes because of environmental conditions. The basic schematic of an inductor-based converter is shown in Figure 2-3. An NMOS power switch transfers the stored energy at the input capacitor C_S to the inductor L_S, after which the energy stored in L_S is transferred to the output capacitor, commonly by a PMOS transistor.

Well-designed power switches and the timings can result in a high-efficiency converter for a specific application. The switches have conductance and dynamic losses; therefore, dependent on the converter's input and output, the switches can be sized and their working frequency can be optimized [63]. If switch leakage and the losses due to L_S parasitic conductance and parasitic capacitance are taken into account, a more efficient converter can be achieved in the lower power applications [64]. The conductance, dynamic, and leakage losses are not the only issues that limit the efficiency of a converter. The efficiency can be influenced by other factors that can prevent transferring the entire available power of the transducer to the converter. The factors include the limited size of the passive elements (both C_S and L_S), as well as limitations in a low-power circuit to generate the exact optimized timings. The losses and these factors have to be studied together. Besides, when different types of transducers are required to be employed in the system, a new optimizing strategy has to be introduced to enable the converter to keep its efficiency despite changes in the transducer's specifications.

The switching durations and timing of the NMOS and PMOS are controlled and generated by a control section. The ratio of the output voltage to the input voltage is directly related to the ratio of the NMOS switch "on" duration to the PMOS switch "on" duration. Therefore, by generating a high ratio of timing durations for the NMOS and the PMOS, the converter can have a high conversion ratio without any limitation. However, the process variation can deviate the working point of the converter and directly affect its performance. The process variation is one of the

essential challenges in CMOS design, particularly in the low-power, low-voltage regime. If CMOS switches are employed in the architecture, it is mandatory for one control loop to be implemented in the converter to compensate for the variations. In an inductor-based converter with a high conversion ratio, the pulse duration responsible for controlling the PMOS can be extremely narrow. The PMOS should be turned off as soon as the inductor energy is transferred to the output. A slightly larger duration can discharge the output instead of charging it. Therefore, by the changes in the harvester voltage or a variation in the process, this duration has to be adjusted. The control section to tune the PMOS duration is always implemented for the low-voltage inductor-based converter, even if the available power is very limited. In [65], a 1.1 nW power converter is designed and implemented with this minimum control section for a particular biopotential application with very limited variations in the transducer specifications. A converter for a specific type of TEG is designed in [66] with optimized parameters and the loop to control the PMOS to harvester from available power as low as 2 µW at 20 mV voltage.

Since the loop "should be made as simple as possible" to be low power, it is commonly implemented by digital circuits. A sufficient supply has to be provided for these circuits. However, converters may not be able to provide enough supply during a cold-start operation. To eliminate the digital control section while avoiding losses, the PMOS can be replaced by a diode. On-chip diodes have either very high voltage drops or high leakages. On the other hand, external Schottky diodes are costly since they occupy extra space on the PCB. The active analog diode can be a solution in this case [67], however, they are power hungry and their implementation can be complicated [68, 69].

The converter input capacitor C_S is charged by the transducer gradually because of the transducer's output resistance. The NMOS switching duration determines the amount of the stored charges in C_S that have to be transferred to L_S in each cycle. Therefore, the duration sets the average input voltage of the converter or the C_S voltage, thus, the mimicked input impedance of the converter. To transfer the maximum power to the converter, the input impedance of the converter has to be set and matched with the output impedance of the transducer. When the output impedance of the transducer is changed because of environmental conditions or because of a change in transducers, this duration has to be tuned. The converters designed in [70, 71] added an extra loop to tune the duration and to maximize the power transferred to the converter. In those works, the converters' working frequency is constant, then the converter input power can be estimated just by the duration that the output capacitor is being charged.

The open-circuit voltage of transducers and, therefore, their available power can increase or decrease with variations in the harvested sources. The converter speed can be increased or decreased proportionally to maintain converter efficiency. The converter's speed is the same as its switching frequency. Then, the speed of the pulse generators which control the NMOS and PMOS switches can be tuned manually to maintain the converter efficiency [72, 73]. This solution is not user-friendly when frequent replacement of the transducer or even environmental variations are expected.

If the type of the transducer is known, the speed of the converter can be set automatically just by detecting the open-circuit voltage of the transducer and without sensing the transferred power [74, 75]. Then, the converter speed can be changed to have a hard-coded predefined ratio between the input voltage of the converter and the sensed open-circuit voltage of the transducer. That ratio is based on the transducer type used in the converter. The architecture implementation can be ultra-low power; however, even for a specific transducer, the ratio may need to be changed in different working conditions since transducers' characteristics vary in different working conditions. On the other hand, in low-voltage transducers, losses can be comparable to the available power, and the speed should be adjusted not only to maximize the available power but also to minimize the losses.

A more reasonable power estimation is needed to tune the speed of the converter, mainly, if different types of transducers are intended to be used as the harvester. Power estimation in converters is usually proceeded by more sophisticated control systems [76]. They use multipliers or current and voltage sensors to calculate their output power [77, 78]. These converters can have efficiencies higher than 90%, however, they are targeted at higher voltage and higher power transducers. Their control system alone can consume the entire power available from a mm-scale transducer.

The inductor-based converter in this study must be efficient in the low voltages. The power switches and its timing should be designed to have a minimized loss and maximized power transfer simultaneously. The converter's transducer can be replaced, or its open-circuit voltage and its impedance can change with the environmental condition. An optimization procedure should be introduced to enable the converter to keep its efficiency with variations in its transducer specifications. The mandatory control section for tuning the PMOS duration has to be implemented. The converter should tune the NMOS duration as well, to achieve a high efficiency and an input impedance matched to its transducers. On the other hand, the speed of the converter should be tuned automatically by another closed-loop control system to keep the efficiency with environmental variations. Power-

hungry methods to examine and estimate power transfer in the converter have to be avoided, while a reasonable power estimation process which takes both power transfer and losses into account should be introduced and employed. The control section has to be implemented with digital low-power circuits, and must adjust all the control parameters in a stable manner.

This work does not focus on the cold start, and it is assumed that the output energy storage has some initial charge (for example through the regulator power converter) during start-up. However, the low-voltage start-up issue has been addressed in the literature. The available solutions include a mechanical MEMS switch [72] instead of a CMOS switch, big off-chip transformer [79] to convert the small potential to a bigger one, or Radio with off-chip antenna [80] to harvest radio frequency (RF) energy for start-up. When a complete electrical start-up solution is desired, charge pump start-up with low drop-out diodes [81, 82], or ultra-low voltage oscillators followed by a voltage multiplier and a rectifier [83-85] can be employed.

In the following chapters, details of the converter design are discussed. The different mechanisms involved in losses and power transfer are shown, and a method to optimize the switches and timing considering that different harvesters can be used as the transducer is developed. The low power implementation of the closed loops is described, and the design of a nano-power energy estimation block and timing generators are introduced. This is followed by a discussion about how the measured results in the converter are distinguished from the prior-arts, which have been described in this section.

2.4 Conclusion

The wearable devices' subsystems have been introduced and designed to determine the requirements for the energy harvester power converter. The system should be able to provide enough power for its analog front-end, which consists of an amplifier and an ADC. A low-power closed-loop capacitive feedback amplifier and a SAR ADC were designed in UMC 0.18 µm CMOS process. They consume 9 µW and 0.1 µW from a 1.2 V supply. The amplifier is designed to decrease its power consumption to a level that the implementation of the wearable device is feasible. A fully symmetric OTA and CMF are employed in the design. The linearity of the HVR in the feedback network is enhanced with matching the threshold voltages of the HVR's NMOS transistors. Its gain can be adjustable in a range from 40 dB to 58 dB. The SAR ADC has been designed with a higher clock frequency to relax the constraints for the on-resistance and the leakage of the sampling switches. Since

with a higher frequency, the ADC operates for a shorter period, the switch has a more extended input tracking time, and therefore, a switch with a smaller on-resistance can be used. Conversely, as the hold time is reduced, more leakage current is tolerable and the off-resistance of the switches can be reduced. The static power consumption of the ADC could be reduced, since the ADC was in the idle mode for a long duration, whereas the dynamic power increase was negligible.

Different types of transducers harvest the required energy for the wearable device. Since the available transducer power was limited, the converter, which should maintain its efficiency for a broad range of transducer voltages and available powers, had severe efficiency requirements. Based on a review of the state-of-the-art, an inductor-based architecture was recommended for the converter. It was suggested that the optimization process which will be employed in the design of the converter should consider the variations in the converter's transducer specifications. The converter should adjust its NMOS and PMOS switching durations and its speed in a stable manner to achieve a high efficiency with different transducers and environmental variations. To control these timings, it was discussed that a new ultra-low-power approach should be employed to reasonably estimate the output power of the converter.

3 Integrated power converter design for low-voltage harvesters

This chapter describes a detailed design procedure for an efficient low-voltage harvesting integrated power converter. The procedure is based on the examination of power loss and power transfer in a converter for a self-powered medical device. The efficiency limit for the system is derived and the converter is optimized for the worst-case scenario. All optimal system parameters are calculated while considering the transducer constraints and the application form factor. Circuit blocks including pulse generators are implemented based on the system specifications and optimized converter working frequency. It is demonstrated that a voltage doubler with a wide-area capacitor, which is typically employed in power converters to provide high-voltage switch gating, can be excluded from the design without any negative impact on efficiency. Measurements of the designed power converter show that an efficiency of 54% and 70% is achieved with two different mm-scale transducers with open-circuit voltages of just 20 mV and 100 mV, respectively. Nearly 20% of the chip area is saved in the implementation compared to a typical converter design. The entire electronic board can fit into one EEG or ECG electrode, and the electronic system can convert the electrode to an active electrode.

3.1 Efficient low-voltage power conversion: Overview

As discussed in the Chapter 2 section 2.3, in zero-power applications aimed at small-scale medical monitoring sensors, body energy harvesters produce unreliably small amounts of power and, moreover, mostly at low voltages. Furthermore, local processing operations in body sensor nodes can be power-hungry. Therefore, designing an optimized architecture with an ultra-low-power custom integrated circuit is an inevitable choice.

The conversion of small output voltages, in the range of a few tens of millivolts, has already been achieved but with low efficiency [63]. In this chapter, a detailed design procedure of an optimal integrated power converter [86, 87] aimed at an autonomous EEG or ECG active electrode in a body-powered system will be presented. The procedure is based on the examination of power losses and power transfer in the power converter system and its circuit blocks. In the literature, the loss analysis of converters has been used for the study of power converter characterization [63, 88]. Recently [65], this analysis has been used for optimizing specific circuit parameters such as switch sizes or frequency, independently, for a fixed architecture and a transducer. However, in a body-powered system, different types of transducers with diverse electrical specifications are used, and for that reason, a design procedure has to be adopted so that the resulting converter can work optimally with different types of transducers. Additionally, the procedure by itself should be algorithmic based on transducer characteristics. This feature is beneficial when different specific optimized power converters are needed for a different set of transducers. A step-by-step design method is crucial to saving design time.

One important reason to migrate to a battery-less system was the small form factor requirement for such a system, since batteries set the entire volume of an electronic integrated device. Therefore, the form factor limit of the application has to be considered in designing the power converter.

In this chapter, the design process for a more efficient converter system based on the transducers' characteristics and the system form factor will be discussed. The procedure is introduced based on a formula that will be derived for loss and power transfer in the converter, as well as derived efficiency limits imposed by the transducers' specifications. Since a converter is needed for different transducers, inflexible converter parameters is designed for the worst-case scenario, while others can be reconfigured in a way that the extracted equations suggest. Therefore, the converter can work optimally with different types of transducers with different specifications and can keep its efficiency in the conversion of small input voltages, in the range of a few tens of millivolts.

This chapter is organized into five sections. Section 3.2 introduces the design method for the converter. Section 3.3 describes a circuit design method based on the system specifications introduced in section 2.2. The measurement results are presented in section 2.4, followed by a discussion of the conclusions drawn from these results.

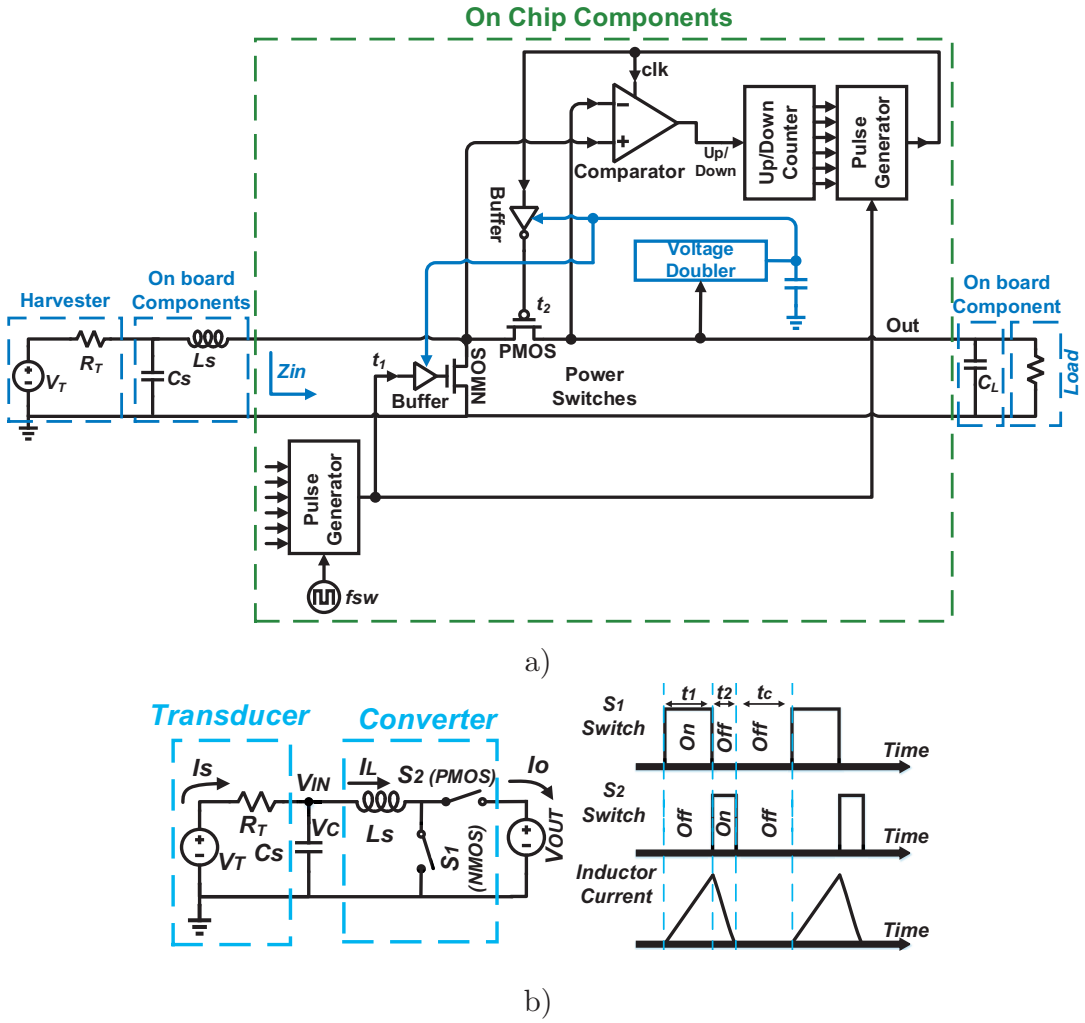


Figure 3-1: a) General architecture of a converter [65, 70, 72] and b) its basic schematic, and timing diagram.

3.2 Efficient power converter design

Figure 3-1 a) shows the typical modern discontinuous conduction mode (DCM) power converter architecture [65, 70, 72] considered in this work. The timing diagram for such a converter is shown in Figure 3-1 b). In this architecture, the harvester with the open-circuit output voltage V_T charges the input capacitor C_S for duration t_C while both the NMOS and PMOS switches are off. Then the NMOS transistor is turned on, the PMOS transistor is kept off, and the harvested energy stored in C_S is transferred to the inductor L_S during period t_1. After t_1, the NMOS is turned off and the PMOS is switched on, so the energy will be transferred from L_S to the final load during period t_2. This process is repeated at frequency f_{SW}.

Duration lengths t_1 and t_2 are set by two dedicated pulse generators. In the DCM mode, the PMOS is turned off at the end of t_2 exactly when the current in the inductor reaches zero; consequently, the DCM architecture avoids a negative current flow in the inductor. In an ultra-low-power scheme, if the source current is continuously being transferred to the load by switches and energy storage elements, the average transfer current would be practically insignificant. An average current might be comparable with the leakage current of the switches that are conducting the transfer current. Therefore, for a low-power application, DCM converters have a higher efficiency than converters that transfer current continuously, working in the continuous conduction mode (CCM).

A pulse generator and a comparator are used to synchronize the switching off of the PMOS. The comparator in Figure 3-1 a) is activated by the falling edge of pulse t_2, and compares the voltage at both ends of the PMOS switch at the moment that the PMOS transistor is turned off. Consequently, it detects whether the PMOS is turned off early or late at the end of t_2. If the left side of the switch has a higher voltage than the right side, it means that the switch has been turned off too early and vice versa. Based on the output signal of the comparator, the pulse width of t_2 is tuned by the counter and the pulse generator dedicated to t_2. For example, if the switch is turned off too late, according to Figure 3-1 a) the comparator sends a high state to the following counter to elevate one bit in the counter's output. The output of the counter controls the pulse length of the pulse generator. With a higher value at the output of the counter, the pulse generator produces a wider pulse, and therefore the feedback loop will correct the switching pulse widths for the PMOS transistor. This procedure is repeated on every cycle until the pulse duration causes the PMOS to be turned off slightly early. Then, the counter starts to count in the reverse direction and it decreases the pulse duration. Since it is almost impossible to have a pulse length precisely equal to the duration needed, the LSB of the counter toggles from this moment while the other bits and feedback get locked.

Here, circuit blocks including the analog comparator are activated only when they are triggered by clock signals. Apart from this architecture, in the literature, controlling the PMOS switch with analog implementations [89] or digital loops [76] is common. In analog implementations, the switch acts as an active diode. It means that a comparator continuously monitors the voltage across the switch and turns the switch off as soon as the voltages at both ends are the same; i.e., the current of the switch reaches zero. Although this method makes the system simpler, it requires a high speed comparator which is undesirable in an ultra-low-power application. On the other hand, even though pure digital circuit control loops may create highly precise pulses for the switch, digital circuits and the analog-to-digital conversion

process are extremely power-hungry and make the system complex. Accordingly, the architecture employed here offers a proper compromise between a continuous analog control loop and a power-hungry precise digital control loop, thus minimizing the system's quiescent power consumption.

3.2.1 Power transfer and power loss in a low-voltage power converter

In addition to the system's quiescent power consumption, power transferred to the system from the source contributes to the system's efficiency. Presuming there are low loss onboard components and a big onboard inductor L_S, the energy transferred from the source to the converter system can be written as:

$$E_T = \frac{L_S I_P^{\,2}}{2} + \frac{V_{IN} I_P t_2}{2}, \tag{3-1}$$

where the first term and second term are related to the energy transmitted from the source during t_1 and t_2 from source, respectively. V_{IN} is the converter input voltage, and I_P is the peak current of the inductor in Figure 3-1 b). Simplifying equation (3-1) by knowing $I_P = t_1 V_{IN}/L_S$, the transferred power can be expressed as:

$$P_T = f_{SW} E_T = V_{IN}^{\,2} \left[f_{SW} \left(\frac{t_1^{\,2}}{2L_S} + \frac{t_1 . t_2}{2L_S} \right) \right]. \tag{3-2}$$

In equation (3-2), the statement in brackets can be interpreted as the system input admittance. To maximize power transfer, the input impedance of the system, Z_{in}, should be matched to the harvester impedance, R_T. If it is assumed that t_1 is much longer than t_2 (it will be shown in section 3.3 that this is in fact true here), the input impedance can be written as:

$$Z_{in} \approx \frac{2L_S}{t_1^{\,2} f_{SW}}. \tag{3-3}$$

Therefore, Z_{in} is related to t_1 and is tuned by the pulse generator dedicated to t_1.

Although the active circuit block's power consumption is important in determining efficiency, the switching mechanism has a high impact on system losses. Switching losses can be divided into static losses related to the "on"-resistance of switches, dynamic losses including the charging and discharging losses of switches' gates and buffers' gates, and leakage loss. The switch leakage loss is given by the product of the switch leakage current [90] and the voltage difference across the terminals of the switch:

$$P_{leakage} = v_{DS}\left(\mu_0 C_{ox}\frac{W}{L}(m-1)V_t^2 .e^{\frac{(v_{GS}-v_{th})}{m.V_t}}\left(1-e^{-\frac{v_{DS}}{V_t}}\right)\right), \tag{3-4}$$

where μ_0, C_{ox}, W, L, V_t, and m are the carrier mobility, gate-oxide capacitance, width, length, thermal voltage, and slope shape factor of the switch, respectively. v_{DS} is the drain-source voltage, v_{GS} is the gate-source voltage, and v_{th} is the threshold voltage of the switch.

In the converter system, two switches are responsible for transferring power from the source to the load. The NMOS switch has a leakage current from the converter input; the PMOS leakage comes from the converter output. The input voltage of the converter is so small that it makes the last term in the leakage current expression for the NMOS transistor negligible. Additionally, a small voltage difference across the NMOS switch (the first term of equation (3-4)) causes the leakage power of the NMOS transistor to get much smaller than the PMOS transistor. However with a reasonable transistor sizing, in the microwatt power scheme, an examination has shown that PMOS power leakages do not have a major effect on efficiency, since its leakage is on the order of tens of nanowatts. A simplified loss of the converter switches can then be stated as:

$$P_{Loss} = I_{Ls,RMS,t1}{}^2\left(\mathrm{R}_{NMOS}+\mathrm{R}_{PMOS}\frac{t_2}{t_1}\right)+f_{SW}V_{SW}{}^2\eta_{SW}\left(1+\frac{1}{\alpha}\right)(C_N+C_P), \tag{3-5}$$

where the first term in the equation represents static power and the second term corresponds to dynamic loss. R_{NMOS}, C_N, R_{PMOS}, and C_P are the channel's resistance and the effective gate's capacitance of the NMOS and PMOS switches, respectively. The ratio of the switch sizes to the size of the buffers that drive the switches was introduced by α. V_{SW} is the switching voltage, and η_{SW} is the efficiency of the circuit that provides this switching voltage. If a switching voltage is supplied directly by the output voltage of the converter, η_{SW} becomes equal to one. However, if a circuit such as the voltage doubler depicted in Figure 3-1 a) provides the switching voltage, η_{SW} will be the voltage doubler's efficiency.

The gate capacitances are directly related to the dynamic loss. The gate capacitor of a transistor biased in the depletion mode or in the cut-off region has a small value that is equal to two gate-junction overlap capacitors. When the gate voltage exceeds the transistor's threshold voltage, the transistor's channel is inverted, and the capacitance increases abruptly. The value of the capacitance becomes comparable to that of a gate-oxide capacitor. The dynamic power dissipation in gate capacitance $P_{D,CG}$ then can be calculated as:

$$dP_{D,CG} = f_{SW}.d(\mathrm{V}_{SW}\mathrm{Q}_G)\,. \tag{3-6}$$

The gate capacitor is charged by the constant voltage V_{SW}. The capacitor's charge Q_G can be written as a product of the capacitor voltage V_G to its capacitance. If the gate's capacitance is named C_{OV} and C_O in the depletion and inversion regions, respectively, the power dissipation can be written as:

$$P_{D,CG} = f_{SW}\left(\int_0^{V_{th}} V_{SW}C_{OV}dV_G + \int_{V_{th}}^{V_{SW}} V_{SW}C_O dV_G\right). \tag{3-7}$$

Since the overlap capacitance C_{OV} is negligible with regard to the oxide capacitance C_O, equation (3-7) can be simplified as follows:

$$P_{D,CG} \approx f_{SW}{V_{SW}}^2 C_O\left(1-\frac{V_{th}}{V_{SW}}\right). \tag{3-8}$$

Considering the technology used for the power converter, equation (3-8) agrees with the gate capacitance variation study carried in [91]. The value of $C_O(1-v_{th}/V_{SW})$ is named the effective gate capacitance and is estimated in this chapter to be half of the gate-oxide capacitance.

On the other hand, the static loss term in the equation (3-5) was directly related to the root-mean-squared (RMS) current through L_S. The current can be written as:

$$I_{Ls,RMS,t1} \approx \frac{V_{IN}}{\left(L_S f_{SW}\right)^{1/4} {Z_{in}}^{3/4}}\,. \tag{3-9}$$

This simplified closed-form equation was obtained using equation (3-3) and was written assuming that V_{IN} is almost constant during inductor charging. However, V_{IN} might vary during charge transfer. The exact current–voltage relations for the schematic shown in Figure 3-1 b) were derived and verifies the inductance–current behavior of equation (3-9).

Equation (3-8) and equation (3-9) give better insight into the converter loss sources. Then, it may be possible to find an operating point where the losses are minimized.

3.2.2 Loss optimization

From equation (3-5) and equation (3-9), it is clear that the inductance value is directly involved in the losses and that, in order to have maximum efficiency, the biggest possible inductance should be selected. However, the system form factor confines the inductance value. Besides the inductance value, the ohmic loss of the inductor should be negligible compared to the available power. Equation (3-9) suggests that the RMS current through the inductor can reach 5 mA when a transducer with the lowest voltage (from Table 2-5) with 40 μW of the available output power is used at the input of the converter. Therefore an inductor with an ohmic resistance of less than 0.2 Ω must be used to have a loss of less than 10% of the available power because of the inductor ohmic loss.

In this project, with our PCB restricted to 1.2 × 1.2 cm, there is room for a converter's chip on one side of the board and other external elements on the other side. An area of 0.8 × 0.8 cm is dedicated to the inductor, and the largest possible low-resistance inductor within this package size has an inductance of 47 μH with an ohmic resistance of less than 0.15 Ω. Losses resulting from the parasitic capacitance of the inductor are about 0.1 μW, less than 10% of the lowest available power.

There is a trade-off in switch sizing. Widening the switch transistors decreases their channel resistance, but increases their gate capacitance. Indeed, the static power losses decrease with wider switches although the dynamic power consumption increases. However, both static and dynamic losses rise with switches that have longer lengths. By keeping the length of the switch transistors to a minimum, the only adjustable switch design parameter is their width. To find the optimum switch sizing for each working frequency, the following two equations have to be solved.

$$\begin{cases} \dfrac{\partial P_{Loss}}{\partial W_n} = 0 \\ \dfrac{\partial P_{Loss}}{\partial W_p} = 0 \end{cases}, \tag{3-10}$$

where W_n and W_p are the widths of the NMOS and PMOS switches. As was stated before, each onboard parasitic loss, including inductor ohmic loss and its dynamic parasitic capacitance loss, was less than 10% of the available power, and was independent of the transistors' sizes. Switch leakage losses are ignored in the power loss equation (3-5) since their contribution to the total loss is negligible. Then the optimum NMOS switch width $W_{n,opt}$, and PMOS switch width $W_{p,opt}$ can be derived as:

$$W_{n,opt} = I_{Ls,RMS,t1}\sqrt{\frac{R_{NMOS,0}}{f_{SW}\beta C_{N,0}}},$$
$$W_{\mathrm{p},opt} = I_{Ls,RMS,t1}\sqrt{\frac{t_2}{t_1}\frac{R_{PMOS,0}}{f_{SW}\beta C_{P,0}}}, \quad \beta = V_{SW}{}^2\eta_{SW}\left(1+\frac{1}{\alpha}\right), \tag{3-11}$$

where $R_{NMOS,0}$, $C_{N,0}$, $R_{PMOS,0}$, and $C_{P,0}$ are the resistance and capacitance per unit width for the NMOS and PMOS transistors, respectively.

As is clear from equation (3-11) and equation (3-9); the optimal values for the switches depend on the converter's input voltage. When optimal switch sizes are set for a specific type of transducer, they cannot be changed when a different transducer is connected to the system. Therefore, from an efficiency point of view, it is better to optimize the power converter switches for the worst working condition of the transducers introduced in section 2.3. The efficiency η of the converter can be written as:

$$\eta = \frac{P_L - P_Q}{P_{\mathrm{ave,S}}}, \tag{3-12}$$

where P_L, P_Q, and $P_{ave,S}$ are the output power, system power consumption, and maximum power available from the source, respectively.

In a well-designed system for an ultra-low-power scheme, P_Q should be negligible compared to P_L. The output power can be written as the difference between the transferred power P_T from equation (3-2) and the entire power loss P_{Loss} from equation (3-5). Considering equation (3-11) along with equation (3-5) it can be concluded that the transistors' optimum widths are located at the point where the switches' static losses and switches' dynamic losses are equal. Hence, to find the efficiency limit for the system, equation (3-12) can be modified by considering equation (3-2), equation (3-5) and equation (3-11) as follows:

$$\eta_{\max} = \frac{V_{in}{}^2 Z_{in} - 2I_{Ls,RMS,t1}{}^2\left(\mathrm{R}_{NMOS} + \mathrm{R}_{PMOS}\frac{t_2}{t_1}\right)}{P_{\mathrm{ave,S}}}, \tag{3-13}$$

where the first term in the numerator is the maximum input available power from the source. Therefore, equation (3-13) can be simplified as below.

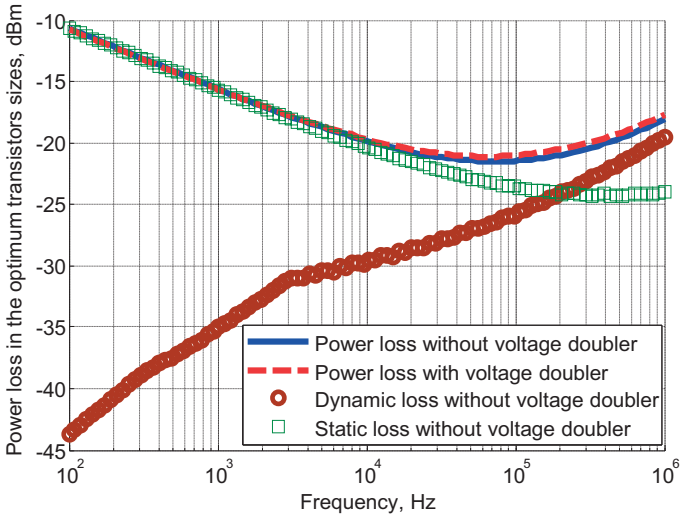


Figure 3-2: Optimum power loss for optimized switch sizes versus frequency.

$$\eta_{\max} = 1 - 4\frac{Z_{in}^{1/4}}{V_{in}}\left(\frac{f_{SW}}{L_S}\right)^{1/4}\left(\sqrt{\mathrm{R}_{NMOS,0}\,\beta C_{\mathrm{N},0}} + \sqrt{\mathrm{R}_{PMOS,0}\,\beta C_{\mathrm{N},0}\,\frac{t_2}{t_1}}\right). \tag{3-14}$$

Equation (3-14) demonstrates that, at each working frequency, the maximum achievable efficiency has an inverse relationship with the transducer characteristics $Z_{in}^{1/4}/V_{IN}$, which is the transducer efficiency bound (TEB), given that the other parameters are constant. Here, the macro TEG (TEG1 from Table 2-5) which has an open-circuit output voltage of only 20 mV can have a lower maximum achievable efficiency since it has a much higher TEB compared to the other TEGs. Consequently, the switches will be optimized for the TEG1 case.

Once the power switches have been designed and set for the worst-case scenario, the optimum working frequencies $f_{\mathrm{SW,Opt}}$ for the other operating cases can be calculated from equation (3-11).

$$f_{SW,Opt} \approx \left(\frac{V_{IN}^{\ 4}}{L_S}\right)^{1/3}\frac{\delta}{Z_{in}}, \tag{3-15}$$

where δ is a constant related to the designed switches' resistance and capacitance.

By considering the losses that were not included in equation (3-5), such as onboard component parasitics and leakages, the power loss of the converter with the low voltage transducer was numerically extracted and is drawn in Figure 3-2 for $W_{n,opt}$ and $W_{p,opt}$ at each f_{SW}. Figure 3-2 confirms that the converter loss is minimized at the point where the dynamic loss and static loss are almost equal.

3.2.3 Power transfer optimization

Equation (3-1) shows that the amount of transferred power from a transducer to a converter is directly related to the inductor peak current for an impedance-matched converter. In the ideal case that an extremely high inductance is used in the system and V_{IN} is constant, the inductor peak current $I_{p,peak}$ increases linearly as a function of t_1.

$$I_{p,peak} = \frac{V_{IN}.t_1}{L_S}. \tag{3-16}$$

Equation (3-16) indicates the highest achievable inductor peak current for the converter. Nevertheless in the actual case, a limited energy stored in C_S charges L_S which has a limited value. Therefore, the actual peak current is deviated from the value given by equation (3-16). The inductor current i_{char} and capacitor voltage $v_{Cs,t1}$ during t_1 has been derived as below.

$$i_{char} = \left[\mathrm{V_0 e^{-t\beta}\cos(\omega t) + \left(\frac{V_t - V_0/2}{Z_{in} C_S \omega} + \frac{i_0}{C_S \omega} \right) e^{-t\beta}\sin(\omega t) - V_t} \right] / Z_{in} + C_S \times \ldots \tag{3-17}$$

$$\left[-\mathrm{V_0}\beta \mathrm{e^{-t\beta}\cos(\omega t) - \omega V_0 e^{-t\beta}\sin(\omega t)} + \left(\frac{\mathrm{V_t - V_0/2}}{Z_{in} C_S \omega} + \frac{\mathrm{i_0}}{C_S \omega} \right) \left(-\beta \mathrm{e^{-t\beta}\sin(\omega t)} + \omega \mathrm{e^{-t\beta}\cos(\omega t)} \right) \right]$$

$$\mathrm{v_{Cs,t1} = V_0 e^{-t\beta}\cos(\omega t) + \left(\frac{V_t - V_0/2}{Z_{in} C_S \omega} + \frac{i_0}{C_S \omega} \right) e^{-t\beta}\sin(\omega t)} \tag{3-18}$$

$$\text{with } \beta = \frac{1}{2 Z_{in} C_S}, \quad \omega_0 = \frac{1}{\sqrt{L_S C_S}}, \quad \omega = \sqrt{\omega_0^2 - \beta^2},$$

where V_0 and i_{01} are the capacitor C_S voltage and inductor current at the end of the t_C, respectively, and are used as initial conditions. R_S is the resistance of L_S. The term i_0 is equal to zero for a converter that works in DCM. The initial condition V_0 can be found by calculating the C_S voltage $v_{Cs,tc}$ during t_C.

$$v_{Cs,tc} = V_t \left(1 - e^{\frac{-t}{Z_{in} C_s}} \right) + V_{01} e^{\frac{-t}{Z_{in} C_s}}, \tag{3-19}$$

where V_{01} is the voltage of capacitor C_S at the end of t_1.

The inductor peak current I_p at the end of t_1 is inversely related to f_{SW}, L_S, and C_S. If the system has a low working frequency f_{SW}, I_p may reach a small value in

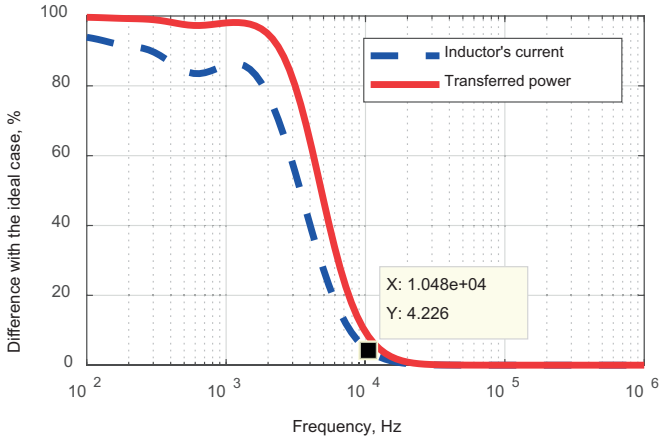


Figure 3-3: The difference between the actual and the ideal inductor peak current, and the difference between the actual and ideal transferred power.

comparison to $I_{p,peak}$, and consequently, the transferred power is decreased. With regard to the form factor, which limits the board area to the size of one EEG or ECG electrode, and moreover, limits the speed of the converter, as will be discussed in the next chapter, a ceramic capacitor C_S with a capacitance of 22 µF was selected. This is the largest commonly available capacitor with a size of 1.6×0.8 mm^2.

The difference between the inductor current at the end of t_1 from equation (3-17) and the maximum inductor peak current $I_{p,peak}$ is sketched against the working frequency in Figure 3-3 in percentage, for an assumed 22 µF C_S and 47 µH L_S. Figure 3-3 illustrates that when the working frequency is increased past 10 kHz, the difference between the actual and the maximum inductor peak current is less than 5% of $I_{p,peak}$, so the actual transferred power would be just less than 10% of the maximum possible transferred power.

On the other hand, the static loss from equation (3-5) is directly related to the peak current $I_{p,peak}^2$ from equation (3-9) and equation (3-16). Therefore, it is expected that, with a reduction in the inductor peak current, the static loss and the converter's total power loss will decrease as well. The static loss and the converter's total power loss calculated with the actual inductor current derived from equation (3-18) are redrawn in Figure 3-4. Losses are minimized when f_{SW} is around 1 kHz (or lower, near 100 Hz), and losses increase almost linearly with increasing working frequency. With a frequency lower than 1 kHz and a C_S of 22 µF, equation (3-18) and Figure 3-3 demonstrate that the difference between the inductor peak current and its ideal case is significant, and almost no power is transferred to the converter.

Figure 3-4: Optimum power loss for optimized switches' sizes versus frequency.

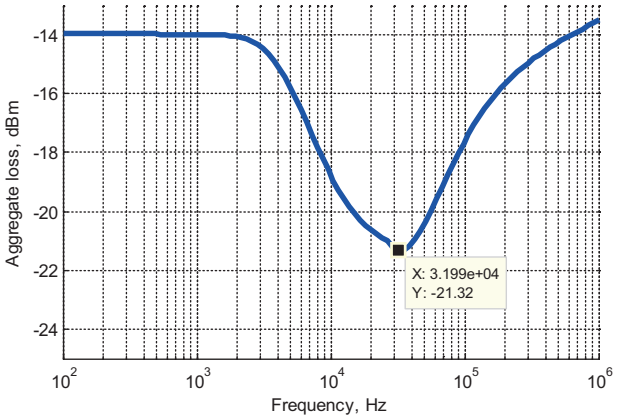


Figure 3-5: Converter aggregate loss versus frequency for TEG1.

Therefore, to find an optimized working frequency both the losses and power transfer have to be considered. Figure 3-5 shows aggregate losses calculated from equation (3-5), and losses that result from flawed power transfer to the converter. As this figure illustrates, the optimum working frequency for minimum aggregate losses is located around 30 kHz. The optimum frequency is less than the 100 kHz that was obtained in Figure 3-2 when the actual power transfer was not considered.

3.2.4 Switch sizing optimization

The "on"-resistance and leakage loss of the switches are inversely related to the switches' gate voltages. A voltage doubler is usually used to provide a higher gate voltage. The output of the voltage doubler is stored on on-chip capacitors. The on-

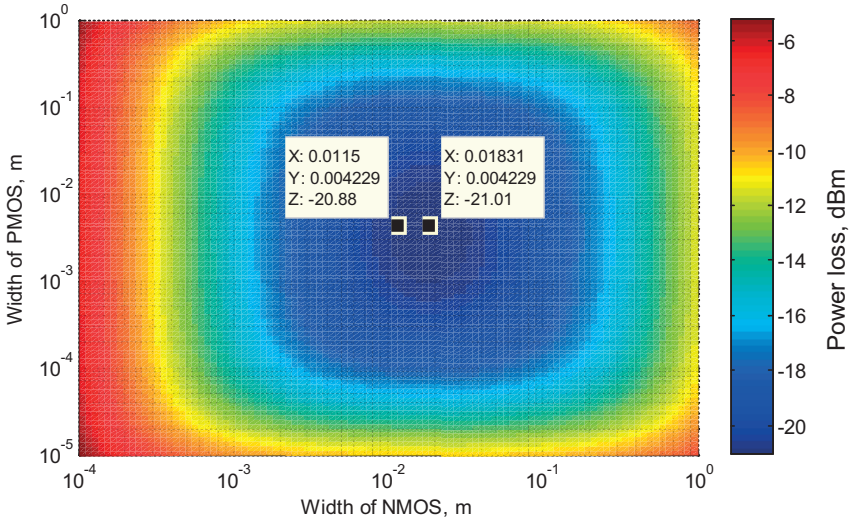


Figure 3-6: Power loss as a function of switches' sizes at the optimum working frequency.

chip capacitance of the voltage doubler must be large since it has to supply enough energy for the power transistors. The voltage doubler will occupy more than 50% of the area of the power converter because of its on-chip capacitors. As Figure 3-2 demonstrates, if the voltage doubler is removed, the power loss remains constant. In this case, the optimal size for the switches will be bigger than the system with a voltage doubler.

Power loss as a function of switch sizes for the selected f_{SW} while considering all losses without a voltage doubler is shown on Figure 3-6. The optimal widths of NMOS and PMOS for the selected f_{SW} induce large parasitics and make it hard to draw a compact layout. By accepting a deviation of less than 5% from the optimum (Figure 3-6), a 40% smaller transistor with a reasonable width can be achieved. With this technique, the area of the chip taken up by the switches is 30% larger, but the overall circuit area is reduced by 20%, and the complexity is drastically reduced.

3.3 Circuit design for the system specifications

In designing an ultra-low-power system, the aim is to maintain a high efficiency while keeping the system as simple as possible. This section will describe how circuit blocks were designed and implemented to fulfill the specifications of an efficient system as described above.

In this design a DCM architecture was employed due to its higher achievable efficiency. An adaptive length pulse generator coupled with a comparator was used

to precisely synchronize the PMOS switch turn off with the moment the current in the inductor reaches zero. A low-complexity track-and-latch comparator structure consuming less than 100 nW at 20 kHz was chosen here, since speed is not a major concern; indeed, the working frequency is a few kHz and the comparator's output voltage has to be ready only at the next clock cycle.

3.3.1 t_2 pulse generator design

The inductor discharge duration t_2 can be calculated by solving the inductor current equation. With analysis of the schematic in Figure 3-1 b), the inductor's current during discharge i_{dis} to the output capacitor can be written as:

$$\begin{aligned} i_{dis} &= i_{01}e^{\beta t}\cos\omega t + \frac{V_{01}-V_{02}-Ri_{01}/2}{L\omega}e^{\beta t}\sin\omega t \\ \text{with } \beta &= \frac{1}{2R_sC_L},\quad \omega_0 = \frac{1}{\sqrt{L_sC_L}},\quad \omega = \sqrt{\omega_0^{\,2}-\beta^2}, \end{aligned} \tag{3-20}$$

where V_{01}, V_{02}, and i_{01} are the capacitor C_S voltage, capacitor C_L voltage, and the inductor current at the end of t_1, respectively. To find the initial condition related to C_S and L_S, equation (3-17), equation (3-18), and equation (3-19) are used. By putting i_{dis} equal to zero and considering that the argument of the trigonometric function is small, the equations can be approximated by the Taylor series, and t_2 can be found as:

$$t_2 \approx \frac{t_1.V_{IN}}{V_{OUT}}. \tag{3-21}$$

A t_2 pulse generator has been implemented to enable the system to provide an output voltage in a range of 1 V to 2 V from the converter input. The measured specifications of the mm-scale TEGs shown in Table 2-5 suggest TEG1 and TEG2 produce about 20 mV and 100 mV as open-circuit output voltages, when they harvest energy from a human body in a normal environmental condition. Then, the input voltage will be 10 mV and 50 mV for TEG1 and TEG2 with an impedance-matched converter. A safety margin between one half and two times that of the transducer output voltage is considered in designing the t_2 pulse generator.

For TEG1 at 20 mV and the determined optimum working frequency, t_1 has to be about 30 µs for an impedance-matched converter from equation (3-3). However, when the output voltage of the transducer changes from 10 mV to 40 mV, according

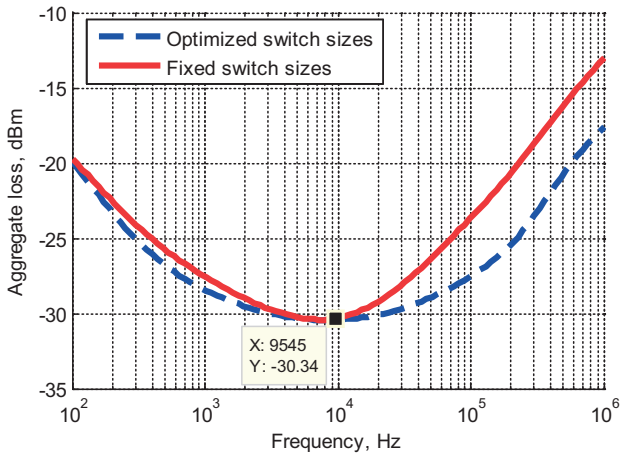


Figure 3-7: Converter aggregate loss versus frequency for TEG2.

Table 3-1: Design specifications of t_1 and t_2.

	V_{in}	f_{SW}	t_1	V_{OUT}	t_2
TEG1	5—20 mV	25—35 kHz	40—25 µs	1—2 V	100—500 ns
TEG2	25—100 mV	3.4—24 kHz	12—4.7 µs	1—2 V	150—460 ns

to equation (3-5) and equation (3-17) the optimal working frequency shifts from 25 kHz to 35 kHz and consequently t_1 has to be adjusted from 40 µs to 25 µs.

The same optimization procedure was followed for TEG2 as well. TEG2's aggregation loss with the optimized switch widths for each frequency is sketched in Figure 3-7. Since the switch sizes were determined based on the worst-case scenario, the aggregation loss is plotted as well for the fixed switch sizes. The minimum aggregate loss frequency for the transducer's open-circuit nominal output voltage, which is around 100 mV in both cases, is almost the same and is located at 10 kHz (Figure 3-7). In this case, an impedance-matched converter charges its inductor for 7 µs. Meanwhile, if the transducer's output voltage moves from 50 mV to 200 mV, the optimal frequency for minimum aggregation loss varies from 3.4 kHz to 24 kHz; consequently, the inductor charge duration decreases from 12 µs to 4.7 µs. These system specifications and the calculated value of t_2 from equation (3-21) are summarized in Table 3-1.

The interval t_2 has to be generated precisely. If t_2 is too short, the energy stored in the inductor L_S will not be completely transferred to the load, and if t_2 is too long, reverse energy will be transferred from the load to L_S. If the error in the length of t_2 is defined as t_{err}, the loss $P_{dis,loss}$ caused by this error is related to t_{err} and in the worst case it is given by:

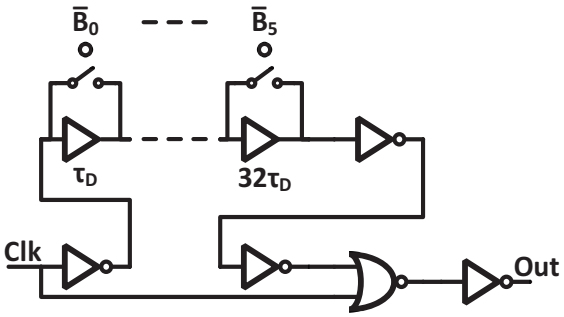


Figure 3-8: Pulse generator schematic.

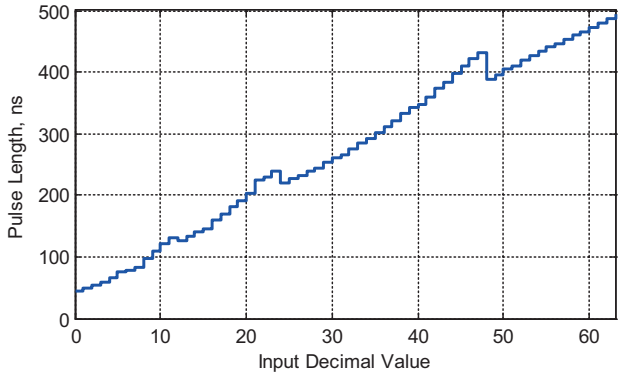


Figure 3-9: Length of generated t_2 pulses for each input of the pulse generator.

$$\frac{P_{dis,loss}}{P_{dis}} = \frac{t_{err}}{t_2}. \tag{3-22}$$

If a loss of less than 10% is required in the worst case at this stage, and considering that the shortest duration of t_2 is 100 ns, a t_{err} smaller than 10 ns is needed. By designing an appropriate pulse generator providing pulses with durations of 100 ns to 500 ns (from Table 3-1) with steps smaller than 10 ns, the system will be efficiently functional with different transducers with less than a few hundreds of millivolts of open-circuit output voltages. The schematic of the pulse generator employed here is shown in Figure 3-8. It consists of a NOR gate[1] with both inputs connected to the same signal but with one input that has a configurable delay. Delay blocks are formed by a capacitor and binary weighted on-chip resistors. Transmission gate switches are used to bypass binary weighted delay cells to keep the switch functionality and its resistance independent of charging the capacitor of the delay cells. For such a pulse generator, the required number of bits N can be calculated as follows:

[1] A Digital logic gate that implements logical NOR.

$$t_{err} = \frac{\text{Maximum pulse length}}{2^N}. \tag{3-23}$$

By solving equation (3-23) it can be determined that a minimum of 5.3 bits are needed here. Therefore, a 6-bit variable delay generator has been designed to generate t_2. The pulse lengths as a function of input bits are depicted in Figure 3-9. As can be seen in Figure 3-9, pulses with durations between 44 ns and 480 ns are generated and the average of t_{err} is equal to 7 ns. Due to the delay generated by the CMOS transmission gate switches, the output of the pulse generator is not completely monotonic. The maximum deviation between the ideal and the actual output is 21 ns. This value is higher than the expected t_{err}. However, the maximum error and the major non-monotonic behavior happens when the pulse length is about 400 ns (Figure 3-9). Therefore, the resultant loss according to equation (3-22) in the worst case is negligible in comparison to the power transferred at this point, although these issues are solved by changing the CMOS switches in the circuit that is designed in the next chapter.

The range of generated pulse lengths here is also slightly narrower than expected. The pulse generator can lock over the entire considered TEG2 output voltage range, while in the case of TEG1, the lock range is limited to 37 mV instead of 40 mV. These ranges are wide enough for typical small-scale energy harvesting from a human body. The power consumption of this pulse generator is less than 200 nW at 25 kHz. Such conservative circuit implementations allow the system to work around its optimum point when the input voltage varies depending on the environment, or even when a higher voltage TEG is used as a transducer.

3.3.2 t_1 pulse generator

A similar approach is taken for designing the t_1 pulse generator. The only change is the difference between the required pulse lengths for TEG1 and TEG2 as defined in Table 3-1. The pulse generator is designed to produce the required t_1 pulses just for TEG2. Considering the desired frequencies and t_1 lengths needed for TEG1 from Table 3-1, it can be inferred that an inverted output of this pulse generator can be used for TEG1. Therefore, a simple inverter gate placed at the output of pulse generator t_1 will make it able to generate the required pulse for TEG1 as well. By implementing a one bit multiplexer, it is possible to switch between the range delays for TEG1 or TEG2. Measurement results indicate that this 6-bit pulse generator produces pulse lengths from 40 ns to 13.8 μs with an average step of less than 400 ns. The pulse generator's clock (Figure 3-1) is provided by a seven-stage ring

oscillator followed by a level shifter. The oscillator frequency can be manually set by an off-the-shelf resistor with a size of 1.6 × 0.8 mm^2.

3.3.3 Deadtime delay generator

The generated t_1 and t_2 pulses control the power switches through chains of buffers. Buffers drive power switches and create a deadtime between the instant in which NMOS is turned off and PMOS is turned on. An optimum deadtime $t_{D,OPT}$ is the duration that the parasitic capacitance in the transistor's drain node V_D is charged to the power converter output voltage V_{OUT} by the inductor's peak current. If the PMOS transistor stays in the cutoff region more than $t_{D,OPT}$, V_D will be higher than V_{OUT} and the lossy parasitic diode of PMOS may conduct the inductor's peak current. If the voltage drop of the parasitic diode is assumed to be $V_{d,PMOS}$, after t_R duration from $t_{D,OPT}$, the PMOS parasitic diode will be turned on.

$$t_{D,OPT} + t_R = \frac{\left(V_{OUT} + V_{d,PMOS}\right)}{I_P} C_{par}\,, \tag{3-24}$$

where $C_{par,T}$ is the total parasitic capacitance at node V_D.

$$C_{par,T} = C_{par} + \frac{C_j' A_D}{\left(1 - \frac{V_{BD}}{\phi_j}\right)^{m_j}} + \frac{C_{jw}' P_D}{\left(1 - \frac{V_{BD}}{\phi_{jSW}}\right)^{m_{jSW}}}\,, \tag{3-25}$$

where C_{par} is the inductor and the converter chip parasitic capacitance, and C_j and C_{jw} are the zero-bias drain bottom-well capacitance and side-wall capacitance per unit area and length, respectively. A_D and P_D are area and perimeters of the drain. ϕ_j and ϕ_{jSW} are the built-in junction potential and side-wall junction potentials, respectively. V_{BD} is the bulk-drain voltage, and m_j and m_{jSW} are process-dependent constants.

The loss resulting from a deadtime of duration t_i that is longer than $t_{D,\,OPT} + t_R$ can be estimated as:

$$P_{\mathrm{Dh,Loss}} \approx V_{\mathrm{d,PMOS}} I_P \left(t_i - t_{\mathrm{D,OPT}} - t_R\right) f_{SW}\,. \tag{3-26}$$

On the other hand, if the PMOS switch is turned on before $t_{D,OPT}$, an inverse current from the system output capacitance passes through PMOS and charges the drain node parasitic capacitance up to V_{OUT} because of charge sharing. The resulting loss can then be stated as:

Table 3-2: Deadtime ranges for the no-loss condition.

	V_{in}	t_D
TEG1	5 mV	4.4—8.2 ns
	10 mV	2.6—4.6 ns
	20 mV	1.4—2.4 ns
TEG2	25 mV	3—5.6 ns
	50 mV	3—5.6 ns
	100 mV	2—3.6 ns

$$P_{Dh,Loss} = V_{OUT}{}^2 C_{par,T} \left(1 - \frac{t_i}{t_{D,OPT}}\right)^2 f_{SW}\,. \tag{3-27}$$

With the mentioned design parameters and using equation (3-25), the parasitic capacitance $C_{par,T}$ is calculated to be about 24 pF in the worst case. With the calculated parasitic capacitance, equation (3-24), and considering Table 3-1 for TEG1 and TEG2, the deadtime t_D ranges for the no-loss condition were derived and summarized in Table 3-2. The buffer tapering factor of a power converter can be designed as [92] suggested. Here a tapering factor of 6 was considered. Buffers with this tapering factor produce propagation delay of 0.7 ns. The designed buffer chain here creates about 3 ns of deadtime, which is enough to not have any deadtime losses in the typical working conditions of the TEGs, according to Table 3-2. Equation (3-26) and equation (3-27) demonstrate that with the designed buffer chains, the deadtime causes losses of 60 nW and 140 nW in the converter with input voltages 5 mV and 20 mV, respectively, when TEG1 is attached to the power converter input. These calculations and likewise the simulations show that these losses are negligible (less than 10% and 1%, respectively) compared to the input available power from TEG1 with the mentioned voltages at the input of the power converter.

3.3.4 Power switch implementation

The power switches are relatively wide and their "on"-resistance is on the order of 0.1 Ω for NMOS switches and 1 Ω for PMOS. For such low-resistance switches, all parasitic resistance coming from metallic connections and intrinsic transistor parasitics becomes more important and it should be kept below 0.01 Ω. Layout design is critical because each via and metallic square connection introduces a resistance of, respectively, 7 Ω and 65 mΩ. Slightly narrower switches were selected

related to the actual optimum point (Figure 3-6), and in that case static losses are dominant. As a first step in drawing the layout for the switches, smaller but more fingers are selected. This changes the layout parasitic compromise in favor of less parasitic resistance. The NMOS transistor is divided into 24 transistors each of which have 100 fingers. Individual metal layers placed on one finger have a resistance of 2 Ω. For that reason, four metal layers have been stacked on each finger and the layers are connected together with a maximum possible number of via; this means eight here. With this pattern, post-layout simulations show that parasitic resistance in the structure does not have a significant effect on static or dynamic power loss.

3.4 Measurement results and discussion

With the introduced algorithmic design procedure and taking into account the form factor, an ultra-low-power DC–DC converter for the thermal body harvesters was designed in UMC 0.18 μm CMOS technology. It is assumed here that the output energy storage C_L has some charge, which is used to start up the system. This means that the cold-start technique [67, 80, 81] was not considered in the presented work.

The size of C_L set the output voltage fluctuations. Since the output power is on the order of a few tens of microwatts, and working frequency is on the order of a few tens of kilohertz, an output capacitance in the range of nanofarads is sufficient to have less than 10% ripples. However, in batteryless energy harvesting applications, the output power is not continuous and reliable. In the case of a power shortage from the source, a power management system has to send a signal to the other blocks to make them ready to switch into sleep phase or standby mode. For this reason, it is important to have an energy storage as big as possible at the output. Here, it was decided to put a 22 μF output capacitance with a size of 1.6 × 0.8 mm^2.

The area of the power converter is 0.14 mm^2 and its microchip is shown in Figure 3-10. The chip, its on-board components, and the two-sided target PCB shown in Figure 3-11. The chip is placed on a much larger package (44 pins package) than the power converter needs, since several test blocks were added on the chip. Therefore, the size of the PCB will be determined by the external inductor and capacitors. As shown in Figure 3-11 b), the entire PCB can have a size of 9.2 × 10.7 mm^2, which is smaller than the considered active electrode.

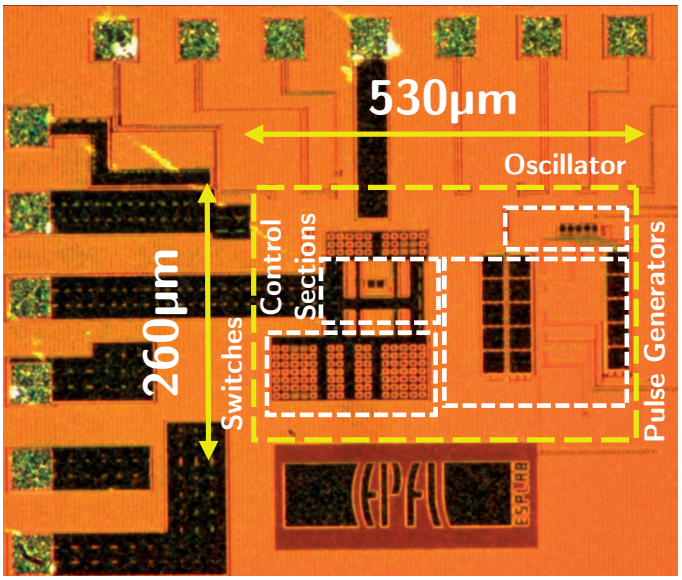
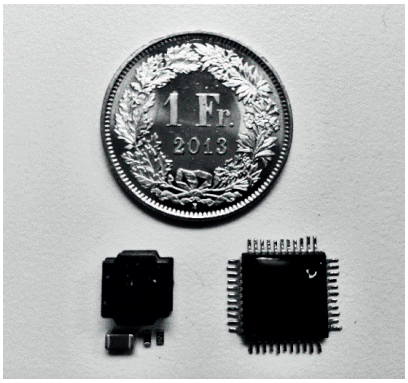
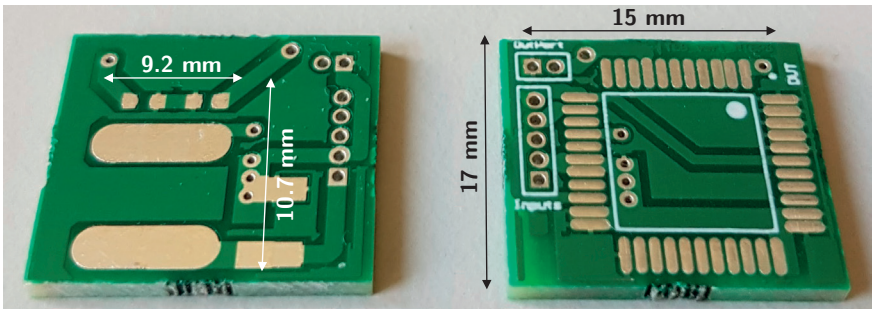


Figure 3-10: Microchip of the converter designed in UMC 0.18 µm CMOS.

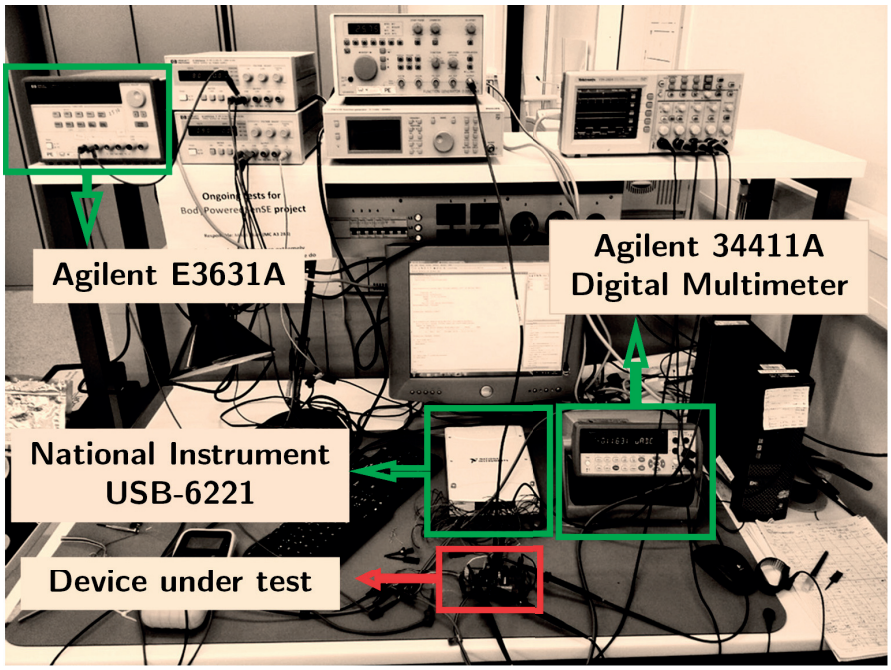


a)

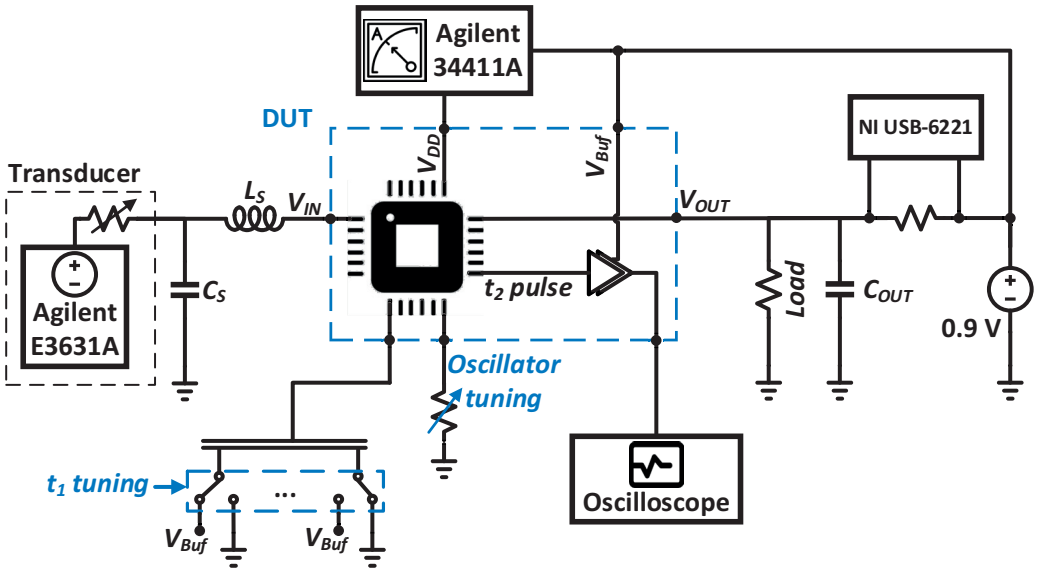


b)

Figure 3-11: (a) All the necessary components for the PCB, including the chip, an inductor, two capacitors and a resistor. (b) A two-sided target PCB fabricated for the chip.



a)



b)

Figure 3-12: a) actual and b) schematic of power converter measurement test setup.

The converter measurment setup is shown in Figure 3-12. The test PCB is larger than the PCB drawn in Figure 3-11 b) since additional test structures were added. For the inductor L_S and the capacitor C_S, a 47 µH onboard inductor and a 22 µF onboard capacitor are used for tests. National Instrument USB-6221 was used for data acquisition and high-precision power measurements in conjunction with an

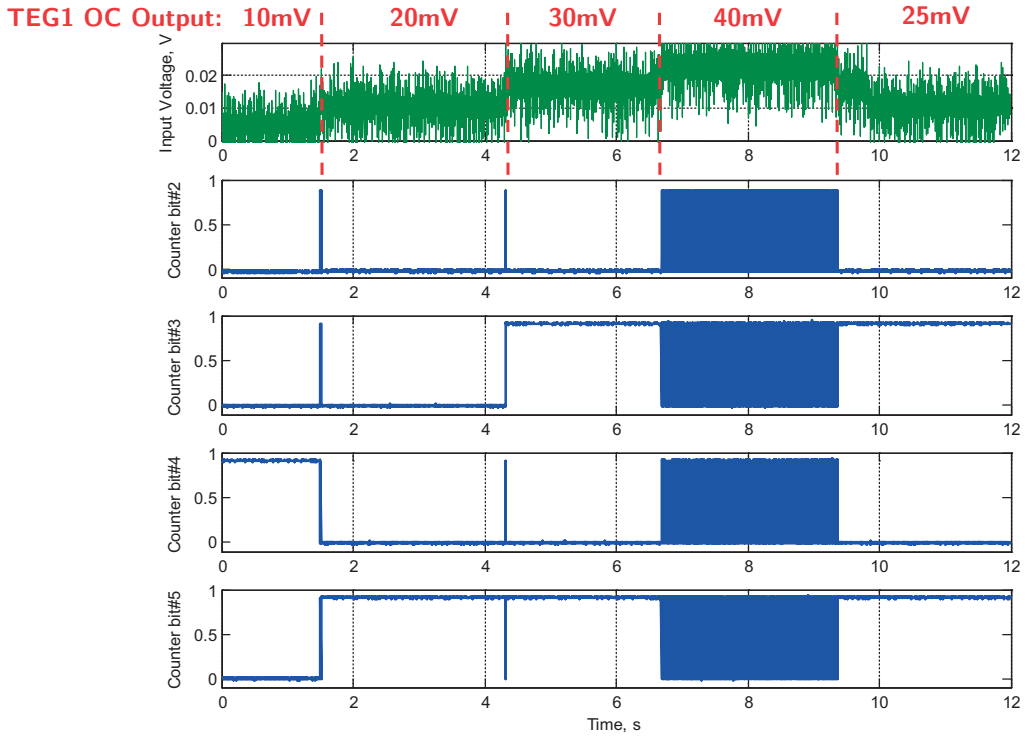


Figure 3-13: The converter input voltage and counter output bits for lock and unlock conditions of the synchronizing feedback.

Agilent 34411A Digital multimeter. To emulate the TEG1 harvester behavior, an Agilent E3631A power supply and a series resistance of 2.65 Ω were used. The digital multimeter has a resistance of 200 Ω when it measures currents in the microampere regime. Another approach for current measurement is to use a resistance that is ten times smaller connected to a high-resolution, high-sampling-rate, analog-to-digital converter of the stated data acquisition system. The former method is easier and faster whereas the latter has more precision. The data reported in this section are extracted with the first method, but important circuit specifications, such as output power, were verified by both.

The converter synchronization feedback can lock the TEG1 output voltage up to 40 mV. As was discussed in section 3.3, lengths of the t_2 pulses are slightly narrower than expected; therefore, the lock range is a little below 40 mV at a frequency of around 30 kHz. As explained in section 3.3, the LSB of the counter in the feedback path is always toggling with the clock. Therefore in a lock situation, pulses generated by the pulse generator t_2 toggle continuously around the desired value. Measurements of the converter's input voltage and input bits of the pulse generator t_2 are depicted in Figure 3-13 for a fixed frequency of around 30 kHz. The

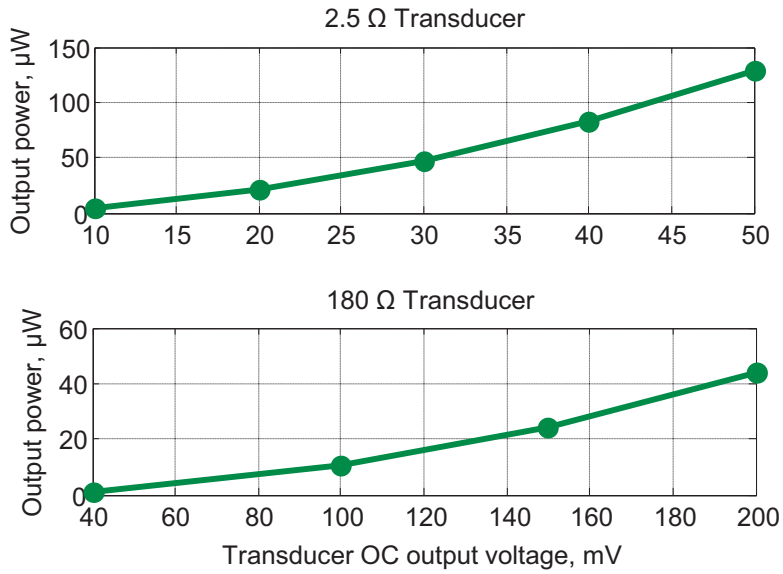
Table 3-3: The counter output and optimum working frequency measurements with the variations in the transducer output voltage.

Transducer output	Counter output (b5 ... b1)	Optimum working frequency
TEG1:		
10 mV	01000	26 kHz
20 mV	10000	28.5 kHz
30 mV	10100	32 kHz
40 mV	11010	39 kHz
TEG2:		
40 mV	01000	7.5 kHz
100 mV	10000	13 kHz
150 mV	11000	15 kHz
200 mV	11110	18 kHz

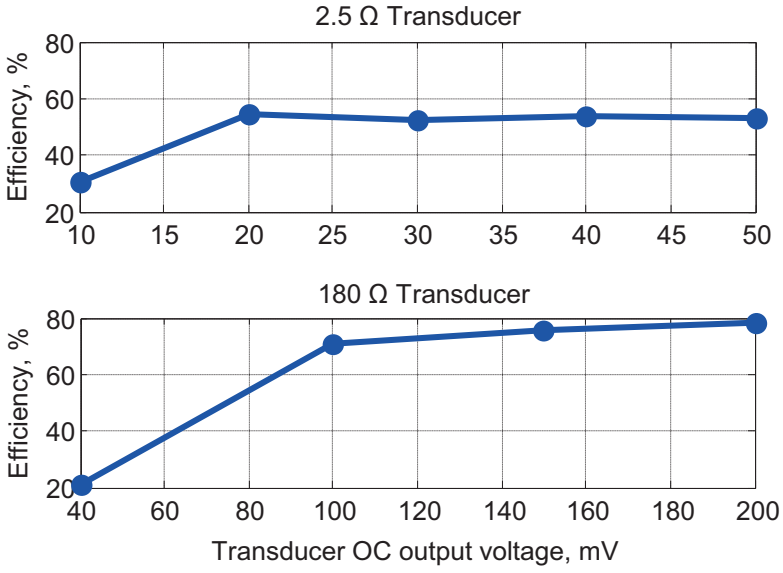
first two LSB of the counter output are not shown. The first bit is constantly toggling and the second bit is sensitive to small input variations.

The measured counter output in the working frequency for which the system efficiency is maximized is reported in Table 3-3 as a function of the transducer output voltage. As shown in this table, with a slight increase over the optimum working frequency calculated for TEG1 at an open-circuit output voltage of 40 mV, and therefore a narrower required duration for t_2, the system can be locked on this operating point as well. In the designed power converter with the fixed-size power switches, the measured optimum working frequencies reported in Table 3-3 can follow equation (3-15), when static loss and dynamic loss are the main contributors in the total loss.

The measurement of the optimal working frequency for TEG1 and TEG2 (i.e. the 20 mV and 100 mV transducer output open-circuit voltage) are 28.5 kHz and 13 kHz. These frequencies are about 5% less and 20% higher than the values calculated and reported in the previous sections. Owing to the dynamic power consumption of the sub-sections, it was expected to have an optimum frequency smaller than the one calculated above. However, the measured optimum frequency is the same as, or slightly higher than, the calculated optimum frequency perhaps because of the methods that were used to change the balance between the dynamic and static losses in favor of less static losses in implementing the switches.



a)



b)

Figure 3-14: Measurements of the converter's (a) output power and (b) efficiency for TEG1 and TEG2.

Measurements of converter output power and its efficiency (defined by equation (3-12)) are illustrated in Figure 3-14 a) and b) as a function of the open-circuit output voltage variations for TEG1 and TEG2. Although the output power for both TEG1 and TEG2 and the efficiency for TEG2 increase with increasing transducer output voltage, the converter efficiency for TEG1 remains almost constant for values over 20 mV. This behavior can be explained by the fact that the switches

Table 3-4: Summarized measurement results of this design and the prior art.

	[72]	[70]	[63]	This work
Topology	Inductor based	Inductor based	Inductor based	Inductor based
Technology	0.35 µm	0.35 µm	0.13 µm	0.18 µm
Voltage Conversion	26—100 mV to 1.8V	60—300 mV to 2 V	40—500 mV to 1 V	10—200 mV to 0.9V
Output Power	10 µW @ 25 mV	1.3 mW @ 100 mV	25 µW @ 40 mV	22 µW @ 20 mV
Quiescent Power	-	5 µW	2 µW	1.6 µW
Efficiency at 20 mV OC	<20%	<40%	<30%	54%
Efficiency at 100 mV OC	60%	55%	68%	71%
Area	1.6 mm^2 [a]	2.5 mm^2 [a]	0.12 mm^2 [b]	0.14 mm^2 [b]

[a] Entire chip.
[b] Core.

were optimized for a TEG output voltage of 20 mV, and the synchronization feedback is unable to lock for a transducer output voltage higher than 40 mV. The power consumption of the system is 1.6 µW at 20 kHz including dynamic power required for the power switches.

An efficiency of 54% was measured for an open-circuit output voltage of 20 mV for the TEG1 emulator, while the measured efficiency TEG2 emulator was 71% for an open-circuit output voltage of 100 mV. These values are close to the quantities that were derived with the equations in section 3.2 and illustrated in Figure 3-5 and Figure 3-7, and also circuit simulation results. Simulations suggested efficiencies of 60% and 76%, and the equations (considering power consumption) anticipated efficiencies of 74% and 87% for TEG1 and TEG2 in this microwatt regime. Lastly, it should be stated that these results also are in accordance with outcomes of equation (3-14); for a transducer with a higher TEB (lower voltage and smaller output resistance), the maximum achievable efficiency is less than for the other transducer. Table 3-4 summarizes chip performances and other state-of-the-art results.

3.5 Conclusion

The equations for energy transfer and losses were used to design a general power converter and to reach the efficiency limits of the architecture. All the parameters were calculated so that the final converter can be efficient in different conditions while the converter's electronic board can be mounted in an active EEG or ECG electrode. Furthermore, the method led to a low-complexity, low-power consumption, and small-area design through elimination of the voltage doubler for gate switching. The converter can optimally boost a voltage level of 20 mV or 100 mV provided by two different mm-scale harvesters to around 1 V at its output with efficiencies of 54% and 71%, respectively. In the conversion process, the system synchronization feedback is locked to the harvesters' output variations. The working frequency and t_1 parameters were extracted for different harvesters and ambient conditions. In the next chapter, a design methodology will be introduced to implement a new power converter architecture that can configure t_1 and f_{SW} to maintain its efficiency despite changes in the transducer's specifications.

4 Self-reconfigurable efficient power converter

This chapter describes a self-reconfigurable converter that maintains its efficiency, despite changes in the harvester's characteristics. This is achieved by an optimization process that adjusts the converter's timings within their dedicated loops, to decrease losses and increase power transfer. A time-domain state-space averaging model is used to design the system. With a comprehensive view provided by this model, the timing parameters, which were originally interdependent, were redefined to be three independent parameters. This relaxes the control section of the system and reduces the necessary components and, therefore, the power consumption.

A system is implemented to control these three timing variables by three loops in a stable manner. Two converter architectures are proposed and implemented in 0.18 μm CMOS technology. The first converter is suitable for small-scale TEG and PV. The second converter is suitable for both small-scale and moderate size transducers, as it has a more elaborate control system. Both converters are able to harvest energy from low- and high-impedance transducers. Their control system follows changes in the electrical specifications of a harvester, in order to increase the system's output power. Their efficiencies reach up to 40% with an input voltage of just 7 mV. Their power consumption can reach 300 nA at a working frequency of 10 kHz.

The control sections of the systems are implemented with only a few low-power, sufficiently precise, custom mixed-signal blocks. They clock asynchronously with a working frequency that corresponds to the available system power. To generate the working frequency and the other timings, a highly tunable, low-power, and supply-independent digitally controlled oscillator (DCO) is proposed and employed in the system. Furthermore, to achieve the required precision in monitoring available

power by the mixed-signal control system, some low-power methods are introduced to decrease switch charge injection and clock feedthrough effects.

4.1 Self-reconfiguration of energy harvester converters: Overview

The targeted wearable medical device utilizes an energy harvester as its energy source. Possible harvester types include small-scale thermoelectric generators and photovoltaic cells, based on the placement of the sensors. Small-scale harvesters for body sensor applications face several challenges as stated in Chapter 2 section 2.3. They produce unreliably small amounts of energy at low voltages. Additionally, a transducer's specifications change due to environmental conditions, or replacing a transducer with another one. Therefore, a power converter aimed at this application should not only be designed to be efficient with a high conversion ratio as was shown in Chapter 3, but should also be capable of reconfiguring itself, to keep its efficiency despite changes in the transducer's specifications.

As was described in Chapters 2 and 3, previous studies have suggested ample efficiencies for low-voltage harvesters [70]. On the one hand, a converter must tune its switching durations to achieve a high efficiency and an input impedance matched to its source while harvesting from different transducers [70, 71]. On the other hand, a converter must continuously adjust its switching frequency in order to keep its efficiency and minimize its losses when its input power changes due to environmental variations [93, 94].

The converters with higher conversion efficiencies in the low voltages with nanopower management systems [66] mostly do not have a control mechanism to monitor the available power or to configure themselves and their timings due to environmental conditions or to their transducers being replaced. The converters that can adjust their timings commonly have sophisticated power-hungry control systems that target higher power transducers [76]. They use multipliers and dynamic or static power-hungry current and voltage sensors to calculate their output power [77, 78]. These converters' efficiencies can shrink drastically with low-voltage harvesters.

To avoid complicated and power-hungry blocks responsible for estimating output power and, at the same time, to be able to briefly follow transducer behavior by changing the timings of the system with low power consumption, open-loop systems have been suggested [74, 75]. In an open-loop system, a converter is disconnected from its transducer at certain intervals by a switch; then, the open-circuit voltage

of the transducer is recorded in a capacitor. Afterward, the timings of the converter are changed to have a hard-coded predefined ratio between the input voltage of the converter and the recorded open-circuit voltage. That ratio is based on the transducer type used in the converter. If a thermoelectric generator is needed, the ratio is fixed to 50%. When a PV cell is needed, this ratio is set to between 70% and 80% [95] for an optimum working condition.

This architecture has been one the most effective low-voltage low-power implementations, particularly when the tuning of the timings results in variations in switching frequency, and therefore, calculating the output power of the converter becomes complicated. However, due to the fixed ratio, this architecture can be efficient just for one type of transducer. Even for a specific transducer, the ratio may need to be changed in different working conditions, since transducers' characteristics vary in different working conditions.

Moreover, it was shown in Chapter 3 that the efficiency related to the power loss of a converter decreases as its input voltage decreases. Therefore, to limit power loss, it might be beneficial to have slightly mismatched impedances between a converter and its transducer to increase the input voltage of the converter. In this case, both the power loss and the transfer power of the converter decrease; however, the resultant output power may increase for very low-voltage transducers, particularly low-impedance TEGs. As a result, to maintain the efficiency of a low-voltage converter, a low-power method is needed to examine the actual output power of the converter.

Therefore, to design an efficient converter that is capable of harvesting energy from different transducers requires that the converter examines its output power and adjusts both its switching frequency and switching durations in a closed-loop system, to follow the transducers' characteristics with a low-power consumption method. This requires the converter to have two control loops: one for frequency and one for switching durations. Converters also have another internal loop that keeps track of their output-to-input voltage variations. Having these three loops working together raises a serious concern regarding stability. Moreover, the entire control system has to be implemented with low-power techniques to limit power consumption to the order of a few hundred nanowatts.

These issues are addressed in this chapter, first by analysis of the system in the time domain with the state-space averaging (SSA) model. Compared to a frequency-domain approach [96], a time-domain approach offers a more comprehensive view of the system, and helps to simplify the architecture and to decrease the system's

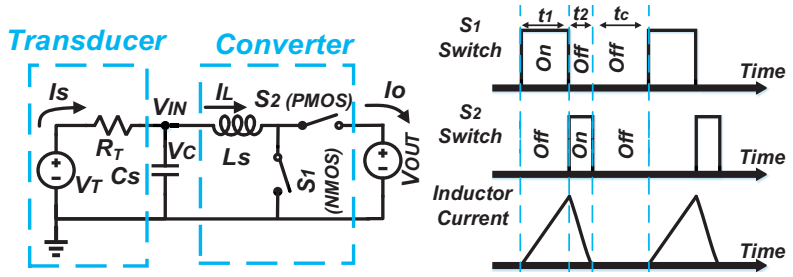


Figure 4-1: Simplified architecture of a converter and its timing diagram.

power consumption. This chapter employs the SSA model to present a design methodology for an efficient reconfigurable ultra-low-power converter. The designed converter obtained from the SSA model will be implemented with a control system that is just precise enough. Unnecessarily high precision imposes complexity in the implementation that leads to a power-hungry system. Low-power circuits and techniques will be introduced in this chapter to create the ultra-low-power converter for energy harvesting.

The system is implemented using 0.18 µm CMOS technology. It can work at an optimal point with different transducers and environmental conditions. Section 2 describes the control system of the converter. The system implementation is presented in section 3 followed by measurement results in section 4. Finally in section 5 a conclusion is drawn from this chapter.

4.2 Control system modeling and design

In the continuous mode of a conducting transistor in ultra-low power, the leakage current in the channel is of the same order of magnitude as the current passing. Therefore, power converters that operate in discontinuous conduction mode (DCM) are preferred in low-power applications as stated in Chapter 3. Figure 4-1 depicts a schematic and timings for a DCM converter.

The PMOS switch is controlled by t_2. To be optimum, it has to be turned off exactly when the inductor current reaches zero [97]. Switching the PMOS off at the wrong moment will reduce the energy transfer. Assuming an ideal inductor L_S and a constant voltage at the output, t_2 is estimated as:

$$t_2 \approx (V_{IN} / V_{OUT}) t_1 . \tag{4-1}$$

To improve efficiency, losses have to be minimized. Dynamic losses are mostly proportional to the switching frequency f_{SW}. Conversely, increasing f_{SW} lowers the inductor peak current and thus static losses. Equations for losses are given in [86],

and in Chapter 3, in section 3.2. To obtain the optimum switching frequency $f_{SW,Opt}$, their derivative to time must be solved. Following this approach, $f_{SW,Opt}$ can be written from equation (3-15) and equation (3-3) as:

$$f_{SW,Opt} \approx (V_{IN} / L_S)^{2/3} d_1 \delta, \quad d_1 = t_1 / (t_1 + t_2 + t_C) = t_1 / T, \tag{4-2}$$

where δ is a constant related to switch conductance and capacitances, and d_1 is called duty cycle[1] in this chapter. Additionally, to maximize the transferred power, the input impedance of the converter, Z_{in}, should be matched to the harvester's output impedance. Z_{in} can be written as:

$$Z_{in} = 2L_s f_{sw} / (d_1^2), \quad d_1 = t_1 f_{SW}. \tag{4-3}$$

A harvester's impedance changes with environmental conditions. Therefore, for maximum power transfer, Z_{in} should track the harvester's impedance. From equation (4-1), equation (4-2) and equation (4-3), it can be concluded that, by tuning t_2, f_{SW} and t_1, the system can be optimized in terms of losses and power transfer. Since these parameters are interdependent, the control loops for each will be concurrent, therefore, the overall stability of the system will be concerned. To study the dynamic of the system under variable switching timing, an SSA model of the system is used. The SSA models the converter as a linear system. In [98], the behavior of a DCM converter was accurately predicated through SSA modeling. A recent approach of SSA modeling, which treats switch durations as discrete control parameters [99], is extended and used in this chapter.

Assuming a constant output voltage, the power converter circuit can be seen as a voltage-to-current converter. In a state-space equation, the variables to characterize the power converter are represented as the input vector matrix $\mathbf{u}=[v_T \; v_{OUT}]^{\mathrm{T}}$ (bold variables indicate vector matrices), the output $\mathbf{y}=[i_O \; i_S]^{\mathrm{T}}$, and the state variable $\mathbf{x}=[v_C \; i_L]^{\mathrm{T}}$. A generalized state-space equation can be written as:

$$\begin{aligned} d\mathbf{x}(t) / dt &= \mathbf{A}_N \mathbf{x}(t) + \mathbf{B}_N \mathbf{u}(t) \\ \mathbf{y}(\mathrm{t}) &= \mathbf{C}_N \mathbf{x}(t) + \mathbf{D}_N \mathbf{u}(t), \end{aligned} \tag{4-4}$$

where $\mathbf{A}_N$, $\mathbf{B}_N$, $\mathbf{C}_N$, and $\mathbf{D}_N$ are representations of the converter schematic in the state of N, where N has a value of 1, 2, or 3 and refers to the different SSA states during t_1, t_2, and t_C, respectively. Considering a full period of T and operating piece-

[1] Duration t_1 is referred as the converter phase in some literature.

wise averaging all the states over the cycle of T, the model in equation (4-4) can be rewritten

$$\begin{aligned} d\langle \mathbf{x}(t)\rangle_T / dt &= 1/T\left[t_1\mathbf{A}_1 + t_2\mathbf{A}_2 + (1-(t_1+t_2))\mathbf{A}_3\right]\times\langle \mathbf{x}(t)\rangle_T \\ &\quad + 1/T\left[t_1\mathbf{B}_1 + t_2\mathbf{B}_2 + (1-(t_1+t_2))\mathbf{B}_3\right]\langle \mathbf{u}(t)\rangle_T \\ \langle \mathbf{y}(t)\rangle_T &= 1/T\left[t_1\mathbf{C}_1 + t_2\mathbf{C}_2 + (1-(t_1+t_2))\mathbf{C}_3\right]\langle \mathbf{x}(t)\rangle_T \\ &\quad + 1/T\left[t_1\mathbf{D}_1 + t_2\mathbf{D}_2 + (1-(t_1+t_2))\mathbf{D}_3\right]\langle \mathbf{u}(t)\rangle_T. \end{aligned} \tag{4-5}$$

Since the efficiency of a converter decreases along with its input voltage (Chapter 3, section 3.2), the worst-case scenario for efficiency, i.e. the lowest voltage harvester, must be considered when designing the control loop. The dynamic behavior of the other scenarios will be examined with the proposed solution.

Since v_{IN} is much lower than v_{OUT}, from equation (4-1), $t_1 + t_2$ can be estimated by t_1. The value of $1/T$ is replaced by f_{SW}. Then, the system control variables will be f_{SW}, S_2 switch "on" duration t_2, and S_1 switch "on" duration t_1. In order to implement a system with three loops working together to control these variables, the variables have to be generated and set independently. f_{SW} will be generated by a DCO. By tuning a DCO's frequency, its timings, i.e., the durations that its output level is "high" or "low", are changed too. Since the DCO timings are dependent on f_{SW}, it is not possible to use the DCO timing as t_1 or t_2 and merge one of the pulse generators with the DCO to control the system. At least two pulse generators and one DCO have to be implemented in the system.

However, it is possible to rewrite the time-domain SSA model of the converter in equation (4-5), and consider t_1/T as a control variable instead of t_1. In this case, the duty cycle of the DCO can be utilized to generate t_1/T. Since the duty cycles of a DCO do not have a time dimension, the duty cycle can be set independently from the DCO frequencies. Therefore, one DCO can be used to generate both f_{SW} and t_1/T as the control variables. By redefining the control variables, not only will one pulse generator be removed from the system, but also most components dedicated to the f_{SW} loop can be shared with the t_1/T loop as will be shown in section 4.3. Moreover, converging to the optimum point will be more practical without a complicated control structure.

Replacing t_1/T with d_1, the static and dynamic responses of the SSA model in equation (4-5) can be written as

$$\langle \mathbf{x}(t)\rangle_T = \mathbf{X} + \hat{\mathbf{x}}(t), \langle \mathbf{y}(t)\rangle_T = \mathbf{Y} + \hat{\mathbf{y}}(t), \langle \mathbf{u}(t)\rangle_T = \mathbf{U} + \hat{\mathbf{u}}(t), \tag{4-6}$$
$$d_1(t) = D_T + \hat{d}_1(t), f_{SW}(\mathrm{t}) = F_{SW} + \hat{f}_{SW}(\mathrm{t}), t_2(t) = T_2 + \hat{t}_2(\mathrm{t}),$$

where capital letters indicate static quantities, and a ^ denotes dynamic quantities. Considering equation (4-5) and knowing $\boldsymbol{X}/dt=0$, the static response, or operating point, of the system can be written as:

$$\mathbf{X} = \text{-}\mathbf{A}^{-1}\mathbf{B}\mathbf{U} \tag{4-7}$$
$$\mathbf{Y} = (\text{-}\mathbf{C}\mathbf{A}^{-1}\mathbf{B} + \mathbf{D})\mathbf{U},$$

where

$$\mathbf{A} = [\mathbf{A}_1, \mathbf{A}_2, \mathbf{A}_3]\mathbf{S}, \mathbf{B} = [\mathbf{B}_1, \mathbf{B}_2, \mathbf{B}_3]\mathbf{S}, \mathbf{C} = [\mathbf{C}_1, \mathbf{C}_2, \mathbf{C}_3]\mathbf{S}, \tag{4-8}$$
$$\mathbf{D} = [\mathbf{D}_1, \mathbf{D}_2, \mathbf{D}_3]\mathbf{S}, \text{ and } \mathbf{S} = [D_T, T_2 F_{SW}, (1 - D_T)]^T.$$

Substituting equation (4-6), equation (4-7), and equation (4-8) into equation (4-5), and neglecting high-order dynamic terms, results in the dynamic response of the control variables, i.e. t_2, f_{SW}, and d_1, combined with the dynamic response of the inputs as follows:

$$d\hat{\mathbf{x}}(\mathrm{t}) / dt = \mathbf{A}_{\mathbf{dy}}\hat{\mathbf{x}} + \mathbf{B}_{\mathbf{dy}}[\hat{\mathbf{u}} \quad \hat{t}_2 \quad \hat{f}_{SW} \quad \hat{d}_1]^T, \tag{4-9}$$
$$\hat{\mathbf{y}}(\mathrm{t}) = \mathbf{C}_{\mathbf{dy}}\hat{\mathbf{x}} + \mathbf{D}_{\mathbf{dy}}[\hat{\mathbf{u}} \quad \hat{t}_2 \quad \hat{f}_{SW} \quad \hat{d}_1]^T,$$

where $\mathbf{A_{dy}}$, $\mathbf{B_{dy}}$, $\mathbf{C_{dy}}$ and $\mathbf{D_{dy}}$ are computed based on $\mathbf{A}_\mathrm{N}$, $\mathbf{B}_\mathrm{N}$, $\mathbf{C}_\mathrm{N}$, $\mathbf{D}_\mathrm{N}$, F_{SW}, D_T, T_2, $\mathbf{X}$, $\mathbf{U}$ and $\mathbf{Y}$. From equation (4-9), the output to the new input transfer function can be written as:

$$\mathbf{H} = \mathbf{C}_{\mathbf{dy}}[s\mathbf{I} - \mathbf{A}_{\mathbf{dy}}]^{-1}\mathbf{B}_{\mathbf{dy}} + \mathbf{D}_{\mathbf{dy}}, \tag{4-10}$$

where $\mathbf{I}$ is the identity matrix.

4.2.1 t_2 control loop

The transfer function to the input of t_2 is represented by the (1,3) element of $\mathbf{H}$. Here the goal of the control system is to keep the inductor's current equal to zero at the end of t_2. Employing current sensors in the power path deteriorates the efficiency of the system due to the dynamic and static losses of the sensors. However, since the inductor's current passes through S_2, detecting the instant that the current is zero is enough to sense S_2's voltage. The block diagram of the hardware

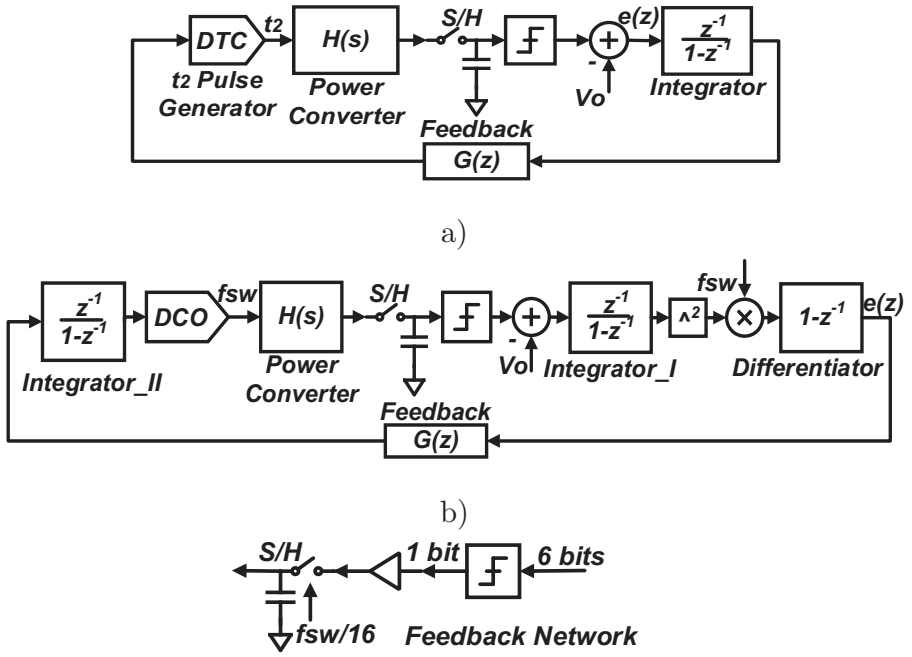


Figure 4-2: a) t_2 control loop block diagram, b) f_{SW} control loop block diagram, and c) suggested feedback network *G(z)* for the f_{SW} control loop.

related to the control loop of t_2 is shown in Figure 4-2 a). Continuous operation is not needed in the control section. Thus, this loop is implemented in the digital domain to decrease the power consumption and increase the functionality. The simplest implementation would be a one-bit ADC (a sample and hold *S/H* and a quantizer) that is triggered at the end of t_2 and senses the drain voltage of S_2 (PMOS). The ADC's output then is subtracted from the converter's output voltage to generate an error signal *e(z)*. *e(z)* is fed into an integrator to update t_2. A feedback network *G(z)* may be placed in the loop to ensure the stability of the system. A digital-to-time converter (DTC) converts *G(z)*'s output to a pulse width of t_2.

In order to find *G(z)*, it is necessary to look at the loop transfer function. The power converter's output is sampled and quantized; thereby *H(s)* is converted to the Z-domain by the zero-order hold element method. The resulting *H(z)* represents *H(s)* and *S/H* in the discrete domain. Since stability analysis and feedback design are easier in a continuous domain, *H(z)* and the discrete integrator (shown in Figure 4-2 a)) are transferred to a continuous ζ domain. An integral numerical approximation method is used for the conversion. It was found that the system has a 55^o phase margin *PM* which is sufficient for a stable functionality. As a result, *G(z)* can be just a unity gain feedback here.

4.2.2 f_{SW} and d_1 control loops

The control section should also control f_{SW} to maximize the transfer power to the converter's output. In order to maximize this power, the control section keeps the derivation of the output power to time equal to zero. The output power of a converter can be calculated by multiplying the converter's output current by the converter's output voltage. As can be seen in Figure 4-1, the converter connects to the output voltage source during t_2. Since L_S is big enough, the converter charges the voltage source with triangular-pulse-shaped currents. The peak of the current pulses is $(V_{IN}.t_1)/L_S$, and the output voltage is V_{OUT}. The output power P_{OUT} is then calculated by multiplying the root mean square (RMS) of the output voltage ($V_{OUT,\,RMS}$), and the RMS of the output current ($I_{OUT,\,RMS}$):

$$P_{OUT} = \underbrace{V_{OUT}\sqrt{\frac{t_2}{T}}}_{V_{OUT,RMS}} \cdot \underbrace{\frac{V_{IN}t_1}{L_S}\sqrt{\frac{t_2}{3T}}}_{I_{OUT,RMS}} . \tag{4-11}$$

Now, P_{OUT} can be estimated by using equation (4-11) and equation (4-1):

$$P_{OUT} \approx f_{SW}t_2^{\,2}\left(V_{OUT}^{\,2}\Big/2L_S\right). \tag{4-12}$$

Given that the output power in each cycle can be estimated by f_{SW} multiplied by the t_2 square of two from equation (4-12), the loop responsible for controlling f_{SW} is depicted in Figure 4-2 b). f_{SW} is generated by a DCO, and its value in the discrete domain is proportional to the input bits of the DCO. A differentiator generates $e(z)$ from the output power. A method similar to the one used for the t_2 loop of Figure 4-2 a) is adopted to calculate the PM here. However, due to a high gain of the system, the f_{SW} loop does not have enough PM for its stability in unity feedback. Decreasing the clock frequency or adding a quantizer in the feedback loop lowers the gain of the system and provides more PM. A feedback network that meets the 55° PM for the f_{SW} loop is proposed in Figure 4-2 c). The Bode diagram of the f_{SW} loop transfer function is plotted in Figure 4-3 for three different values of the input capacitor. For a larger input capacitance, the f_{SW} loop has to be slower, and its feedback gain should be even lower. Therefore, the speed requirement of the system limits the input capacitance.

The same block diagram as in Figure 4-2 b) is employed to set d_1, although the DCO is replaced by a digitally controlled duty-cycle generator. The system suffers from the same stability issue as the f_{SW} control loop. To solve this, the same $G(z)$ used for f_{SW} control is used here. Moreover, to save resources and power, and since

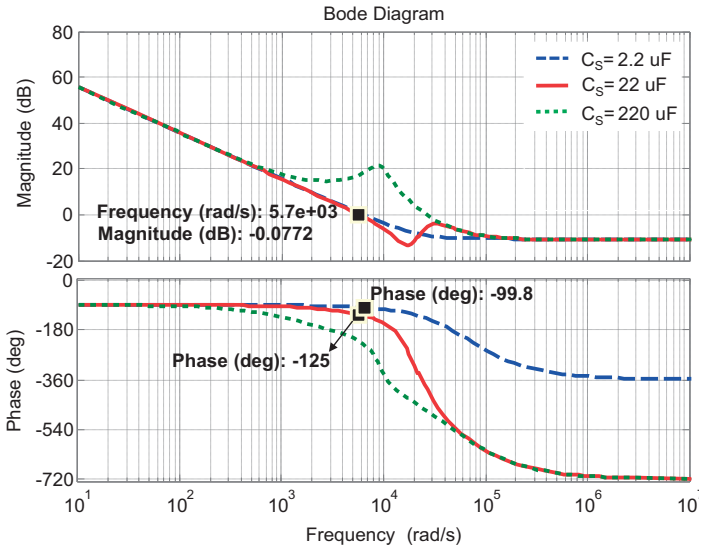


Figure 4-3: Bode plot of the f_{SW} loop for three values of the input capacitor.

variations in a harvester are very slow, $G(z)$ is multiplexed in time to control f_{SW} and d_1. This provides an 85° PM for the d_1 loop.

4.3 System implementation

In this section, a low-power system architecture is proposed to implement the control loops shown in Figure 4-2. The simplified implemented system is shown in Figure 4-4. This implementation is made of three main parts: a t_2 loop, f_{SW} and d_1 loops, and the core structure of the converter. The core of the converter consists of an NMOS switch and a body protected PMOS switch, which are controlled by t_1 and t_2 pulses. The body protected transistor has a PMOS switch core and two auxiliary PMOS transistors. The auxiliary transistors keep the substrate connection of the switch tied to the switch's terminal, which has a higher voltage level to avoid leakage current from its well. The t_1 and t_2 pulses are provided by the t_2 loop and the f_{SW}/d_1 loops. The system level and block level functionalities of these loops are discussed in more detail in this section, followed by suggestions for their implementations. Furthermore, some low-power techniques and circuits are suggested for the blocks employed in this architecture to make the system suitable for low-voltage low-power harvester applications.

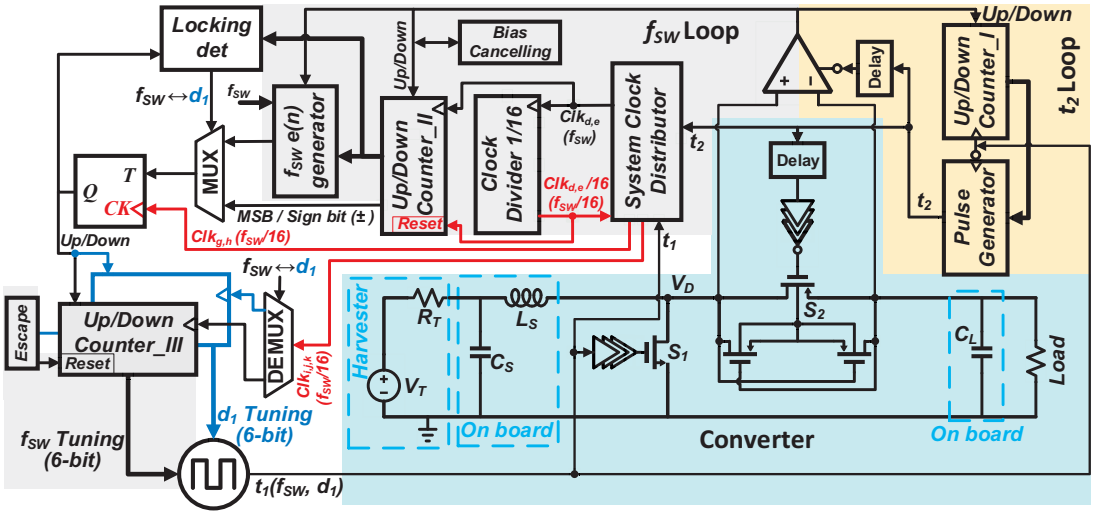


Figure 4-4: Simplified system implementation of the control loops and the converter.

4.3.1 Implementation of the t_2 loop

A simplified t_2 control loop implementation of Figure 4-2 a) is shown in the upper right of Figure 4-4. The chain responsible for error signal generation in Figure 4-2 a) (*S/H*, one-bit ADC, adder) was implemented with a latch comparator. The comparator's output controls the up/down function of a counter (*Counter_I*) which realizes the integrator in Figure 4-2 a). Having a unity feedback in the loop as *G(z)*, *Counter_I* represents t_2 in the digital domain. The implementation of the t_2 loop in the system level resembles some previous work [63, 70, 72]; however, the approach to implement this system were proposed here.

Counter_I is a 7-bit counter that is modified to not return from its maximum value to its minimum value and vice versa. This becomes important when the power available from the input is so low that t_2 should have its minimum value. At this point, *Counter_I*'s output becomes zero. Since *Counter_I*'s output is set by its up/down bit controlled by the one-bit ADC, its value toggles around an ideal value that it is supposed to have in the steady state. If *Counter_I* changes suddenly from zero to its maximum value, a very wide t_2 will be generated, and the output storage element will be discharged to the inductor.

From Figure 4-2, the output of *Counter_I* is connected to the t_2 pulse generator. This pulse generator is implemented by a NOR gate whose inputs have the same signal but delayed. The delay is set by the counter's output. The generated pulse

widths are controlled by seven bits, which provides a good trade-off between complexity and performance. Post-layout simulations show that the designed pulse generator can monotonically generate pulse widths in the range of 40 ns to 690 ns.

The pulse generator produces pulses to switch S_2 (PMOS) "on", which should be triggered when S_1 is switched "off". However, the t_2 pulses should not be applied to the PMOS transistor the instant S_1 is turned off. There should be a small interval, a *deadtime*, between these two events. The deadtime should be long enough that the parasitic capacitor at the drain node of the switches, C_{PAR}, is charged to the level of V_{OUT} by I_L, and has to be short enough that the C_{PAR} voltage does not exceed the forward voltage of the parasitic lossy diode of the PMOS. To generate the deadtime, a variable delay block is placed between the t_2 pulse generator and the PMOS buffers. The value of the delay has to be set once at the beginning of the chip operation.

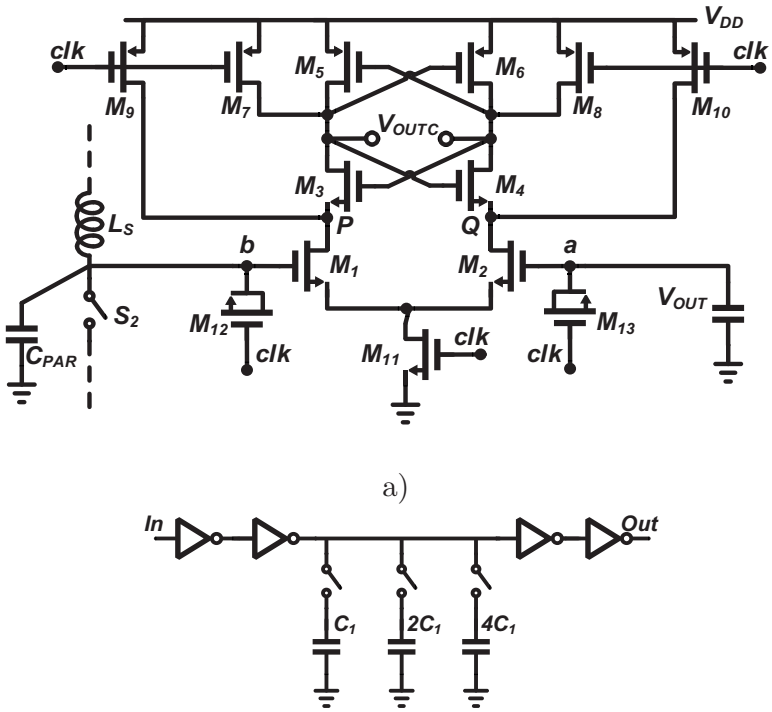
Since the output power was estimated by t_2 from equation (4-12), the blocks that have been designed here for the t_2 loop will be shared with the f_{SW} and d_1 loops as well. In these blocks, the latch comparator is one of the most important components, since it is an interface between the analog power electronics section and the digital control section. In the next subsection, the design and the challenges of the latch comparator are discussed.

4.3.2 Latch comparator

The latch comparator employed in this design is a modified StrongArm latch [100-102]. The comparator schematic along with the components connected to its inputs is shown Figure 4-5 a). Since the comparator is one of the key building blocks in this architecture, non-idealities in the comparator are introduced, and some low-power techniques are suggested to reduce the errors that result from the non-idealities.

4.3.2.1 Charge injection in the comparator

Since the input common-mode voltage of the comparator is in the same level as V_{DD}, NMOS transistors are used as its input stage. One of the comparator's inputs, node *a*, is connected to a large energy storage element; the other input, node *b*, is connected to the drain of the PMOS power switch. At each falling edge of t_2 pulses, the PMOS switch is turned off, and the comparison process has to be started. The moment that the PMOS is switched off, its channel residual charge is injected to the node *b* comparator input and the level of input voltage is raised significantly. This leads to wider-than-expected t_2 pluses. Therefore, the output storage element



a)

b)

Figure 4-5: Schematic of a) the latch comparator circuit and its b) variable delay generator.

will be discharged, rather than charged, by the input. This effect deteriorates the efficiency of the converter considerably.

The injected charge can be seen as an impulse current that charges up the parasitic capacitance C_{PAR} and inductance L_S at the end of the t_2 interval, i.e. after the PMOS is switched off. Subsequently, the voltage on node b will have a sinusoidal behavior, which depends on the resonance frequency of L_S and C_{PAR}, ω_0, and the charge injected to C_{PAR}, Δq_J:

$$v_b = \left(\Delta q_J / C_{PAR} + V_0\right)\cos\left(\omega_0 t\right) + I_0\sqrt{L_S / C_{PAR}}\,\sin\left(\omega_0 t\right), \tag{4-13}$$

where V_0, and I_0 are the initial capacitance voltage and the initial inductance current at end of the t_2 interval, respectively. V_0 is equal to V_{OUT}, since node b was shorted to the output at the end of t_2. If I_0 is zero, a delay time t_D is needed to discharge node b to its initial value V_{OUT}. t_D can be calculated as:

$$t_D \approx \sqrt{\frac{2L\Delta q_J}{V_{OUT}}}. \tag{4-14}$$

Since the PMOS transistor specifications are not changed during its working operation, its channel residual charge remains unchanged; therefore, t_D is constant during steady-state operation of the converter.

As equation (4-13) illustrates, a positive or negative I_0 causes respectively a higher or lower voltage level than V_{OUT} on node b after a t_D duration from the instant the PMOS is switched off. Therefore, if a delay equal to t_D is placed between the t_2 generator and the *clk* node of the comparator, the comparator can detect whether the inductor's current is positive or negative at the end of the t_2 duration. Therefore, it is not necessary to add active charge injection cancelation circuits here.

Since S_1 and S_2 sizes do not change in different working conditions, C_{PAR} and injected charges remain almost constant. It is necessary to set t_D just once by a delay generator block similar to the schematic shown in Figure 4-5 b). t_D is tuned by binary weighted capacitors placed in the middle of a inverter chain.

It is worth mentioning that, as equation (4-13) and equation (4-14) suggest, the S_2 resistance value almost does not have an effect on the dynamic range of the comparator input voltage at node b. Thus, S_2 can be designed based on loss and power transfer considerations only.

4.3.2.2 Comparator offset

In addition to the charge injection, the comparator offset can also introduce an error into the t_2 pulse durations. The t_2 durations are set by a discrete feedback loop, which cannot be fixed exactly equal to the time span needed for the inductor current to reach to zero. The actual t_2 durations toggle in the vicinity of the ideal value of t_2. That is to say, the generated t_2 is wider or narrower than its ideal value in each cycle. When t_2 is narrower, the small residual current in L_S will not be transferred to the output and will be dissipated. The resulting loss $P_{LOSS,t2(1-x)}$ for a t_2 duration equal to $t_{20}(1-x)$, where t_{20} is the t_2 ideal value and x is a positive value much smaller than 1, is calculated using equation (4-11):

$$P_{LOSS,t_2(1-x)} = V_{OUT}\frac{V_{IN}t_1}{L_S}\cdot\frac{t_2 x}{\sqrt{3}T}. \tag{4-15}$$

A wider t_2 charges L_S by the output source energy. This energy was transferred and processed by the converter once, and was stored in the output storage element. A t_2 that is $(1+x)$ wider than the ideal t_2 imposes a loss on the converter equal to the power needed to charge L_S for x duration, and can be written as:

$$P_{LOSS,t_2(1+x)} = \frac{1}{2}\left(\frac{V_{OUT}t_2x}{L_S}\right)^2 L_S f_{SW}. \tag{4-16}$$

The ratio of the loss calculated from equation (4-15) to equation (4-16) is x (the mentioned ratio duration), which has a value much smaller than one. Therefore, it is more desirable to generate t_2 slightly narrower perhaps by a very small negative offset in the comparator. The comparator's offset is related to the ratio of the parasitic capacitance in node P to the node Q in the schematic of Figure 4-5 a). Since the comparator has to consume a small dynamic power, its input transistors are designed to be small and, therefore, their parasitic capacitors are small as well. It has been calculated that adding just a few femto-farads capacitance at node P will result in an offset two times bigger than the desirable value.

In a previous study [66] to tackle this issue, some extra blocks were added to that system's digital control section, separated from the comparator. Those blocks assisted to generate two narrower t_2 pulses, which were followed by one wider t_2, instead of the usual case in which one narrow pulse is followed by one wide pulse. There, the t_2 durations are shorter on average; however, output source discharging still exists. In this section, a completely symmetrical layout for the converter is employed instead; the t_D delays that were generated by Figure 4-5 b) are increased to compensate for any possible remaining positive offset from the comparator, and to create a very small negative offset for that. Since the comparator offset does not change dynamically, thanks to transistors M_9 and M_{10}, the desired offset value is not changed during working operation. One time tuning of t_D both for creating the negative offset and for eliminating the charge injection from the PMOS switch is enough. To tune t_D, it is sufficient to use a transducer with known characteristics as the source of the power converter, and to set t_D to the value so that the output power in steady state is maximized.

4.3.2.3 Comparator noises

Unlike the comparator's offset, its input-referred noise has a dynamic behavior, and the circuit has to be sized to keep the noise within a tolerable level. Since the comparator's input noises are not transferred to the comparator's output with a small signal gain, a large-signal noise-included transient simulation should be employed to calculate the input-referred noise of the comparator. For this purpose, a small positive voltage V_S on the order of a few millivolts has to be placed over the comparator's common-mode voltage at its input. Then the comparator has to be clocked repeatedly, and its output has to be read after each clock cycle. In a noiseless circuit, if the offset of the comparator has been compensated for, the comparator output should be one after each clock cycle. However, in the presence of noise,

the output will be one for n_1 times and zero for n_0 times. n_0 is the probability of having an input noise smaller than $-V_S$.

$$n_0 = \Pr\left\{V_{n,COMP} \le -V_S\right\} = \int_{-\infty}^{-V_S} f_X(x)dx, \tag{4-17}$$

where $f(x)$ is the noise probability density function and $V_{n,COMP}$ is the input-referred noise of the comparator. $V_{n,COMP}$, calculated in Appendix A, is equal to the $f(x)$ variance. The designed comparator was simulated with the above procedure, and its input-referred noise was calculated to be 600 µV using equation (A-2), while its dynamic power consumption reaches 10 nW at 20 kHz in the worst case.

Kickback noise can also deteriorate comparator precision. When the clock goes high, nodes S, P, and Q from Figure 4-5 a) go down very fast. Owing to the gate-source and gate-drain coupling capacitance of M_1 and M_2, the gate terminals of M_1 and M_2 start to sink some charges from the comparator's inputs. This effect can slightly decrease the input voltage level. To partially compensate for the depleted charges, M_{12} and M_{13} with a coupling capacitance similar to M_1 and M_2 are added to the inputs of the comparator. They are clocked in the same time as M_{11} is clocked. M_{12} and M_{13} have been introduced to a comparator in [103] but the transistors' purpose is not clear at that work.

4.3.3 Implementation of the f_{SW} and d_1 loops

The digital control section dedicated to the f_{SW} loop has to be implemented in concurrence with the t_2 loop. In order to implement this loop, to enhance the output power, the loop error signal $e(n)$ must be calculated. $e(n)$ is represented by the derivative of the output power (Δp) and is estimated from equation (4-12) as:

$$\Delta p(n) = p(n) - p(n-1), \text{and } p(n) = m.f_{SW}(n) \times t_2^{\,2}(n), \tag{4-18}$$

where n is the discrete time variable of the f_{SW} function and has positive integer values.

Based on equation (4-18), to produce $e(n)$ for the f_{SW} loop, multibit adders and power-hungry and multipliers are needed. In this section, two approaches will be suggested to implement the f_{SW} loop from Figure 4-2 b) and c) with low power consumption. In the first approach, an inexact, multiplier-less, low-power implementation of the f_{SW} loop, previously introduced by the author of this thesis in [104], will be described in detail. It will be shown that regardless of the inexact implantation of the f_{SW} loop, the achievable converter maximum efficiency is satisfactory for small-scale TEGs as the converter's transducer. In the second approach,

the complexity of the system will be increased, and equation (4-18) is estimated by just one low-power multiplier which is precise enough. It will be shown that the resulting system can have a higher efficiency and robustness for different types of small-scale and moderate size transducers.

4.3.3.1 Low-complexity f_{SW} loop

Due to the integrator behind the DCO in Figure 4-2 b), and *S/H* blocks shown in Figure 4-2 c), variations in the f_{SW} loop are much slower than t_2. Therefore, it might be reasonable to consider $f_{SW}(n-1)$ equal to $f_{SW}(n)$ as a constant, compared to the variations in t_2. As a result, Δp can be estimated with Δt_2^2. As shown in Figure 4-2 b) and Figure 4-2 c), a *6 to 1 quantizer* is placed after the *differentiator*. As a consequence, just the sign bit of the differentiator is transferred to the next block. The sign of Δt_2^2 is the same as the sign of $t_2(n)-t_2(n-1)$. Therefore, now the goal is just to generate $t_2(n)-t_2(n-1)$ as an estimation for the error signal $e(n)$ for the f_{SW} loop.

In this case, it is no longer necessary to implement any multiplier. This estimation is acceptable if, with a slight change in frequency in direction of increasing of the output power, $t_2(n)-t_2(n-1)$ will not be negative, and vice versa. Appendix B and simulations confirm that this approximation is acceptable when the losses in the system are considerable in comparison to the available power, which is the case for the small-scale low-voltage TEGs, as was shown in Chapter 3, section 3.4. In this case, it is possible to use $\Delta t_2(n)$ instead of equation (4-18) as an $e(n)$ estimation.

A simplified schematic of the implemented multiplier-less f_{SW} loop of Figure 4-2 b) is depicted in the upper left of Figure 4-4. The latch comparator was used for the f_{SW} loop to implement the *S/H*, *quantizer* and *adder* similar to the t_2 loop. Figure 4-2 b) showed that the comparator is connected to *Integrator_I* and the output of *Integrator_I* is $t_2(n)$. In the absence of the *multiplier* and *square of two blocks*, *Integrator_I* is connected to the *differentiator*. The *differentiator* is implemented just by a counter that resets the integrator's value every 16 cycles (update rate of the f_{SW}). As a result of this reset, the output of the integrator will be directly $t_2(n)-t_2(n-1)$. *Integrator_I*, the *6 to 1 bit quantizer* and the *differentiator* in Figure 4-2 b) and c) are implemented within *Counter_II* of Figure 4-4. Therefore, after every 16 cycles, the sign bit of *Counter_II* will be transferred to the flip-flop and the counter will be restarted. The f_{SW} $e(n)$ generator block and the multiplexer *MUX* after that, which are shown Figure 4-4, are not implemented in this section. *Integrator_II* in Figure 4-2 b) is implemented within *Counter_III* in Figure 4-4. Its clock is divided by 16 to fulfill the frequency division proposed in

Figure 4-2 c). A flip-flop is added to the network to toggle the direction of *Counter_III*, whenever Δp has a negative value.

Small logics are added to detect if the system is locked on a new f_{SW}. When for two consequent updates of f_{SW}, Δp remains almost zero, the system is locked. This is achieved by monitoring the output of *Counter_II*. Then, a demultiplexer *DEMUX* will change the direction of the f_{SW} loop to tune d_1. A logic perturbs the value of d_1, and Δp will be observed. Since f_{SW} is constant when the d_1 loop is activated, inherently it is not necessary to have any multiplier to generate *e(n)*. Therefore, independent of the losses in the system, this implementation is always accurate for generating *e(n)*. Again, when the system reaches its stable point, this process will be reversed from d_1 to f_{SW}. Simulations have shown that f_{SW} and d_1 are unstable without the proposed feedback, and the system could not be locked to a high efficient working point.

4.3.3.2 Moderate-complexity f_{SW} loop

In the previous implementation, the multipliers in equation (4-18) were eliminated, and thus a reduction in power consumption and area were achieved. As was shown in Appendix B, this realization was effective when losses were considerable. The efficiency could have reached a maximum of about 70%, enough for the two small-scale low-voltage TEGs considered in Chapter 3, section 3.3. Table 3-4 suggested that a maximum efficiency of about 71% and 54%[2] can be obtained by a converter connected to the small-scale TEGs in their typical working conditions. However, this may not be efficient enough for some transducers, like a moderately sized TEG transducer or PV harvesters.

Moreover, since the working frequency growth was not monitored by the control section, the system can be locked to a working point that the system impedance would be matched with the transducer's, and the ratio of the transfer power to the available power would be high; however, the system's working frequency is higher than expected. For example, a system with a low f_{SW} and a high d_1 can have the same input impedance as a system with a higher f_{SW} and a lower d_1 from equation (4-3). However, in the latter case, since f_{SW} is higher, the dynamic power consumption of the control section and the DCO will be increased. Even though the system is locked in a local power transfer optimum point, the entire efficiency will be deteriorated because of excess dynamic power consumption.

[2] With considering the power consumption of the converter.

Nevertheless, the precise implementation of equation (4-18) is not reasonable for a low-power system. *Counter_I* and *Counter_III*, which generate t_2 and f_{SW}, are 7-bit and 6-bit counters, respectively. Consequently, for an exact realization of Figure 4-2 b) and c), a 14-bit square of two and a 20-bit multiplier are needed, which demand large amounts of power and area. However, as was stated in section 4.3.3.1, the update rate of f_{SW} is much slower than t_2; moreover, only the sign of equation (4-18) is needed as the one-bit $e(n)$. Thus, it might be possible to simplify equation (4-18) and implement it with a low power consumption hardware. The $f_{SW}(n)$ and $t_2(n)$ can be written as

$$f_{SW}(n) = ay(n),\ t_2(n) = bz(n), \tag{4-19}$$

where $y(n)$ and $z(n)$ are the output of *Counter_III* and *Counter_I* at the instant of n. a and b are the gain of the DCO and the t_2 pulse generator, respectively. By replacing equation (4-19) in equation (4-18), Δp can be rewritten as a function of $y(n)$ and $z(n)$ as:

$$\Delta p(n) = e(n) = b^2 a\left[z^2(n)y(n) - z^2(n-1)y(n-1)\right]. \tag{4-20}$$

Between the *nth* and *(n−1)th* instants, y changes by just one bit, whereas z can change by multi bits. The variations in z, and y during *n−1* instant to n, are named Δ_t and LSB_f, respectively. After reordering equation (4-20), it can be rewritten as:

$$\begin{aligned} e(n) &= 2b^2 az(n)\left[LSB_f z(n)/2 + \Delta_t y(n-1)\left(1 + 1/2z(n)\right)\right] \\ LSB_f &= y(n) - y(n-1) \\ \Delta_t &= z(n) - z(n-1), \end{aligned} \tag{4-21}$$

where LSB_f can just be positive one or negative one.

The outputs of *Counter_I* and *Counter_III*, which are z and y, are always positive integers. Considering different transducers' specifications, the converter is designed to have a z much bigger than the one for the steady-state operation. Thus, it is possible to neglect $1/(2z(n))$ against 1 and rewrite equation (4-21) as:

$$e(n) \approx \left[LSB_f z(n)/2 + \Delta_t y(n-1)\right] 2b^2 az(n). \tag{4-22}$$

From Figure 4-2 b) and c), only the sign of $e(n)$ from equation (4-22) was important for the f_{SW} loop. As y and z have positive values, the proposed implementation for the f_{SW} loop here checks whether LSB_f and Δ_t have the same sign. If they have the same sign, the single-bit $e(n)$ will be generated with the same sign as LSB_f and Δ_t. If they do not have the same sign, a hardware compares the $z(n)/2$

term with $\Delta_t \times y(n-1)$ to generate an appropriate sign for $e(n)$. Here, one multiplier is needed to generate $\Delta_t \times y(n-1)$.

Since the product of the multiplier is just used to compare with the $z(n)/2$ term, it is enough to have the same number of bits as $z(n)/2$ has at the output of the multiplier. In this case, a custom multiplier with a reduced number of bits should suffice. The output of this multiplier will stay at its maximum value for a larger product, and it will not always have an exact result. This reduction in the number of bits in the multiplier from 20, which was expected from equation (4-18), to just 6 here drastically reduces the power and area consumption.

Moreover, in a steady-state operation, Δ_t is always one or zero, and $y(n-1)$ is updated just once every 16 cycles. Therefore, it can be expected that the power consumed for generating $e(n)$ will be reduced even more by this implementation.

The hardware needed to execute the comparison between the two terms in the right side of equation (4-22) is drawn in Figure 4-6 a). To realize $z(n)/2$, the LSB of the 7-bit *Counter_I* was dropped, and $\Delta_t \times y(n-1)$ is compared with $z(n)$'s last six most significant bits. Due to the discrete characteristics of the feedback loops, $t_2(n)$ toggled around its ideal value; therefore, the *LSB* of *Counter_I* continuously toggled in each cycle in the steady-state operation. By dropping this bit in $e(n)$ calculations, even more dynamic power was saved in this hardware, and a smaller multiplier was employed.

The timing diagram of the schematic in Figure 4-6 a) and the $e(n)$ updating cycle are shown in Figure 4-6 b). $z(n)$ and Δ_t are updated in every positive edge of the clock cycle, whereas $y(n)$ is updated once, at the end of every 16 cycles, and at the falling edge of the clock. In a window between the rising and the falling edge of the 16th clock, both $z(n)$ and $y(n-1)$ are available. Therefore, $e(n)$ can be generated by a combinational logic in this window, and it has to be sampled at the end of the 16th clock cycle. The combinational logic is employed here to avoid power-hungry sequential circuits.

4.3.3.2.1 Implementing the $z(n)$ path to generate an error signal in the f_{SW} loop

A detailed examination of equation (4-22), which calculates Δp, gives better insight into the system operation in increasing output power. With a better understanding of equation (4-22), it may be possible to increase the system efficiency by some modifications of the control system. The first term on the right side of equation (4-22) is related to $z(n)LSB_f$. $z(n)$ is linked to t_2, which represents the current transferred to the output in each cycle, while the single-bit LSB_f shows whether the current transfer rate increases or decreases. Therefore, the $z(n)LSB_f$ term in Δp

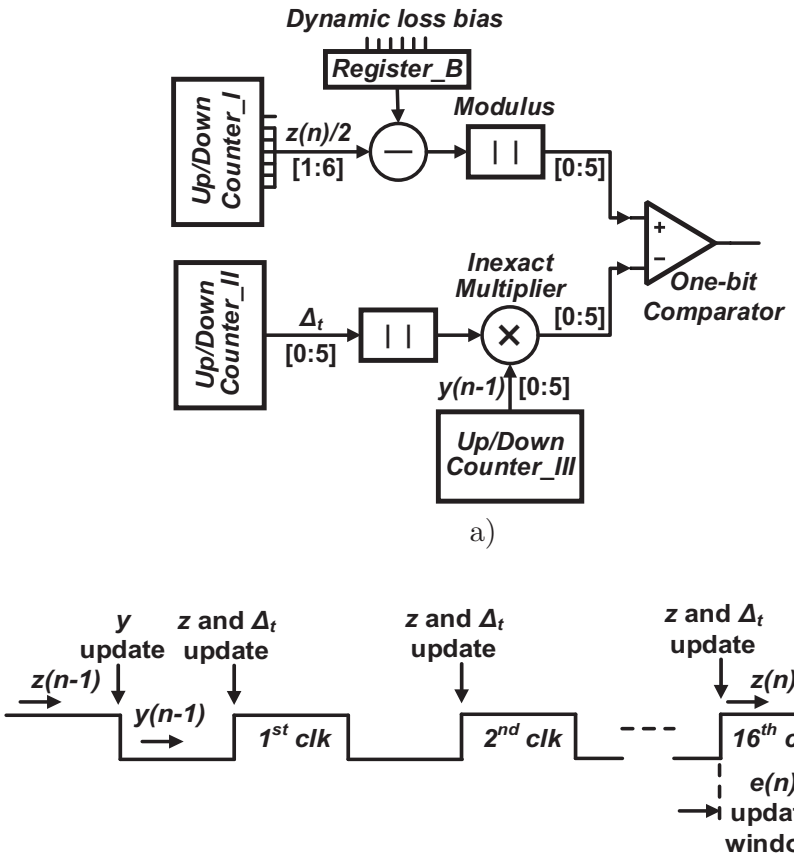


Figure 4-6: a) Schematic of the hardware responsible for the multiplication and comparison needed to generate *e(n)* and b) timing diagram of *e(n)* updating in the f_{SW} loop.

from equation (4-22) is a transfer power term whose value is directly related to changes in the working frequency. On the other hand, as was mentioned in section 4.2, the dynamic loss of the system was directly related to changes in the working frequency. Thus, *z(n)* can be inversely linked to the dynamic energy loss in the power transfer path in each cycle.

The second term on the right side of equation (4-22) is related to $\Delta_t \times y(n-1)$. Δ_t is related to variations in t_2, which can represent changes in the inductor's peak current in each cycle. As was mentioned in section 4.2, the static loss of the system is directly related to changes in the inductor's peak current. Therefore, Δ_t can be inversely associated with the static energy loss in the transfer path. Since *y(n−1)* is related to the working frequency, the $\Delta_t \times y(n-1)$ term becomes a power term whose value is inversely related to the static power loss in each cycle.

Based on the intuitive discussion about equation (4-22), $z(n)$ and $\Delta_t \times y(n-1)$ can be stated as:

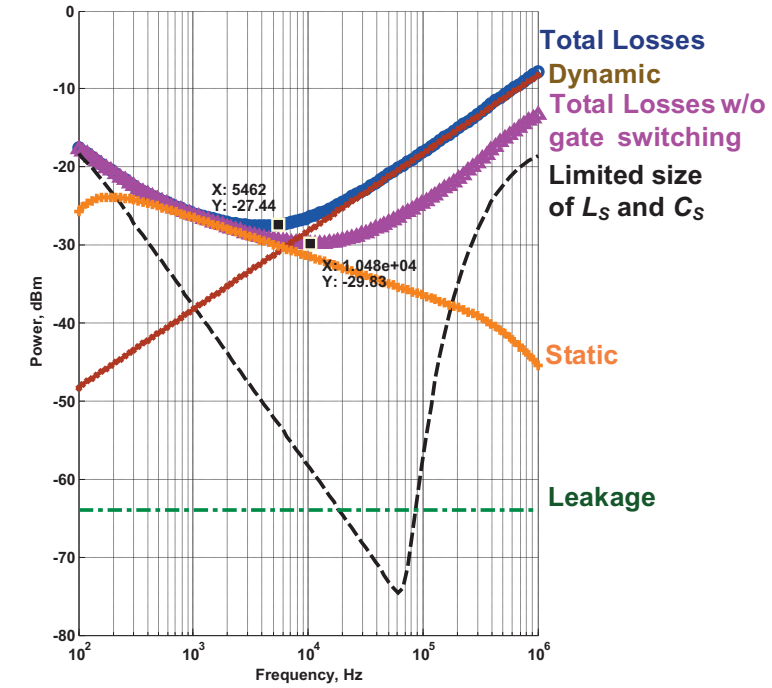
$$z(n) \propto \left(1/\text{dynamic energy loss}\right)$$
$$\Delta_t y(n-1) \propto \left(1/\text{static power loss}\right). \tag{4-23}$$

Δp which was achieved by equation (4-22) is expected to anticipate dynamic and static losses in the power path from the converter's input to its output in each cycle. However, there are other losses in the system that do not take place on the power path, and they involve in the system efficiency. These losses have two main sources: the dynamic loss in the gate of the power switches and the power consumed by the analog and digital circuits.

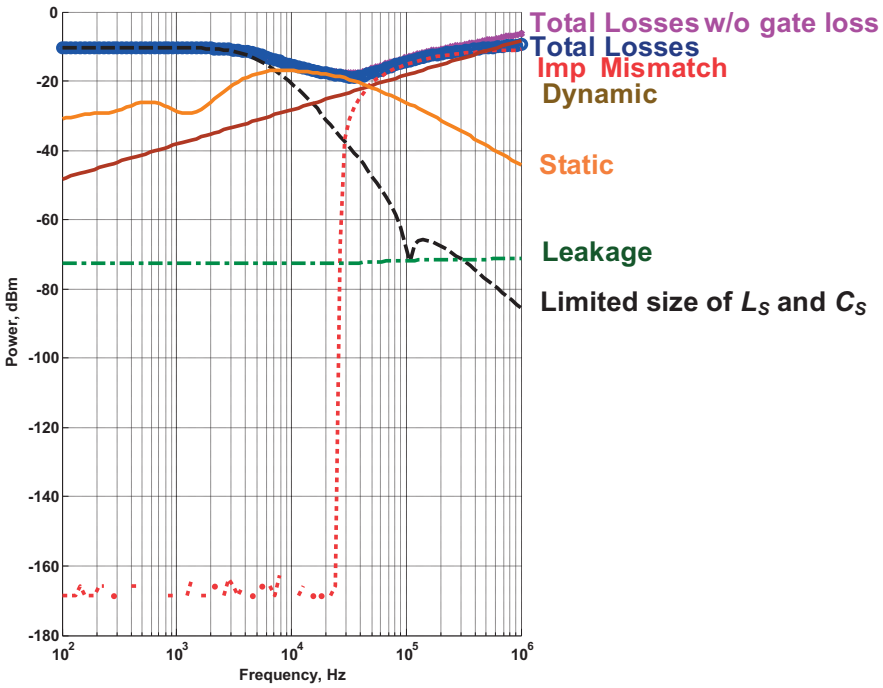
The dynamic power that is consumed by the gates of the power switches has to be taken in consideration, particularly when the switches are very large, and they have a large gate capacitance. In low-power applications, the switches are rather large; however, the dynamic power consumed by the gates of the switches should not be considered to be the only source of the dynamic power loss. The dynamic power loss by parasitic capacitance on power path C_{PAR} has almost the same contribution to the dynamic power as the gate of the switches. C_{PAR} is created by the drain capacitance of the switches, their metallic connections, the PCB tracks, and the pads, pins, and electrostatic protection circuits in both the converter and inductor chips.

Since the switch gate capacitance loss is not monitored by the control system, its effect on the system efficiency has to be studied and its exact contribution to the entire system loss has to be found. Figure 4-7 illustrates the system losses as a function of working frequency for two types of transducers: a high-impedance transducer and a low-impedance transducer. As is shown in Figure 4-7 a) for a high-impedance transducer (180 Ω, with an open-circuit voltage of 130 mV), dynamic and static losses are the main contributors to the entire system loss near the optimum working frequency. To study the impact of the switch gate power loss, its effect has been removed and the total loss is redrawn again. As can be seen in Figure 4-7 a), by not considering power loss in the gate of the power switches, the total loss will decrease by about 2 dB in the optimum point, which translates to less than 0.2 dB error in the power transfer. These values are acceptable in a low-power application, in exchange for having a low-power system as was described above.

Figure 4-7 b) depicts the losses for the system with a low-impedance transducer (2.5 Ω, with an open-circuit voltage of 30 mV). According to equation (4-3), for a



a)



b)

Figure 4-7: Contributions of different types of losses in the total loss of the system with a) a high-impedance transducer and b) a low-impedance transducer.

low-impedance transducer, a very high d_I is necessary, which in some cases could be not realized in a DCM implantation. Therefore, there will be power loss owing to an impedance mismatch of the converter with this transducer. As Figure 4-7 b) illustrates, near the power loss optimum point, the static loss and the impedance mismatch loss are the main contributors to the entire loss. Therefore, the system can converge on its optimum point even without monitoring the loss that is introduced by the gates of the power switches.

The other source of loss that does not take place on the power path is the dynamic power consumption of the circuit blocks. The circuits were designed to consume much less power than the expected available power from the input. Almost all the circuit blocks consume only dynamic power. The static power consumption is very limited in the system.

The dynamic power consumption of a circuit block is related to its clock frequency. Here, the clock signal of the entire system is designed to be asynchronous, and the clock frequency for all the circuit blocks is f_{SW} or a fraction of f_{SW}. Therefore, the dynamic power consumption of the circuit blocks is also directly related to f_{SW} and, consequently, from equation (4-2) and equation (4-3), the dynamic power consumption of the blocks is related to the available power from the input transducer. Therefore, not only is the dynamic power of the circuit blocks limited compared to the available transducer power, but with a reduction in the available transducer power, power consumption of the circuits will also be reduced and may stay in an acceptable range compared to the available transducer power. However, since the system frequency variations with the available power are not linear from equation (4-2) and equation (4-3), if the available transducer power reduces continuously, the power consumption by the circuits can become significant at a certain point.

As it has been stated in this section, the dynamic losses that do not occur in the power path do not play a main role in the overall loss of the system in a normal condition; however, if they were introduced to the feedback loop, the efficiency of the system could be even higher. As was mentioned before in this section, the source of these losses was mainly the power consumption of the circuits and the loss in the gate of the power switches. The supply voltage and the capacitance of the circuits and the power switches do not change in all operating conditions. Therefore, their dynamic energy losses remain constant regardless of the transducer specifications employed in the system or the operational working point of the converter. This constant energy loss can be introduced in the feedback loop to increase the efficiency.

As was summarized in equation (4-23), *z(n)* could have been inversely linked to the dynamic energy loss in the power transfer path in each cycle. Therefore, the loss resulting from the circuit blocks and the gates of the power switches can be defined as a constant, which is subtracted from *z(n)* in each cycle. This constant or bias is introduced into the feedback loop by a register, called *Register_B* in Figure 4-6 a). The value of this register, *dynamic loss bias*, has to be set once from outside the chip.

Since the static power consumption of the circuit blocks is limited, it is not necessary to add a subtractor in the Δ_t path of Figure 4-6 a), as was added in the *z(n)* path.

4.3.3.2.2 Implementing the Δ_t path to generate an error signal in the f_{SW} loop

The circuit that generates *e(n)* for the moderate-complexity f_{SW} loop is placed between *Counter_II* and *T flip-flop* in Figure 4-4. *Counter_II* as an integrator accumulates output bits of the comparator during each cycle. *Counter_II*'s output is Δ_t from equation (4-22), and it is connected to the f_{SW} *e(n) generator* block from Figure 4-4 to generate *e(n)* in the f_{SW} loop. The counter's output bits are transferred to the next block at the end of the 16^{th} cycle.

Figure 4-8 a) shows two examples of actual t_2 variations and the resulting output from *Counter_II* in one cycle. In the first case, *Counter_II*'s output is zero, and it predicates that the new Δ_t has the same value as Δ_t in the former cycle. In the second case, however, *Counter_II*'s output is again zero while Δ_t decreases in the new cycle. This occurs because a limited even number of data points are integrated and the actual variation is an odd number. Therefore, it may be necessary to keep the last value of *Counter_II*'s input as its initial value for the next cycle. This initial value has to be considered and added to the new cycle of Δ_t, if the last input value of *Counter_II* in the former cycle and the latter cycle is not the same.

This can be important because, with a small change in f_{SW} or d_1, t_2 which was related to the output power can be changed just one level in each cycle. Figure 4-8 b) shows the digital circuit implemented for this purpose. As will be discussed in section 4.3.6, it is not possible to have an extra clock cycle just to accumulate the initial value. However, it is necessary to accumulate this initial value if its value is not the same as the last input value of the counter in the new cycle. This means that adding the initial value has same effect on the system as not considering that last value in the new cycle. Therefore, instead of adding the initial value to the system at the end of the new cycle, the schematic in Figure 4-8 b) does not count the last input of the new cycle. The last input value is stored in the D flip-flop. If this stored value in the D flip-flop is a different from the last *Counter_II* input in

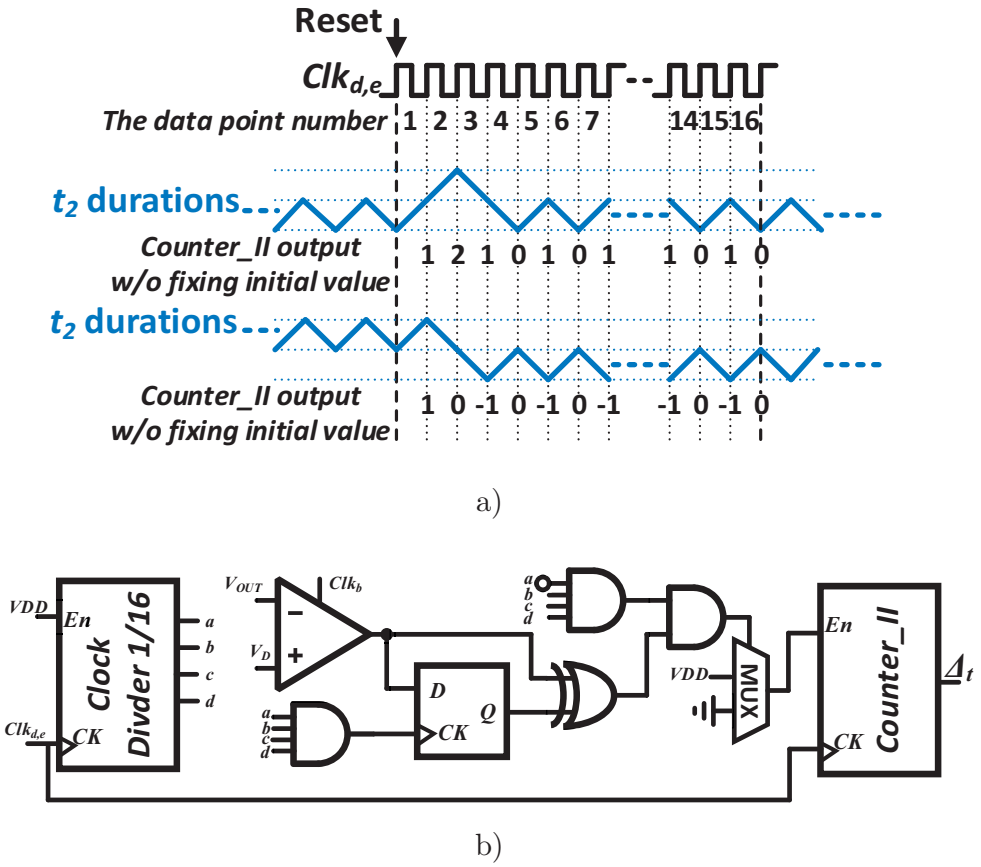


Figure 4-8: a) The output of *Counter_II* without fixing the initial value issue and b) hardware to fix the initial value issue of *Counter_II.*

the new cycle, zero signal will be sent to *Counter_II*'s enable pin. The schematic shown in Figure 4-8 b) is named *Bias Cancelling* in Figure 4-4.

4.3.4 System convergence to the maximum efficiency

The system in Figure 4-2 was implemented with some approximations described in this chapter. It was modeled at the system level to simulate and verify its functionality. The system's simulated output power for all the working points is shown in Figure 4-9 a) for a 2.5 Ω low-impedance transducer with an open-circuit voltage of 20 mV, and in Figure 4-9 b) a 180 Ω high-impedance transducer with an open-circuit voltage of 130 mV.

As seen in Figure 4-9 a) for the low-impedance transducer, there is no local maximum point in the output power response, and the system can converge to its maximum output power. For the high-impedance transducer, however, there are

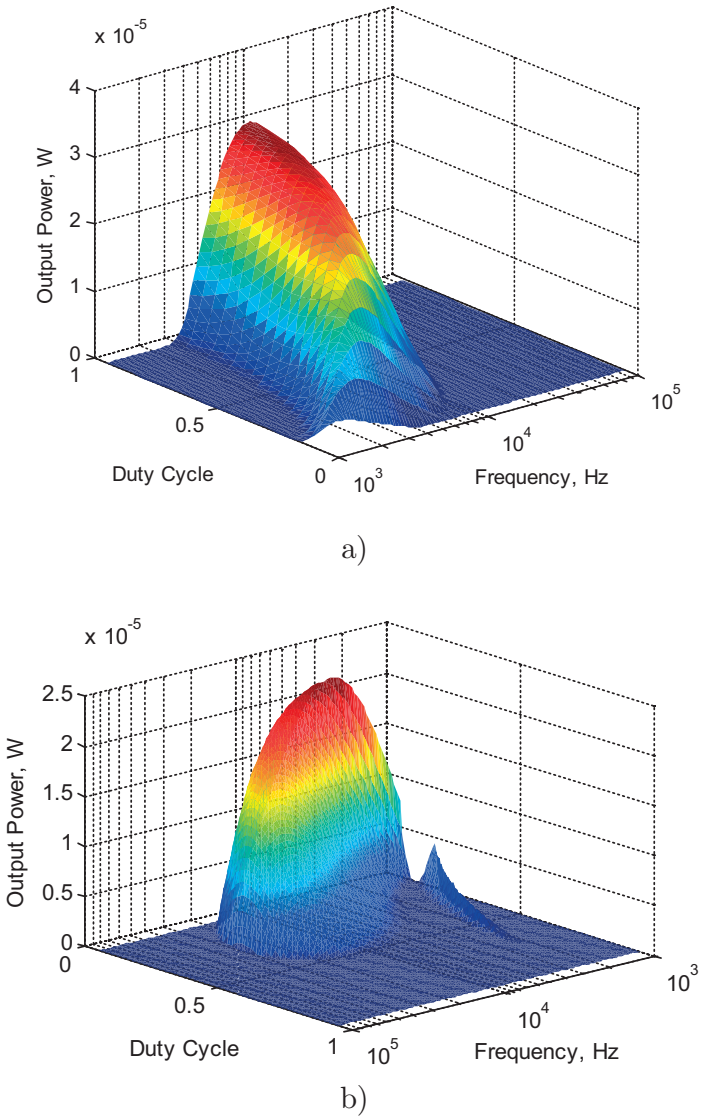
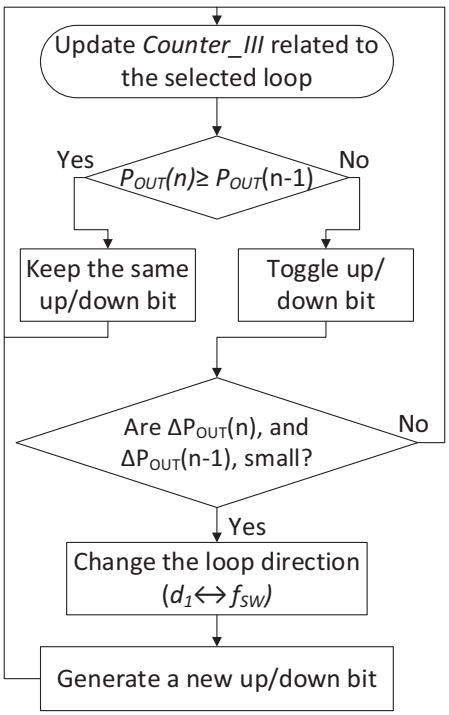


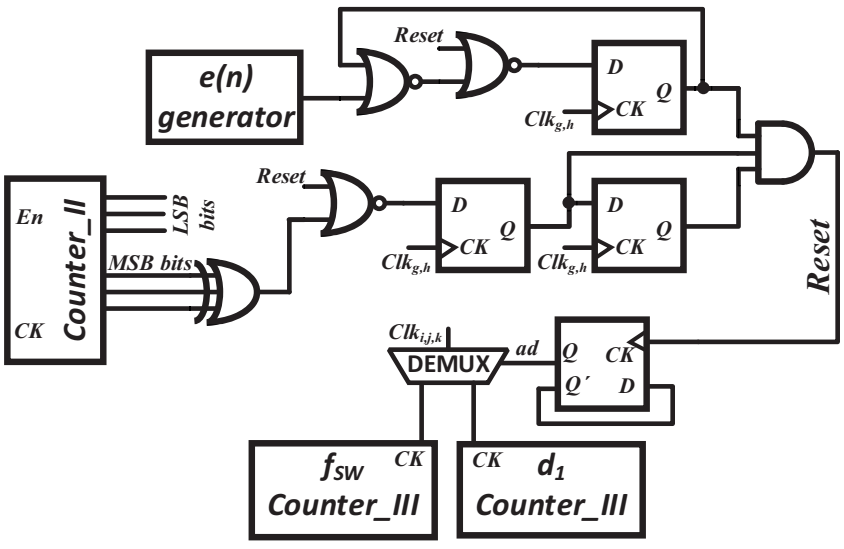
Figure 4-9: The output power of the implemented converter versus its duty cycles and frequencies for a) a low-impedance transducer and b) a high-impedance transducer.

local maximum points in Figure 4-9 b). Converging to the local maximum points has to be avoided, particularly in the area in which the output power is insignificant.

Insignificant output power results in a small t_2, whose value can be comparable with its resolution. Since the ratio of the t_2 value to its resolution is low in the area in which the output power is insignificant, the local maximum in that area cannot be detected by the actual circuit implementation. As Figure 4-9 b) illustrates, there is no local maximum in the area in which the output power is not insignificant. The



a)



b)

Figure 4-10: a) Flow diagram to find and lock in the maximum output power and b) a simplified schematic to implement the flow diagram in a).

converter shows the same response as Figure 4-9 b) for the other high-impedance transducers considered in this study.

To reach the maximum output power, the flow diagram in Figure 4-10 a) is implemented in the system. First, the system searches and finds an area in which the output power is maximized by sweeping d_1. Then, it finds a maximum output power point by sweeping f_{SW} in the area that was found before by sweeping d_1. This procedure is repeated up to the point that the system is locked to an f_{SW} and d_1 in which the output power is maximized.

The system finds a maximum point by monitoring the output power. When Δp becomes negative, it means that a maximum point has just been observed by the system. To make sure that this change in Δp was not caused by a sudden interference in the system, the loop also checks whether the output power variations were small in the two last cycles.

The simplified schematic in Figure 4-10 b) is based on the flow diagram sketched in Figure 4-10 a); this block is named *Locking det* in Figure 4-4. In the upper part of this block's schematic in Figure 4-10 b), the circuit checks whether Δp becomes negative. In the middle part, the schematic examines the most significant bits MSBs of *Counter_III* to see whether the changes in Δp were small in the two previous cycles. If both conditions are satisfied, a reset signal is generated and it will change the direction of the loop. This signal resets the flip-flop values in the schematic of Figure 4-10 b) as well. Design of the clock signals will be discussed in section 4.3.6.

Figure 4-9 reveals another potential challenge to converge to the maximum efficiency. As Figure 4-9 b) illustrates, in some working points with large duty cycles, the power transferred to the output of the converter with a high-impedance transducer is zero or extremely small. t_2 here can be locked to a minimum value. Once the t_2 value becomes very small, the system's resolution to detect small changes in the output power is decreased. Therefore, it would be possible for the f_{SW} loop to stay continuously active, without detecting any negative *e(n)* from the loop. In this case, *Counter_III* (and thus f_{SW}) reaches its maximum, and then starts again from its minimum. The d_1 loop cannot be activated to change d_1 to a smaller value, to escape the system from these working points.

To avoid such a circumstance, a small digital logic was added to the system to detect if f_{SW} *Counter_III* reaches its maximum from its minimum two times, without any changes in d_1. Once this digital block detects this situation, it restarts both f_{SW} and d_1 to their minimum values. As Figure 4-9 a) and b) suggest, in these minimum points, there is sufficient power to be detected by the system, or the system will eventually reach a detectable output power when f_{SW} is rising from its minimum. This block is named *Escape* in Figure 4-4.

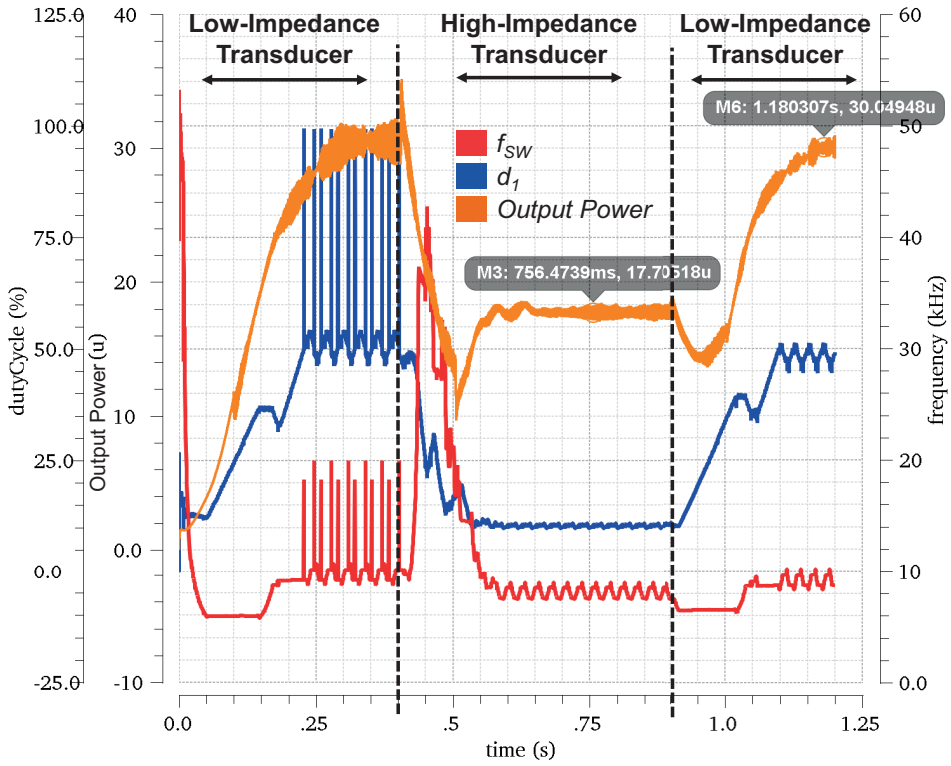


Figure 4-11: Circuit-level simulation of the whole converter system which is showing transferred output power, f_{SW}, and d_1 of the converter with different types of transducers.

Figure 4-11 illustrates a circuit-level simulation of the whole converter system. Here it assumes that a TEG with an open-circuit voltage of 20 mV and 2.5 Ω of output impedance is connected to the system for 0.4 s, and after that, the system is connected to another TEG with an open-circuit voltage of 130 mV and 180 Ω of impedance for another 0.5 s. To check the robustness and stability of the system, the first transducer is reconnected to the converter, up to the end of the simulation time.

The transferred output power of the system, the system's f_{SW}, and d_1, are depicted for 1.2 s. A small bias as the dynamic power consumption of the system is introduced in *Register_B*. The simulation results show that f_{SW} and d_1 converge to a working point that the output power of the converter falls to within less than 10% of the maximum value, which was anticipated from Figure 4-9 a) and b). Moreover, Figure 4-11 shows that, when the converter is reconnected to the first transducer, it has almost the same working point in the steady state as it had in the beginning.

The transfer output power is calculated and plotted by using a moving average window on instant transfer output power data. The spikes on the frequency and duty cycle diagram are created when the duty cycle changes from below 50% to

higher than 50% and vice versa. As will be explained later, at this point the DCO output is inverted. This results in erasing a part of one t_c duration from Figure 4-1, which the simulator considers as one clock with very high frequency and duty cycle. Other simulations were run for different transducers, and in those cases also the system performs as was anticipated from the discussion above.

Equation (4-3) and Figure 4-11 anticipate a lower impedance than was expected when the transducer with 180 Ω is connected to the system. Figure 4-11 illustrates that the system's duty cycle has been minimized and cannot get smaller to provide a higher input impedance for the converter in that case. On the other hand, when the 20 mV, 2.5 Ω transducer is connected to the system, Figure 4-11 and equation (4-3) anticipate a higher converter input impedance than was expected, although the duty cycle could have reached a higher value. Equation (3-13) shows that efficiency, which was related to the power loss of a converter, decreases as its input voltage decreases. Here, un-match impedances between the converter and its transducer have increased the input voltage of the converter. Therefore, both the power loss and the transfer power of the converter have decreased; however, the resultant output power has increased for the low-voltage 20 mV transducer.

4.3.5 Digitally controlled oscillator

An energy harvester switching power converter may not have a well-regulated supply voltage. However, the control variables, f_{SW} and d_1, have to be immune from supply variations, and they have to be set by the control system only. Therefore, the DCO, which is responsible for generating f_{SW}, and d_1, is implemented here based on a relaxation oscillator architecture. In this architecture, the frequency and duty cycle are generated by supply-independent current sources that charge and discharge passive elements.

Figure 4-12 shows a relaxation oscillator schematic in which both the frequency and the duty cycle can be tuned independently. The current source I_1 passes through R_{ref} to create a supply-independent reference voltage at the V_{in-} input of the comparator. On the other input of the comparator V_{in+}, a constant current source I_2 charges a capacitor bank linearly over time, and creates ramp voltage. As soon as the ramp level reaches I_1R_{ref}, the output of the comparator triggers the D flip-flop, and the output state of the D flip-flop will be toggled. Consequently, the part of the capacitor bank that was connected to the input of the comparator, C_1, will be connected to the ground to be discharged, and the other part of the bank that was connected to the ground before, C_2, will be connected to the input

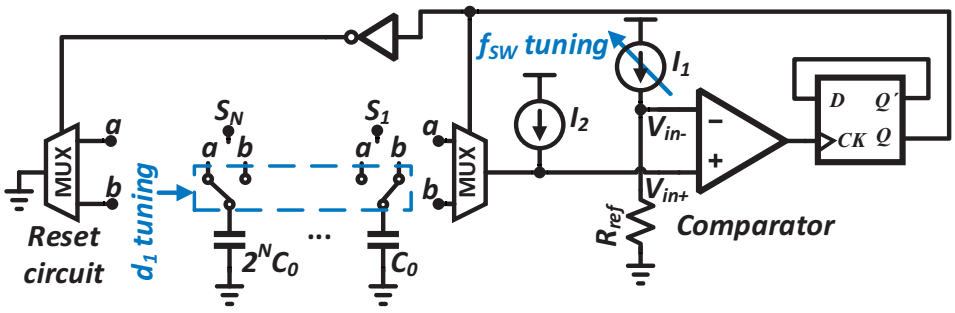


Figure 4-12: A relaxation oscillator with a tunable frequency and duty cycle.

of the comparator to be charged by I_2. The charging times for C_1 and C_2 are t_1 and t_C, and they can be calculated as:

$$t_1 = C_1 R_{ref} I_1 / I_2 \,,\; t_C = C_2 R_{ref} I_1 / I_2 \,. \tag{4-24}$$

From equation (4-24), the DCO frequency f_{SW} and its duty cycle d_1 can be written as:

$$f_{SW} = \frac{1}{t_1 + t_C} = \frac{I_2}{I_1 R_{ref}\left(C_1 + C_2\right)}, \tag{4-25}$$

$$d_1 = \frac{C_1}{C_1 + C_2}. \tag{4-26}$$

C_1 and C_2 together shape a capacitor bank, whose total capacitance is always constant. The capacitors of the bank can move from one side of the bank to the other side, namely from node a to node b, by S_1 to S_N switches. Therefore, the duty cycles are adjusted by designating the capacitors from node a to node b or vice versa. Since the total capacitance is constant, the DCO's frequency can be tuned by the digitally controlled current mirror I_1, which injects or steers current through the resistor R_{ref}.

Since the comparator in this architecture has a limited speed, the capacitors on V_{in+} always charge a ΔV more than V_{ref}, before output state toggling in the DCO. Since V_{ref} at high frequencies is smaller than its nominal value, and the converter speed is comparable with the working frequency, ΔV may reach the same order as V_{ref}. Here, the capacitors at the input of the comparator and the parasitic capacitance at V_{in+} are charged to $V_{ref}+\Delta V$. In the next state, V_{in+} with its parasitic capacitor connects to the other section of the capacitor bank by the switches in the multiplexers. Meanwhile, the charge injection and clock feedthrough of those switches will increase parasitic capacitance voltage even more than $V_{ref}+\Delta V$.

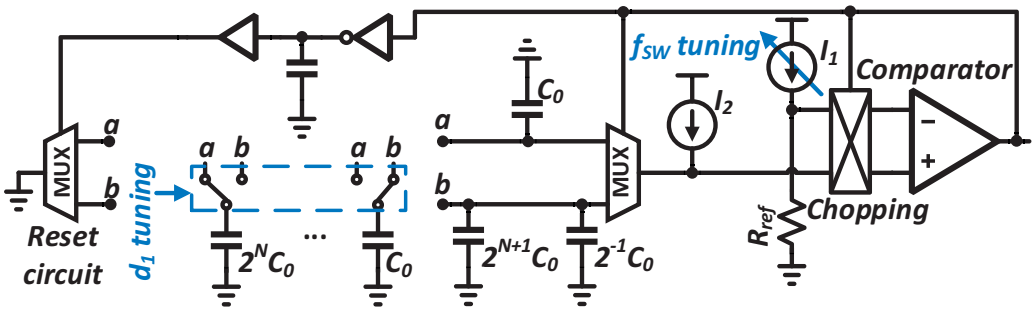


Figure 4-13: The comparator's input chopping in a relaxation oscillator with a tunable frequency and duty cycle.

If the DCO has a high duty cycle, the other section of the capacitor bank, which will be connected to the input of the comparator, may have a small capacitance. Once this section is connected to V_{in+}, the charges on the comparator's input parasitic capacitance will be distributed, and will charge the small capacitor connected to V_{in+}. The small capacitor may even be charged to a voltage higher than V_{ref} at the beginning of the cycle. In this situation, the DCO will stop working.

To limit the capacitor bank's voltage level to a value less than V_{ref} at beginning of a cycle, the comparator's input can be chopped as shown in Figure 4-13. With this method, the input node whose parasitic capacitor has been charged up to V_{ref} by I_1 and R_{ref} will be connected to the small capacitor at the beginning of the new cycle. Here, since the maximum voltage at the comparator's input parasitic capacitor was V_{ref}, after charge distribution, the voltage level on the small capacitor will be less than V_{ref}. Chopping in a relaxation oscillator was suggested before in [105, 106] to eliminate offset of the comparator. However, in this work, the chopping method is introduced mainly to achieve a high duty cycle signal from the DCO over a wide frequency tuning range. Moreover, the DCO can benefit from reduction of low-frequency noise and offset provided by the chopping method.

As Figure 4-13 illustrates, a small delay is also added to the address bit of the *Reset multiplexer*. This delay keeps the discharging capacitors connecting to the ground, in a very short duration, while they are connected to the input of the comparator. This will partially discharge the input parasitic capacitor even less than V_{ref} at the beginning of the new cycle. This delay should be short enough not to dissipate I_2 to ground nor to limit the frequency or the duty cycle of the DCO.

This DCO was designed to have a tunable duty cycle from about 50% to 90%. If a lower duty cycle is needed in the control system, the output of the DCO is multiplexed with its inverted output. To have duty cycles higher than 50%, the biggest capacitor in the capacitor bank is designed to not be switched by the tuning

circuit, and is fixed in the bank. This prevents charge injection and large dynamic power consumption of a big switch responsible for moving this large capacitor from one node the other. This is helpful particularly when a duty cycle around 50% is needed as the converter's operating point in the steady state.

A small capacitor is placed next to the big fixed capacitor. The small capacitor is sized to be bigger than all the parasitics resulting from the connections in the bank, to make sure that duty cycle is always bigger than 50%. Another small fixed capacitor is placed on the other node in order to avoid having just parasitic capacitance when the duty cycle of the DCO is maximized. The smallest capacitor and R_{ref} are designed to have a good trade-off between dynamic and static power, respectively, with the noise level. The capacitor is selected to be big enough to keep the sampling noise level less than the system noise, and small enough to keep the entire area and dynamic power consumption at an acceptable level. An R_{ref} with a reasonable area is selected to create a V_{ref} much bigger than comparator input-referred noise by consuming negligible static power.

A simplified switch-level implementation of the chopping circuit and the multiplexers is shown in Figure 4-14 a). To make the schematic more clear, the short delay for the reset circuit is not depicted. The comparator is implemented by a two-stage amplifier as shown in Figure 4-14 b), and is supplied by 0.9 V as is the rest of the control section. The amplifier bias current is provided by a low-voltage CMOS current source with a start-up [107] circuit. The two-stage amplifier has a gain-bandwidth product that depends inversely on a small gate-drain overlap capacitance; it can have a higher speed than the other configurations for a comparator, particularly at low voltages. Since PMOS transistors have lower low-frequency noise and can be biased in the saturation region with an input common-mode voltage near ground, they are employed as the input stage. For a continuous comparator, a previous study [108] suggested to be followed by a Schmitt trigger to sharpen the edges and make the output rail-to-rail. The Schmitt trigger is designed here to have a small hysteresis to not limit the frequency or the duty cycle of the DCO.

Post-layout simulations show that the proposed architecture for the DCO with a tunable duty cycle and frequency can be monotonically tuned in a frequency range of 3.75 kHz to 84 kHz, and a duty cycle range of 50.3% to 92% while consuming only 150 nW of static power and 35 nW dynamic power in 10 kHz.

The proposed converter architecture uses the d_1 parameter to control the S_1 power switch, instead of the common practice in the literature where t_1 has been used to control the NMOS power switch and has been generated separately by a pulse generator. Thanks to this DCO, the architecture here provides the possibility

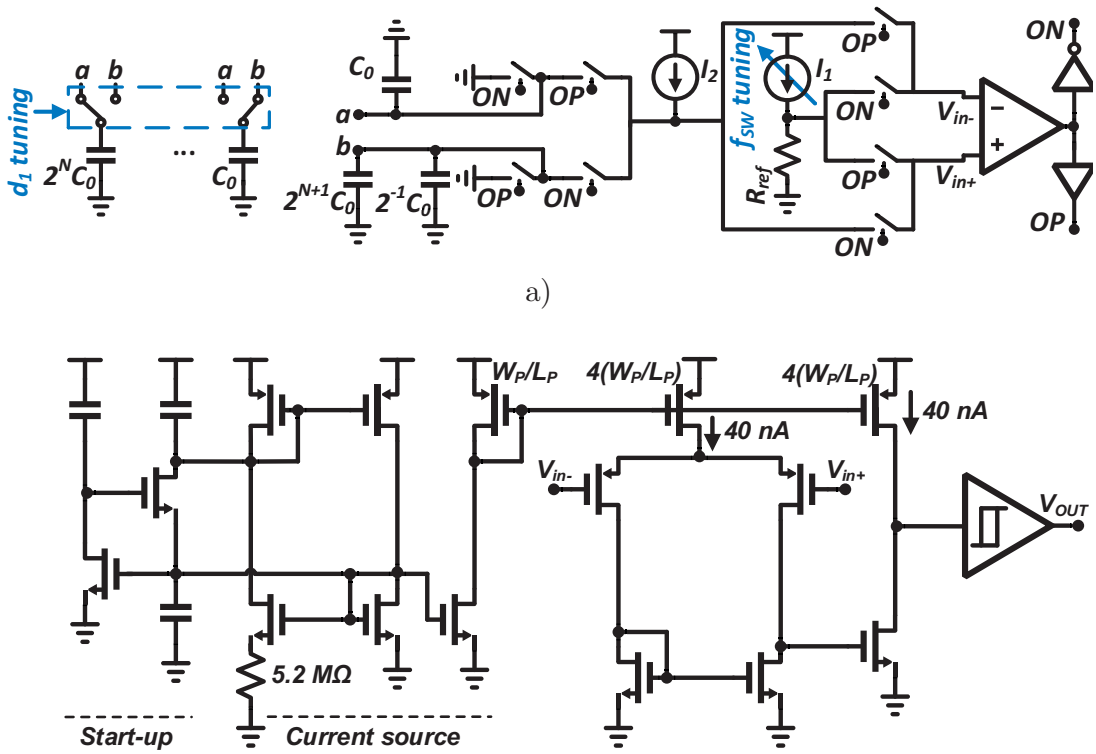


Figure 4-14: a) Simplified schematic of the proposed tunable relaxation oscillator with a chopper at the comparator's input and b) schematic of the continuous time comparator with its low-power current source.

to have two control variables independent of each other, while both are generated by just one block.

4.3.6 Control system clock design

The core converter circuit needs two non-overlapping pulses t_1, and t_2 as was described in section 4.2. t_1 pulses were generated directly by the DCO with a d_1 duty cycle and f_{SW} frequency. t_2 pulses were produced by a t_2 pulse generator, which was triggered by the falling edge of t_1 after a short delay. To keep the system low power without any extra clock or pulses, the control system was designed to be asynchronous, and its blocks were just clocked by t_1 or t_2. Since t_1 and t_2's frequency were f_{SW}, and from equation (4-2) f_{SW} was related to the available power, the system's control section power consumption was proportional to the available input power. Thus, the system efficiency was maintained with different working conditions. However, such an asynchronous architecture could increase system complexity, and complicate clock assignment to different blocks.

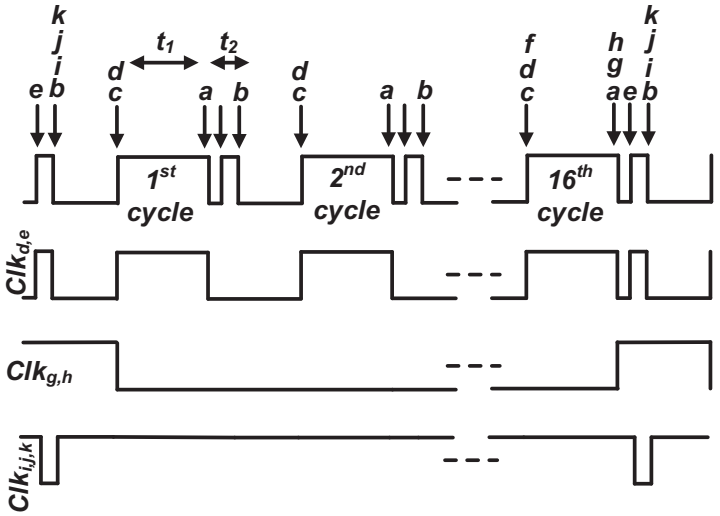


Figure 4-15: The clock assignment for each block in the control system.

As a new set of t_1 and t_2 are generated and applied to the converter core in one cycle, it is necessary to readout the corresponding output power in the same cycle. Accordingly, based on the recorded output power, the required computations have to be executed by the control system in the same cycle. Then, the inputs of the DCO and the t_2 pulse generator have to be updated to generate new durations for t_1 and t_2 for the next cycle. In such a system without any extra clock source, the converter has to be triggered just with the t_1 and t_2 pulses in each cycle, and the resulting output power has to be read at the same cycle. It is not possible to dedicate an entire cycle to just one specific assignment from the tasks that were mentioned above.

To design the clock assignment for the control system based on these requirements, the timing sequence of the main control sections has to be known. In Figure 4-15, t_1 and t_2 pulses are drawn, and the moments that the main control blocks (which have been described in this chapter) have to be triggered are marked. The falling edge of t_1 has to trigger the t_2 pulse generator. Later at the falling edge of

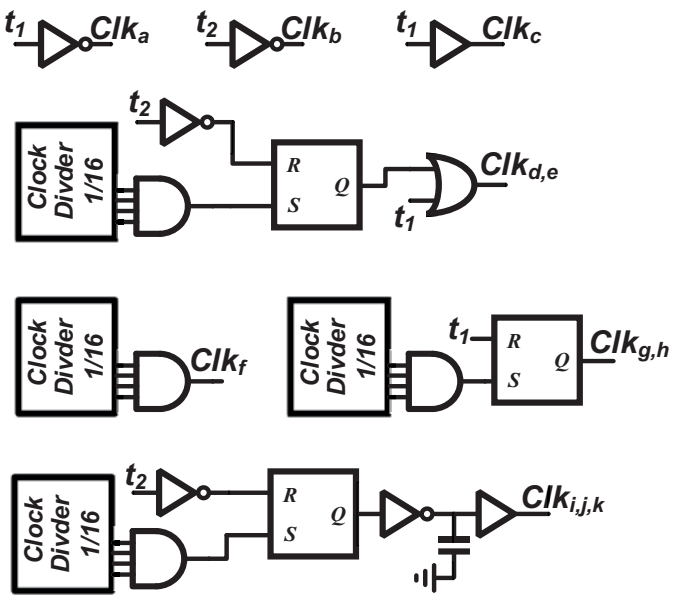


Figure 4-16: The digital circuits implemented to create system clocks.

the generated t_2, the data related to the output power has to be read. Therefore, at the end of t_2, the latch comparator has to be activated. The data related to the output power should be available at the beginning of the next t_1, so at this moment *Counter_I* has to be updated. Simultaneously at this moment, Δt_2 in the digital domain which was *Counter_II*'s output has to be updated, and the *clock divider 1/16* counter has to start to count. Additionally, these two counters need to be restarted at end of the 16th cycle. Therefore, a clock $clk_{d,e}$ that is triggered by these counters as shown in Figure 4-15 is created following the schematic in Figure 4-16.

At the beginning of the 16th cycle, the input of *Counter_II* is stored by the *Bias_cancelling* block for a possible correction of *Coutner_II*'s value as was described in section 4.3.3.2.2. Once information related to Δt_2 becomes ready at the 16th cycle, the loop can be clocked to start computing whether the f_{SW} or d_1 value has to be decreased or increased. At the same time, the loop has to be clocked to decide whether the system is locked on a new f_{SW} or d_1. To execute these functions, the system is clocked by $Clk_{g,h}$. As shown in Figure 4-15 and Figure 4-10 b), $Clk_{g,h}$ activates the *e(n)* generator block that computes the up/down bit of *Counter_III*, and the *Locking det* block, which makes the decision to change the direction of the loop from f_{SW} to d_1 or vice versa. The digital circuit for $Clk_{g,h}$ is shown in Figure 4-16.

Once the up/down bit of *Counter_III* is computed and the loop that should be activated is selected, the *Counter_III* dedicated to that loop will be updated by

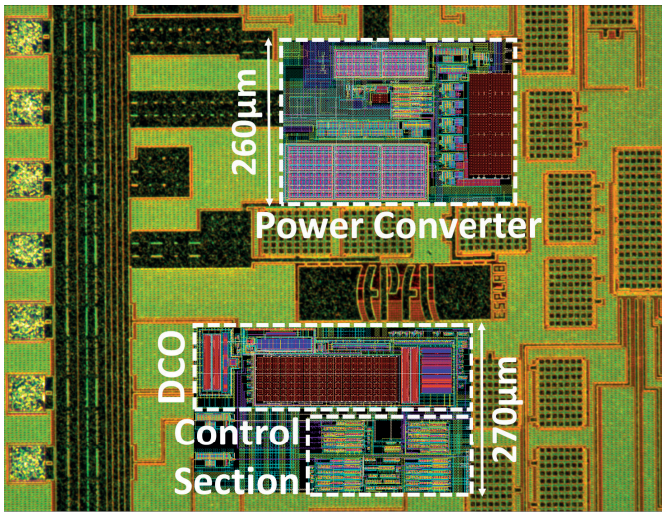


Figure 4-17: The converter with a low-complexity control section microchip designed in UMC 0.18 µm.

$Clk_{i,j,k}$ as shown in Figure 4-15. Additionally, if the d_1 loop has to work, and based on the computations, it should be changed from a value a little higher than 50% to lower than 50% or vice versa; a logic circuit responsible for inverting the DCO output, the d_1_*inverting* block, has to be activated too. If the output of the DCO is commanded to be inverted by the d_1_*inverting* block, exactly after the rising edge of $Clk_{i,j,k}$, a t_1 pulse will be generated because of toggling of the DCO output from zero to one. To avoid short circuiting the output source to ground, the new t_1 must not have any overlap with the previous t_2.

Additionally, the $Clk_{i,j,k}$ clock is used for a logic circuit that monitors whether the system is stuck in the area with a low available power from Figure 4-9. This logic circuit block was named *Escape*. If the system is stuck in the low available power area as described in section 4.3.4, the *Escape* block would reset *Counter_III*. The schematic that generates $Clk_{i,j,k}$ is shown in Figure 4-16. To satisfy the non-overlapping condition from the paragraph above, $Clk_{i,j,k}$ is made with a delay version of t_2 at its 16th cycle. The small delay schematic depicted in Figure 4-16 prevents a new t_1 from having any overlap with the previous t_2 when the d_1_*inverting* block is activated.

4.4 Measurement results

The proposed low-voltage low-power converters along with the control sections and pulse generators were designed and implemented in UMC 0.18 µm CMOS technology. The converter with the low-complexity control section, *Chip I*, and the

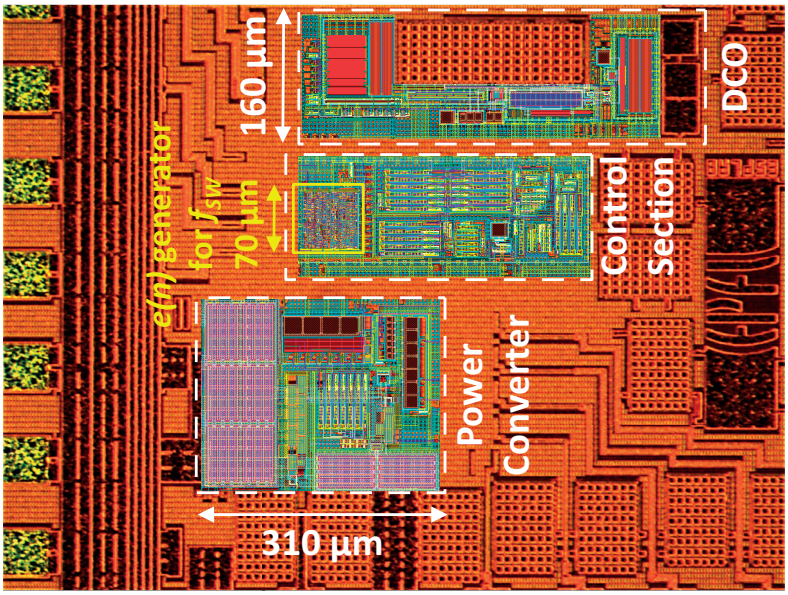


Figure 4-18: The converter with a moderate-complexity control section microchip designed in UMC 0.18 µm.

converter with the moderate-complexity control section, *Chip II*, occupy an area of 0.2 mm^2 and 0.21 mm^2, respectively. Microphotographs of *Chip I* and *Chip II* are shown in Figure 4-17 and Figure 4-18.

The components on the PCB were selected to have a good trade-off between the efficiency, form factor, and performance of the system. L_S is a low-resistance inductor, which was selected to have the highest possible inductance in the area available on the PCB. A 47 µH 0.2 Ω inductor with an 0.8 × 0.8 cm^2 form factor was selected for this application.

For the input capacitor, the available area on the PCB is not the main concern to determine its capacitance. As was shown in Figure 4-3, and discussed in section 4.2.2, when the input capacitance increases, the speed of the control loops has to be reduced to have a stable control system. Therefore, the size of the capacitance has to be chosen to have enough speed in the loops to follow variations in the converter's transducer in different environments. However, in this work, since the porotypes of the chips had a complex mixed-signal asynchronous architecture, it was necessary to implement systems that could be verified by simulations. Therefore, the actual size of the input capacitor was selected to have systems fast enough to be able to simulate and to verify their different functionalities. A 22 µF and a 100 µF capacitor with form factor 1.6 × 0.8 mm^2 and 1.6 × 1.2 mm^2 were selected for this application. As discussed in section 3.2.3, these values are acceptable from an efficiency point of view.

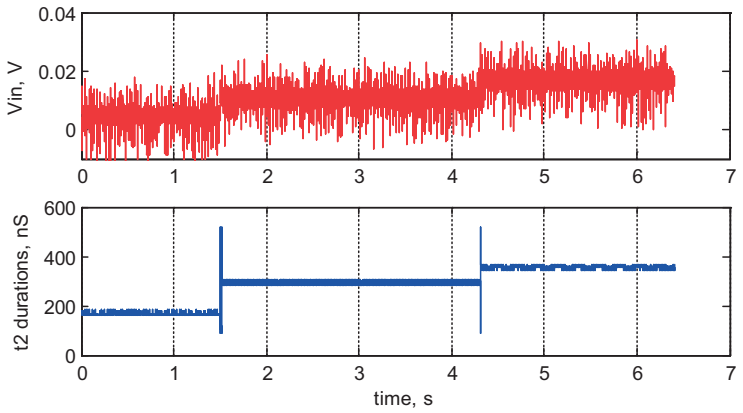


Figure 4-19: System input voltage variations and consequent t_2 durations.

The energy storage can be a high-capacity capacitor bank or a supercapacitor, whose voltage can be fixed by a regulator, or a second-stage conventional switching converter as it was described in section 2.3. With a 100 µF output capacitance, less than 1% ripples are expected on the output voltage during one cycle of frequency update in the worst case scenario. Here, it is assumed that the output energy storage has some charge during start-up by the regulator, that is to say, the cold start is not necessary for this architecture to focus.

Once the f_{SW} loop is not considered, both systems have an almost identical working operation. In the beginning of this section, we will use the *Chip I* converter to characterize the common specifications of the converters with opening the f_{SW} loop. After that, the loop will be closed and the entire performance of each chip is measured and discussed separately. Last, the chips' performances are summarized with the other state-of-the-art.

As a common specification of the converters, t_2 stability is validated with deactivating the f_{SW} and d_1 loops, and applying 10 mV steps as the open-circuit voltage of an emulated transducer. The transducer is a low-voltage 2.5 Ω TEG, the previously mentioned worst-case scenario. Figure 4-19 illustrates the measurement results, which show that t_2 follows the converter input variations. Simulations anticipate a power consumption of less than 120 nW at 20 kHz for the blocks that set t_2, excluding the dynamic power necessary to switch S_1 and S_2.

4.4.1 *Chip I* characterizations and discussions

Measurements of f_{SW}, d_1, and the average current delivered to the output when all the loops are working in *Chip I* are presented in Figure 4-20. The open-circuit voltage of the 2.5 Ω TEG increases from 10 mV to 30 mV. The converter and all

the other sections are supplied by a 1.1 V source which has the same level as the output voltage of the converter. f_{SW} and d_1 become stable after about 3 seconds.

As this Figure 4-20 illustrates, for 10 mV of open-circuit voltage of the low-impedance transducer[3], about 50% of the available power is transferred to the output with 5 kHz working frequency and 60% duty cycle. When the input power is increased by raising the open-circuit voltage of the emulated transducer to 30 mV, the working frequency is increased, as expected, and it reaches 21 kHz. Here 63% of the available power is transferred to the output. A transfer power of more than this value is not expected from this converter, as was explained in section 4.3.3.1. To calculate the efficiency η, the power consumption of the system has to be subtracted from the transferred power. Measurements show that for just 15 mV of input voltage, the converter's η reaches 52%.

The data plotted in Figure 4-20 were extracted by a National Instrument data acquisition device. This device has a 250 kS/s sampling rate which is not fast enough for measuring the duty cycles precisely, particularly in high working frequencies. Here, we tried to avoid aliasing by filtering the data, however, a 20% to 30% inaccuracy was observed in the duty cycle data. The precise value of the duty cycle is expected to be 20% to 30% higher than the data plotted here. If the duty cycle is higher than 50%, the actual value of the duty cycle can be expected to be 20% to 30% higher than was read from the device, and vice versa.

Figure 4-21 illustrates f_{SW}, d_1, and the delivered output current when the output resistance of the transducer increases from 42 Ω to 192 Ω. These values are close to the output resistance of the midrange- and high-impedance TEG used for the application[4]. The measured values of both f_{SW} and d_1 decrease once the available power from the transducer is decreased and the impedance of the transducer is increased. This is in very good agreement with simulations and the discussions in this chapter. Here, with the 42 Ω emulated transducer which has 90 mV of open-circuit voltage, almost 80% of the available power is transferred to the output. However, this value is not expected to be repeatable as the maximum transfer power for this architecture was calculated to be about 70% in Appendix B. The system is locked to a working point near the absolute power transfer maximum.

[3] All the measurements are carried out with emulated transducers in the measurement results section.
[4] When the measurements of this section proceeded, the optimized midrange- and high-impedance TEG transducers were reported to have the impedances as mentioned here.

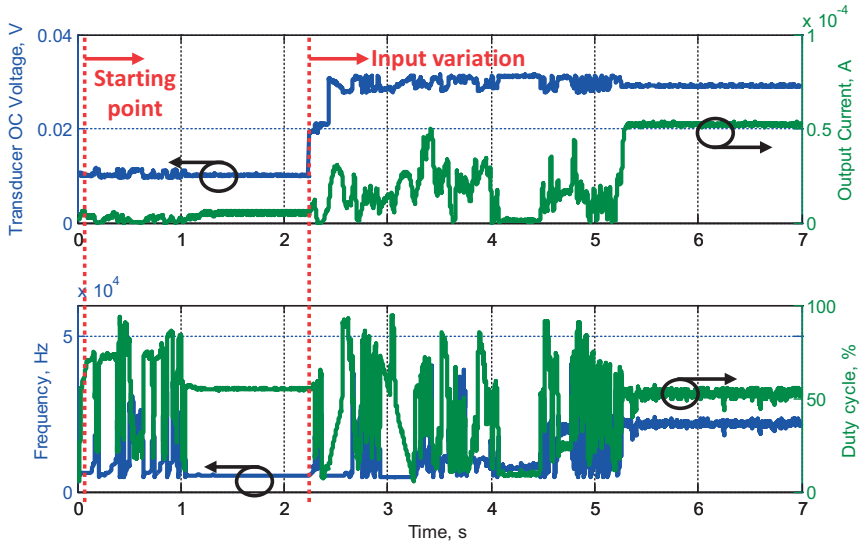


Figure 4-20: f_{SW}, d_1, and output current variations of the converter in *Chip I* with harvester output open-circuit voltage variation.

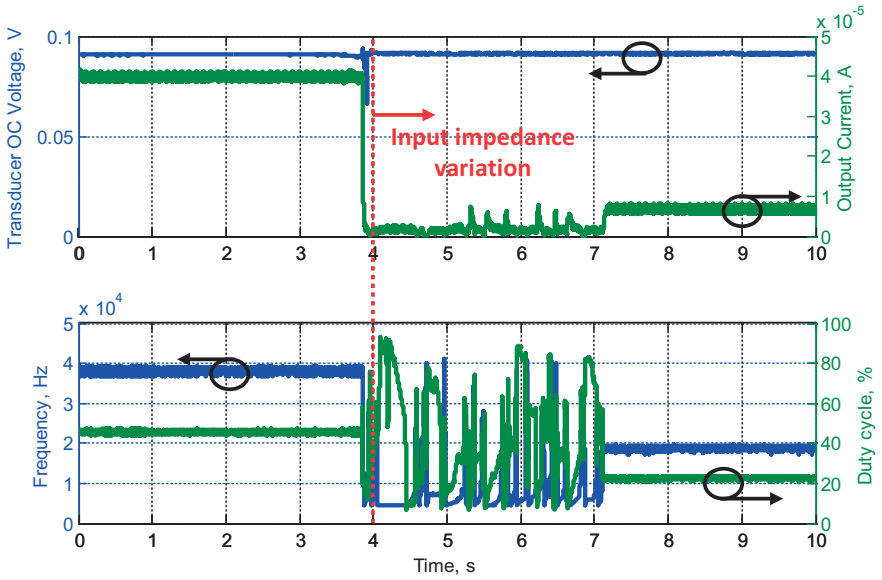


Figure 4-21: f_{SW}, d_1, and output current variations of the converter in *Chip I* with variations in the harvester's resistance.

η of the converter for a high-impedance transducer is measured at 64% by using a 560 Ω PV emulated transducer with 400 mV of open-circuit voltage. Measurements showed that the system locked on an f_{SW} of 7 kHz and d_1 of 4.5% as its working point when this transducer is connected to the converter.

The measured power consumption of the f_{SW} and d_1 loops is 800 nW including 500 nW of the DCO at 10 kHz. The quiescent power consumption of the entire system including all control loops and the dynamic power required for the power

switches is 2.1 μW at 10 kHz. If the dynamic loss of the switches is excluded, the system power consumption is just 1.2 μW at 10 kHz. Increasing the transducer's available power increases η only up to about 70% as was suggested in section 4.3.3. Beyond this point, Δp can no longer be estimated using Δt_2^2.

4.4.2 *Chip II* characterizations and discussions

The previous chip used the fact that the variations in t_2 were much faster than f_{SW} to successfully establish the entire system without any power-hungry blocks. However, as was shown and discussed in section 4.3.3 and in Appendix B, this implementation limited the converter efficiency to a maximum of about 70%, which may not be enough for some transducers. Moreover, since its working frequency growth was not monitored, the working points that were obtained once by the converter were not repeatable in some cases.

The converter in *Chip II* has a more elaborate complexity in design, however, it consumes an ultra-low power similar to *Chip I*. Here, a holistic view of the system was used to make the power- and area-hungry components precise enough to save a drastic amount power and resources. The main additional block in *Chip II* is the section that produces $e(n)$ for the f_{SW} loop. As shown in Figure 4-18, this section has an area of 70 × 70 μm, which is less than 10% of the entire control section with an area of 135 × 380 μm, and it consumes just 12 nW at 10 kHz, which is less than 40% of the control section and less than 5% of the entire system consumption at this frequency. The small-area and low-power headroom control section which consumes just dynamic power can be considered to add to the low-power converters in which the working frequency is adjusted manually, or by power-hungry analog sections. Furthermore, the digital inputs of the DCO and the t_2 pulse generator which were related to the value of f_{SW}, d_1, and t_2, provide valuable information concerning the transducer available power, type of the transducer, and its voltage level for high-level energy aware algorithms which may use in the application.

Moreover, *Chip II* does not have the limited efficiency and unpredicted working points with a specific type of transducer as was shown in Figure 4-11 and section 4.3.4. Therefore, it will be used as the main candidate for the energy harvesting section of the project mentioned in Chapter 2. The blocks that *Chip II* has in common with *Chip I* are redesigned to have more optimum power consumption. Since the front-end designed for this project needs a minimum regulated 1.2 V supply voltage, and the supply should be provided by the output of the converter, *Chip II* was designed to have a 1.6 V output. In this case, a sufficient margin is available

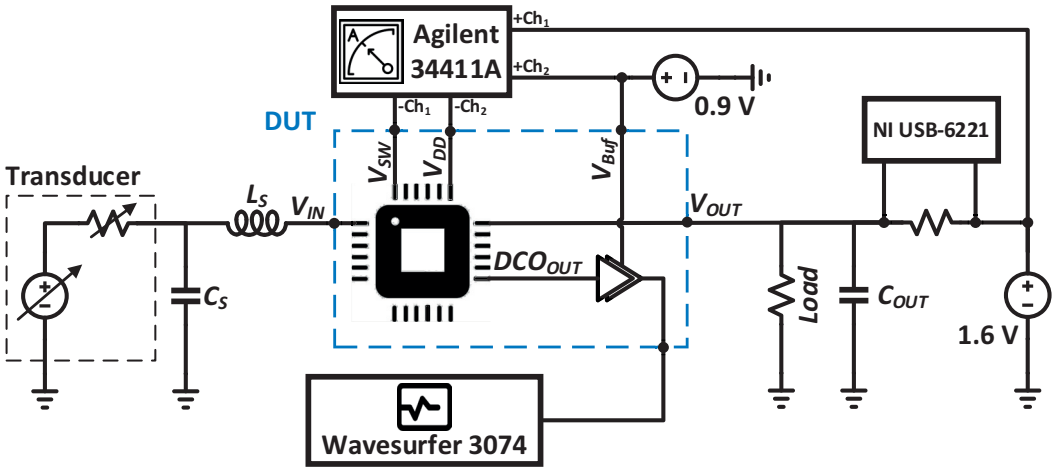


Figure 4-22: *Chip II* test setup.

to provide a regulated supply for the front-end. However, to keep the power consumption low in the control system, all the blocks in the system are supplied by 0.9 V that can be provided by the switch capacitor converter mentioned in Chapter 2. This voltage is the half of the supply used in the in standard 0.18 µm CMOS technology, and it provides a sufficient headroom for the analog circuits, while keeps the digital circuit consumption negligible compared to the available power. Besides, the digital standard cell libraries available in the technology are expected to be operational [109] with this supply voltage.

Here just S_1 and S_2 are switched by the same voltage as the output, i.e. 1.6 V. The switches are controlled by the control system through level shifter circuits and chains of buffers. Each multi-stage tapper buffer chain has an aspect ratio of 6, which provides a good trade-off between switching dynamic loss and short-circuit loss due to non-zero rise or fall time. The delays of the chains were considered in the design of the deadtime delay generator block. Here, the dynamic power loss in the power switches is considered in computing η of the system, and will not be reported as part of the system power consumption.

The test setup of *Chip II* is shown in Figure 4-22. A National Instrument USB-6221 data acquisition system and an Agilent 34411A Digital Multimeter are used to measure output power and power consumption of the device under test (DUT), respectively. To emulate transducers behavior, an Agilent E3631A power supply and a series resistance are employed. A Teledyne LeCroy WaveSurfer 3074 is connected to the DCO output to record the f_{SW} and d_1 data.

Measurements of f_{SW}, d_1, and the average current delivered to the output in *Chip II* are presented in Figure 4-23. The open-circuit voltage of the 2.5 Ω TEG increases

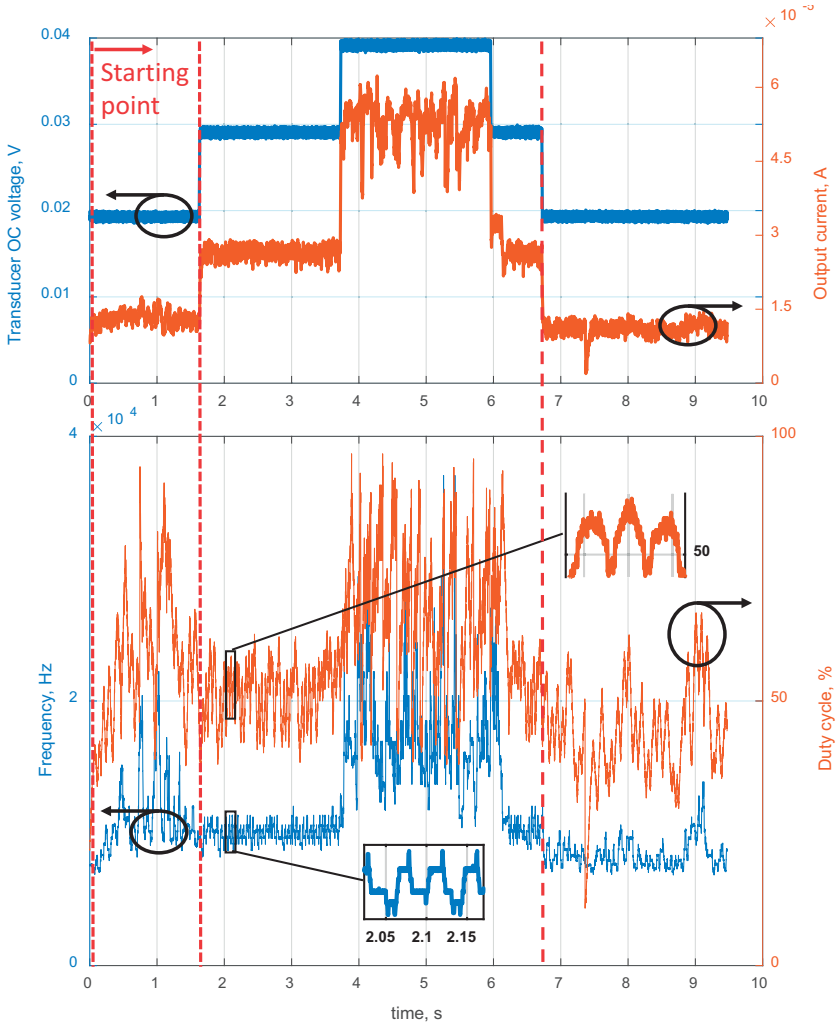


Figure 4-23: f_{SW}, d_1, and output current variations of the converter in *Chip II* with harvester output open-circuit voltage variation.

from 20 mV to 40 mV, and it returns to 20 mV. f_{SW} and d_1 become stable after less than 0.2 s. As this figure illustrates, for 20 mV of voltage of the low-impedance transducer, about 50% of the available power is transferred to the output with 9 kHz working frequency and 44% duty cycle. When input power is increased step by step by raising the open-circuit voltage of the emulated transducer, the working frequency is increased step by step, as was expected, reaching 10 kHz and 19 kHz for 30 mV and 40 mV, respectively. Here, on average 51% and 57% of the available power is transferred to the output for the open-circuit voltage of 30 mV and 40 mV. As shown in Figure 4-23, when the power decreases to the same level as it was before, the system will be locked to almost the same working point as it had at the beginning. f_{SW} and d_1 are magnified to compare the behavior of the converter in the measurement with the simulation result in Figure 4-11. As seen in these figures,

the measured values of f_{SW} and d_1 are in very good agreement with the simulation results.

A 100 µF C_S is used at the input of the converter for this measurement. As discussed in section 4.2.2, increasing the C_S capacitance decreases PM of the system. As seen in Figure 4-23, the selected C_S does not provide a sufficient PM for f_{SW} to be perfectly stable with a transducer open-circuit voltage of 40 mV. This issue disappears with a smaller C_S, although, the average transfer power here is acceptable for the application. The variations on d_1 can be reasonable since on the one hand, more than a 95% of the available power can be transferred with a large impedance mismatched as about -40% to +50% (which corresponds +25% to -20% variations in d_1), and on the other hand, the input voltage is not ideal and it has ripples.

When the transducer open circuit voltage decreases from 30 mV to 20 mV, f_{SW} is not reduced proportionally. As discussed in section 3.2.3 and shown in Figure 3-3 and Figure 3-4, with the limited passive components, the power transfer losses will be more dominated than converter's static and dynamic losses for the working frequencies below 8 kHz. When the static and dynamic power losses are not dominated anymore, equation (4-2) is not valid. Therefore, as measurement results confirm, it is expected that the converter limits f_{SW} at about 8 kHz to maintain the system efficiency.

As stated above, the f_{SW} and d_1 data are extracted by a Teledyne LeCroy - WaveSurfer oscilloscope. The device has 1 MS/s rate for recording data in a 10 s window. This provides adequate speed to measure and characterize the f_{SW} and d_1 data in detail. *Chip II* flows the diagram in Figure 4-10 a) to find and lock in the maximum output power. According to the diagram, the system changes its direction from the f_{SW} loop to the d_1 loop when P_{OUT} becomes smaller than its previous value, and $e(n)$ becomes negative. When $e(n)$ is zero, f_{SW} and d_1 vary in the vicinity of the actual locking point. However, *Chip I* changes its loop direction when $e(n)$ becomes zero; therefore, f_{SW} and d_1 vary in a smaller window about the locking point, and thus the locking procedure is slower.

Figure 4-24 illustrates the entire power consumption of the system with variations in the available power from the 2.5 Ω transducer. The emulated transducer available power is changed by altering its open-circuit voltage while keeping its impedance constant. Since, the architecture in *Chip II* was implemented asynchronously and was clocked by f_{SW}, it was expected that the power consumption of the system would vary with the available power and output power of the converter. Therefore, the measurement results in Figure 4-24 are in good agreement with the expected results.

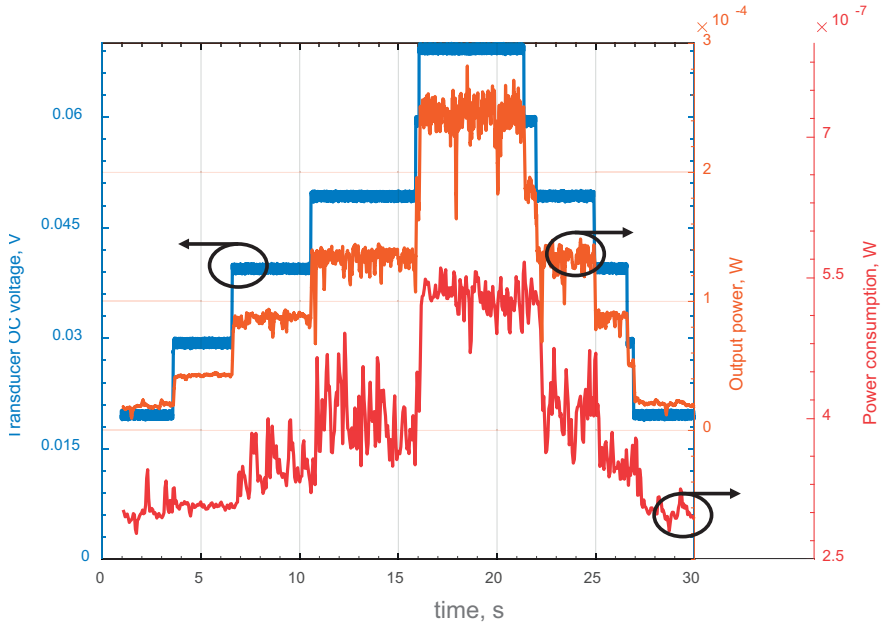


Figure 4-24: The entire power consumption of the system in *Chip II* with the variations of the harvester input available power.

As stated in section 4.3.3.2, the combination of the dynamic loss energy by the gates of the power switches and the system power consumption was considered as a constant introduced to the converter by a register, called *Register_B*. Measurements of f_{SW}, the system power consumption, and the power loss in the gates of the power switches are plotted in Figure 4-25 with variations of the *Register_B* value. By increasing the value, the control system considers more dynamic losses in the converter; therefore, it locks to a lower frequency to have an optimum point. Accordingly, the power loss of the system and the dynamic power loss in the gates of the power switches are decreased as expected from an asynchronous system.

The input impedance, d_I, and f_{SW} of the system are depicted in Figure 4-26 with variations in the open-circuit voltage of an emulated 20 Ω transducer. This is similar to the TEG with a midrange impedance used for the application. As discussed before, to have higher efficiency in ultra-low-voltage conditions, it is more beneficial to have a higher input impedance converter, with a higher input voltage, than a matched system with a lower input voltage. Here measurements confirm this expectation from the system. When the transducer output voltage is low, the input impedance of the system is slightly higher than the impedance of the transducer. The system input impedance reduces when the transducer's voltage becomes larger.

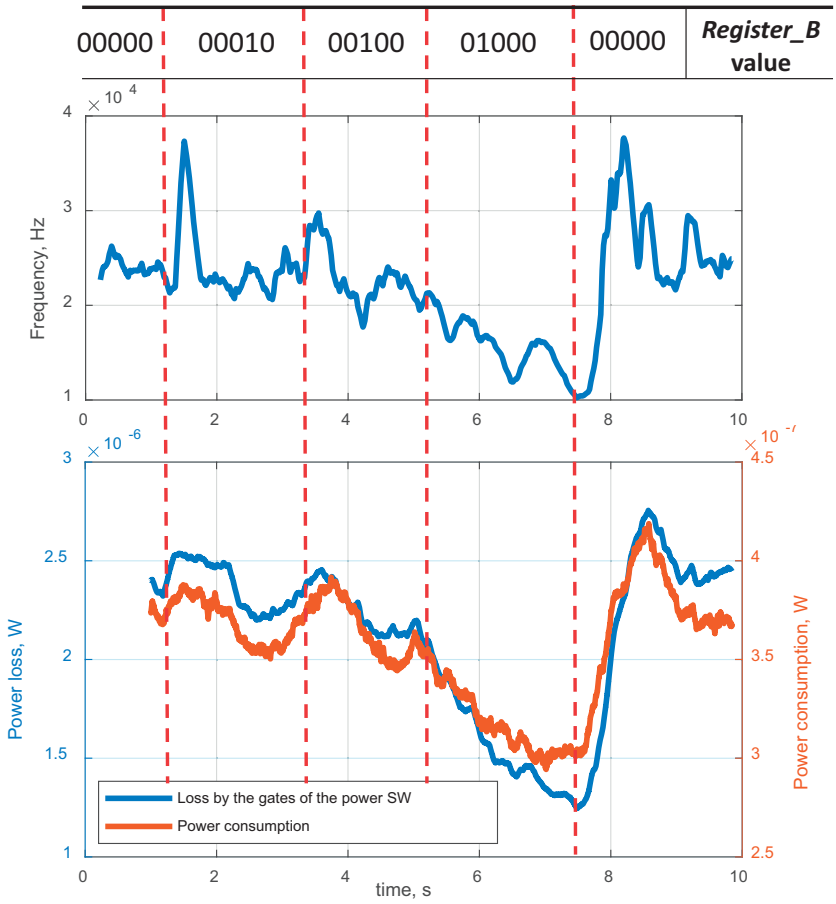


Figure 4-25: The entire power consumption of the system, dynamic loss by the gates of the power switches, and f_{SW} in *Chip II* with the variations of the *dynamic loss bias* value in *Register_B*.

Figure 4-27 illustrates the delivered output power and η of the converter with increasing available power from a transducer with 20 Ω impedance in a range of a few microwatts to several hundreds of microwatts. Since the designed pulse generator and the DCO have a wide tuning range, the converter can transfer power to its output in this wide range of the available power. η varies in the range of 63% to 73% in the entire region.

Figure 4-28 illustrates f_{SW}, d_I, and the delivered output current when the output resistance of the transducer changes from 2.5 Ω to 180 Ω. As was mentioned in Chapter 2, these impedances are similar to the output resistance of the two types of TEG used this study. The measured values of both f_{SW} and d_I decrease once the available power from the transducer is reduced and the impedance of the transducer is increased. This is in very good agreement with simulations and the discussions in section 4.3.3. Here, with the 2.5 Ω emulated transducer which has 30 mV of open-circuit voltage, almost 50% of the available power is transferred to the output,

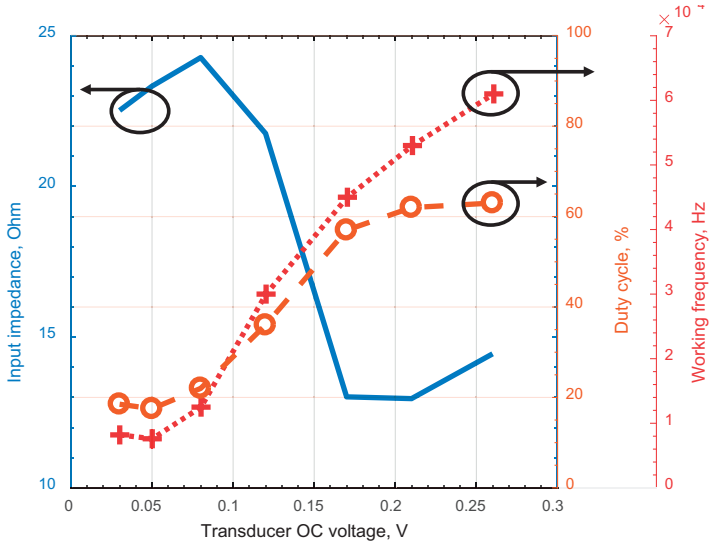


Figure 4-26: *Chip II*'s converter input impedance, d_I, and f_{SW} with the variations of the harvester output open-circuit voltage.

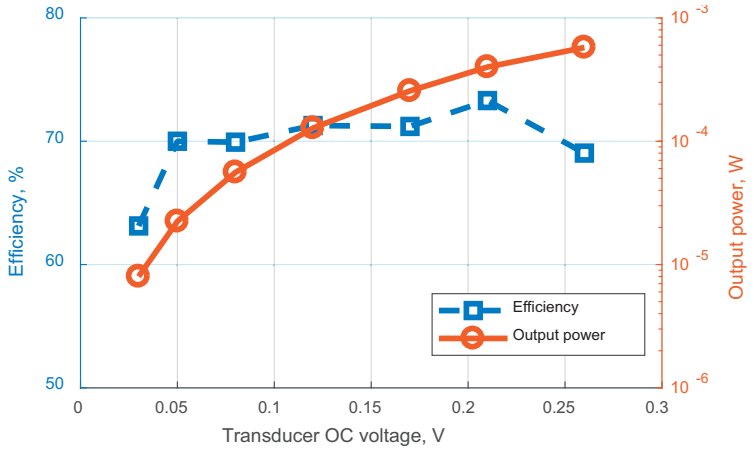


Figure 4-27: η and output power variations of the converter in *Chip II* with the harvester output open-circuit voltage.

whereas for the 180 Ω emulated transducer, 69% of the available power is transferred to the output. Here, the input impedance of the system from equation (4-3) is limited by the lowest value of the duty cycle that can be generated by the DCO. The DCO in *Chip II* has a more conservative design and its duty cycle can decrease to the minimum of about 10%. According to the measurement results, the duty cycle of the DCO in *Chip I* could be as low as 4%. Therefore, for high-impedance transducers, the system cannot be entirely matched. However, the efficiency is sufficient for the mentioned application.

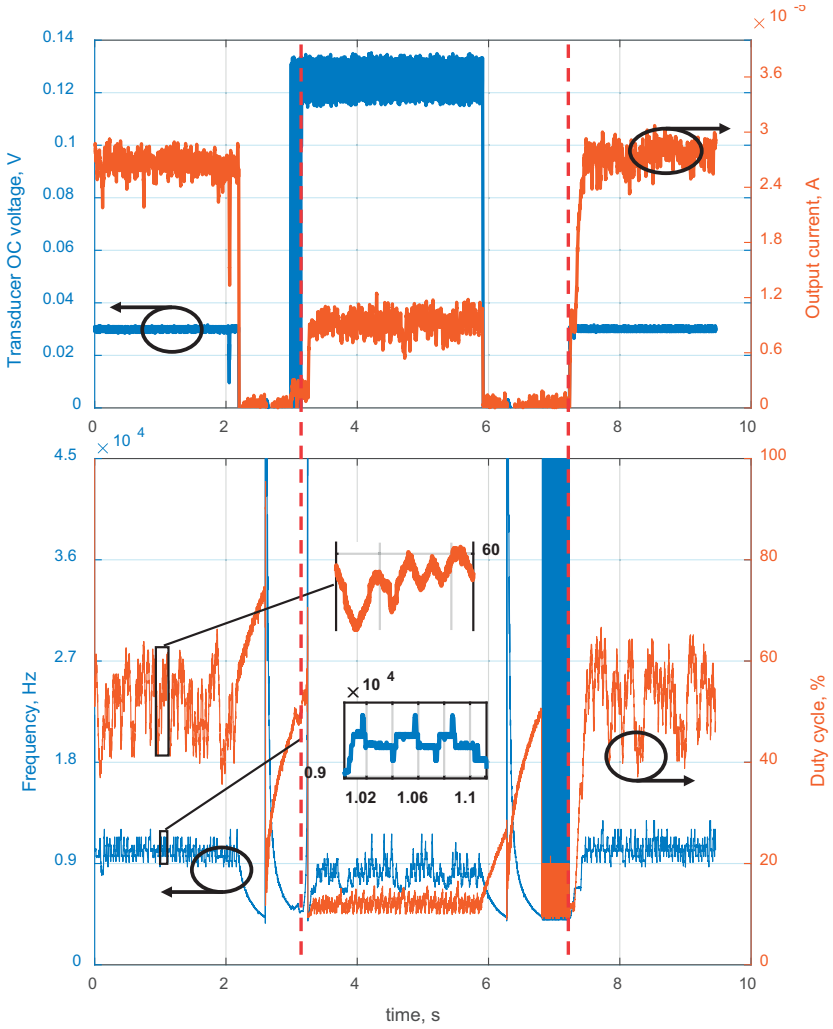


Figure 4-28: f_{SW}, d_1, and output current variations of the converter in *Chip II* with the harvester impedance variation.

Counter_III, which was dedicated to d_1, is modified to not toggle when it reaches its minimum value. This is helpful to keep at least the input impedance of the system at its maximum, when a high-impedance transducer is used as the harvester in the system. However, if a higher impedance is expected from the system, a pulse-skipping block should be added to the control section. When *Counter_III* reaches its minimum, and the control section still needs a smaller value of d_1, this pulse-skipping block can be activated. At this instant, it should skip one t_1 pulse, and consequently the other pulses that are generated by t_1.

The measurement results show that the entire system of *Chip II* including all three loops in the control section and the DCO consumes 280 nW at 10 kHz work-

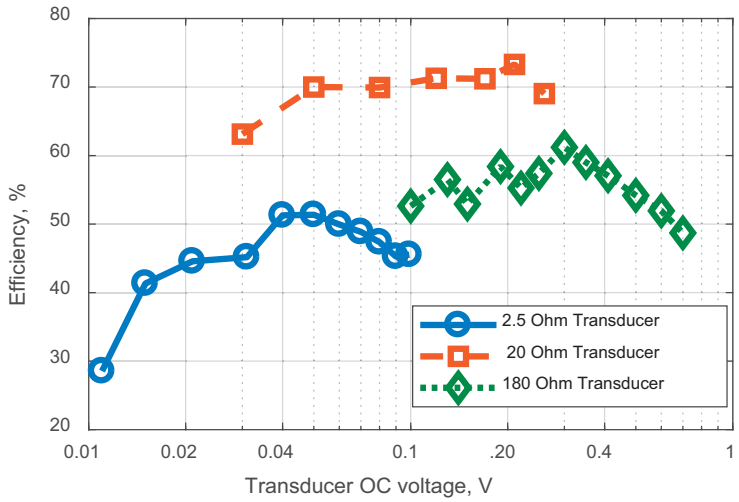


Figure 4-29: η of the converter in *Chip II* for the high-, midrange-, and low- impedance TEG transducers.

ing frequency. The dynamic loss by power switches is 1040 nW at 10 kHz. Figure 4-29 illustrates η of the converter in *Chip II* for the three main types of the TEGs introduced in Chapter 2 section 2.3. The system's η including its system power consumption is 41% for the emulated low-impedance TEG transducer with just a 15 mV of open-circuit voltage and a 2.5 Ω impedance. The input voltage of the converter is about half of the transducer's open-circuit voltage, that is to say the converter is not only functional but also has an η of more than 40% for an input as low as 7 mV. This η reaches more than 63% for just 15 mV of input voltage with the midrange-impedance TEG. η is measured to be 53%, and 70% for 100 mV and 50 mV of open-circuit voltage from the 180 Ω and 50 Ω TEGs, respectively. The system can be functional at very low input voltages in the range of just a few millivolts to half a volt with ample efficiencies. The conversion ratio can be higher than 320 to just 1.5 while the converter maintains its efficiency. These measurement results satisfy the requirements introduced in Table 2.5. For higher impedance transducers such as a 500 Ω PV cell, η is 32% with an open-circuit voltage of 400 mV. The reduction in the transfer power for very high-impedance transducers is mainly due to the limit that was put on the DCO to generate low d_1.

The system's efficiencies for the different types of transducers are listed in Table 4-1 summarizes the chip performance and other state-of-the-art results related to inductor-based converters. For the low-impedance (1 Ω to 5 Ω) transducer, η is not reported for an open-circuit voltage as low as 15 mV in the recently related literature [67, 72]. The lowest voltage in which η is reported, is found to be 30 mV [63] its η is stated in Table 4-1.

Table 4-1: *Chip II* η with different types of transducer.

	15 mV 2.5 Ω TEG	100 mV 180 Ω TEG	50 mV 20 Ω TEG	450 mV 300 lux PV	450 mV 1500 lux PV
Chip II η	41%	53%	70%	31%	56%

Table 4-2: Summarized results of this work and the prior-arts.

	[63]	[94]	[66]	[110]	[70]	*Chip I*	*Chip II*
Technology, µm	0.13	0.13	0.18	0.32	0.35	0.18	0.18
V_{OUT}, V	1	1.1	2	1.5	1.8	1.1	1.6
transducer OCV range [a], dB	22	30	15.5	31.6	15[b]	32	36.5
η @ 15 mV low-Z[c] TEG	13%[d]	- [e]	-	-	-	52%	41%
η @ 50 mV midrange-Z TEG	-	55%	-	-	<40%	61%	70%
η @ 130 mV high-Z TEG	-	-	85%	-	-	54%	57%
η @ 0.5 V PV	-	- [e]	-	65%	75%	60%	54%
Quiescent power, µW	2	0.3	0.16[f]	0.17	5	1.2	0.28
Self-tuning	No	Yes	No	Yes	Yes	Yes	Yes
Area, mm^2	0.12	0.15	0.3	0.59	25[g]	0.2	0.21

a. The open-circuit voltage (OCV) range is calculated by $20\log10(V_{OCmax}/V_{OCmin})$, where V_{OCmax} and V_{OCmin} are the maximum and minimum OCV reported for each converter.
b. This work is a multi-input converter. The stated number is related to the input with the maximum range. The combined OCV range of all inputs is 39 dB.
c. Low impedance
d. η is measured for 30 mV of OCV.
e. It was tested, but not reported.
f. The power consumption of the control section is reported.
g. The entire chip area.

As shown in Table 4-2, the work gives ample η for both low- and high-impedance transducers in an extensive range of available power and input voltage while the other prior-art might report a high η for a specific type of harvester in a restricted range. *Chip I* has a better η than *Chip II* in some points; however, *Chip II* can transfer power to the higher potential at its output and, as discussed in this section, it is more robust, and always locks to the expected working point.

4.5 Conclusion

A design methodology was introduced based on a time-domain analysis to implement a converter with multi-stable control loops. The method allows the system to follow changes in the harvesters' specifications, and to keep the converter at an optimal working point. The control section estimated the power transfer and losses in the converter through small digital blocks with sufficient precision and ultra-low-power consumption. The entire digital control section consumed 30 nW with the mm-scale transducers. One relaxation oscillator was implemented and served as the frequency and pulse generator for the system. A chopper at the input of the oscillator was employed to broaden its frequency and duty cycle tuning range. The entire converter system was implemented by custom asynchronous mixed-signal blocks that were clocked by the oscillator output. Since the oscillator frequency was increased with the available power from the transducers, the power consumption and performance of the system were increased with the available power. The converter can harvest energy from low- and high-impedance transducers in a wide range of available power and voltages. It has more than 40% efficiency with an open-circuit voltage of only 14 mV from a 2.5 Ω TEG. The efficiency reaches 53% and 70% with the high-impedance and midrange-impedance TEG with an input voltage of just 50 mV. The converter conversion ratio can be higher than 320 to just 1.5 while the converter maintains its efficiency. The wide range of operation and the efficiency at low voltages are the important improvements with respect to the prior art.

5 Conclusion and future directions

5.1 Conclusion and summary

In this dissertation, a new design methodology has been introduced to enable an energy harvester power converter to efficiently transfer power from different types of transducers and, moreover, at low voltages. Ultra-low-power architectures and circuit topologies have been suggested to implement the proposed design methodology. This work was primarily motivated by the fact that autonomous wearable devices can employ different harvesters based on the sensor placement, or can operate under the different ambient conditions, and their power converter should transfer power in all circumstances without replacement or manual tuning, via an energy efficiency that meets the stringent system requirements.

The power consumption of the wearable device and the available power from the harvester set the efficiency required by the converter. Commonly harvesters produce a low amount of energy at low voltages. Thus, the consumption of the device through the signal conditioning circuit becomes an important factor to set the requirements. The prior-art signal conditioning circuits, which consist of an amplifier and an ADC, have accomplished a superior performance. Nevertheless, their amplifier power consumption exceeds the possible available power for a feasible autonomous device. In this study, the requirements of the signal conditioning circuit for this application were examined, and a suitable amplifier was designed. It is an entirely symmetric, two-stage amplifier and consumes 9 µW. The ADC was implemented with the ultra-low-power SAR architecture. It employed a higher clock frequency to shorten the duration of its operation and thereby shorten its sampling hold time. The method results in relaxed requirements for the sampling switches and, therefore, lower power consumption. As discussed, the consumption of the designed conditioning circuits does not exceed the available power. However, it still leaves a severe constraint on the efficiency required by the power converter.

The converter's losses and power transfer were examined to design an efficient power converter. The efficiency bound of the converter was introduced as a function of the transducers' electrical specifications. In order to satisfy the efficiency requirements of the autonomous device, the converter's power switches were optimized for the transducer that could result in the lowest efficiency. The tuning ranges of the switching durations were extracted through the introduced power and loss examination, to maintain converter efficiency despite changes in the ambient conditions or transducer specifications. The off-chip inductor was sized as large as the form factor allowed, whereas the capacitor was selected with the introduced design trade-off between speed and efficiency. The implemented converter could boost input voltages as low as 10 mV and 50 mV, which were expected from two different types of mm-scale transducers, with 54% and 71% efficiency, respectively. The converter efficiency had an important improvement at low voltages compared to the prior-art.

A design methodology was suggested to implement the control section of the converter to tune the timings of the power switches automatically with variations to keep the converter efficiency. The PMOS switch "on" duration keeps track of the converter output-to-input variations. The NMOS timing matches the converter impedance to the transducer. The adjusting switching frequency preserves the converter in the low-loss and high-transfer-power operational point. Having these three loops working together raised a serious concern regarding stability. The proposed design methodology analyzed the system with the state-space averaging (SSA) model and suggested the design of the control loops. Ultra-low-power architectures were introduced to implement the design loops. The obtained implantation of the PMOS and NMOS duration control loops had a less complicated architecture and could resemble or partially resemble the state-of-the-art implementations. However, the prior art acquired an intuitive procedure to attain the design. The proposed more elaborate frequency control implementation could not have been achieved without analysis and the introduced design methodology.

The control section estimated the power transfer and loss with a sufficient precision through the suggested nanowatt digital blocks without any current sensor or power-hungry analog section. A DCO circuit was suggested to generate both frequencies and NMOS durations at the same time. The DCO inputs were chopped to generate a wide tuning range frequency and duty cycle. The power switch frequency served as the system clock as well. The entire architecture was designed asynchronous. Therefore, the performance and power consumption of the system depended on the available power from the input. The measurements illustrate that the entire

power consumption of the converter is less than 300 nW for the low-voltage transducers. The conversion ratio can be automatically adjusted at least in a range of 320 to just 1.5 while the converter maintains its efficiency. The converter not only operates with input voltage as low as 7 mV but also it has more than 40% η. The efficiency reaches 70% for just 50 mV of input voltage with the midrange-impedance TEG. Efficiency is measured to be 53% for a high-impedance TEG with an open-circuit voltage of just 100 mV. Preserving efficiency in an extensive range of the transducers' specifications and achieving such high efficiencies at low voltages are essential improvements respecting to the prior-art. The study enables the converter to be employed in the mm-scale autonomous wearable device and paves the way to reach an efficient low-power universal energy harvester power converter.

5.2 Future directions

There is still an opportunity to improve the efficiency of the proposed architecture for a broader range of the transducers. The suggested DCO was designed with conservative requirements. The range of its duty cycle was limited to 9%. Higher impedance transducers may require much less duty cycle from the DCO. The lower duty cycle can be provided by adding a small digital block at the output of the DCO as a pulse-skipping block. If the control section needs a smaller duty cycle and the DCO has already reached its minimum, the pulse-skipping block can eliminate one pulse and send an instruction to *Counter_III* to increase the DCO frequency at the same time. Therefore, the generated signal will be similar to the DCO output with the same frequency but at the lower duty cycle.

In the converter architecture, as stated in Chapter 4, the speed of the loops was designed to be sufficiently fast to enable us to simulate and verify the architecture functionality. Now, it is possible to lower the speed of the loops much more, and therefore have a more prominent input capacitance in the system. As discussed in Chapter 3, the larger capacitor can be beneficial in increasing the transfer power without deteriorating the entire form factor of the system.

The converter efficiency is expected to be increased even more if the efficiency improvement techniques presented in the literature are added to the converter. Tuning the switch sizes with the available power was presented in [111, 112]. A current source was employed to detect the available power in the same works. In this work, the switch sizes can be configured with the digital f_{SW} data available in the control system. With a variation in the switch sizes, the parasitic drain capacitance will be changed. Therefore, the deadtime and the delay in the path of the latch comparator clock should be modified as well.

The duration of the deadtime may need to be tuned with variations in the inductor peak current when the available power is very limited. A combination of f_{SW} and d_l in the digital domain can be used to control the deadtime delay generator circuit. However, with the deadtime set by the buffer chain and the designed delay circuit, the loss due to the deadtime was seen to be negligible in this work.

With the introduced design methodology, the control parameters can be expanded, and new loops can be examined and introduced. For example, in a batteryless system, the regulator converter stage can be eliminated and the output voltage can be set by an additional control loop. The regulator converter was responsible for transferring the extra charges to the battery to regulate the output voltage. Therefore, the new control loop can set the $Register\_B$ value as a control parameter and can control the speed of the converter to limit the charge transfer to the output when an output regulation is needed.

Energy can be harvested from high-frequency mechanical vibrations using piezoelectric generators as transducers. Piezoelectric transducers produce an alternating voltage, in contrast to the transducers employed in this study. Adding an extra rectifier after the transducer would convert the alternating voltage to a constant voltage, and therefore, our converter architecture can be employed to harvest energy in this case as well.

At the application level, the switched capacitor regulating converter was not implemented in this work. Therefore, the analog front-end has not yet been supplied by the energy harvesting circuit. The next step of this work will be designing the switched capacitor converter based on the work mentioned in Chapter 2 and realize the entire sensor node described there.

Additionally, the designed converter has the potential to be employed as a platform for other types of autonomous biosensors, such as for animal health monitoring. This is an emerging market and has gained worldwide attention. In this domain, batteries supply the sensors' electronic interfaces. Battery-powered systems are not ideal or practical for farms with large numbers of livestock. Therefore, current animal health monitoring devices are typically suggested for use in farms with high-value small-scale livestock such as cattle. The mm-scale device introduced here, with its low-cost and non-power-hungry sensors, could be employed to track the development of symptoms of an animal by monitoring the animal's vital signs such as its heart rate or body temperature over long periods of time. Then, the farmer would be able to identify a suspected sick animal or the source of a possible disease outbreak in a herd. Therefore, such device could be employed at farms with both high- and low-value livestock.

AAppendix

A.1 Calculating the input-referred noise of the dynamic comparator

The right-hand side of equation (4-17) is considered as Cumulative Distribution Function (CDF) of normal distribution with density function of $f_X(x)$ in V_S. In general, CDF of a normal distribution for a density function with mean μ, and variance σ, can be written as,

$$F(x) = \frac{1}{2}\left[1 + erf\left(\frac{x-\mu}{\sigma\sqrt{2}}\right)\right], \tag{A-1}$$

where *erf(x)* is error function. If white noise is considered as the main source of the noise in the circuit, μ is zero and the σ can be calculated by equation (A-1) and equation (4-17).

$$\sigma = \frac{V_S}{\sqrt{2}}\left[erf^{-1}\left(\frac{n_1 - n_0}{n_1 + n_0}\right)\right]^{-1}. \tag{A-2}$$

BAppendix

B.1 Error signal approximation in the frequency loop without any multiplier

In this appendix, it is considered that the converter is working in the steady-state operation, and the control loop has tuned d_1, and its direction is going to be changed from d_1 loop to the f_{SW} loop. During d_1 tuning, f_{SW} was constant, and $e(n)$ for the d_1 loop was just depended on Δt_2. Therefore, the d_1 loop has converged to the point that the converter's output power has been maximized with matching the input impedance of the converter to the output impedance of the harvester. When the f_{SW} loop is activated, the control loop perturbs f_{SW} and observe Δt_2. If it is shown that with a slight increase in frequency in the direction of increasing the output power, Δt_2 will not be negative, it can claim that the f_{SW} loop can converge to a point where losses are minimized and transferred power is maximized without any multiplier. The output power here is considered as the power transfer to the converter's input, subtracted by the losses.

Assume the f_{SW} loop changes f_{SW} by one bit, from f_{SW0} to f_{SW1} where $f_{SW1}=f_{SW0}(1+x)$, and x is positive and much smaller than 1. To estimate the new output power related to f_{SW1}, the new t_2 has to be calculated as a function of x. t_2 for low-voltage transducers, which were subject of this study, can be estimated as,

$$t_2 \approx t_1 V_{IN} / V_{OUT}\,,\; V_{IN} = V_T Z_{IN} / \left(R_T + Z_{IN}\right), \tag{B-1}$$

where, V_T and R_T were open-circuit voltage and impedance of the transducer, and Z_{IN} was estimated by equation (4-2). Therefore, t_2 as a function of f_{SW} can be rewritten as below.

$$t_2 = \frac{V_T}{V_{OUT}} \cdot \frac{1}{f_{SW} + R_T . d_1^2 / 2L_S} . \tag{B-2}$$

With Tylor expansion of equation (B-2), the new t_2; $t_{2,\, f_{SW1}}$, can be approximated as a function of x, f_{SW1}, and the earlier t_2; $t_{2,\, f_{SW0}}$.

$$\begin{aligned} t_{2,\, f_{SW1}}\Big|_{f_{SW1}=f_{SW0}.(1+x),\, x \ll 1} &\approx \underbrace{t_{2,\, f_{SW0}}}_{t_{2,0}} + t_{2,\, f_{SW0}}{}^{/} f_{SW0} x, \\ t_{2,\, f_{SW1}} &\approx t_{2,0}\left(1 - x/2\right). \end{aligned} \tag{B-3}$$

The transferred power to the input of the converter, P_T can be written as power charges L_S during t_1, and the power transferred to the input during t_2.

$$P_T = f_{SW}\left(\frac{L_S I_P{}^2}{2} + \frac{V_{IN} I_P t_2}{2}\right),\ I_P = \frac{V_{IN} t_1}{L_S} . \tag{B-4}$$

Then the transferred power as function of f_{SW1}; $P_{T,\, f_{SW1}}$ can be written by equation (B-2) and Tylor expansion of equation (B-4) as,

$$\begin{aligned} P_{T,\, f_{SW1}} &\approx \underbrace{P_{T,\, f_{SW0}}}_{P_{T,0}} + P_{T,\, f_{SW0}}{}^{/} f_{SW0} x + P_{T,\, f_{SW0}}{}^{//} \left(f_{SW0} . x\right)^2 , \\ \mathrm{P}_{T,\, f_{SW1}} &\approx \mathrm{P}_{T,0}\left(1 - \left(x/2\right)^2\right). \end{aligned} \tag{B-5}$$

This reduction in the transferred power is resulted from impedance mismatch, because of the slight change in f_{SW}. For calculating the total output power, the transfer power has to be subtracted by the converter static and dynamic losses.

$$P_{OUT} = P_T - P_L, P_L = \underbrace{I_{Ls,RMS,t1}{}^2 \left(\mathrm{R}_N\right)}_{P_{LS}:Static\ Loss} + \underbrace{f_s V_{OUT}{}^2 C_{Par}}_{P_{LD}:Dynamic\ Loss} , \tag{B-6}$$

where $I_{Ls,RMS,t1}$ is L_S root mean square current during t_1, and R_N is the S_1 on-resistance. Again with Tylor expansion of equation (B-6), losses at f_{SW1}; $P_{L,\, f_{SW1}}$ can be estimated by

$$\mathrm{P}_L\left(f_{SW1}\right) = P_{LS,0}(1 - x) + P_{DS,0}(1 + x). \tag{B-7}$$

As mentioned above, the control loop was tuned d_1 before activating the f_{SW} loop, and the transfer power was maximized locally by the d_1 loop with a matched impedance. However, since the f_{SW} loop was responsible for tuning the working frequency to minimize the losses and maximize the transfer power, the converter

has not been reached to the point that losses are minimized. Therefore, at that point one of the static or dynamic losses had to be dominated.

Assume the static loss was dominated there, and the dynamic loss could have been neglected. Although the one-bit increase in f_{SW} slightly deviated the converter from its locally maximized transfer power based on equation (B-5), the losses have been reduced as shown in equation (B-7). Then, the new output power for f_{SW1} can be written with equation (B-5), equation (B-6), and equation (B-7).

$$\begin{aligned} P_{OUT} &= P_T - P_L = P_T.(1-\alpha),\ \alpha = P_L / P_T, \\ P_{OUT,f_{SW1}} &= P_{T,0}\left(1 - x^2/4\right).\left(1 - \alpha\frac{1-x}{1-x^2/4}\right) \\ &\approx P_{T,0}\ \underbrace{\left(1-x^2/4\right)}_{\text{Impedance Mismatch}}.\underbrace{\left(1-\alpha+\alpha.x\right)}_{\text{Loss Improvement}}. \end{aligned} \tag{B-8}$$

Equation (B-8) illustrates an increase in f_{SW} results in a reduction in t_2 due to impedance mismatch, and in the same time, an increase in t_2 due to loss improvement. On the other hand, equation (B-3) showed exactly after an increase in f_{SW}, the t_2 duration was decreased due to shortening the working period. In other words, since the moment that f_{SW} was changed by the slow f_{SW} loop, t_2 durations have been continuously updating due to shortening the working period, the impedance mismatch, and the loss improvement. The shortening period reduced t_2 by $(1-x/2)$. Therefore, if the resultant of the changes due to the loss improvement and impedance mismatch increases t_2 by $1/(1-x/2)$, it will be possible to use Δt_2 as $e(n)$ for the f_{SW} loop.

Between the two updates of f_{SW}, all parameters except t_2 are constant. Therefore, the ratio of the output power at the end of period, $P_{OUT,f}$ to the ratio of the output power at the beginning of the period $P_{OUT,i}$ can be written from equation (4-11) as,

$$\frac{P_{OUT,f}}{P_{OUT,i}} = \frac{t_{2,f}}{t_{2,i}}, \tag{B-9}$$

where, $t_{2,f}$ and $t_{2,i}$ are the value of t_2 at the end, and at the beginning of the updating period. As mentioned above, in order to enable estimating $e(n)$ by Δt_2 and implementing the loop without any multiplier, the left-side in equation (B-9) should be bigger than $1/(1-x/2)$. By replacing equation (B-8) in equation (B-9) and considering that equation (B-9) should be bigger than $1/(1-x/2)$, a new ratio as a function of α (power loss to power transfer) can be written as,

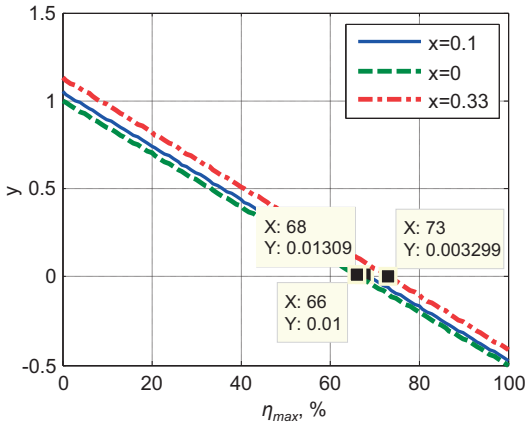


Figure B-1: y from equation (B-11) versus maximum efficiency

$$\frac{P_{T,0}\left(1-x^2/4\right).\left(1-\alpha+\alpha.x\right)}{P_{T,0}\left(1-\alpha\right)} \geq \frac{1}{1-x/2}. \tag{B-10}$$

By reordering equation (B-10), a new equation can be rewritten as,

$$y = (\frac{\alpha}{8})x^3 + (\frac{1}{8} - \frac{3\alpha}{8})x^2 + (\frac{\alpha}{4} - \frac{1}{4})x + \frac{3\alpha}{2} - \frac{1}{2} \geq 0. \tag{B-11}$$

Keeping in mind that maximum efficiency η_{max} could be defined as below,

$$\eta_{\max} = 100 \times \frac{P_T - P_L}{P_T} = 100 \times \left(1-\alpha\right), \tag{B-12}$$

then, y from equation (B-11) can be solved as a function of η_{max} with replacing α from equation (B-12) in equation (B-11).

y is depicted in Figure B-1 as a function of η_{max} for different values of x. As illustrated in Figure B-1, for a η_{max} smaller than 66%, y can be higher than zero, and consequently equation (B-9) can be bigger than *1/(1—x)*. It can be concluded that when the losses are more significant than about one-third of the transferred power, the multipliers in the control section can be eliminated. With this method, the f_{SW} loop cannot reach to the point that the system efficiency is higher than this value; however, this efficiency can be enough for a low-voltage low-power converter.

In the other working conditions which have not been considered here, the same procedure can be applied and followed to show that the system converges to an optimum point where the system efficiency is less than the values shown in Figure B-1.

List of Acronyms

ADC	analog to digital converter
CCM	continuous conduction mode
CDF	cumulative distribution function
CMF	common-mode feedback
CMOS	complementary metal–oxide–semiconductor
CMRR	common-mode rejection ratio
DCM	discontinuous conduction mode
DCO	digitally controlled oscillator
DNL	differential nonlinearities
DTC	digital-to-time converter
DUT	device under test
ECG	electrocardiography
EEG	electroencephalography
ENOB	effective number of bits
FAT	file allocation table
FRAM	ferroelectric random-access memory

HVR high-value resistor

IC integrated circuit

INL integral nonlinearities

IoT internet of things

LSB least significant bit

MIM metal-insulator-metal

mm-scale millimeter-scale

MSB most significant bit

NMOS N-type metal-oxide-semiconductor

OC open circuit

OCV open-circuit voltage

OTA operational transconductance amplifier

PCB printed circuit board

PM phase margin

PMOS P-type metal-oxide-semiconductor

PSSR power supply rejection ratio

PV photovoltaic

RF radio frequency

RMS root mean square

SAR successive approximation

SC switched capacitor

SD secure digital

SNR signal-to-noise ratio

SSA state-space averaging

TEB transducer efficiency bound

TEG thermoelectric generator

THD total harmonic distortion

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EDUCATION

7.2013-11.2017 **PhD**, **École polytechnique fédérale de Lausanne** (EPFL)
Microsystem and Microelectronics, ESPLAB, Neuchâtel, Switzerland

9.2008-1.2011 **MS, Tarbiat Modares university** (TMU),
Electrical Engineering, Tehran, Iran, **Ranked 1st**

9.2004-6.2008 **BS**, **Shahid Beheshti university** (SBU)
Electrical Engineering, Tehran, Iran, **Ranked 1st**

PROFESSIONAL EXPERIENCE

7.2013-11.2017 **Research Assistant: EPFL, ESPLAB:**
Design of low power, configurable, power converter for Zero power active electrode:

- A converter was implemented using 0.18 µm CMOS technology.
- It operates from just a few of millivolts to half a volt with ample efficiencies.
- It works at an optimal point with different transducers and environmental.
- Low power Analog Front-end has been designed as a load.

12.2015-2.2017 **Maximizing autonomy of an IoT device, with Kizy Tracking SA**.

2011-2013 **Analog RF designer: Sharif University of Technology:**
Design, analysis and fabrication of a multimode low noise VCO:

- A low noise wideband VCO chip was proposed, designed and implemented for Software Defined Radio with OFDM modulation.

2011-2012 **Design of DVB-T transceiver down to layout (including Reed-Solomon and Viterbi).**

2008-2013 **Research Assistant: Tarbiat Modares University:**
Design, analysis and fabrication of a wideband low noise mm-Wave CMOS VCO:

- An mm-wave VCO was proposed base on analysis of its large signal model.
- An IC was fabricated with EM simulations and parasitics extractions.

CERTIFICATIONS

1.2016-6.2016 **Business Concept (Swiss Commission for Technology and Innovation (CTI) Entrepreneurship).**

ACADEMIC EXPERIENCES

- Project director of three master students and one bachelor students in circuit design.
- TA: Electrotechnique (EPFL), RFIC (Sharif Uni.), Electromagnetic, Microcontrollers (SBU)

MAIN PUBLICATIONS

Peer-Reviewed Journals:

- Milad, et al. "Design of an integrated thermoelectric generator power converter for ultra-low power and low voltage body energy harvesters aimed at ExG active electrodes." *Journal of Micromechanics and Microengineering* 25.10 (2015)
- Ataei, Milad, et al. "Transformer feedback millimeter-wave VCO with capacitance cancellation technique in 0.18-μm CMOS." *IEICE Electronics Express* 8.11 (2011): 780-787.

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- Ataei, Milad, Alexis Boegli, and Pierre-André Farine. "Phase and frequency self-configurable efficient low voltage harvester for zero power wearable devices." *European Solid-State Circuits Conference, ESSCIRC Conference 2016: 42nd*. Ieee, 2016
- Ataei, Milad, et al. "Design of an integrated thermoelectric generator power converter for ultra-low power and low voltage body energy harvesters aimed at EEG/ECG active electrodes." *Journal of Physics: Conference Series*. Vol. 557. No. 1. IOP Publishing, 2014

PROFESSIONAL TRAINING

- Creative Problem Solving
- Bioelectronics
- Optical Communications
- Software Defined Radio
- RF IC Design
- Analog IC and Convertors
- Low-Power Analog IC Design
- Wireless Communications
- Microwave II
- Integrated filter design
- VLSI
- Power Management
- MMIC Design
- Digital VLSI Architecture
- Semiconductor Fabrication
- Discrete Signal Processing

TECHNICAL SKILLS

- Competent in Cadence (Virtuoso, Spectre, VerilogA), Agilent tools, Hspice, HFSS.
- MATLAB, Simulink and Toolboxes, ModelSim, ISE, Encounter, Altium, Verilog HDL, C

PROFESSIONAL AFFILITIONS

- **IEEE, student member since 2009**
  - Assigned **as** reviewer for journals and conferences*: IEEE Tran. on CAS I, VLSI Journal, BioCAS*, *ICEE.*
  - **Vice president and member of the scientific society of ECE Department in SBU (2006-2007):** We held "Computer Society of Iran-Computer Science CSICC" international conference in Tehran, Iran as the executive group (2007).

LANGUAGES

Persian (Native), English (C1), French (A2), Arabic (A2)

PERSONAL INTERESTS

Mountaineering, Skiing, Horseback Riding, Swimming, and Cycling.