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An open software-radio architecture supporting advanced 3G+ systems

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Abstract

This paper describes a software-radio architecture developed for providing real-time wide-band radio communication capabilities in a form attractive for advanced 3G systems research. It is currently being used to implement signaling methods and protocols similar, but not limited to, evolving 3G radio standards (e.g. UMTS, CDMA2000). An overview of the hardware system is provided along with example software implementations on both high-perfomance DSP systems and conventional microprocessors.

Key words : Mobile radiocommunication, Digital signal processing, Radio interface, Test facility, Software radio, System architecture, Transmitter, Receiver, UMTS.

UNE PLATEFORME RADIO LOGICIELLE OUVERTE POUR LES SYSTÈMES 3G+

Résumé

Cet article décrit une plate-forme radio logicielle reconfigurable, permettant de réaliser d'une manière souple des traitements en temps réel sur une interface radio de type 3G. Cette plate-forme est actuellement utilisée pour implémenter des méthodes de transmission-réception ainsi que des protocoles, inspirés des normes 3G (UMTS, CDMA2000). Une vue d'ensemble de l'architecture matérielle est donnée dans cet article ainsi que des exemples d'implantations logicielles, aussi bien sur processeurs de traitement du signal (DSP) que sur des processeurs classiques.

Mots clés : Radiocommunication service mobile, Traitement numérique signal, Interface radio, Radio logicielle, Installation essai, Architecture système, Émetteur, Récepteur, UMTS.

Contents

I. INTRODUCTION AND MOTIVATION

The presence of several different wireless communication standards and the wide variety of services provided by mobile communication operators has created the problem of providing universal seamless connection to customers with different service requirements at any point on the globe. Software Radio is an enabling technology for systems aiming at handling several different standards and different services and thus represents a solution to this problem. Generally, Software Radio is a very broad term encompassing several levels in the protocol stack (see e.g. [1, 2, 3] and references therein). Motivated by the worldwide activity around third generation (3G) mobile communication systems, Eurécom and EPFL have launched a joint project whose objective is to design and implement a real-time software radio communication platform to validate advanced mobile communication signal processing algorithms. The right to transmit has been granted for one 5 MHz UMTS channel in both France and Switzerland for experimental purposes.

The platform is characterized by the following major features:

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- Flexibility, achievable by a software driven system.
- Duplex communication.
- Multiple antennas transmit and receive signal processing (i.e. joint spatio-temporal signal processing).

Flexibility remains a key word for a software-defined system. In our case it serves several purposes. For instance one may perform propagation channel measurements and transmitter characterization, evaluate the performance of different signal processing algorithms for both single user and multi-user systems under different operating conditions. *Duplex communication is* also necessary to allow higher-layer protocol testing and services, and to analyze more complex system aspects, such as multiple-access, power control, and optimize down-link signal processing from up-link measurements. In a second phase, the platform will allow *Multiple-antenna signal processing,* or more generally, spatio-temporal signal processing (also known as array processing) since this a very promising ensemble of techniques able to significantly increase the capacity of wireless communication systems.

The main focus of this paper is on the description of the basic platform architecture and signal processing to implement the essential physical layer level procedures of the UMTS standard operating in Time Division Duplex (UMTS/TDD) mode.

At the physical layer level, Software Radio generally requires the development of signal processing algorithms suited to implementation on a general purpose programmable processor (as opposed to analog or digital dedicated hardware). For this reason the position of Analog to Digital (A/D) and Digital to Analog (D/A) conversion must be moved as close as possible to the antennas. The goal is to perform operations like *channel selection* [4, 5], synchronization and detection in the all-digital domain, by using high performance Digital Signal Processors (DSPs). Special care must be dedicated to the transmission and reception front-end architecture. In fact, this should be independent on system-dependent parameters like the signal bandwidth and the symbol (or chip, in a CDMA system) rate. When designing software radio algorithms it is assumed that a multi-band Radio Frequency (RF) section takes care of translating the desired signal from a fixed Intermediate Frequency (IF) carrier to the required RF carrier in the transmitter, and vice-versa in the receiver. Then we are concerned with the efficient generation of an IF analog signal from a baseband digital signal (transmitter front-end) and with the reverse operation (receiver front-end). Once the end-to-end transmitter receiver architecture is defined the next step consists in synchronizing the receiver, estimating the channels associated with the users, and eventually detecting the transmitted symbols. All these operations are performed in real-time on our platform.

The adopted modulation scheme (BPSK and QPSK), the spread signal bandwidth (5 MHz), the spreading gain (DS-CDMA with allowed spreading gain of 1, 2, 4, 8, 16) and the frequency band (around 2.1 GHz) are the same as those defined in the UMTS/TDD specifications. The TDD mode has been chosen because under certain circumstances it allows the exploitation of the channel reciprocity between up-link and down-link in duplex communication, and also reduces the DSP computational load for a given bandwidth.

The solutions proposed in this paper can also be applied to a wide class of linearly-modulated digital signals (including most of today's and future mobile communications standards, like GSM, IS-54, IS-136, IS-95, and DECT (see e.g. [6] and references therein), UMTS (both FDD and TDD modes) [7], CDMA2000 (see e.g. [8, 9]) and EDGE (see e.g. [10] and references therein).

II. SYSTEM ARCHITECTURE

In a first phase, the development of the platform has been based on a single antenna architecture for the Mobile Terminal (MT) as well as for the Base Station (BTS). The retained architecture permits to easily enhance the capabilities of the platform without redesigning the essential hardware and software parts.

The BTS and the MT are based on the same hardware platform and differ only in the software implementation. The different hardware parts of the platform are highly partitioned in order to enable the use of as many standard cards and components as possible.

The hardware portion of the test-bed consists of 4 elements which are under software control, namely

1. a PCI bus based reconfigurable data acquisition card (DAQ) based on a Field Programmable Gate Array (FPGA)
2. an RF front-end
   - a single stage up/down-conversion from/to a 70 MHz intermediate frequency (IF) carrier with time-division-duplex (TDD) multiplexing
   - 1 high-speed 12-bit bandpass sampling A/D converter (f_{ADC} = 14.7456 MHz)
   - 1 high-speed 12-bit up-sampling D/A converter ($f_{DAC} = 8 \times f_{ADC}$ = 117.9648 MHz)
   - 8 slow D/A converters for controlling various amplifier gains on the RF card
   - control for various switches on RF card
3. a clock card for generating sampling clocks (fixed frequency) and local oscillators (programmable frequency)

We show a simplified block diagram of the entire system for a single antenna in Figure 1.

We have considered two software implementations, the first using a combination of commercially available embedded DSP cards and a common PC and the second using the DSP units (e.g. MMX) of a standard PC under an operating system proving hard real-time support (e.g. RTLinux). Both run in real-time and are compatible over the air.

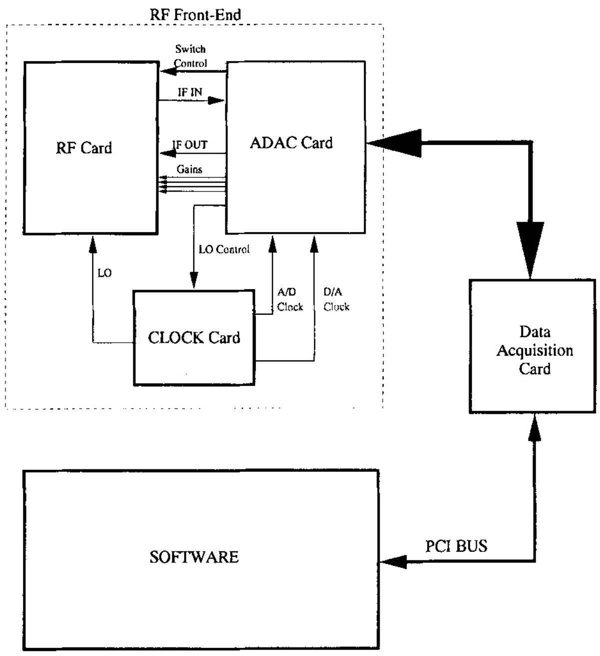


FIG. 1. — System Architecture.

Architecture système.

II.1. RF Front-end

A simplified block diagram of our RF front-end is shown in Figure 2. It was designed in conjunction with STMicroelectronics in Geneva, Switzerland. On reception (Rx), the RF signal is filtered, amplified and down-converted to a 70 MHz intermediate frequency (IF). The local oscillator frequency is digitally tunable in steps of 500 Hz. The IF signal is amplified by a digitally tunable gain control and directly sampled at 14.7456 MSamp/s The samples are transferred via a ribbon cable using high-speed line drivers to the *data acquisition unit* (DAQ). The mode of the transceiver (i.e. transmission, reception, calibration) is fully controllable from the software portion of the platform.

On the transmission end (Tx), samples from the DAQ arrive at a rate of 14.7456 MSamp/s and drive a hardware up-sampling circuit and a high-speed D/A converter (117.9648 MSamp/s) to directly synthesize the 70 MHz IF signal. This procedure is described in more detail in II.1.2. This signal is then amplified, up-converted to RF, filtered and amplified by a variable-gain power amplifier.

Special low-speed lines control the gains of the Rx variable-gain amplifier and Tx Power Amplifier, LO frequency, as well as the antenna switch. Although not included in Figure 2, automatic wide-band calibration capabilities (for both Tx and Rx) are included in the design, which are required for multiantenna systems (see e.g. [11]). These will be used in a later stage of the project where the architecture will be extended to implement multiple antenna transceivers. The basic characteristics of the RF frontend are summarized in Table I.

II.1.1. Passband A/D Conversion

Once the RF signal at the antenna has been down-converted to IF, it is sampled by an A/D converter at a certain rate f_{ADC} (*figure* 9). Calling $r_{IF}(t)$ the received IF analog signal and choosing $f_{ADC} \geq 2W$ according to [4], because of the periodicity of the discrete-time signal spectrum, the resulting real sampled signal $r[n] = r_{IF}(n/f_{ADC})$ is pass-band with a spectrum replica centered at $f_{ADC}/4$ (although f_{IF} and f_{ADC} at the receiver can be different from f_{IF} and f_{ADC} at the transmitter, for simplicity we use the same notation).

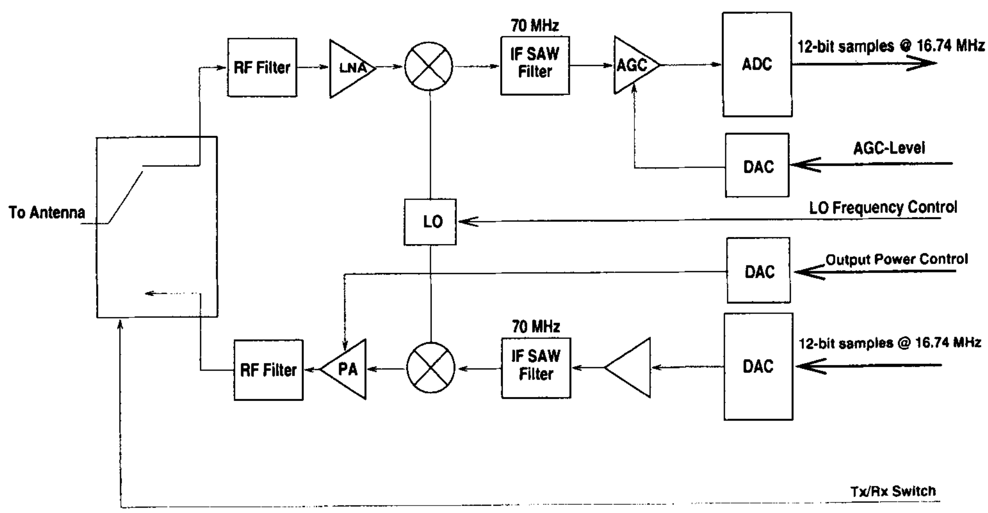


FIG. 2. — RF Front-end.

Tête RF.

TABLE I. — RF Front-end Characteristics.

Les caractéristiques de la tête radiofréquence.

Frequency Band	2100-2170 MHz
Bandwidth	5 MHz (initially)
Transmit Power (per antenna)	1 W
Receiver Sensitivity	–100 dBm
Noise Figure	< 5 dB
Input IP3	> –7 dBm
Duplex mode	Time Division
Rx Gain Control	digital tuning, 1 dB steps over 40 dB
Tx Power Control	digital tuning, 1 dB steps over 80 dB range
Local Oscillator	digital tuning, steps of a few kHz in each band
RF Calibration	digital control, Tx and Rx
Direct IF sampling (70 MHz) on Rx	12-bit A/D @ 14.7456 MSamp/s
Direct IF sampling (70 MHz) on Tx	12-bit D/A @ 117.9648 MSamp/s
Digital Interface	High speed: Low-Voltage Differential Signaling (LVDS) Low speed: 3.3V CMOS line drivers

Notice that here in order to avoid signal re-sampling we suppose the rate f_{ADC} to be a multiple integer of the chip rate (i.e. $f_{ADC} = N_c f_c$ where in our implementation we set $N_c = 4$).

Although a base-band version of the received signal can be obtained by multiplying $r[n]$ by $(-j)^n$ and then by low pass filtering, we will show further how the channel estimation and the data detection processes can be performed at pass-band.

II.1.2. Passband D/A Conversion

D/A converters have an impulse response $P_{DAC}(t)$ that can be approximated as a rectangular pulse of duration $1/f_{DAC}$ with frequency response of the form of $sinc(f/f_{DAC})$. If the discrete-time input of the D/A converter is the pass-band signal $x'[n]$, then the spectrum of the output signal is given by

$$(1) \qquad Y(f) = \sum_i X'(f - if_{DAC})\mathrm{sinc}(f/f_{DAC})$$

where $X'(f)$ is the discrete-time Fourier transform of $x'[n]$, defined by

$$X'(f) = \sum_n x'[n]e^{j2\pi nf/f_{DAC}}$$

Hence, the spectrum replica located at frequency f_{IF} is attenuated and distorted by the D/A impulse response as shown in figure 8(a). A way to reduce the attenuation consists of using a D/A converter working at rate $f_d = L_{D/A}f_{DAC}$, where $L_{D/A}$ is a suitable integer, and up-sampling $x'[n]$ by the factor $L_{D/A}$. By choosing $L_{D/A}$ such that $f_d >> f_{IF}$, the spectrum replica around f_{IF} falls inside the first lobe of the D/A frequency response since its first zero is located at f_d (see figure 8(b)). Moreover it is possible to compensate in part the distortion of the D/A converter by introducing a pass-band FIR filter between the up-sampler and the D/A converter. The filter must be designed in order to enhance the spectrum replica at IF while attenuating the other replicas.

Low complexity implementation. Denote by $x''[n]$ the up-sampled version of $x'[n]$, given by

$$(2) \qquad x''[n] = \begin{cases} x'[k] & \text{for } n = L_{D/A}k \\ 0 & \text{otherwise} \end{cases}$$

and by $h_{D/A}[n]$ the filter impulse response. The filter output is given by

$$(3) \qquad x'''[n] = \sum_m h_{D/A}[m]x''[N-M]$$

If the filter impulse response has length $L_{D/A}$, there is only a single non-zero term in the sum in the right hand side of the above equation. Then, $x'''[n] = h_{D/A}[m]x'[k]$ where $k = [n/L_{D/A}]$ and $m = n$ modulo $L_{D/A}$. Therefore, the computational cost of the filtering operation consists of one real product per output sample at rate f_d. After the D/A conversion, the continuous-time signal $y(t)$ is eventually up-converted to the RF carrier and sent to the antenna.

II.2. Data Acquisition Card

The data acquisition card is a PCI bus-mastering device permitting high-speed full duplex parallel transfer of digital data from an external device. It contains the necessary glue logic which connects the input (A/D) and output (D/A) sample streams as well as some control signals to the main CPU/DSP. A PCI architecture was adopted since it is the most general purpose bus architecture and is used on most standard PCs, as well as DSP systems. It consists of two components, namely a powerful Xilinx Field Programmable Gate Array (FPGA) XCV300 [12] and a bus-mastering PCI controller PLX9080 [13]. The format is a *PCI Mezzanine Card* (PMC) to allow for integration into both embedded DSP architectures and ordinary PCs. A simplified overview of the DAQ is shown in Figure 3.

Firmware on the FPGA for formatting and transferring data via the DMA engines of the PLX9080 to the host (DSP, CPU) memory has been developed in VHDL *(Very High Speed Integrated Circuit Hardware Description Language)*. After an initial configuration phase, transfers are continuous and completely transparent to the host, who just "sees" a circular buffer containing samples acquired from or to be transferred to the external RF front-end.

The basic components of the DAQ are the following

1. Line Drivers/Receivers for transfer from external devices via ribbon-cables

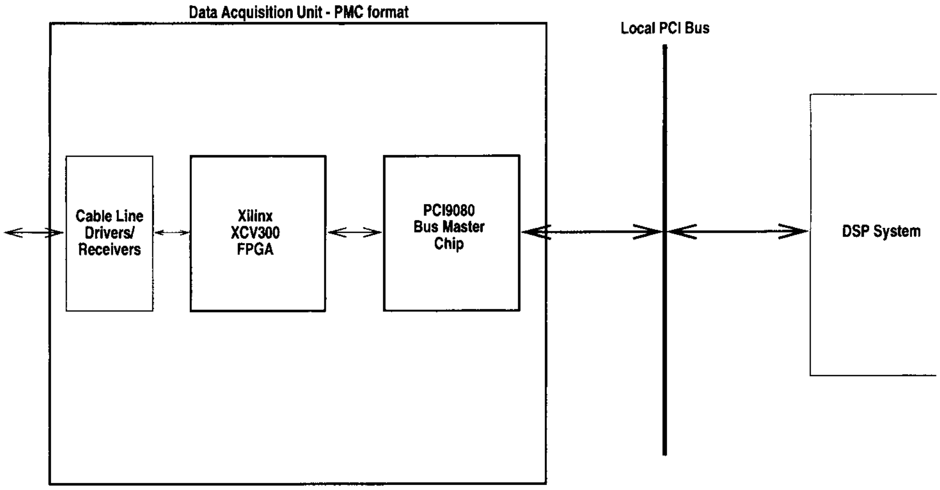


FIG. 3. — Data Acquisition Unit.

Unité d'acquisition de données.

2. A reconfigurable FPGA-based 16-bit bi-directional interface external device (up to 30 Msamp/s full-duplex)
3. A PCI bus-mastering controller for direct transfer of samples to/from memory (DMA) on PCIbased signal processing units (e.g. DSP cards, high-performance PCs, workstations (SPARC, PowerPC, Alpha), embedded processor cards, etc.)
4. A *Processor Mezzanine Card* (PMC) form-factor for maximum flexibility

The FPGA is programmed via the PCI bus by serial download.

II.3. Texas Instruments TMSC6201 Implementation

The embedded DSP architecture is based on a commercially available dual-DSP card (Spectrum Signal Processing Daytona [21]. The basic architecture is shown in Figure 4 and is centered around 2 Texas Instruments TMSC6201 fixed-point DSPs. These DSPs are capable of providing a maximum of 1600 MIPS each. Our DAQ is placed on the local PCI bus of the DSP board and transfers samples to/from both of the memory buffers on the DSPs busses. These buffers are used as temporary storage as the internal (fast) memory of the DSP is rather small. The DSP DMA engines take care of automatically transferring data to their internal memory concurrently with the signal processing functions. One DSP is used exclusively for transmission functions and the other for reception.

The DSPs are used for the front-end processing as described in the previous sections. Symbol rate data is transferred via the PCI bus to the PC which hosts the DSP card. This data is processed by the Pentium and handles tasks such as Viterbi decoding, carrier frequency offset compensation, higher layer protocol stacks, etc.

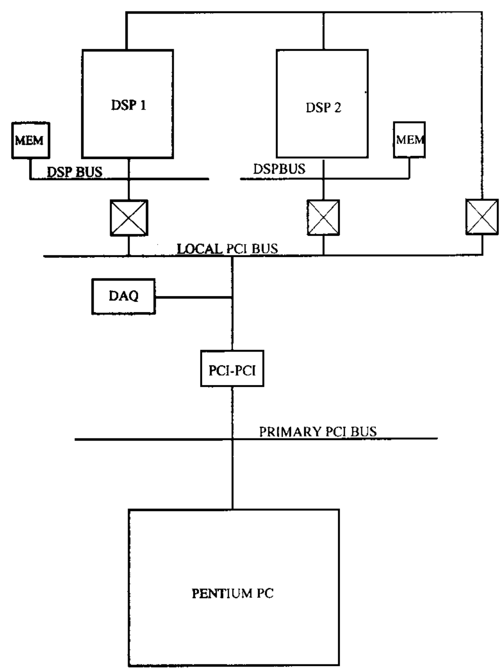


FIG. 4. — Embedded DSP Architecture.

Architecture DSP intégrée.

II.4. RTLinux-based PC Implementation

The second implementation does not rely on embedded DSPs. Here the DAQ is placed on the master PCI bus of a workstation, possibly multiprocessor, running the hard real-time extension to the Linux operating system, RTLinux[22]. The software radio runs in kernel space and is integrated into the IPv4 (Internet Protocol) subsystem of Linux as a network device.

This x86 implementation makes use of the MMX (multimedia extensions) SIMD (single instruction multiple data) instructions for obtaining maximum processor efficiency for intensive DSP computations. All DSP routines use fixed-point arithmetic and are written in C with embedded assembly macros for time-critical code sections. We typically make use of

1. MMX packed 16-bit arithmetic (multiply, add, MAC, interleaving, etc.)
2. loop unrolling
3. software pipelining

Because of the high-level software structure, this should be portable to other process or architectures (e.g. PowerPC, Alpha, etc.). For the same reason, it is easily portable to large-scale SMP (symmetric multi-processing) platforms which couid be useful for advanced base-station implementations.

III. DIGITAL SIGNAL PROCESSING

This section gives an overview of some theoretical principles on which the platform software has been implemented. We have implemented variant of the UMTS-TDD 3GPP standard [14] and are now implementing a complete subset of layers 1 and 2 of the true standard (including 1.28 MChips/s version). The main difference of the current implementation is that the hardware portion provides a clock yielding a symbol (chip) rate of 3.6864 Msymbols/s and not 3.84 Msymbotl/s.

3.1. Frame/Slot structure

The frame structure of this TDD implementation is shown in Figure 5. We see that each frame is composed of 15 slots which can be arbitrarily distributed between up-link and downlink streams. The first slot in every frame contains the synchronization sequence and is by default a downlink slot. The synchronization sequence is used by the mobile terminals to obtain slot timing synchronization.

3.2. Basic Transmitter structure

The implementation of the transmitter allows for the generation a composite signal containing up to 8 variable-rate, variable power data streams per slot. It is shown in Figure 6. The rates of the different streams is

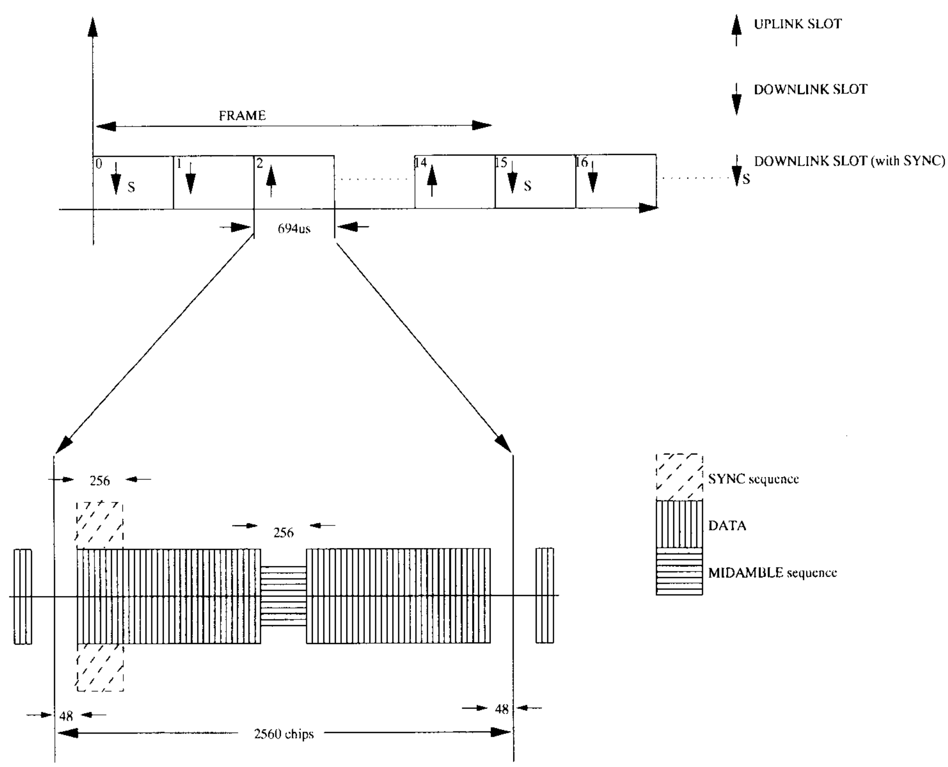


FIG. 5. — Slot structure.

Structure des créneaux temporels

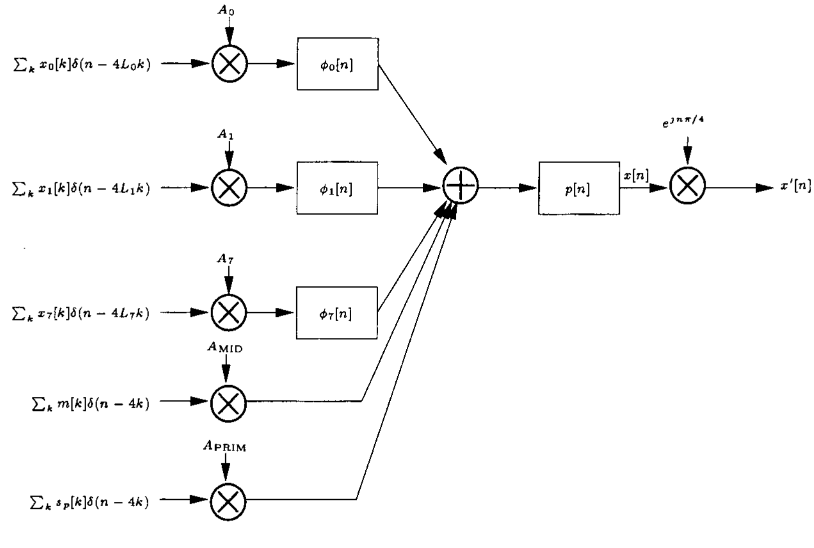
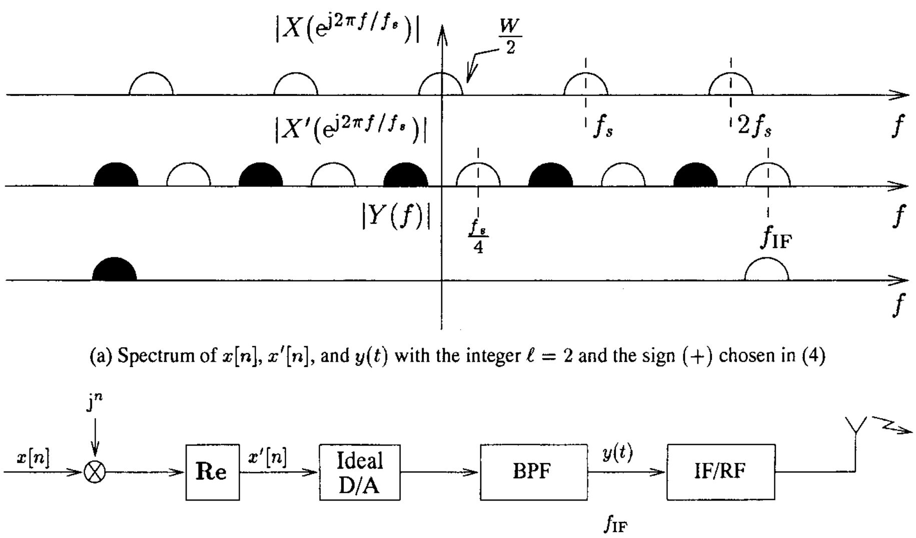


FIG. 6. — Basic TX structure.

Structure de base de l'émetteur.



(a) Spectrum of $x[n]$, $x'[n]$, and $y(t)$ with the integer $\ell = 2$ and the sign $(+)$ chosen in (4)

(b) System model

FIG. 7. — Alternative approach for IF up-conversion.

Approche alternative pour la conversion en FI.

controlled by OVSF spreading sequences $\phi_i[n]$ and the amplitudes by A_i. The choice of $\phi_i[n]$ dictates the spreading factor L_i, which ranges from 2^n, $n = 0..4$.

Two possible midambles, $m[k]$, can be inserted having lengths of either 256 or 512 chips. These are superposition of either 3 or 8 cyclic shifts of a training sequence with a periodic extension. This structure allows for efficient channel estimation techniques based on the *Fast Fourier Transform (FFT)*.

The beginning of synchronization slots (only BS) contains a primary synchronization sequence $s_p[k]$ of length 256 chips superimposed on the data.

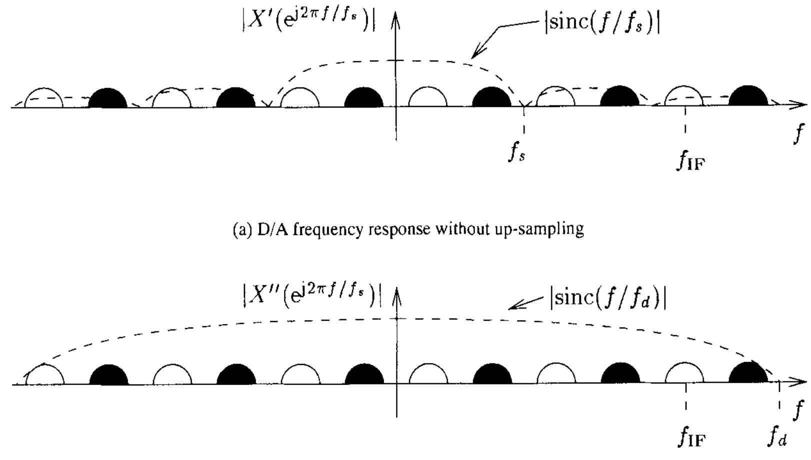
The composite signal is filtered by a 12-tap root-raised cosine FIR filter, $p[k]$, which simultaneously up-converts the signal to a carrier frequency of $\pi/2$. To this end, we choose the sampling rate f_{DAC} according to the classical expression

$$(4) \qquad f_{DAC} = \frac{f_{IF}}{\ell \pm 1/4} \text{ for a positive integer } \ell$$

Then, we generate the discrete-time real signal

$$(5) \qquad x'[n] = \mathrm{Re}\{x[n]e^{j2\pi(f_{IF}/f_{DAC})n}\} = \mathrm{Re}\{j^{\pm n}x[n]\}$$

In this way, the periodic spectrum of $x'[n]$ shows a spectrum replica centered at f_{IF} (see Fig. 7(a)). After D/A conversion, a pass-band filter centered at f_{IF} removes the other replicas, generating the desired IF modulated signal.



(b) D/A frequency response with up-sampling

FIG. 8. — D/A frequency response.

Réponse en fréquence de la CNA.

The discrete-time modulation by $f_{DAC}/4$ in (5) requires a negligible computational cost since it corresponds to change alternatively the signs of $x[n]$ as can be noticed in expanding equation (5). In order to avoid aliasing when taking the real and imaginary part, the sampling rate must satisfy also the condition $f_{DAC} \geq 2W$.

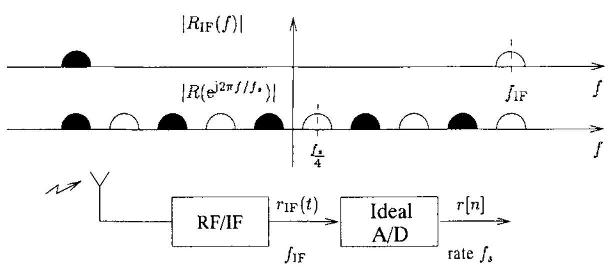


FIG. 9. — Receiver front-end.

Tête de récepteur.

III.3. Receiver

In this section we analyze some of the theoretical aspects of the receiver signal-processing. In particular we give a description of the receiver front-end architecture shown in Figure 10. Then we focus on channel estimation, matched filter synthesis and symbol detection.

III.3.1. Frame Synchronization

Frame synchronization is achieved using a filter matched to the primary synchronization sequence to estimate the location of the start of a frame. This is achieved by filtering the bandpass received signal $r[n]$ as

$$(6)\quad r_s[n] = \left\{\sum_{k=0}^{255} s_p[k]\delta(n+4k)\right\} * r[n] = \sum_{k=0}^{255} s_p[k]r(n+4k)$$

and averaging the $r_s[n]^2$ over several frames. The maximum output of this filter is used to adjust the receive signal strength (via a variable gain IF amplifier) and synchronization is achieved when the maximum is greater than a pre-defined threshold. Note that this filtering operation involves purely real quantities. This is typically the most computationally intensive part of the receiver front-end since it requires a fairly long filter operating at the sampling rate. The 3GPP standard uses a hierarchical

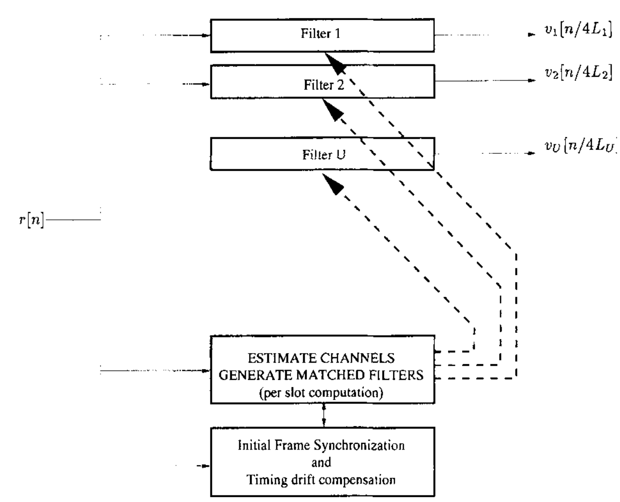


FIG. 10. — Basic RX structure.

Structure de base du récepteur.

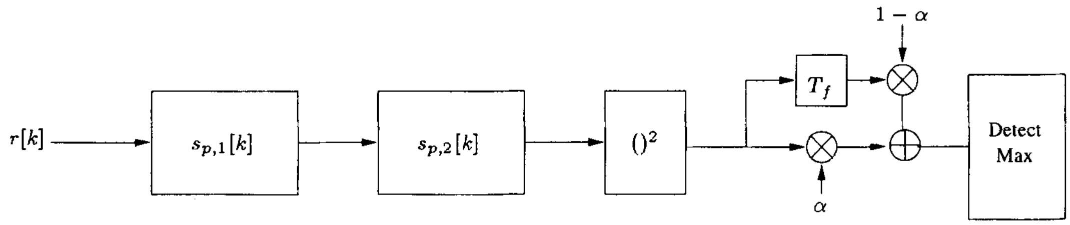


FIG. 11. — Primary Synchronization Processing.

Traitement de la synchronisation primaire.

structure for the primary synchronization sequence which allows the filter to be implemented as a concatenation of 2 FIR filters of length 16. A block diagram of the primary synchronization sequence is shown in Figure 11.

III.3.2. Channel estimation

Here we consider the training-sequence based multi-user channel estimation procedure for block-synchronous CDMA described in the UMTS/TDD standard.

In this scheme users are roughly synchronized to a common time-reference and transmit the training sequence at the same time (user timing errors are included as an effect of the channel and taken automatically into account by the estimation procedure). The maximum channel length (including possible timing errors) is Q symbols and the training sequence sent by each u-th user is a cyclic shift of the same common base training sequence m = $[m[0], m[1],\ldots, m[M-1]]^T$ of length M symbols. This solution allows joint estimation of all user channels if $M \geq QU$, where U is the number of interfering users. It is proposed and described in [16, 17] and with some modifications in [18]. The interested reader is referred to these papers and references therein for more details.

Under these assumptions we can write the received signal sampled at frequency $f_{ADC} = N_c f_c$ during the M symbols spanned by the training sequence as

$$w = \overline{\mathbf{M}}g + \upsilon \tag{7}$$

where

$$w = [w[0], w[1],\ldots w[MN_c-1]]^T \tag{8}$$

is the received signal,

$$g = [g_1^T,\ldots, g_u^T,\ldots, g_U^T]^T \tag{9}$$

is a vector containing the channel impulse responses of the U users,

$$g_u = [g_u[0], g_u[1],\ldots g_u[QN_c-1]]^T \tag{10}$$

is the u-th user channel filter vector and ν is a vector of interference plus noise samples, assumed to be white. The $MN_c \times MN_c$ matrix $\overline{\mathrm{A}}$ is defined as

$$\overline{\mathrm{M}} = \mathrm{M} \otimes \mathrm{I}_{N_c} \tag{11}$$

where (⊗) denotes the Kronecker product and M is a circulant matrix containing all the possible cyclic shifts (by columns) of the base sequence **m**. The matrix $\overline{\mathrm{M}}$ is also circulant and it is unitary similar [19] to the diagonal matrix diag($\overline{\alpha}$), where

$$\alpha = [\underbrace{\alpha^T,\ldots,\alpha^T}_{N_c \text{ times}}]^T$$

and where α is the Discrete Fourier Transform (DFT) of α. After some algebra [18], it is possible to show that the Least Squares estimation of the overall channel impulse response g is given by

$$\hat{g} = \mathrm{IDFT}\left\{\frac{\mathrm{DFT}\{w\}}{\overline{\alpha}}\right\} \tag{12}$$

where DFT and IDFT denote direct and inverse Discrete Fourier Transforms. The ratio of two vectors should be interpreted as the element-by-element division.

This approach can be applied to both base-band and pass-band signals. The receiver can also use the a priori information that the signal bandwidth is limited to W. Notice that this operation in the frequency domain corresponds to low-pass filtering in the time domain, moreover it reduces the computational cost since only a part of the MN_c products (by the element-wise inverses of $\overline{\alpha}$ in (12)) are computed. Eventually, after the IDFT, the processing gives the estimated channel complex envelope. The channel estimation procedure is summarized in Figure 12.

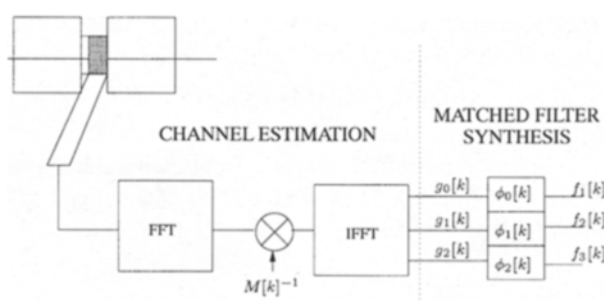


FIG. 12. — Channel Estimation and Matched Filter Synthesis.

Estimation du canal et synthèse du filtre adapté.

III.3.3. Matched Filter synthesis and data detection

Given the channel estimates, we are then interested in synthesizing a Matched Filter (MF) matched to the cascade formed by the user data spreading sequence, the chip pulse shape filter and the user channel. This is also shown in figure 12. The overall impulse response for code i is given by

$$f_i(t)=\sum_{k=0}^{L_i-1}\phi_i[k]g(t-k/f_c) \tag{13}$$

where L_i is again the spreading gain. Using the sampled channel estimate $g[k]$ we synthesize the discretetime filter $f_i[k] = f_i(t)\,|_{t=k/f_{ADC}}$ matched to the overall response as follows

$$\hat{f}_i[k]=\phi_i[k]*\hat{g}[k] \tag{14}$$

In order to extract the data symbols we filter the received signal with the MF obtaining

$$v_i[k]=r[k]*\hat{f}_i^*[-k] \tag{15}$$

In this setting $r[k]$ *is* real while $\hat{f}_i[k]$ is complex so the product requires two real multiplications. On the contrary the baseband samples of $r[k]$ would be at half the sampling rate but would be complex. So the two complexities are identical.

Notice that the signal after matched filtering is still pass-band and the symbol estimates after subsampling are given by

$$\hat{b}_i[k]=v_i'[N\,N_c k] \tag{16}$$

where $v_i'[k]$ *is* the complex envelope of the MF output. But since

$$v_i'[k]=(-j)^k v_i[k] \tag{17}$$

substituting into (16) and for $N_c = 4$ we get

$$\hat{b}_i[k]=(-j)^{N N_c k}v_i[N\,N_c k]=v_i[4Nk] \tag{18}$$

In this way the symbol estimates are given by sub-sampling the MF output at symbol rate without taking care of the demodulation.

III.3.4. Carrier synchronization and decoding

The carrier synchronization is done at symbol rate with a classical decision directed algorithm [20]. The algorithm then takes a decision on the symbols and recovers the data (in our example a video stream).

III.3.5 Re-sampling

The baseband processing algorithms such as synchronization, channel estimation and data detection assume that the signal is sampled with an integer number, N_c, of samples per chip. In the current implementation we set $N_c = 4$. This solution avoids utilization of re-sampling techniques at both the transmitter and receiver front-end. These techniques have been studied in [15] and will be implemented in the next version of the software.

IV. VALIDATION OF THE EXISTING PLAFFORM

The platform described in this paper has been validated by the transmission and the reception of two user full-duplex real-time video flows in an indoor environment. Two H263 video streams are transmitted in parallel and decoded in real time. For this we use the following parameters:

- spreading factor 16
- bit rate 397 kbps (peak) per user
- TDD configuration: 1 Tx slot followed by 1 Rx slot (transmission is done every 2 slots)
- two synchronous full-duplex streams per slot
- RF band: 5 MHz at 2.1 GHz

V. CONCLUSION

This first demonstration shows that the architecture of the platform is capable of sustaining real-time communications and is thus promising for future developments. The platform is currently being enhanced and opened to both industrial and academic collaboration. The enhancements will consist of

- support for multiple antenna transceivers
- more sophisticated signal processing algorithms
- multi user detection
- layer 2 (RLC,MAC) functionality

Collaboration has already begun under the label of the RNRT *(Réseau National de la Recherche en Télécommunications)* financing program organized by the French Ministry of Industry and Finance. Three projects have been initiated covering the following topics:

- radio subsystem improvement (flexibility and sensitivity)
- compliance with the 3GPP UMTS/TDD specification
- higher-level protocol stacks
- integration to an IPv6 experimental backbone

VI. CREDITS

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BIOGRAPHIES

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Alain ENOUT received his engineering diploma in signal processing from ISMRA (Institut des Sciences de la Matière et du Rayonnement, École Nationale Superieure d'Ingenieur de Caen) in 1986. He also received a Diplôme d'Études Approfondies in instrumentation and control.
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