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The 2008 CAV Award citation

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The 2008 CAV Award is given to Rajeev Alur and David Dill for their 1990 paper on "Automata for modeling real-time systems", which introduced the formalism that is now known as *timed automata*.

This work by Alur and Dill is concerned with real-time systems, whose execution is constrained by timing considerations. With the ubiquity of embedded computers, there is an urgent need for a formal methodology of verifying such systems. During the late 1980's there were several attempts to extend the theory of reactive-system verification to real-time systems. Alur and Dill's work put this research direction on a firm foundational footing.

The model of timed automata introduced by Alur and Dill in their 1990 paper has become the standard formal model for the verification of real-time systems. The paper, which is among the most cited papers in formal verification, not only introduced the model, but already established its main properties, namely, the reducibility of emptiness to a finite-state construction and the undecidability of universality. These two possibility and impossibility results have provided the foundation for the theory and practice of the verification of real-time systems.

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The CAV Award is given annually

"For a specific fundamental contribution or a series of outstanding contributions to the field of Computer-Aided Verification."

This is the first year that the CAV Award is given. It was presented at the CAV conference on July 10, 2008, in Princeton, New Jersey.

Rajeev Alur

Dr. Alur is Zisman Family Professor in the Department of Computer and Information Science at University of Pennsylvania. He obtained his bachelor's degree in computer science from the Indian Institute of Technology at Kanpur in 1987, and PhD in computer science from Stanford University in 1991. Before joining the University of Pennsylvania in 1997, he was with the Computing Science Research Center at Bell Laboratories. Dr. Alur's research spans formal modeling and analysis of reactive systems, hybrid systems, model checking, software verification, and design automation for embedded software. His awards include the President of India's Gold Medal for academic excellence, a CAREER award of the US National Science Foundation, and an Alfred P. Sloan Faculty Fellowship. He is a Fellow of the ACM, a Fellow of the IEEE, and recently served as the chair of ACM SIGBED (Special Interest Group on Embedded Systems).

David L. Dill

Dr. Dill is a Professor of Computer Science and, by courtesy, Electrical Engineering at Stanford University, where he has been on the faculty since 1987. He has an SB in Electrical Engineering and Computer Science from the Massachusetts Institute of Technology (1979) and a PhD from Carnegie-Mellon University (1987). Dr. Dill has research interests in a variety of areas, including computational systems biology, the theory and application of formal verification techniques to system designs, and voting technology. He has also done research in asynchronous circuit verification and synthesis, and in verification methods for hard real-time systems. He was one of the founders and the Chief Scientist of 0-In Design Automation (later acquired by Mentor Graphics), and the founder of the non-profit organizations Verified Voting Foundation and VerifiedVoting.org. His awards include the ACM's Distinguished Dissertation award for his PhD thesis, a Presidential Young Investigator award from the National Science Foundation, a Young Investigator award from the Office of Naval Research, and the Electronic Frontier Foundation's Pioneer Award (for work in electronic voting). He is a Fellow of the IEEE and ACM.