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LiNiO Junction Gate for High-performance Enhancement-mode GaN Power Transistor

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Abstract

GaN metal-oxide-semiconductor high electron mobility transistors (MOS)HEMTs) offer outstanding properties for next-generation power electronics devices. The high conductivity, high voltage blocking capability, high operation frequency, and device-level integration can be achieved on the same technology platform. Moreover, the development of large-scale GaN-on-Si substrate reduces the cost of GaN lateral devices. That GaN power device has already been widely used in today's consumer electronics, and communications base stations with its superiority of power density, and energy efficiency.

Despite the ideal side of GaN material for power transistor, the junction less structure of HEMT made it hard to achieve enhancement-mode (e-mode) operation. Existing solutions either rely on complicated processes or sacrifice device performance. A simple process, high performance, and reliable operation e-mode device are desired.

This thesis proposes Li doped NiO as gate material combined with Tri-gate structure to achieve e-mode operation. This relied on a simple oxide deposition process, without using barrier recess or regrowth, and achieved a high-quality interface. These critical characteristics haven't been demonstrated on gate stack engineering for normally-off devices and reveal the outstanding stability of LiNiO as a junction gate.

Moreover, to maximize the GaN power transistor performance boundary, a multi-channel junction gate device was developed, which uses multiple 2DEG channels to significantly reduce the device resistance while still operating at high breakdown voltage ($V_{\mathbf{BR}}$). The multi-channel junction gate device presents state-of-the-art performance, stable operation, and simple process e-mode GaN transistor.

Apart from achieving e-mode operation, the possibility of device-level integration was also explored. Reverse current conduction ability was achieved together with good on-state performance and voltage blocking capability. And the alternative method of regulating electric field to Tri-gate by grayscale lithography was developed.

The results in this thesis reveal the great value of using oxide semiconductor LiNiO as junction gate, demonstrating high performance, e-mode, and reliable device, and unleashing the performance potential through multi-channel epitaxy.

Keywords

GaN, LiNiO, Tri-gate, E-mode, Monolithic integration, freewheeling diode, slanted field-plate.

Résumé

Les transistors à haute mobilité électronique (MOS)HEMT en métal-oxyde-semiconducteur GaN offrent des propriétés exceptionnelles pour les dispositifs électroniques de puissance de la prochaine génération. La conductivité élevée, la capacité de blocage de tension élevée, la fréquence de fonctionnement élevée et l'intégration au niveau du dispositif peuvent être obtenues sur la même plate-forme technologique. De plus, le développement du substrat GaN sur Si à grande échelle réduit le coût des dispositifs latéraux GaN. Le dispositif de puissance GaN a déjà été largement utilisé dans les produits électroniques grand public d'aujourd'hui et dans les stations de base de communication grâce à sa supériorité en termes de densité de puissance et d'efficacité énergétique.

Malgré le côté idéal du matériau GaN pour les transistors de puissance, la structure sans jonction du HEMT rend difficile le fonctionnement en mode amélioration (e-mode). Les solutions existantes reposent sur des processus compliqués ou sacrifient les performances du dispositif. Un processus simple, des performances élevées et un fonctionnement fiable en mode e sont souhaités.

Cette thèse propose du NiO dopé au Li comme matériau de grille combiné à une structure Tri-gate pour atteindre un fonctionnement en mode e. Elle s'appuie sur un processus simple de dépôt d'oxyde, sans utiliser d'évidement ou de recroissance de la barrière, et permet d'obtenir une interface de haute qualité. Ces caractéristiques critiques n'ont pas été démontrées dans l'ingénierie des piles de grille pour les dispositifs normalement éteints et révèlent la stabilité exceptionnelle du LiNiO comme grille de jonction.

De plus, pour maximiser la limite de performance des transistors de puissance GaN, un dispositif de grille de jonction multicanaux a été développé, qui utilise plusieurs canaux 2DEG pour réduire de manière significative la résistance du dispositif tout en fonctionnant à une tension de claquage élevée (VBR). Le dispositif à grille de jonction multicanaux présente des performances de pointe, un fonctionnement stable et un transistor GaN e-mode de processus simple.

Outre l'obtention d'un fonctionnement en mode électronique, la possibilité d'une intégration au niveau du dispositif a également été explorée. La capacité de conduction du courant inverse a été obtenue

avec de bonnes performances à l'état actif et une capacité de blocage de la tension. Une méthode alternative de régulation du champ électrique sur le tri-gate par lithographie en niveaux de gris a été développée.

Les résultats de cette thèse révèlent la grande valeur de l'utilisation du semi-conducteur d'oxyde LiNiO comme porte de jonction, démontrant une haute performance, un mode e et un dispositif fiable, et libérant le potentiel de performance par l'épitaxie multicanaux.

Mots-clés :

GaN, LiNiO, Tri-gate, E-mode, Monolithic integration, freewheeling diode, slanted field-plate.

Symbols and Acronyms

Symbol	Quantity	Measurement unite or value
E_G	Band gap	eV
Ecrit	Critical electric field	MV/cm
μ_n	Electron mobility	$cm^2/V \cdot s$
n_i	Intrinsic carrier density	cm^{-3}
P_{SP}	Spontaneous polarization	
P_{pz}	Piezoelectro polarization	
N_s	Carrier density	cm^{-3}
I_D	Drain current	A/mm
G_m	Transconductance	mS/mm
V_{BR}	Breakdown voltage	V
V_G	Gate voltage	V
V_D	Drain voltage	V
W_{fin}	Fin width	nm
D_{fin}	Fin-to-fin distance	Nm
R_{ON}	On-resistance	Ω·mm
V_{TH}	Threshold voltage	V
$I_{ON, max}$	Maximum on-current	A/mm
E_V	Valence band offset	eV
E_c	Conductance band offset	eV
$R_{ON,SP}$	Specific ON resistance	$m\Omega \cdot cm^2$
R_S	Sheet resistance	Ω/sqr.
I_{OFF}	Off-state current	A/mm
D_{it}	Interface trap density	$eV^{-1} \cdot cm^{-2}$
L_{Fin}	Fin length	nm
Q_G	Gate charge	C/cm^2

Abbreviation	**Full name**
GaN	Gallium nitride
Si	Silicon
SiC	Silicon carbide
2DEG	2-Dimensional electron gas
EV	Electric vehicle
HV	Hybrid vehicle
LED	Light-emitting-diode
RF	Radio frequency
FOM	Baliga' s Figure of Merit
GIT	Gate injection transistor
HD-GIT	Hybrid-drain-embedded gate injection transistor
LDMOS	Lateral diffused MOSFETs
SS	Subthreshold swing
IGBT	Insulated-gate bipolar transistor
FP	Field-plate
e-mode	Enhancement-mode
ALD	Atomic layer deposition
XRD	X-ray diffraction
HfON	Hafnium oxynitride
TOS	Transparent oxide semiconductors
UV	Ultraviolet
TFT	Transparent thin-film-transistor
HTL	Hole-transporting layer
PLD	Pulse laser deposition
HRTEM	High-resolution transmission electron microscopy
RHEED	Reflection high-energy electron diffraction
SAED	Selected area electron diffraction
MRAM	Magnetic memory
TMOs	Transition-metal oxides
RRAM	Resistive random-access memory
RIE	Reactive ion etching
PECVD	Plasma-enhanced chemical vapor deposition
ICP	Inductively coupled plasma
ESL	Etching stop layer
NiO	Nickel oxid

BHF	Buffered hydrofluoric acid
EPD	End-point-detection
EDX	Dispersive X-Ray Analysis
IBE	Ion beam etching
HADDF	High-angle annular dark-field
STEM	Scanning transmission electron microscope
EDS	X-ray spectroscopy
FWHM	Full-width half-maximum
XPS	X-ray photoelectron spectroscopy
UV-Vis	Ultraviolet-visible spectroscopy
TCAD	Technology Computer-Aided Design
NBTI	Negative bias temperature instability
PBTI	Positive bias temperature instability
RCA	The Radio Corporation of America
HTRB	High-temperature reverse bias
FIB	Focused Ion Beam
HSQ	Hydrogen silsesquioxane(s)
SEM	Scanning electron microscopy
RTA	Rapid thermal annealing
RT	Room temperature
TMAH	Tetramethylammonium hydroxide
PR	Photoresist
HRXRD	High-resolution X-ray diffraction
RC-MOSHEMTs	Reverse-conduction GaN-on-Si metal-oxide-semiconductor high electron mobility transistors
ILD	Interlayer dielectric
SBD	Schottky barrier diode
HBD	Hard breakdown
S-FP	Slanted field plate
FOX	Flowable oxide
PEC	Proximity effect correction
IDM	Integrated device manufacturer
DUV	Deep ultraviolet

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Chapter 1 Introduction

Power electronic devices can control energy conversion by changing current, voltage, or frequency. Due to the rapid development of high-speed trains, electric or hybrid vehicles (EV &HV), and next generation communication technologies and smart devices, power electronics has gradually become an important technology in the era of solid-state electronics. The ability to control or convert higher electrical power and faster operating speed is a key requirement for power electronic devices. Looking at the size of the power electronics market, data for 2019 shows a market of $17.1 billion accounted for by various forms of power electronics devices (Figure 1-1)[1].

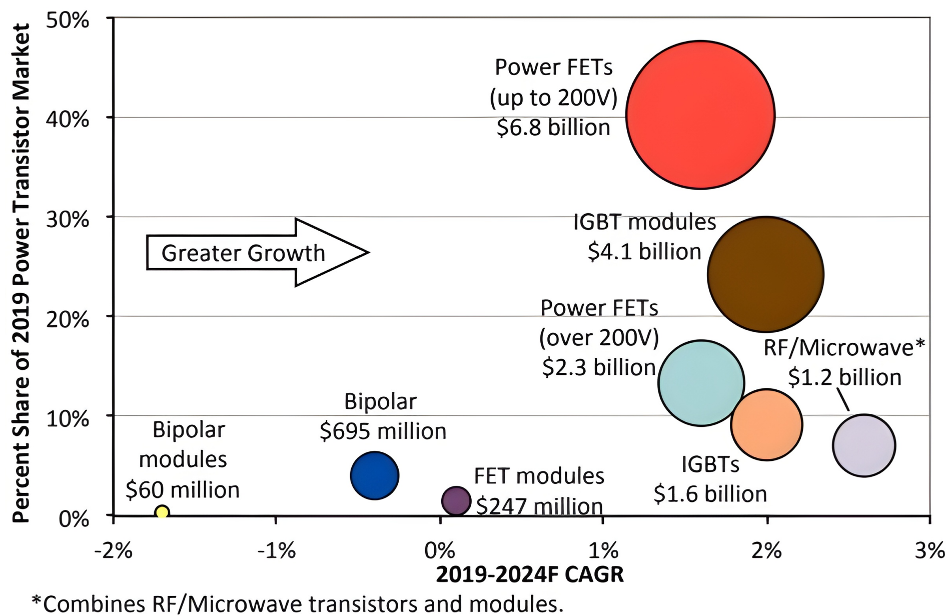

Figure 1-1 The power market share of different categories of power electronic devices [1].

Power electronic devices include transistors, diodes, and thyristors with various functions. Silicon-based (Si) devices continue to dominate today's power electronic device market. However, after several decades of development, the Si power device has reached its limits due to the material limitations of Si. The low operating frequency and low critical electric field of Si lead to large size of Si power devices and bulky circuit design based on Si power devices. It is a challenge for Si power devices to meet the requirements of the growing demand for fast, compact, and ultra-high power density conversion systems.

On the other hand, gallium nitride (GaN) is fast becoming a popular material for next-generation power electronics. This is due to its superior material properties and the availability of low-cost, large-size GaN-on-Si or GaN-on-SiC wafers, which is benefited from mass investment in the light-emitting diode (LED) industry. GaN has been widely and rapidly adopted in consumer electronics, base station components RF and military RF /microwave applications.

In the following sections, we first review the history of GaN lateral device development and introduce the advantages of GaN as a power electronic material as well as its lateral structure over other structures or materials. Then, we discuss the key requirements and challenges of GaN devices for the next generation of power electronic devices before we propose the methods to meet these requirements for future GaN power electronics.

1.1 GaN is an excellent material for power application.

The primary reason GaN stands out from Si or SiC as a material for power devices is its superior material properties. GaN offers a wide band gap, a high critical electric field, and high electron mobility at the same time, (Table 1-1). The combination of these remarkable properties of GaN results in high operating frequency, low switching losses, and high power density of GaN power devices. In recent years, there has been an explosion of investment and development in GaN power electronic devices industry. Several major companies such as GaN System, EPC, TSMC and Infineon have already launched mass production products. Technological giants, such as Apple, Huawei, and Xiaomi have used GaN switches in their consumer products to achieve higher power density and a smaller footprint. The reasons for the quick and wide adoption of GaN power devices in the technology industry can be attributed to the high Baliga's Figure of Merit (BFOM) [2], which leads to lower on-resistance (R_{ON}) at certain footprints and voltages, and the wonderful Baliga's High Frequency Figure of Merit (BHHFM) that helps reduce the size of the peripheral circuit. On the one hand, thanks to the significant investment and rapid acceptance of GaN power devices, GaN power devices are quickly becoming a high-performance and low-cost choice. However, the actual performance of GaN products is still far inferior to its material limitation. There are still several problems that prevent GaN from wide adoption.

Table 1-1, Comparison of Si, SiC, and GaN physical properties [3, 4].

Material	E_G[eV]	E_{crit}[MV/cm]	μ_n[cm^2/V·s]	BFOM (ε_r·μ·E_c^3)[rel. to Si]	n_i[cm^{-3}]
Si	1.12	0.23	1400	1	$1.4\cdot10^{10}$
4H-SiC	3.26	2.2	950	500	$8.2\cdot10^{9}$
GaN	3.39	3.3	800/1500	2400	$1.9\cdot10^{10}$

Vertical and lateral GaN transistors are two common configurations of using GaN as channel material of transistor. Vertical GaN transistors can exhibit high performance. However, the expensive free-standing GaN substrate and the complex fabrication process of the vertical GaN transistor limit its development. Currently, the main GaN device configuration is the lateral GaN HEMT structure fabricated on AlGaN/GaN HEMT epitaxy which is grown on Si or SiC substrate. Spontaneous polarization (P_{SP}) and piezoelectric polarization (P_{pz}) in AlGaN/GaN HEMT epitaxy can form a two-dimensional electron gas (2DEG) with high carrier density (N_s) at the interface between AlGaN and GaN. The 2DEG channel exhibits excellent conduction properties with a high electron mobility of over 2200 $cm^2/V\cdot s$ and a high N_s over 10^{12} cm^{-3}. However, this junction-less transistor structure has two problems: 1) the device naturally works as normally-on type[5], and 2) the device has no reverse conduction capability like a normal Si MOSFET, which requires an additional freewheeling current path.

Table 1-2 Substrate cost for different power devices [6].

Device Structure	GaN-on-GaN vertical devices	GaN lateral HEMTs	SiC Power Devices	Si Power Devices
Available substrate	50 mm GaN	200 mm Si/ 75 mm SiC	75 mm SiC	200 mm Si
Sub. cost per cm^2	\$50 ~\$100	~\$0.08/~\$6	~\$6	~\$0.08

There are solutions to achieve enhancement mode (e-mode) GaN transistor. However, performance always be sacrificed to achieve e-mode operation. An ideal GaN power transistor can achieve e-mode operation while maintaining good performance. In addition, the device should have high reliability. There are also some problems apart from performance, such as current collapse and dynamic R_{ON} degradation, which have been thoroughly studied [4]. To benchmark the performance of different GaN transistors, the Baliga FOM was introduced to describe the theoretical limit of the specific R_{ON} as a function of V_{BR}:

$$\begin{array}{cc} \text{Baliga FOM (Vertical)} & \text{Lateral FOM} \\ \frac{V_{BR}^2}{R_{on,sp}} = \frac{1}{4}\varepsilon\mu E_{crit}^3 & \frac{V_{BR}^2}{R_{on,sp}} = q\mu n_s E_{crit}^2 \end{array} \tag{1-1}$$

The elementary charge constant is denoted by q, the mobility by μ, n_s is sheet carrier density, ε is the dielectric constant, while E_{crit} is the critical electric field of the channel material. The theoretical performance can be calculated on the right-hand side of the formula. A good FOM is the essential requirement for GaN power transistors and will be considered in all devices in the later chapters.

1.2 Development of large-scale GaN-on-Si wafer

Apart from nearly perfect material properties, the successful development of large-size, low-cost GaN-on-Si wafers is another critical factor for the adoption of GaN in future energy applications.

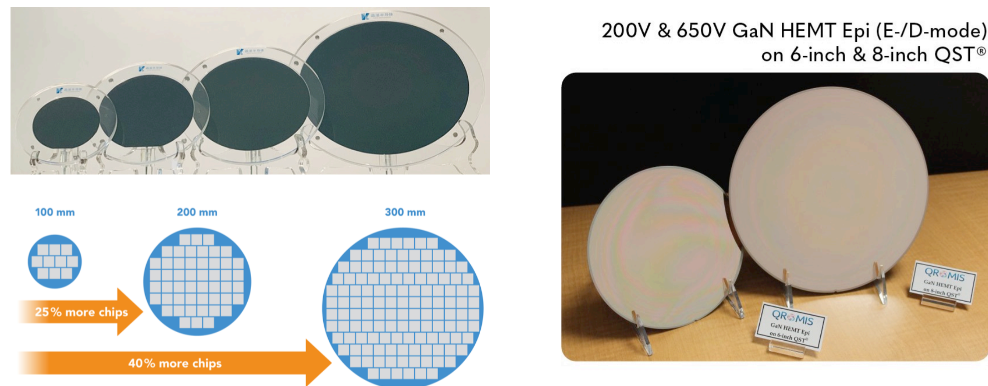

Figure 1-2 12-inch crack-free 1200 V GaN-on-Si wafer, and 8-inch GaN-on-QST® wafer for RF application.

Single-crystalline GaN can be grown on various substrates, such as Al_2O_3, Si, SiC, and AlN (Figure 1-2). Growing GaN epitaxial layers on Si can utilize the existing infrastructure of Si foundries. This can eliminate the need for costly special substrates and specialized foundry sites. Enkris Semiconductor has announced the possibility of 300 mm GaN-on-Si HEMT epitaxy that has excellent film thickness uniformity and high breakdown voltage of over 1200 V. This wafer size is compatible with the advanced 300-mm CMOS process line. Despite the challenges of large-scale GaN-on-Si wafer fabrication, including the control of stresses and defects, the successful demonstration of the 300 mm GaN-on-Si substrate enables a bright future for GaN integrated circuits.

1.3 Requirements for future GaN transistors.

In today's GaN lateral power transistor research, pursuing high power FOM toward material limitation, achieving device-level integration, and e-mode operation are considered several major directions that will have a significant impact on the future development of GaN power devices. In recent years, active development of the tri-gate structure has achieved low R_{ON} and high V_{BR} at the same time, successfully pushing the device performance limit.

Device-level monolithic integration is another main category of future GaN lateral device research. At present, only discrete GaN devices are successfully used in power circuits which require numerous peripheral circuits such as driving, control and protection. When various functional devices are monolithically integrated, system robustness and power consumption can be improved. In addition, the smaller footprint and less wiring lead to higher efficiency and multifunctional design modules,

making thermal management easier [7-10]. The popular lateral GaN HEMT configuration has a planar top-gate design, which is beneficial for various functional integrations, such as driving logic circuits and current regulation diodes.

Achieving e-mode is another important focus in GaN power transistor research, as this is a necessary property of GaN to be used in commercial applications. Many methods have already been developed to achieve e-mode operation such as F-implantation, gate recess and p-GaN gate. However, the p-(Al)GaN gate is still the only device-level solution for e-mode operation that has been successfully used in real application scenarios. This is mainly due to its superior stability and proven reliability compared to any other techniques. The combination of p-(Al)GaN gate and planar HEMT structure is the current standard configuration of GaN lateral power devices although the use of the p-GaN gate comes at the expense of the performance of the HEMT structure.

1.3.1 Technologies to push the performance limits.

GaN has a good high power FOM due to its material properties. However, the performance of lateral GaN device is still far from the theoretical predictions.

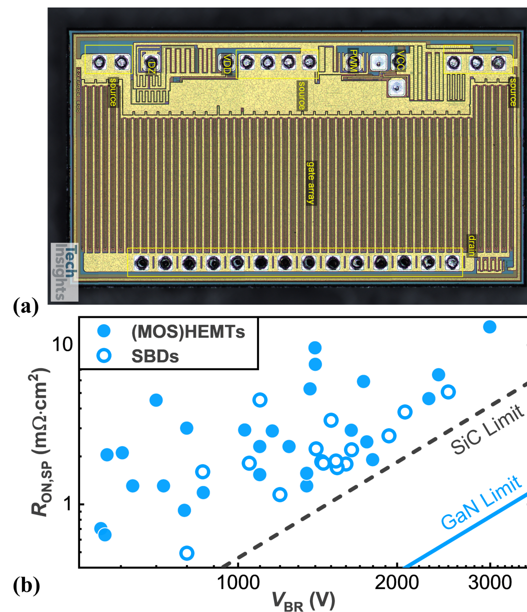

Figure 1-3 (a) Optical microscope image of Navitas 650 V GaNFast Power IC [11]. (b)$(V_{BR})^2/R_{on,sp}$ FOM of current GaN-on-Si devices.

The first reason is the R_{ON} of the lateral device including not only the drift region but also the resistance of the gate and ohmic contact region. However, the FOM for high power describes only the channel resistance in the drift region. The second reason is the non-uniform electric field distribution of lateral device. The electric field distribution along the longitudinal direction of the device is very non-uniform due to the asymmetric gate and AlGaN/GaN heterostructure as well as the buffer leakage

of the GaN-on-Si epitaxy. As a result, the breakdown field of a typical GaN material is limited to 3 MV /cm. However, the record-results are as low as 0.6 MV /cm, far from the material limit. The third reason is the limitation of single layer 2DEG. The 2DEG can have high *N*s and high mobility at the same time. However, further scaling the current loading capability of the HEMT structure is difficult because there is a trade-off between mobility and *N*s. In vertical devices. The current can be easily scaled by increasing the device area. However, in a lateral GaN transistor, the current loading capability can only be achieved by increasing the gate width. This leads to a non-area efficient design where the metal wire occupies most of the die area (Figure 1-3 (b)). All this results in the performance of the cutting-edge lateral GaN transistor far from the material properties (Figure 1-3 (a)). This tri-gate structure is a breakthrough technology to improve the FOM of lateral GaN transistors, which does not require a complex multilayer gate or source field plate [12, 13]. The field-plate structures require multiple metal/oxide deposition and patterning processes, which significantly complicates the process. But the tri-gate structure modulates the electric field in the direction of the device width [14], through a concise device design. This simple, high-performance, and flexible device structure not only enhances the DC performance of the device, but also offers the possibility of integration with other technologies, such as various gate stacks and device-level integration.

1.3.2 High-performance e-mode GaN transistors.

High-performance operation in e-mode is a major challenge for GaN power transistors.

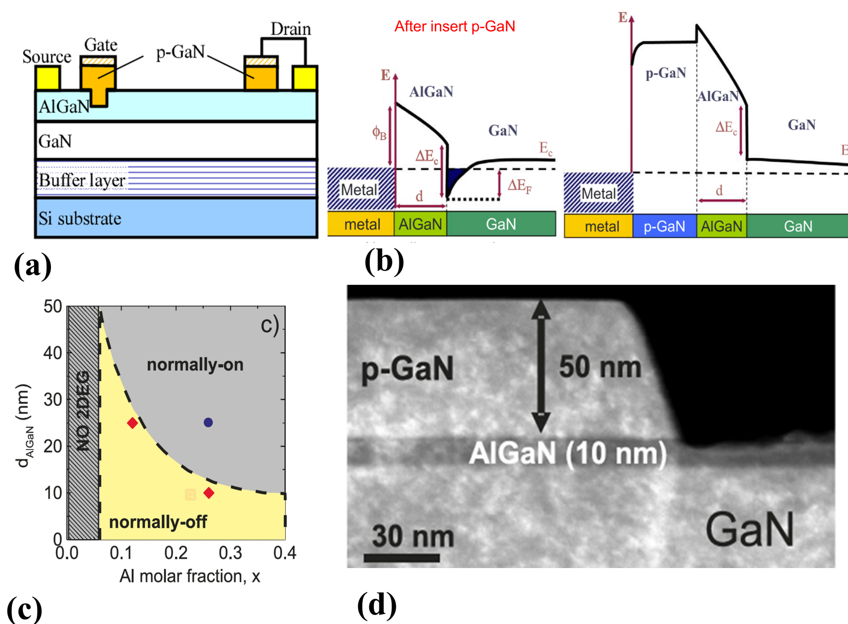

Figure 1-4 (a) Schematic of p-GaN gate e-mode transistor [15, 16], (b) schematic of the operation principle of p-GaN gate e-mode device. (c) Device operation mode as a function of Al percentage and thickness of the AlGaN barrier, (d) cross-section TEM image of the p-GaN/AlGaN/GaN heterostructure after p-GaN dry etching [17].

Various technologies have been explored to realize the goal: recess-gate structure, p-(Al)GaN gate structure, implanted gate structure, cascode configuration, and nanowire structure. If we look at the existing e-mode GaN products in the market today, p-GaN and the cascode structure are the only two commercial solutions.

1.3.2.1 Recess-gate technology.

Early work to achieve e-mode transistors is done with recess-gate HEMT structures [18, 19]. But the small maximum I_D, small transconductance G_m, and high gate leakage limit the performance of this structure. To overcome these problems, researchers have proposed to insert a thin oxide layer between the gate and the recess barrier [20] to form a MOSHEMT structure. Recess-gate MOSHEMT can have a very positive V_{TH} [21] and a high operating frequency [22]. Recess-gate structures can be fully or partially recessed [23], which is distinguished by the etching strategy of the barrier. There is a trade-off between the difficulty of the process (controlling the etch depth) and the performance of these two configurations.

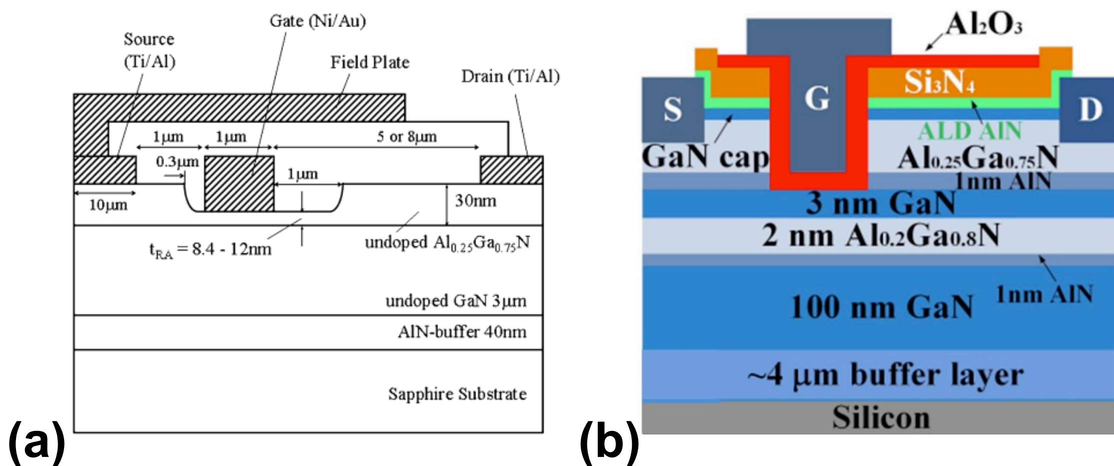

Figure 1-5 (a) Cross-sectional structure of fabricated AlGaN/GaN HEMT with recessed-gate structure [24], (b) Cross-sectional structure of gate recess GaN MOSHEMT with AlN/Si_3N_4 passivation and post-recess channel protection layers [25].

The main advantages of the MOSHEMT structure are a high V_{TH}, a large V_G swing and a low gate leakage current. This leaves enough safety margin for gate overdrive and is very attractive for RF applications.

To achieve a small R_{ON} while maintaining a high V_{TH}, precise barrier etching techniques have been developed, resulting in damage-free partial barrier recess. A standard configuration is a MOSHEMT consisting of a partially etched barrier under the gate [23]. However, this is difficult to achieve because time-controlled etching is not a reliable process that can lead to non-uniform V_{TH} among

different devices. Besides, the low deposition temperature oxide layer in the recess gate structure also has a quality problem because it has high density of bulk traps and interface traps. The reliability of MOSHEMT structures, especially recess-gate MOSHEMT is rarely recorded. These two drawbacks limit their acceptance in the industry. Research in the field of recess-gate MOSHEMT has focused on precise control of etching depth [26], surface protection, passivation [27-30] and improving the reliability of recess-gate MOSHEMT [31].

1.3.2.2 P-GaN Gate technology.

The use of p-GaN/p-AlGaN on top of AlGaN/GaN can raise the conduction band of GaN channel near the 2DEG region. A suitable combination of p-GaN and barrier layer could lead to a complete depletion of the 2DEG with a gate bias of zero. The p-GaN gate devices can be divided into two categories according to the work function of the gate metal: ohmic gate and Schottky gate. The ohmic gate is developed by Panasonic [15, 32] and contains Pd and p-AlGaN in the gate stack, a technology called gate injection transistor (GIT). This configuration achieved high current drive performance a problem for most p-GaN gate devices [32]. Reliability is an issue for the e-mode device. In the ohmic gate device, the gate leakage current is higher, but the absence of a depleted region does not cause a high peak field at the gate-metal/p-GaN interface, as is the case with a Schottky gate. In some extreme case studies, excellent stability of the positive gate bias has been observed in a measurement range far beyond normal operation [33]. In addition to excellent stability in the on-state, the GIT device also shows superior reliability in the off-state according to industrial criteria [15]. Moreover, excellent dynamic performance up to 850 V [15] has been achieved using a hybrid drain embedded gate injection transistor (HD-GIT) structure. One of the main differences of the ohmic gate type from the Schottky type is the relatively larger gate current at positive bias. However, most of the ohmic gate's good performance can be shown at a very low V_G. This is a major difference from Schottky p-GaN gate devices or MOSHEMT devices, which must be operated at very high V_G. In addition, the gate stack of the GIT transistor behaves like a diode when turned on. This means that in the event of a voltage spike at the gate, no breakdown will occur. Another category of p-GaN transistors uses a Schottky gate. The main advantages of the Schottky type are a larger V_{TH} than ohmic type and a low gate current [34]. EPC and TSMC are the main suppliers of this type of device and provide integrated device manufacturer (IDM) service to other design companies such as GaN System and Navitas. The lower I_G value and higher V_{TH} also lead to a much simpler gate driver design than GIT-type devices. The verified industry-level reliability and stable performance make the p-GaN gate GaN transistor the only commercialized device-level solution.

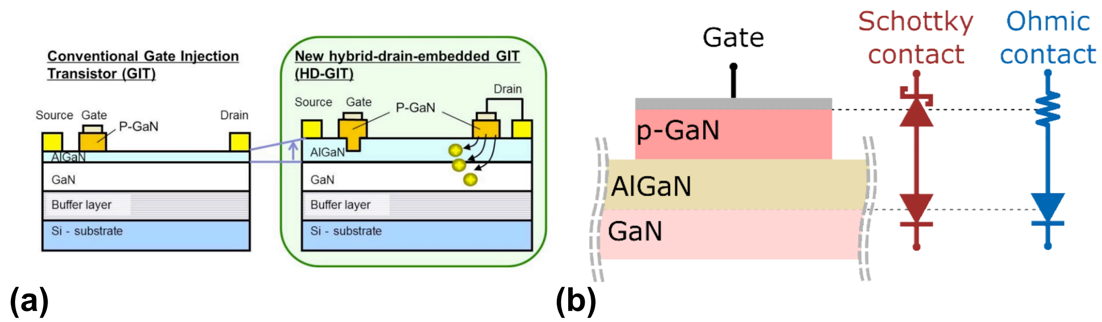

Figure 1-6 (a) Configuration of HD-GIT device, (b) cross-section of gate region and equivalent circuits corresponding to the Schottky and ohmic gate [35].

1.3.2.3 Cascode technology.

In the Cascode GaN e-mode device, a normally-off low-voltage Si MOSFET and a normally-on high-voltage GaN transistor are integrated in a single package [36, 37]or on the same chip [37]. The source of the Si MOSFET is connected to the gate of the GaN HEMT, as shown in Figure 1-7. Normally, low-voltage lateral-diffused MOSFETs (LDMOS) are used [38]. It is one of the two commercially available methods to fabricate normally-off GaN products. The advantages of this package-level solution include a robust gate structure, high threshold voltage, simple gate drive, low reverse recovery loss, and body diode integrated. A very large V_G swing of 15-25 V has been demonstrated [39]. From the tear down image of a commercial cascode device under the optical microscope, it can be seen that the LDMOS occupies a large area in the whole package (Figure 1-7 (b)).

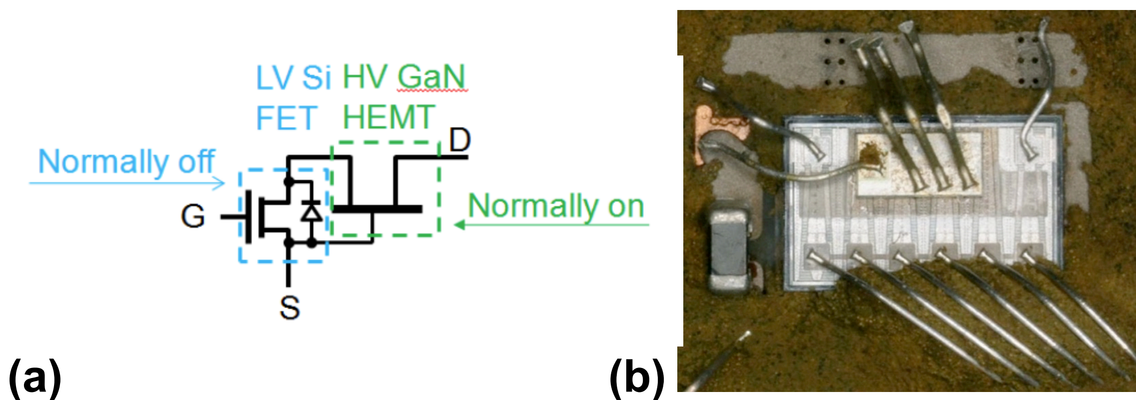

Figure 1-7 (a) Transphorm GaN Switch [36]. (b) Tear down of Nexperia’ s GaN transistor (GAN063-650WSA).

The R_{ON} of cascode structure would include R_{ON} of Si LDMOS and GaN HEMT. The increase of R_{ON} compared to independent GaN HEMT would be more significant for lower voltage devices. In addition, in the cascode configuration, the advantage of high-temperature capability of GaN is not feasible due to the low operating temperature of Si devices.

In summary, cascode configuration is a simple and reliable technology route to quickly adopted GaN transistor. However, the existence of low voltage Si transistor in cascode configuration results in weaker performance and larger dimension over other e-mode solutions. These limit the further development of cascode configuration.

1.3.3 GaN integration circuits.

The GaN transistor is an ideal component for future power applications. It offers high switching speed, high critical electric field and low resistance at the same time. The GaN power system includes several discrete GaN components that regulate currents of a few amperes and operating voltages below 1 kV. The parasitic inductances in this system limit the operating speed and cause unwanted ringing and power loss. When used as discrete components, GaN power devices are driven by external IC driver circuits used for signal generation. To take full advantage of the fast-switching capability of GaN power devices, the power device and driver must be integrated on the same chip. The integration of power devices and driving circuits can lower the gate-driver inductance and allows the devices to operate at a high frequency. This can further reduce the size of passive components in the circuit [40].

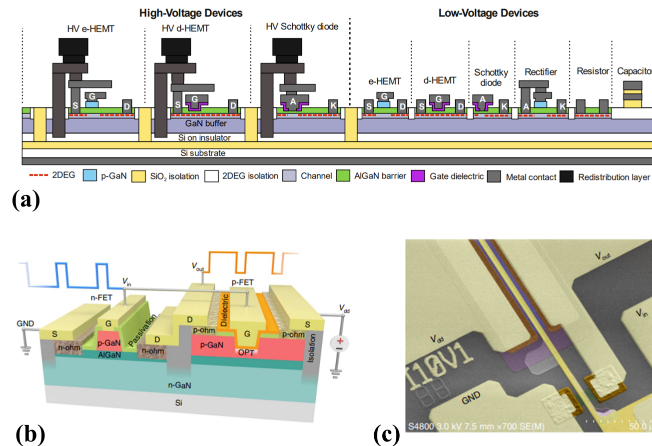

Figure 1-8 (a) IMEC' s 200 V GaN-on-SOI power IC technology [40]. (b) Schematic and (c) SEM image of GaN-based complementary logic integrated circuits [41].

GaN power devices require peripheral logic circuits to drive the transistor. In current commercial product, Si complementary metal-oxide-semiconductors (CMOS) are used for this purpose. Using Si and GaN devices together at the package or circuit level limits the scaling potential of GaN devices in footprint. The development of GaN logic circuits is another direction of GaN device integration. They can form a logic circuit that can operate at high frequency and under harsh conditions [41]. The exploration of GaN-based CMOS devices is challenging due to the lack of p-channel GaN FETs and the difficulty of the process of integrating p-FETs and n-HEMTs on the same substrate.

1.4 Thesis outline

Chapter 2 demonstrates high-performance slanted field-plate MOSHEMTs fabricated by grayscale lithography. To improve the FOM of the lateral GaN transistor without using the traditional complicated multi-level field-plate structure, we developed the slanted field-plate technology, which forms a field-plate with three angles in a single lithography step. The angle of the slanted field-plate can be set in the layout design file. The detailed process flow was discussed, and the device performance was comprehensively shown and compared with the normal MOSHEMTs.

In addition to using a planar field-plate structure to improve the FOM, a tri-gate nanowire structure has also been developed. It can have a high V_{BR} without affecting the device's on-state performance (R_{ON} and I_{ON}, max). However, it is challenging to achieve the e-mode with the tri-gate structure. In Chapter 3, we propose a junction gate structure based on the p-type oxide semiconductor LiNiO to achieve high-performance e-mode operation. We compare different process flows and present our special oxide lift-off technology to precisely pattern the LiNiO layer. In addition, different LiNiO oxides are compared in terms of channel pinch-off ability and band alignment with AlGaN. A comprehensive characterization of the DC, high temperature and reliability performance of LiNiO junction gate devices.

Chapter 4 describes the design and process to achieve a high-performance e-mode multi-channel junction gate transistor using LiNiO. This structure successfully achieves fairly low R_{ON} along with stable operation. Several problems have been solved on the way to high performance e-mode multi-channel devices, including off-state leakage, R_{ON}, negative gate bias leakage and V_{BR}. In the remainder of this chapter, we present comprehensive performance of LiNiO-gated multi-channel devices and compare it to state-of-the-art results in several ways.

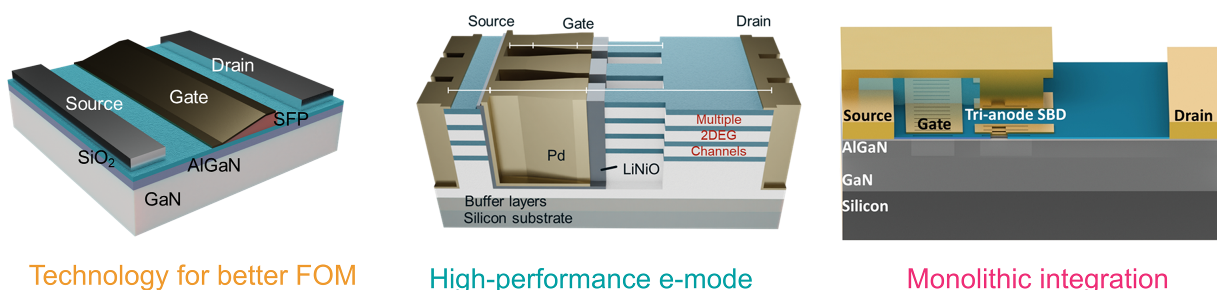

Figure 1-9 Three devices achieved in this thesis, 1. Slanted field plate technology for better FOMs, 2. Using LiNiO semiconductor oxide as junction gate, which works together with tri-gate and multi-channel epitaxy. Enhancement-mode operation, high-performance, and good reliability was reported at the same time. 3. Based on tri-gate structure' s concise process, and high-performance, monolithic integration of freewheeling diode and GaN MOSHEMTs was demonstrated.

Chapter 5 explores the possibility of monolithic integration of tri-gate GaN transistor. The concise planar structure without the use of multiple level field-plates makes the tri-gate structure suitable for device-level integration. In this chapter, we showcase an innovative design to solve another unsolved problem of the (MOS)HEMT structure: the reverse conduction capability. Here, a tri-anode structure is combined with a tri-gate MOSHEMT in such a way that, for the first time, good reverse conduction and, at the same time, good current blocking capability are achieved, along with good on/off forward/ reverse performance.

Chapter 6 concludes the thesis with future perspectives.

Chapter 2 Slanted field-plate technology for higher V_{BR}

2.1 Introduction

Improving V_{BR} and R_{ON} are two directions to bring the FOM of the GaN device to the limits of GaN material. The high electron mobility, high carrier density and large band gap of AlGaN/GaN heterostructures have led to low R_{ON} and high V_{BR}. The specific R_{ON} is mainly determined by the epitaxy, while the V_{BR} can be influenced by the design of the device structure. Due to the non-uniform distribution of electric field along the device length in lateral GaN devices, a peak of electric field forms at the gate edge, causing premature device breakdown. The state-of-the-art V_{BR} of lateral GaN devices is far from the material limit. Field-plate (FP) technology-consisting of a parallel gate or source metal field-plate patterned on the dielectric layer, is an efficient way to create an optimal electric profile [12, 13]. It can relax the electric field at the gate edge, which not only improves the device V_{BR}, but also reduces the current collapse and dynamic degradation of R_{ON}. Multi-stage FPs have shown promising results [42] (Figure 2-1 (a)). However, the process of multi-stage FPs is complex and involves multiple stages of oxide/metal deposition, patterning, and etching (Figure 2-1 (b)). From the numerical analyses [13], slanted field-plate (S-FP) is the most effective in improving the breakdown voltage (Figure 2-1 (c) and (d)). However, it is challenging to achieve an S-FP structure with the desired slanted angle [43-45].

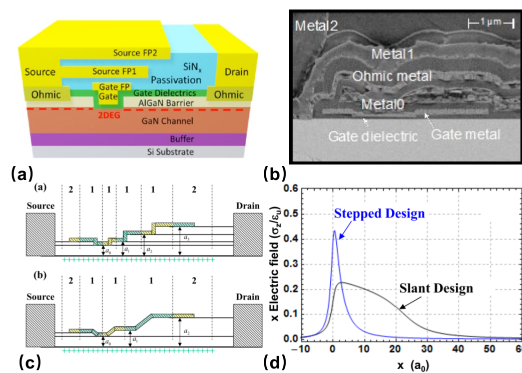

Figure 2-1 (a) Schematic of multi-level field plate [46]. (b) Cross-section SEM of multi-level field plate [40]. (c) Schematic of multi-stage gate field plate and slanted gate field plate [47]. (d) Electric field along the drift region through simulation [47].

Existing solutions for S-FPs are mainly based on unique physical mechanisms (Figure 2-2) that cannot achieve the arbitrary slanted angle and are not reproducible. In this chapter, a novel technology to achieve S-FP is proposed, that is, using grayscale lithography on flowable oxide (FOX) in a single lithography step to fabricate a FP with a triangular shape. The developed FOX functions directly as S-FP dielectric. The V_{BR} shows significant improvement by S-FP, due to the more uniform electric field distribution in the drift region. The S-FP MOSHEMT shows excellent performance with a V_{BR} of 832 V ((L_{GD} = 5 µm, at 1 µA/mm), a small R_{ON} of 4.5 Ω-mm, and a high-power FOM ($V_{BR}^2/R_{ON, SP}$) of 1.24 GW/cm2. This approach uses a simple and flexible process to modulate the electric field in the MOSHEMT and offers a promising technology for future advances in high-performance GaN devices [48].

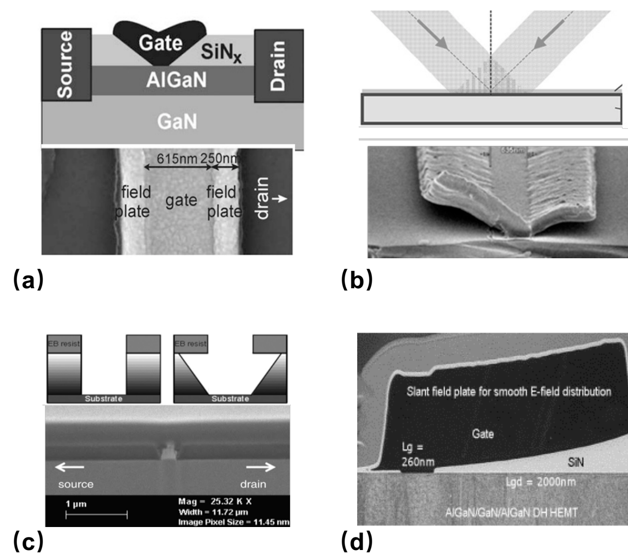

Figure 2-2 (a) Schematic and top-view SEM image of slanted field plate using well-controlled CF_4 etching [13]. (b) Schematic and SEM image of S-FP using angle exposure during lithography [45]. (c) Schematic and cross-section SEM image of S-FP using well-controlled SiCN etching [44]. (d) Schematic and cross-section SEM image of S-FP utilizing the surface tension of HSQ to achieve a slanted etching mask [43].

2.2 Motivation and approach

2.2.1 Grayscale lithography

It is possible to use multiple lithography steps to create a three-dimensional structure. However, this dramatically increases the overall complexity of the process. One attractive method is grayscale lithography, a technique that can produce complex topographies in a single exposure step. Conventional photolithography uses a binary mask, achieving dose adjustment for grayscale lithography using a Cr mask. However, this method is difficult to achieve for its complex mask fabrication process. The development of maskless lithography, such as direct laser writer and ebeam writer, allows lithographic writing with an adjustable dose. The dose can be precisely assigned in the design file. After

a low-contrast lithography process, the thickness of PR, which remains on the sample, can be varied by the laser or e-beam. In this way, grayscale lithography is a promising method for generating arbitrary surface geometries of PR in a single exposure step (Figure 2-3). There are several works on maskless grayscale lithography, including e-beam lithography combined with thermal reflow [49] and grayscale X-ray lithography [50]. In addition, a patterned surface can be transferred to permanent material by dry etching [51].

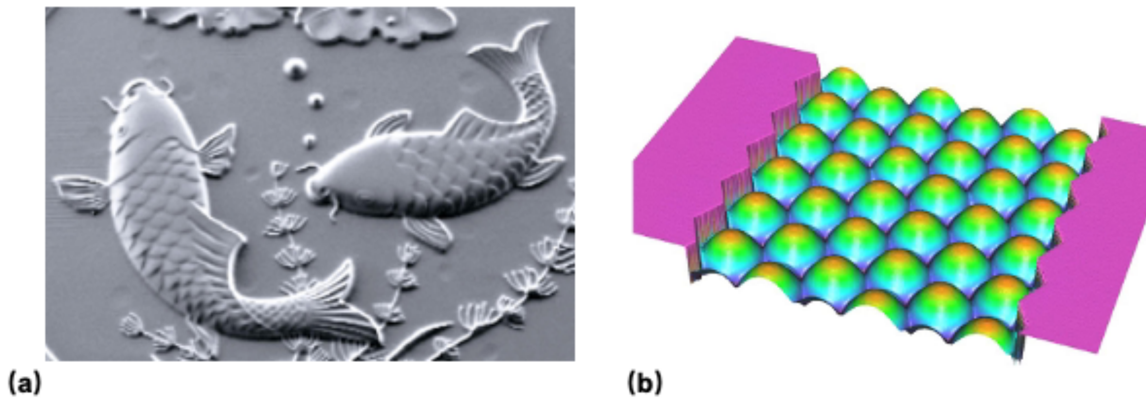

Figure 2-3 (a) SEM image of microfabricated fish relief structures using grayscale lithography. (b) Confocal microscope image of a micro lens array in a honeycomb arrangement (Heidelberg Instruments).

Transferring the exposed topography from PR polymer to a permanent material such as oxide results in imperfect shape control due to the micro-loading effect in the dry etching process. But most PR polymers cannot be directly used as structural materials due to their low permittivity. However, hydrogen silsesquioxane (HSQ) is a unique PR, which converts into polycrystalline SiO_2 after exposure and development. Different HSQ thicknesses on the same chip after the process have already been demonstrated. It has been used in cavity color printing structures [52] (Figure 2-4). And FOX is a kind of HSQ, with thicker spin-on film thickness.

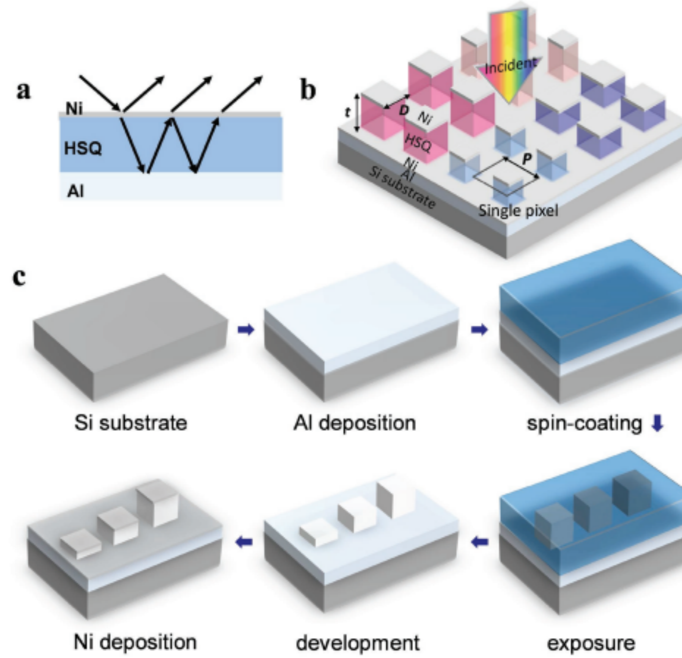

Figure 2-4 Concept and process flow for visible color printing. (a) The basic configuration of an interference color pixel. (b) 3D schematic concept of color printing based on grayscale-patterned resonators. (c) The schematic flow shows process flow [52].

2.2.2 Fabrication process of S-FP by grayscale lithography

S-FP is fabricated through grayscale lithography on FOX photoresist. The design of S-FP can be achieved by modulating the dose of FOX during exposure with e-beam lithography. The exposed and developed FOX serves as a dielectric layer, which becomes S-FP after metal deposition. The S-FP structure can be fabricated in a single step using this technology, and the angle can be adjusted through the layout design by assigning a different dose. Outstanding device performance has been demonstrated based on this S-FP technology.

Grayscale lithography as mentioned above enables the fabrication of a three-dimensional microstructure by photoresist. There are many ways to achieve this, such as multiple exposures and different densities of holes in the Cr mask. The primary mechanism is based on the contrast curve of PR, in which the remaining thickness of PR after development is related to the exposure intensity (Figure 2-5 (b)). With the conventional Cr mask, it is difficult to achieve controllable grayscale lithography due to the inflexibility of Cr mask fabrication. The development of thermal lithography or laser photolithography reduces the difficulty of grayscale lithography and is widely used in the research of structural color material [52] and meta-surfaces [53].

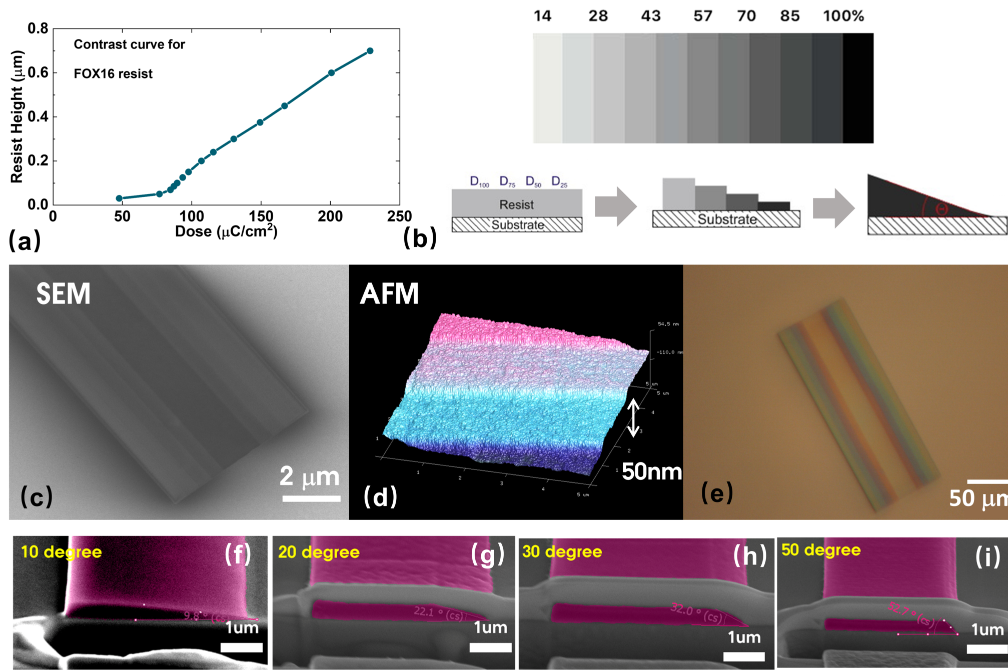

Figure 2-5 (a) Contrast curve for FOX 16, using CD 26 as developer. (b) Schematic of dose adjust method to achieve grayscale lithography. (c) SEM result of the grayscale lithography test structure. (d) AFM results of step structure. (e) optical image of the test structure. (f)(g)(h)(i) cross-section SEM image of different angles of slanted oxide.

However, the accuracy of photolithography is not high enough for the production of S-FP. The minimum dose adjustment step and exposure resolution of the deep ultraviolet (DUV) tool do not meet the requirement of achieving a smooth, slanted PR structure. In this work, we developed EBL grayscale lithography at FOX without the need for a post-exposure process such as thermal reflow. After exposure, a sharp and angle adjustable slanted oxide layer is obtained. The epitaxy in this work consisted of 5μm buffer, 0.3μm undoped GaN channel, 25 nm AlGaN barrier, and 1.8 nm GaN cap layers on a GaN-on-Si substrate. Fabrication began with etching the alignment marks by RIE, then the ohmic source/drain contact is made by a Ti/Al/Ti/Ni/Au stack and RTA. A 25 nm SiO_2 is deposited as the gate dielectric. The S-FP process was carried out in the following step, that a slanted oxide exposure can achieve on a planar surface without and mesa structure. This can improve the uniformity of the S-FP structure along the direction of the device width. The layout beamer software was used to perform the PEC based on the contrast curve from the dose test of low contrast process. Unlike the normal exposure of FOX, which aims at high resolution, the dose used here is much lower. And the developer is CD 26 instead of a developer with high TMAH concentration to have a slow and controllable development process (a less sharp contrast curve is preferred) (Figure 2-5 (a)). The thickness of the spin-on FOX is 700 nm, and different thickness of PR after development can be controlled in our experiment (Figure 2-5 (c)-(e)).

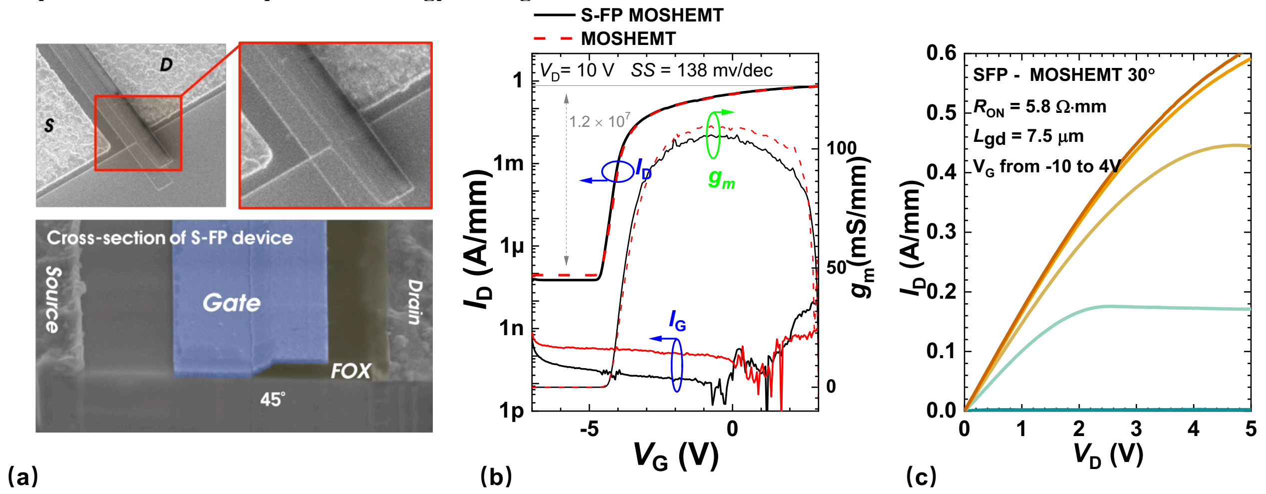

Figure 2-6 (a) SEM images of fabricated slanted FP device. (b)Transfer characteristic of Slanted FP device. (c) The output characteristic of the S-FP device

By modulating the dose in EBL, the S-FP angle could be engineered from 10 to 50 degrees by changing the layout design (Figure 2-5 (f)-(i)), and the developed FOX is directly used as a field-plate dielectric. After that, mesa isolation is performed by RIE etching, and finally a Ni/Au gate is deposited and patterned.

2.3 Results and discussion

In the SEM image of the fabricated device, a very sharp triangle S-FP device is successfully demonstrated. The device characteristics are normalized by the width (100 μm) (Figure 2-6 (a)). The circuit results are tested on 30° S-FP.

Figure 2-6 (b) shows the transfer curve characteristics of S-FP MOSHEMT. When sweeping the gate voltage (V_G) from -10 to 0 Von S-FP device (V_D = 10 V), a small I_{OFF}, on/off ratio of 8 orders and SS of 135.5 mV/dec are obtained. The V_{TH} of the S-FP device is -6.75 V and $G_{m,\ max}$ is 85.5 mS/mm (Figure 2-6 (b)). The I_G of both devices is very small, and the S-FP MOSHEMT device has an even smaller I_G at negative V_G. In the output characteristics (Figure 2-6 (c)), S-FP MOSHEMT shows a very small R_{ON} of 4.5 Ω·mm, which is due to its small L_{GD} of 7.5 μm. The current loading capability is over 600 mA/mm with a small V_G = 4 V.

One concern with the S-FP MOSHEMT device is that the gate dielectric has a gradient. The device could probably turn on gradually, resulting in a worse SS. However, the result shows that the difference between the S-FP device and the reference MOSHEMT is quite trivial. The small size of S-FP could be the reason for this good SS. This ingenious process achieves a slanted structure in a small space, which is of great value for the high-end RF devices.

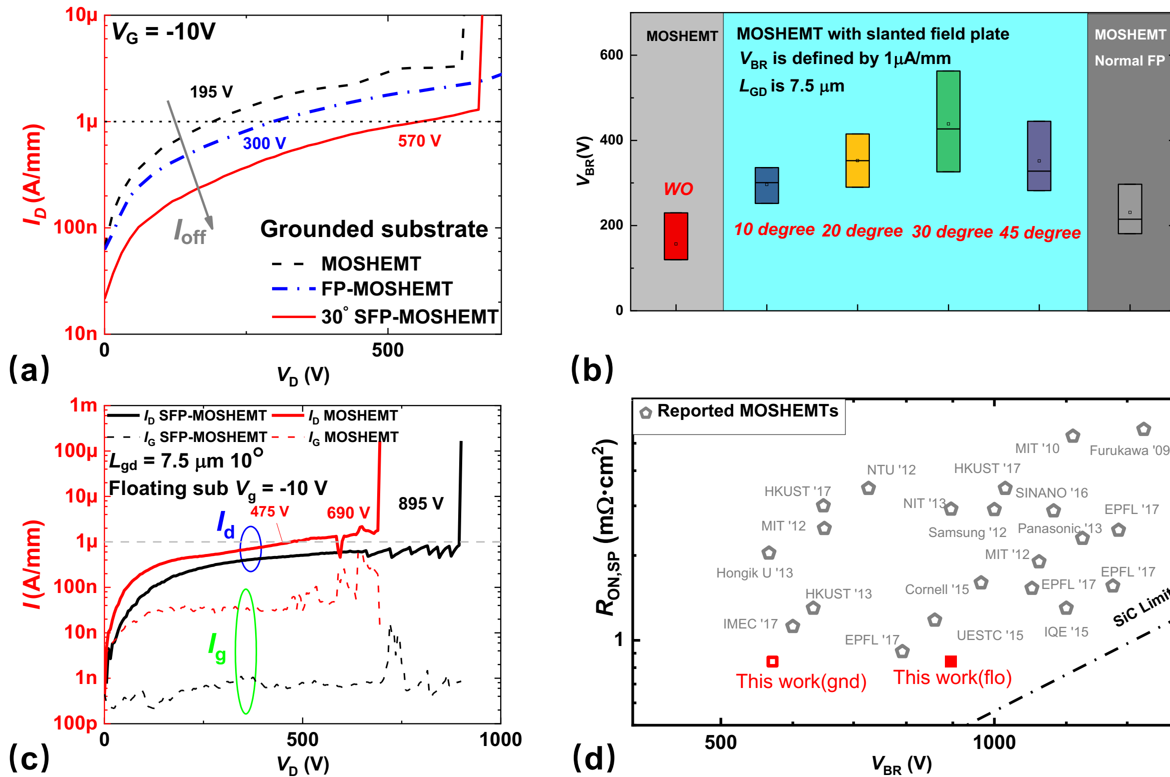

Figure 2-7 (a) Grounded substrate breakdown behavior comparison. (b) Breakdown voltage distribution of the different angles of field plate. (c) Floating substrate breakdown behavior comparison. (d) Benchmark FOM with state-of-the-art MOSHEMT (both floating substrate (flo) and grounded substrate(gnd)).

Figure 2-7 (a) shows the breakdown characteristics of the S-FP MOSHEMT tested on grounded substrate compared to MOSHEMTs with and without a single planar field-plate (90° FOX FP). Compared to MOSHEMTs without FP, the V_{BR} shows a ~ 3 X increase to 570 V (defined by 1 μA /mm). This was achieved with a small L_{GD} of 7.5 μm. Figure 2-7 (b) statistical test of different angles of the S-FP device, the 30 device shows the maximum breakdown voltage. When the device is tested on a floating substrate. The V_{BR} of S- FP MOSHEMT is 832 V at 1 μA/mm with grounded substrate (V_G = -10 V), which improves significantly compared to the reference MOSHEMT without field-plate (Figure 2-7 (c)). Such improvement in V_{BR} is attributed to the more uniform electric field distribution under S-FP. S-FP also results in a very low gate leakage current of only about 11.3 pA/mm even at 900 V when the transistor is in the off-state. When we compare S-FP MOSHEMT with other literature results, this leads to the most advanced FOM result of the S-FP device (Figure 2-7 (d)).

2.4 Conclusion

A novel S-FP technology has been demonstrated, which uses grayscale e-beam lithography. This technology reduces the process complexity and drastically improves the electric field uniformity along the channel. The S-FP structure was created in a single step. The slanted structure is sharp and adjustable. The angle of S-FP can be easily adjusted from the layout design, not during the process,

making it very flexible and beneficial for future high-end power electronics applications. The optimized 30-degree S-FP MOSHEMT exhibited a low R_{ON} of 4.5 Ω·mm while maintaining a high V_{BR} of 832 V. This result demonstrates the significant potential of S-FP technology for GaN power devices.

Chapter 3 LiNiO gate oxide for enhancement-mode tri-gate MOSHEMTs

3.1 Introduction

As demonstrated in the previous chapter, the S-FP technology brings forth better V_{BR} and successfully improves device FOM. Also, a field-plate technology with arbitrary slanted angle is presented for the first time. It opens many opportunities for precise electric field design in lateral GaN devices in the future to achieve uniform electric field distribution throughout the device and chip.

However, the S-FP structure requires much vertical space and special processes, which are not suitable for the integration of GaN power transistors. In addition to the S-FP structure, a tri-gate nanowire structure has already been developed enabling better electric field uniformity through a simple process and structure. Tri-gate MOSHEMTs contain a nanowire region in the gate, and the gate oxide conformally covers the entire fin. The gate metal extends over the fin to form an integrated gate field-plate. The three-sided gate control in the gate region and the built-in gate field plate ensures uniform distribution of the electric field in the channel and reduce leakage. Apart from the high V_{BR}, the optimization of the fin geometry results in no degradation of the R_{ON} by the tri-gate structure.

3.1.1 Tri-gate technology.

The tri-gate structure has been largely proven to have superior gate control capability. Starting at the 22 nm node, Intel begins to use the tri-gate FinFET structure in its processors to improve subthreshold swing (*SS*) [54]. Thanks to the introduction of the tri-gate FinFET, both power consumption and performance have been significantly improved. Due to the much lower leakage current, "there is a 37% power increase at low voltage compared to the previous 32 nm node and a 50% power reduction at the same power," according to Intel (Figure 3-1) [55]. In GaN power transistors, the tri-gate structure has shown excellent high power FOM due to the uniform distribution of the electric field. The first GaN power device with tri-gate structure was

developed by Dr. Bin Lu and Prof. Elison Matioli at MIT [56]. The configuration of the tri-gate GaN power transistor is different from the FinFET structure of the Si logic device, which is entirely built on a Si cell. The tri-gate GaN power transistor has only nanostructure under the gate region. The drift region of the tri-gate GaN power device is still a planar structure to ensure good on-state performance.

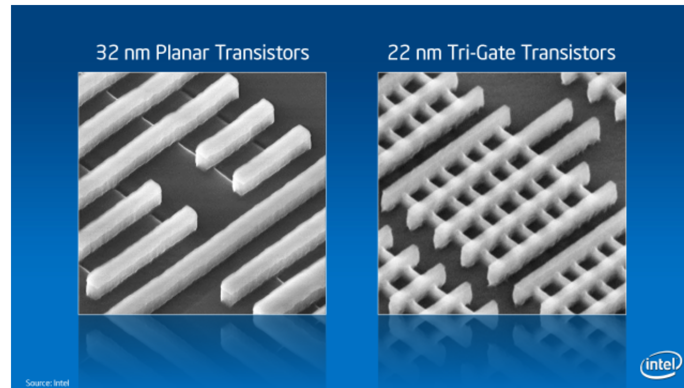

Figure 3-1 Intel's first generation 22 nm manufacturing process tri-gate FinFET structure compare with 32 nm node planar structure [54].

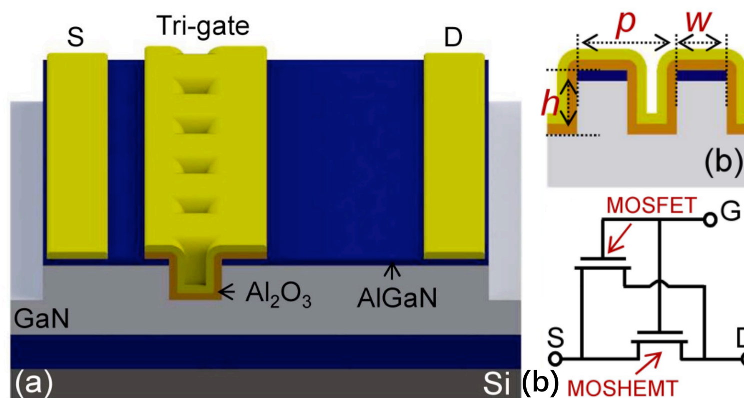

Figure 3-2 (a) Schematic of tri-gate transistor, (b) cross-section schematic of tri-gate nanowire region, (c) equivalent circuit of tri-gate structure [14].

Compared with the planar GaN power transistor, the tri-gate GaN power transistor mainly has the following advantages:

Much improved gate control: the tri-gate structure can effectively increase the gate capacitance, resulting in a near-ideal SS and much higher G_m [14, 57].

Tunable V_{TH}: When the tri-gate fin width decreases, the voltage in the heterostructure can be relaxed in the tri-gate region. Good on-state performance and positive V_{TH} can be achieved simultaneously [57, 58].

Breakthrough FOM for high performance: This is the most appealing advantage of the tri-gate structure in contrast to vertical MOSFET or IGBT structures based on Si or SiC. The use of heterostructures leads to a non-uniform distribution of the electric field along the drift region and to peaks at the gate and drain edges. This limits the V_{BR} of GaN device, making the V_{BR} of the transistor far from the material limit. Especially on GaN-on-Si substrates, the additional leakage through the buffer also leads to early breakdown [42, 59]. Traditionally, the solution for early breakdown is to use a gate FP and a source FP to modulate the electric field distribution along the channel. However, this requires multilayer metallization and precise control of the oxide thickness between layers, which makes the process much more complicated. The electric field can be uniformly distributed along the channel direction by a tri-gate structure and a further optimized oblique tri-gate structure. The V_{BR} of the device with a beveled tri-gate structure has already reached the buffer limit of the GaN-on-Si substrate and a V_{BR} of over 1200 V [60].

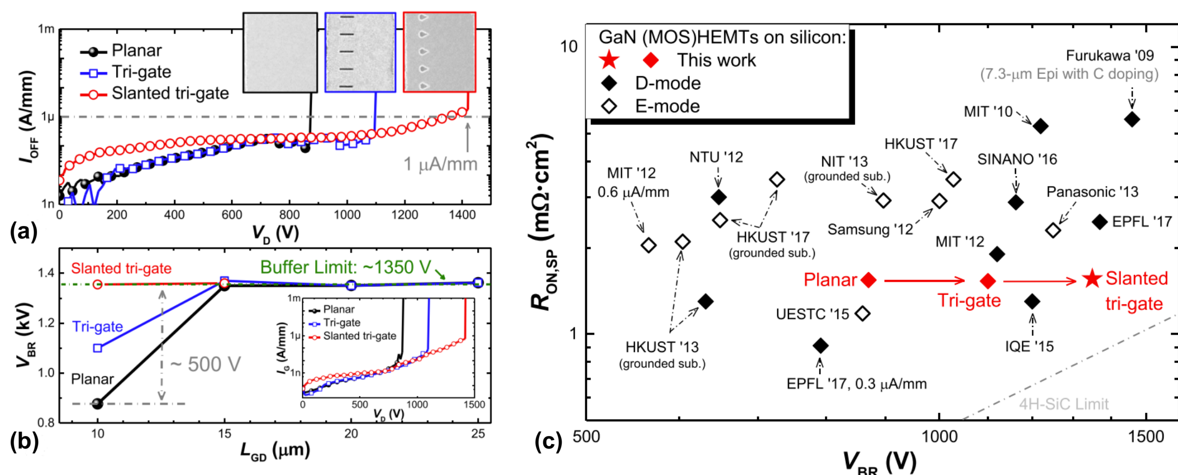

Figure 3-3 (a) Typical breakdown characteristics of MOSHEMTs with planar gates, tri-gates and slanted tri-gates and (b) their L_{GD}-dependent V_{BR} (at 1 µA/mm), measured at V_G of −10 V with a floating substrate, in which the I_{OFF} for all devices was normalized by their footprint width [60].

Better heat dissipation: GaN devices also struggle with self-heating and thermal instabilities. This significantly weakens the performance and reliability of GaN power devices. By using a tri-gate structure, improved thermal performance has been demonstrated [61]. The larger surface area of the nanowire architecture leads to lower channel temperatures compared to normal planar devices.

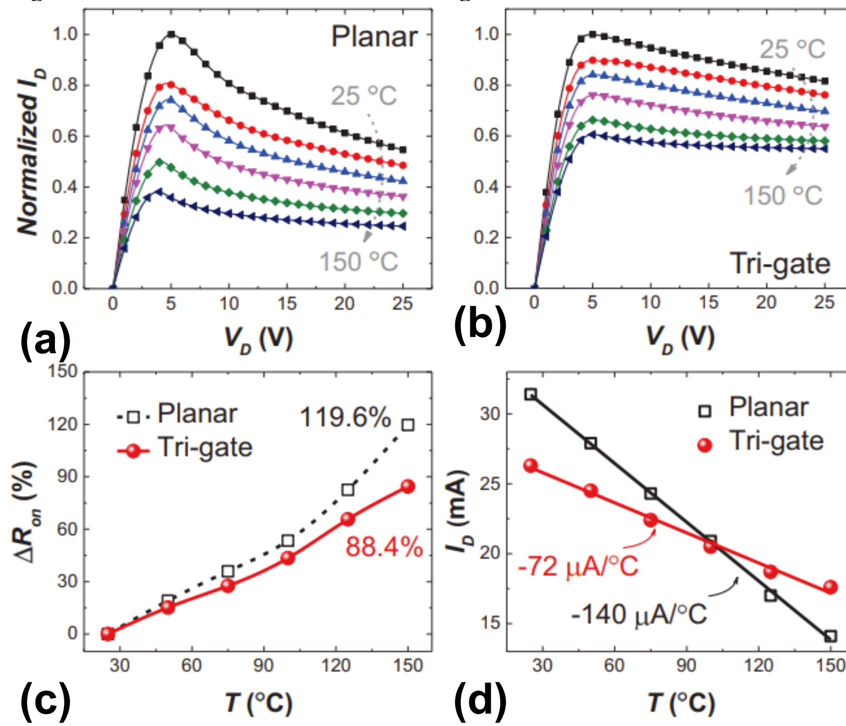

Figure 3-4 Temperature-dependent I_D-V_D characteristics of the (a) planar and (b) Tri-gate HEMTs under similar gate driving voltage; (c) degradation in on-resistance (ΔR_{ON}) versus temperature; (d) I_D of the HEMTs versus temperature at V_D = 25 V [61].

The tri-gate structure is an excellent solution for high-performance lateral HEMT. However, achieving e-mode operation with the tri-gate structure. When the tri-gate fin width decreases, the stress in the junction can relax, partially depleting the 2DEG carriers. However, log-scale e-mode operation solely based on this effect is very difficult to achieve. For a Ni gate, a fin of 15 nm is required to achieve e-mode, which requires high resolution lithography.

The tri-gate structure is an excellent solution for high-performance lateral HEMT. However, achieving e-mode operation on the tri-gate structure is not easy. When the tri-gate fin width scales down, the strain in the barrier layer can be relaxed, and the 2DEG carrier will be partially depleted. However, log-scale e-mode operation based on this effect is very hard to achieve. With Ni gate, W_{Fin} of 15 nm is needed to achieve e-mode, which need high-resolution lithography process.

Existing e-mode GaN transistor products are based on a p-GaN gate or cascode, and there is no report that other widely studied methods such as F-implantation or gate recessing have ever been seriously considered by GaN foundry companies (Table 3-1).

Reliability is another problem with power electronic devices. The much harsher operating conditions (e.g., under high voltage, high operating temperature, high operating frequency, and a

long system replacement cycle) compared to normal logic/memory devices have led to a stringent qualification standard for reliability testing [15]. There are many innovative techniques in GaN lateral devices, but they have limited practicality given the reliability (charge trap gate, recess-gate). The motivation for the work in this chapter is to take full advantage of the high-performance tri-gate structure while developing a novel solution instead of p-GaN to demonstrate e-mode operation with a simple process flow and achieve reliable operation.

Table 3-1 Comparison recent commercial GaN devices [62].

Manufacturer	Year	Device code	Technology
EPC	2016	EPC2040	p-GaN gate gen 4
EPC	2019	EPC2024	p-GaN gate gen 4
EPC	2019	EPC2214	p-GaN gate gen 4
TI	2017	LMG5200	EPC p-GaN gate
GaN Systems	2015	GS61004B	p-GaN gate
Infineon	2018	IGT40R070D1	CoolGaN GIT
Infineon	2018	IGOT60R070D1	CoolGaN GIT
Panasonic	2017	PGA26E19BA	GIT
TI	2016	LMG3410R070	Thin p-AlGaN barrier
Transphorm	2015	NTP8G206NG	Cascode gen 1
Transphorm	2016	TPH3208PS	Cascode gen 2
Transphorm	2017	TP90H180PS	Cascode gen 3
Transphorm	2020	TP65H035G4WS	Cascode gen 4
GaN Systems	2015	GS66504B	p-GaN gate
Navitas	2018	NV6115	PowerIC
Nexperia	2020	GAN06365WSA	Nexperia’ s H1(cascode)
Innoscience	2020	INN650D02	p-GaN gate
PI	2018	SC1923C	Innoswitch-Pro(cascode)

In this chapter, we propose a tri-gate e-mode transistor using p-type LiNiO as a heterojunction gate and present comprehensive discussion of the process and characterization of the device.

3.2 Motivation

GaN HEMTs offer excellent performance for next generation power electronic devices [63]. However, to meet the requirements of fail-safe operation and simplify the gate driver circuit design, an enhancement-mode device is required. Among the existing solutions, p-GaN gates are mostly used as e-mode GaN HEMTs due to their high reliability and stability [64]. However, to successfully achieve low R_{ON} e-mode operation, p-GaN technology requires a unique process

involving thin barrier epitaxy, selective etching of the p-GaN layer, and sometimes barrier or p-GaN regrowth [64]. This makes the process costly and complex and results in poorer performance compared to other technologies, such as recess-gate [4, 34, 65]. An alternative approach to normal p-GaN or recess-gates is the gate stack technique. Positive V_{TH} can be achieved by using a charge-trap gate stack [66] or a negatively charged dielectric [67]. However, there are some concerns, including their thermal instability, the need for initialization procedures [66], and V_{TH} instability under gate bias stress [66], which hinder the use of such technologies in power electronics.

Intrinsic p-type transition metal oxides provide another option for developing gate stacks to achieve e-mode operation. In particular, NiO_x is a promising candidate due to its high hole concentration [68-71]. However, in the reported results of NiO_x MOSHEMTs for e-mode operation, gate recess [68, 69, 71] or high sheet resistance (R_S) epitaxy [70] have to be used together with NiO_x to achieve e-mode operation. These additional requirements limit the device performance in the on-state (R_{ON} and $I_{ON,\,max}$). Moreover, the presence of Ni vacancies in NiO_x leads to instability in the long term and/or during high-temperature operation, which drastically affects the electronic properties of the NiO_x dielectric [72] and limits its application for power electronics.

To achieve e-mode operation without compromising device performance, an alternative approach focuses on the tri-gate structure [14, 56, 60, 73, 74]. By reducing the W_{Fin} in conjunction with the gate stack engineering, positive V_{TH}, low R_{ON}, and high V_{BR} could be achieved simultaneously [56]. In this chapter, we demonstrate high quality LiNiO gate oxide as an alternative material to enable e-mode operation in a tri-gate structure. Due to the lower offset between LiNiO and AlGaN (Ev of 1.99 eV instead of 2.53 eV, Ec of 1.26 eV instead of 2.88 eV [70]), a larger lifting of the conduction band in the GaN channel near the AlGaN/GaN interface can be achieved. This smaller band offset leads to a much lower carrier density in 2DEG and thus a more significant V_{TH} shift. LiNiO films with high hole concentration have also been reported [75, 76]. LiNiO conformally deposited over tri-gates facilitates W_{Fin} requirements to achieve e-mode operation, along with low R_{ON} and high V_{BR}, along with excellent reliability performance and interfacial quality.

3.3 Existing enhancement-mode tri-gate (MOS)HEMT

3.3.1 E-mode operation by structure engineering

Tri-gate FinFET or nanowire devices present a very high on/off ratio, low *SS*, and high power FOM [56]. E-mode operation can be reached solely on fin geometry engineering, which utilize tri-gate strain relaxation of the barrier layer on sidewall depletion to pinch-off channel. The process and structure is simple, but W_{Fin} must be below 30 nm [80] from simulation prediction for log scale e-mode operation (I_D = 1μA/mm). To achieve e-mode based on tri-gate structure, several works on structure or material engineering have been explored.

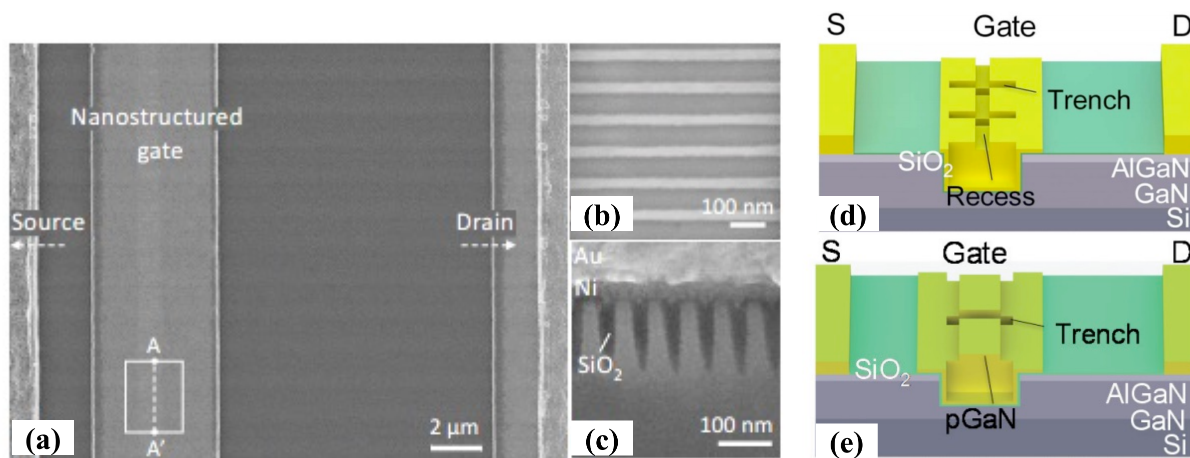

Figure 3-5 Achieving e-mode operation by high work function metal: (a) Top-view image of device access region and the gate region is highlighted. The fin is covered with 25 nm ALD SiO_2, with Pt/Au as gate metal. (b) Zoomed SEM image of the nanowire region before gate oxide deposition. (c) FIB cross-section of the gate nanowires along the AA' line. The fins are covered only by 20 nm ALD SiO_2, on top of which Ni-Au or Pt-Au gate stacks were deposited [58]. Recess-gate: (d) 3D schematic of recessed tri-gate MOSHEMT [77, 78]. P-GaN: (e) Schematic of fabricated p-GaN MOS tri-gate MOSHEMT [79].

High work-function gate metal (Figure 3-5 (a)): Through replacement of Ni with Pt gate, a ~0.8 V positive V_{TH} shift can be achieved. The largest W_{Fin} for achieving e-mode operation was increased from ~15 nm to 35 nm, which is much easier to achieve in fabrication. The maximum V_{TH} (defined by 1 μA/mm) from this technology is 0.6 V. Devices present large current density (I_D) up to 590 mA/mm, small $R_{ON,SP}$ of 1.33 mΩ·cm^2, large on/off ratio above 10^{10}, and V_{BR} of 1080 V (at 1 μA/mm with a grounded substrate). The potential issue of this technology is the limitation of the possibility of maximum V_{TH}. The V_{TH} of device with W_{fin} of 20 nm is 0.65 V, further improve V_{TH} based on W_{Fin} scaling would be very challenging [58].

Recess-gate tri-gate structure (Figure 3-5 (b)): the first e-mode tri-gate device was based on this configuration to demonstrate normally-off operation [56]. The difference between the recess-

gate tri-gate structure with the normal planar recess-gate structure is the recess region in the tri-gate device was at submicron scale. With this method, a very low R_{ON} can be achieved together with high V_{TH} from an optimized device design and process [77, 78]. A very high V_{TH} (defined by 1 μA/mm) of 1.4 V was achieved with 200 nm wide fin, along with a $R_{ON, SP}$ of 1.76 mΩ·cm^2, and V_{BR} of 1650 V at 1 μA/mm (floating substrate). The usage of a small-scale of recess-gate in the tri-gate structure results in a large V_{TH} and high-performance on a normal AlGaN barrier thickness. Moreover, the V_{TH} distribution is much uniform over the planar recess-gate device due to the combination use of tri-gate and recess-gate. The issue of this device structure is the combination of the process difficulties of both tri-gate and recess-gate. It requires precise dry etching control during recess process. The large etch surface and SiO_2 may create the reliability issues in structure [30, 81, 82].

P-GaN tri-gate structure (Figure 3-5 (c)): using p-GaN to achieve e-mode operation is a performance-proof method. The issues p-GaN e-mode device facing is the increase of R_{ON} due to the use of a thinner barrier and cannot bias at large V_G. To present a good performance on p-GaN e-mode device, a short p-GaN region and a thick barrier are desired. However, this would lead to difficulty in achieving e-mode operation. P-GaN, tri-gate, and MOS gate structure have been combined together to overcome the trade-off between e-mode operation and performance [79]. P-GaN was used to lift off conduction band of GaN, while the MOS structure was used to achieve high-performance by strong channel coupling with the gate. In this structure, high-performance was achieved on a thick barrier, which is difficult on a planar p-GaN gate device. On a 200 nm wide fin device, a maximum V_{TH} of 0.9 V can be achieved, together with good R_{ON} and V_{BR}. The issue of this design is also obvious, it requires p-GaN etching, which results in plasma damage drift region surface. And the combination of p-GaN, MOS, and tri-gate structure leds to a very complex design, all the reliability and process issues from these three technologies valid at the same time in this design.

3.3.2 E-mode operation by gate stack engineering

Apart from tri-gate structure engineering to achieve e-mode, gate stack engineering is a promising way due to its simplicity in the design and process. Several works based on different mechanism has been proposed.

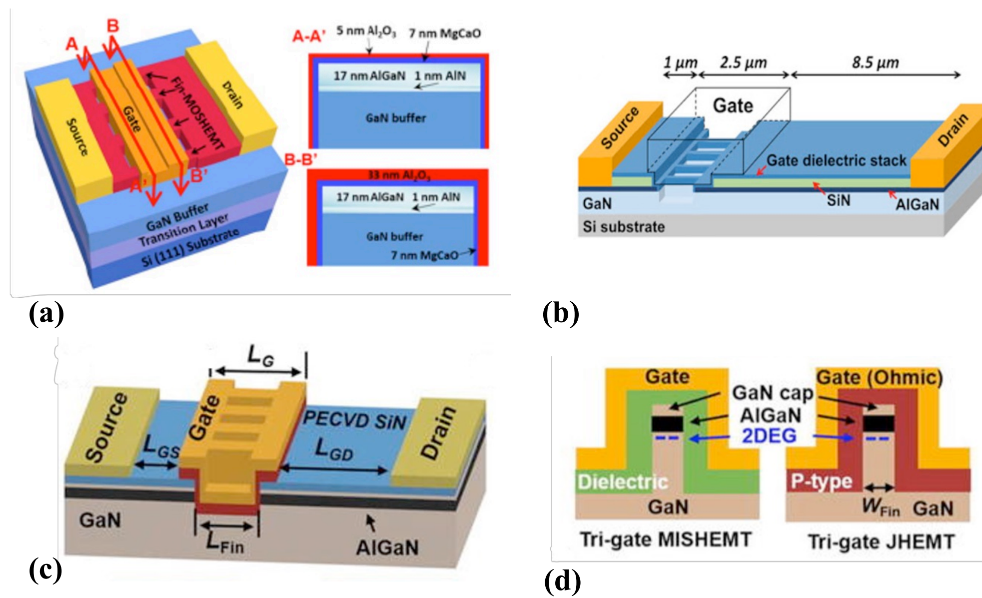

Figure 3-6 (a) Schematic of GaN fin-MOSHEMT with atomic layer epitaxy MgCaO gate dielectric [67]. (b) Schematic cross-section of GaN tri-gate device with hybrid ferroelectric charge trap gate stack: $HfZrO_4$/HfON [83]. (c) and (d) 3D schematic of a tri-gate GaN junction HEMT using NiO_x as a p-type gate material. (b) Fin cross-section view of MIS tri-gate (left) and a junction tri-gate (right) [70].

In atomic layer epitaxy (ALE) MgCaO (Figure 3-6 (a)), there are large amount of built-in negative charges [67]. Combined with the tri-gate structure, the electron in the channel can be further depleted, resulting in a positive V_{TH}. A high-performance e-mode GaN MOSHEMT with V_{TH} = 0 V through dielectric charge engineering. The net negative charge density of the MgCaO layer is roughly estimated to be 4.9×10^{12} cm^{-2} The negative charge density of MgCaO film is roughly estimated to be 4.9×10^{12} cm^{-2}. Through X-ray diffraction (XRD) characterization, a small 3% lattice mismatch between MgCaO and barrier layer was observed. The single crystalline MgCaO guarantees good quality. The device presents a very small hysteresis of 30 mV, high on/off ratio over 10^{11}. This shows the excellent gate oxide quality and good gate control. Moreover, the on-current of this device is also quite large; the maximum I_{ON} is 670 mA/mm [67].

Ferroelectric gate stack (Figure 3-6 (b)): hafnium oxynitride (HfON) ferroelectric layer in the gate stack was designed to trap charges, which can positively shift the V_{TH} [83]. By using a high Al content barrier, the device presents a very small R_{ON} of 5 Ω·mm together with V_{BR} of 788 V

(defined at I_D = 1 μA/mm). Through trapped charges in the HfON layer, a very high V_{TH} of 2.61 V was achieved. However, to achieve e-mode operation, this device requires an initialization process to charge the HfON layer, which requires 1 ms to finish the initialization process. The initialization causes a polarization in the $HfZrO_4$ layer and electron trapped in the HfON layer. The ferroelectricity of $HfZrO_4$ can increase the trapped charge in the HfON layer, thus, a much higher V_{TH} can be achieved over normal trap gate. This fundamentally limits the application of the device, the device in d-mode or e-mode cannot be known due to the unclear amount of trapped charges in the gate layer. Moreover, the use of ferroelectric material limit the high temperature and long-term stress performance of the device. The operation mechanism of this device is fundamentally not suitable for power device application.

Junction gate is another way to achieve e-mode operation. NiO_x junction tri-gate device was developed, which can further lift the conduction band of GaN and deplete the charges in the channel. The device design included a p-type sputtered NiO layer of hole concentration of 5 × 10^{19}cm^{-3}. The device was fabricated on a high R_S substrate of 480 Ω/sqr. The maximum V_{TH} in this work was around 1.1 V, a near-ideal *SS* of 63 mV/dec, high V_{BR} over 600 V. But the on-resistance of this device was only over 9.4 Ω·mm to 17 Ω·mm due to the large fin-to-fin distance and high R_S epitaxy. Moreover, the device presented a very good high-temperature performance, which cannot be demonstrated on normal MOSHEMT or other gate engineering methods. This work disclosed the great potential of junction gate combined with a tri-gate structure to achieve high-performance, stable operation, and simple process device design [70].

Demonstrate e-mode operation on tri-gate by gate stack engineering can demonstrate a much larger V_{TH} over planar device due to the better gate control and stronger barrier strain relaxation in tri-gate structure. Through optimized tri-gate geometry design, the on-state performance is not sacrificed, and a better voltage blocking ability was presented.

However, the device based on trap charge is not suitable for power application, and the potential reliability issue cannot be overcome due to its trapping-detrapping operation mechanism. The junction type gate is another kind of solution; however, the proposed NiO_x junction tri-gate device performs worse than state-of-the-art results. In addition, the low deposition sputter NiO_X rely on Ni vacancy to achieve p-type, which is also an unstable material for long-term operation,

3.4 LiNiO: a promising candidate for p-type gate of lateral GaN transistors

NiO is the first known p-type transparent oxide semiconductors (TOS). It has been widely adopted in ultraviolet (UV) photodetectors, transparent thin-film-transistor (TFT), and hole-transporting layer (HTL) in organic solar cells.

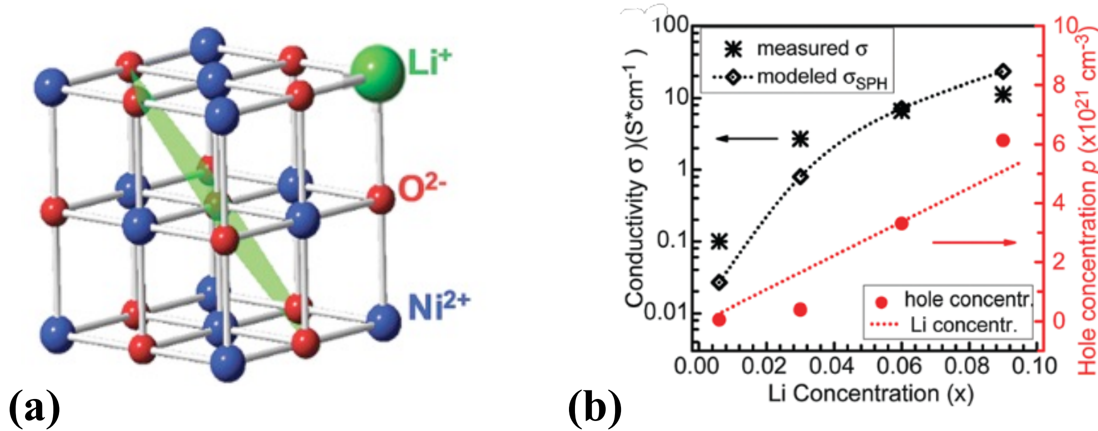

Figure 3-7 Epitaxial growth of $Li_xNi_{1-x}O$ thin films on MgO (001). (a) Crystal structure of doped NiO with Li at Ni atom site. (b) From the combination of Seebeck measurements and film conductivity to get mobility and carrier concentrations [75].

The Ni vacancies in NiO film result in its p-type conduction. Under oxygen-rich deposition environment, Ni vacancies have lower formation energy over oxygen vacancies. Apart from relying on Ni vacancy to achieve p-type, Li doped NiO has been developed with a very high hole concentration over 10^{21} cm^{-3} and it is a stoichiometric material at a stable state. The mon-ovalent Li^+ ion replaces the Ni^{2+} leds to a hole state at this site to maintain the charge neutrality. This is a more controllable way to achieve p-type film since the doping Li can be precisely controlled, which cannot be achieved in NiO_X film. There are mainly two category (Li)NiO materials, polycrystalline (Li)NiO thin films by sputter, thermal oxidation, or sol-gel spin-on method. The (Li)NiO film from this method presents a relatively high mobility over 5 $cm^2 \cdot V^{-1} \cdot s^{-1}$ which is a reasonable value for TOS material. And there is another kind of (Li)NiO that exhibits much lower hole mobility (< 0.1 $cm^2 \cdot V^{-1} \cdot s^{-1}$), which is mostly single crystalline (Li)NiO [75]. In this work, we use pulse laser deposition (PLD) Li-doped NiO to form a junction gate. PLD is a method that precisely controls the film deposition condition, doping concentration, atomic-level precision, and without organic pollution. The single crystalline (Li)NiO has much fewer defects and grain boundaries. This is not only good for film quality and properties uniformity but also beneficial for GaN power transistor's long-term reliability.

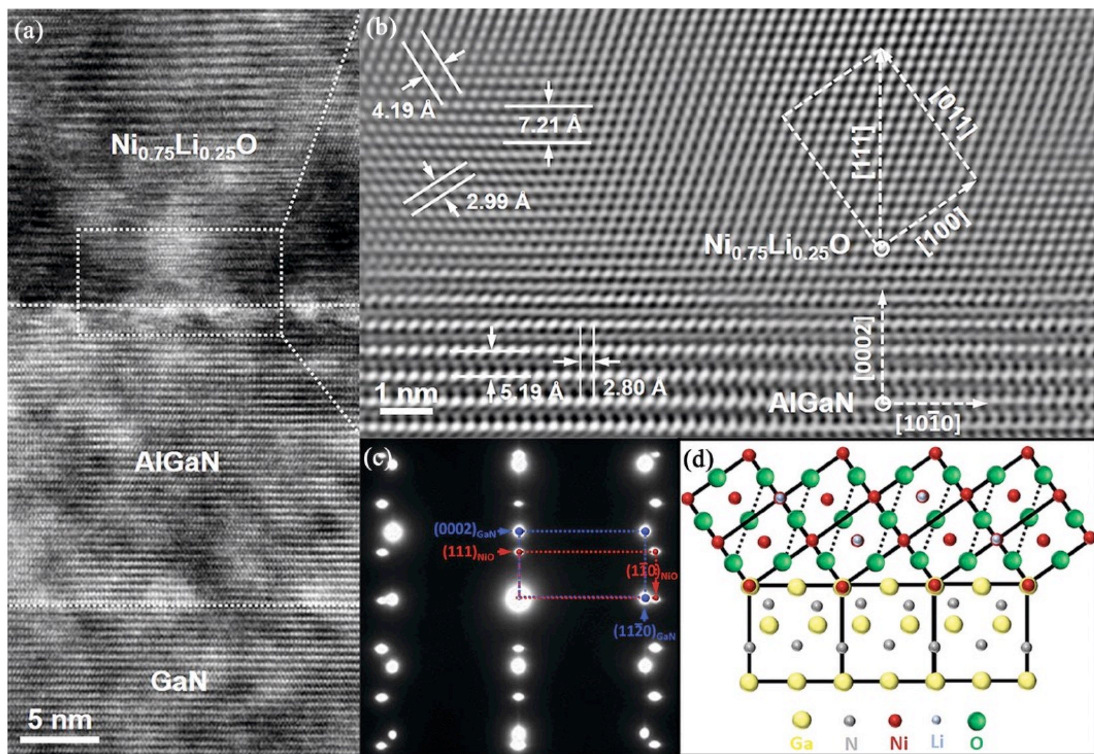

Figure 3-8 Sectional HRTEM images of the (a) $Li_{0.25}Ni_{0.75}O$/AlGaN/GaN heterostructure and the (b) $Li_{0.25}Ni_{0.75}O$ /AlGaN interface. (c) SAED pattern detected at the $Li_{0.25}Ni_{0.75}O$ /AlGaN/GaN interface. (d) Schematic diagram for the out-of-plane atomic epitaxy matching model of the $Li_xNi_{1-x}O$/AlGaN/GaN heterostructure [76].

NiO crystallizes in rock-salted structure. Through in-situ RHEED monitoring, an epitaxial relationship of $Ni_{1-X}Li_XO$/AlGaN/GaN is concluded to be $(111)\left[1\bar{1}0\right]\mathrm{Ni}_{1-x}\mathrm{Li}_x\mathrm{O}//(0002)\left[11\bar{2}0\right]$, HRTEM technique also be used to characterize the epitaxial relationship Figure 3-8. A clear atomic level clean interface can be seen, which is the guarantee of good device quality. The LiNiO film was deposited by the PLD method, a sharp interface was observed without any atom diffusion or reaction. Through crystal planes calibration by calculating the average lattice spacings. $(111)\left[1\bar{1}0\right]\mathrm{Ni}_{1-x}\mathrm{Li}_x\mathrm{O}//(0002)\left[11\bar{2}0\right]$, epitaxial relationship could be further confirmed. Figure 3-8 (c) shows the selected area electron diffraction (SAED) pattern detected at LiNiO/AlGaN interface and aligned to the $\left[11\bar{2}0\right]$ crystal orientation. Figure 3-8 (d) shows the schematic diagram of the out-of-plane atomic epitaxy model between LiNiO and AlGaN [76].

3.5 Process of LiNiO junction gate tri-gate device

3.5.1 Etching properties of (Li)NiO

(Li)NiO is a kind of transition-metal oxides (TMOs) that is a critical material in novel nonvolatile memory development [84, 85] which is mainly used as magnetic memory (MRAM) [86] and resistive random-access memory (RRAM) [87, 88]. A general problem of TMOs is they are inert in dry etching and wet etching. Nearly every normal acid (hot 98% HNO_3, 37% HCl, 49% HF, CH_3COOH) cannot attack PLD deposition (Li)NiO in our experiments. To achieve precisely patterned and high-density devices, selective dry etching is the ideal method. As shown in Table 3-2 the physical properties of different Ni by-product compounds during etching have a very high melting point. Conventional Ar ion beam etching (IBE) is not suitable for lacking etching stop layer (ESL) and redeposition issue [84]. During the development of next-generation memory, the reactive ion etching (RIE) method of (Li)NiO etching was developed. Different etching gas and pressure has been discussed [85] based on CHF_3 etcher, carbonyl compounds such as $Ni(CO)_4$ was considered as the only possible by-product for selection of etching gas to achieve dry etching of (Li)NiO. SanDisk and Samsung have patents related to this [89, 90]. A carbon-based etcher (CF_4, CHF_3) RIE can achieve dry etching on (Li)NiO. But in our GaN transistor application, a perfect AlGaN surface is needed to have high-performance and good reliability. However, using RIE process is difficult to result in undamaged AlGaN surface. Several process flow of LiNiO junction gate transistor was explored in Figure 3-9.

Table 3-2 Physical properties of various nickel compounds [84].

	Melting point (°C)	Boiling point (°C)	Heat of formation ($\Delta_f H^{\circ}$/kJ mol^{-1})
$NiCl_2$	1009	Sublimes	-305.3
NiF_2	1474	-	-651.4
$NiBr_2$	963	Sublimes	-212.1
Ni_3B	1156	-	-
NiB	1053	-	-
Ni_2B	1125	-	-
NiI_2	780	Sublimes	-78.2
$Ni(CO)_4$	-19.3	43	-
$NiCO_3$	-	-	-
$Ni(OH)_2$	230 decompose	-	-529.7
NiO	1955	-	-
Ni_2O_3	600 decompose	-	-489.5

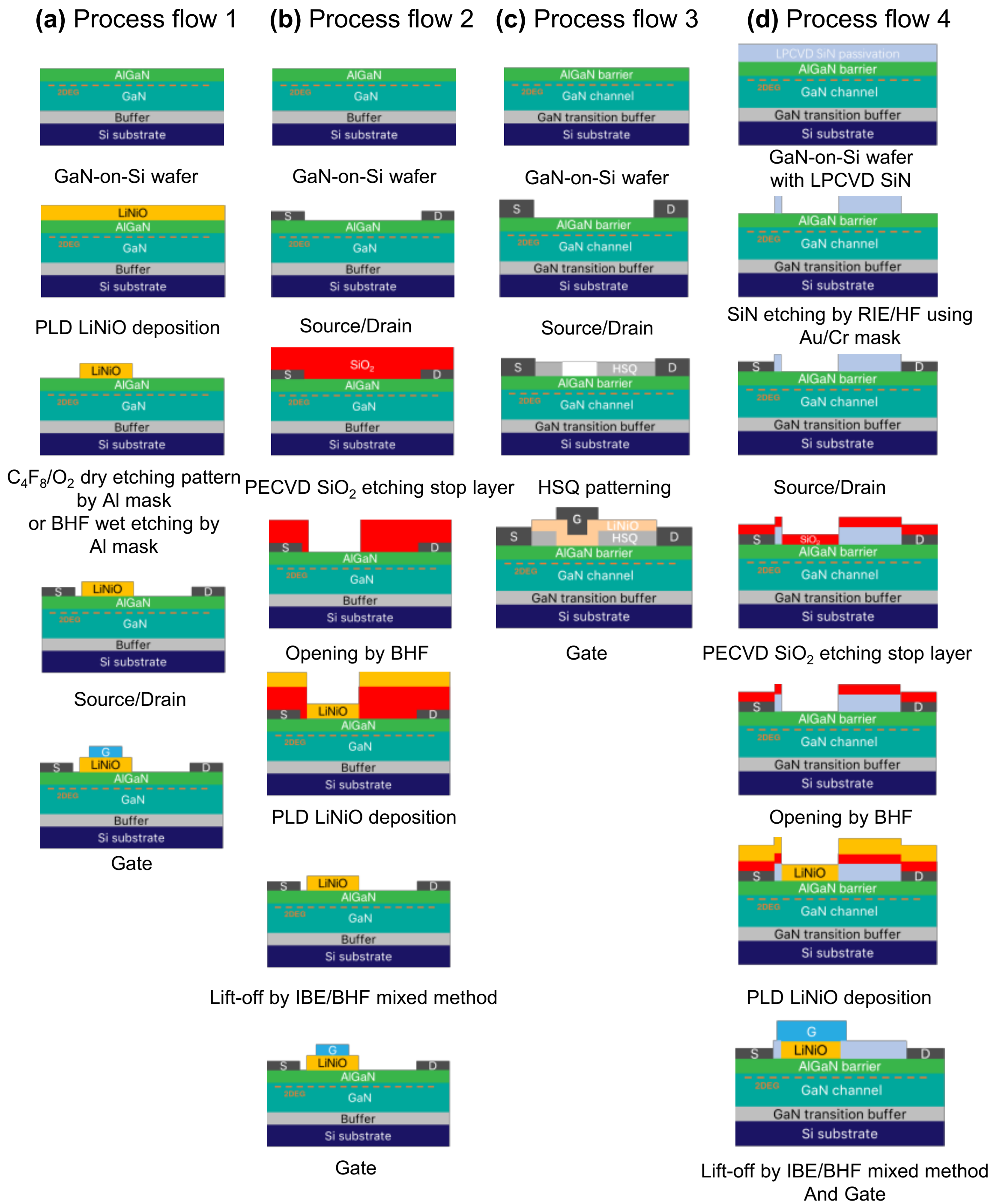

Figure 3-9 Different process flow of LiNiO gate device: (a) direct dry etching of LiNiO using IBE etching or carbon/oxygen-based recipe. (b) LiNiO patterning by oxide lift-off method. (c) LiNiO patterning by HSQ lift-off method. (d) LiNiO patterning and passivation by SiN mixed etching method.

3.5.2 Process of LiNiO deposition, patterning, and integration with tri-gate structure

The LiNiO gate oxide tri-gate MOSHEMTs were fabricated on a GaN-on-Si wafer with a 5 μm-thick buffer and a 25 nm-thick $Al_{0.25}Ga_{0.75}N$ barrier. The device fabrication started with mesa isolation and definition of the tri-gate region by ebeam lithography, followed by inductively coupled plasma (ICP) etching with a depth of 180 nm (Ar/Cl_2). Source and drain ohmic contacts were formed by alloying a Ti/Al/Ti/Ni/Au stack. A 200 nm thick SiO_2 was deposited by plasma-enhanced chemical vapor deposition (PECVD) as the etching stop layer (ESL) and lift-off mask for the LiNiO. The gate region opening was done by buffered hydrofluoric acid (BHF). The LiNiO target was fabricated by solid-state sintering of lithium carbonate (Li_2CO_3) and nickel oxide (NiO) with a 25 % atomic percentage of lithium ($Li_{0.25}Ni_{0.75}O$). PLD deposition was performed by laser ablation with a repetition rate at 5 Hz and energy density of 400 $mJ \cdot cm^{-2}$ with a 248 nm KrF laser [75]. The deposition temperature was 400 ºC, and the oxygen partial pressure was 0.1 Torr. In solemates SMP 800 PLD, the gas flow are: Ar of 30 sccm, O_2 of 30 sccm. Due to the temperature and sample facing down configuration during the deposition, normal kapton tape cannot be used. A 1.5 mm thick Si chip holder was fabricated to support the sample during deposition. Pd/Au was deposited as gate metal. Ion beam etching and BHF etching were used to remove the ESL layer. A 25 nm-thick ALD SiO_2 dielectric was deposited as gate dielectric on reference devices on the same chip.

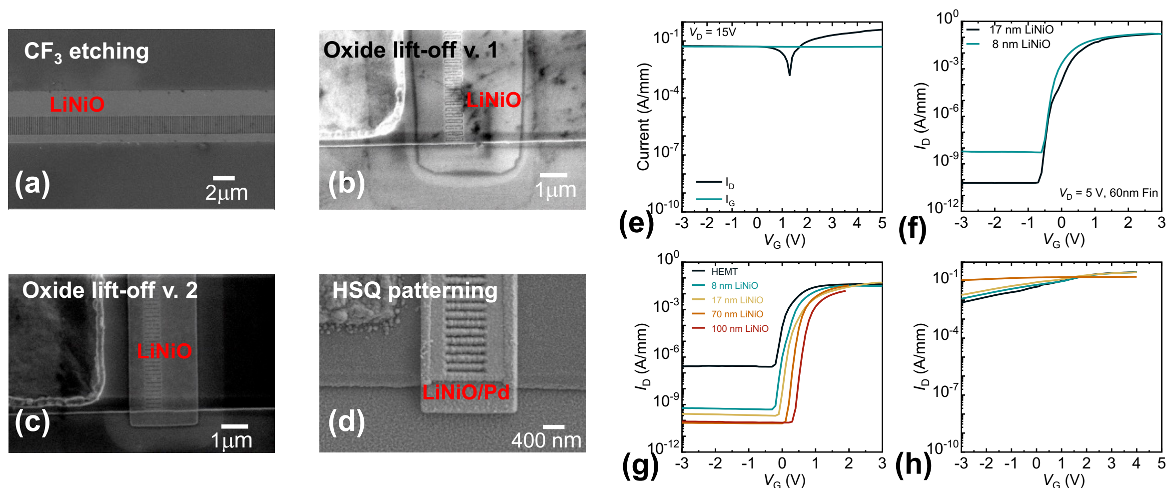

Figure 3-10 (a) SEM image of gate region after LiNiO etching by carbon/oxygen method. (b) SEM image of gate region after LiNiO etching by oxide lift-off method with CHF_3 during the opening. (c) SEM image of gate region after LiNiO etching by oxide lift-off method with IBE during the opening. (d) SEM image of gate region after LiNiO etching by HSQ lift-off method. (e) transfer performance of the device by carbon/oxygen method. (f) transfer performance of the device by oxide lift-off method (CHF_3 RIE based). (g) transfer performance of the device by oxide lift-off method (IBE-based) (h) transfer performance of the device by HSQ lift-off method.

Several processes are evaluated to explore the possibility of different process flows:

Direct dry etch of LiNiO: As shown in Figure 3-9 (a) and Figure 3-10 (a)(e), to utilize the high quality PLD process, there should be no exposed metal on the chip. The LiNiO is deposited immediately after the formation of the tri-gate structure and isolation. After PLD deposition, the LiNiO is patterned by etching with CHF_3 (ICP RIE). During RIE etching, Al is used as a metal mask. However, the CHF_3/O_2 recipe can also attack the AlGaN during etching, and there is no end-point detection (EPD) or etch stop layer (ESL). The etch depth can only be controlled by stepwise EDX examination or from reference chip. Based on the transfer behavior of the finished device, there was no gate control of device fabricated in this process.

Lift-off of LiNiO by PECVD SiO2 mask: Figure 3-9 (b) and Figure 3-10 (b)(c)(f)(g) show the detailed process described previously. The core concept of this process is that thick PECVD SiO_2 functions as a high temperature lift-off mask. The opening of SiO_2 for the deposition of LiNiO is achieved by BHF etching. By controlling the BHF etch time, the gate region surface could be completely cleaned without SiO_2 residue. There are two existing versions of this process, and their only difference is the dry etch method after LiNiO deposition: RIE or IBE. With the RIE process, the opening of LiNiO could be completed within 30 seconds, while this recipe also had a high etch rate of PEDVD SiO_2. The IBE process, on the other hand, had a relatively slow etch rate for LiNiO, which is quite close to the etch rate of SiO_2. Pulse etching and thermal control were required while mounting the chip on the carrier wafer to avoid resist burn-in in IBE process. Based on this oxide lift-off process, a very clean LiNiO pattern could be obtained without damaging the AlGaN surface. Source/drain were formed before LiNiO deposition, and the LiNiO was not annealed at high temperature after deposition. Post process annealing of LiNiO would cause the properties of LiNiO film to be out of control. The quality of the interface between AlGaN and LiNiO could also be affected.

In addition, during PLD deposition, the metal part was covered with SiO_2 and the organic residues on the chip and in the chamber were well controlled. Good quality of the film could be guaranteed and reproduced. The disadvantage of this method is the wet etched gate opening with strong etching in lateral direction, which leads to a less precise pattern. This could be solved by adding another HSQ lift-off mask, which was used in tri-gate multi-channel devices in the next chapter.

Lift-off with HSQ mask and LiNiO direct patterning: process is shown in Figure 3-9 (c) and Figure 3-10 (d)(h), HSQ is a high resolution e-beam resist; it is a type of negative resist with

high resolution. With careful process control, HSQ can achieve sub-10 nm resolution. After exposure, the liquid spin-on HSQ is converted to SiO_2, which is a perfect LiNiO lift-off mask and drastically reduces process difficulties. However, a thick spin-on HSQ mask is difficult to achieve. A typical thickness of high-resolution HSQ is 100-200 nm. The device shown in Figure 3-9 (c) and Figure 3-10 (d)(h) is not performed with the mixed IBE/BHF after PLD-LiNiO deposition for quickly processing. Although the LiNiO pattern is very sharp, the device does not work well, possibly due to HSQ leakage through gate and drain or HSQ residue under LiNiO. This process is not easy to control and thus not practical: HSQ is a negative resist. To achieve the same protection as the PECVD SiO_2 mask described above on the etched surface and source/drain, not only a very thick HSQ but also a very large exposure is required. This leads to an unacceptable EBL write time, and the large exposure area also gives rise a strong secondary electron exposure. The HSQ residues in the gate opening area are unavoidable due to the secondary backscatter electrons. In addition, the exposed HSQ film is not as dense as PECVD- SiO_2 formed at 300 °C. HSQ is an unsuitable mask material for IBE etching due to its high etch rate. For these reasons, the HSQ pattern method is not used for a single channel. By combining the PECVD SiO_2 lift-off method with the HSQ mask, we use a sharp pattern method for the multichannel transistor. The details are presented in the following chapter.

LPCVD SiN self-aligned mask: this process has been used to fabricate devices used for circuit-level and dynamic performance testing. The SiN passivation layer is a standard configuration in GaN lateral transistors (Figure 3-9 (d)) [82]. A high quality, 100 nm thick, high temperature LPCVD SiN was deposited on the RCA cleaned sample prior to all processes. The key process in passivated LiNiO junction transistors is the opening of the SiN in the gate and source/drain regions. Here, we used an EBL lift-off Cr (10 nm)/Au (150 nm)/Ti (40 nm) as a metallic hard mask for etching. Cr serves as an adhesive layer for Au, and a thin Cr layer is used to avoid lateral etching. Au serves as a mask layer for wet etching to prevent the metal mask from dissolving in 49% HF. A Ti layer is on the top to protect Au from dry etching, since Au is not allowed in most dry etch chambers. A mixed dry/wet etch of SiN is used. During dry etching, a CHF_3/SF_6 formulation with anisotropy etched ~90 nm SiN layer. The remaining 10 nm SiN was removed by 49% HF etching. With this mixed etching method, the contact time of the high concentration HF is greatly reduced, and the etching of SiN in the lateral direction is much lower than etching SiN with HF alone. By combining with the PECVD- SiO_2 lift-off method (BHF does not attack SiN during gate opening), a passivated self-aligned LiNiO gate transistor can be fabricated.

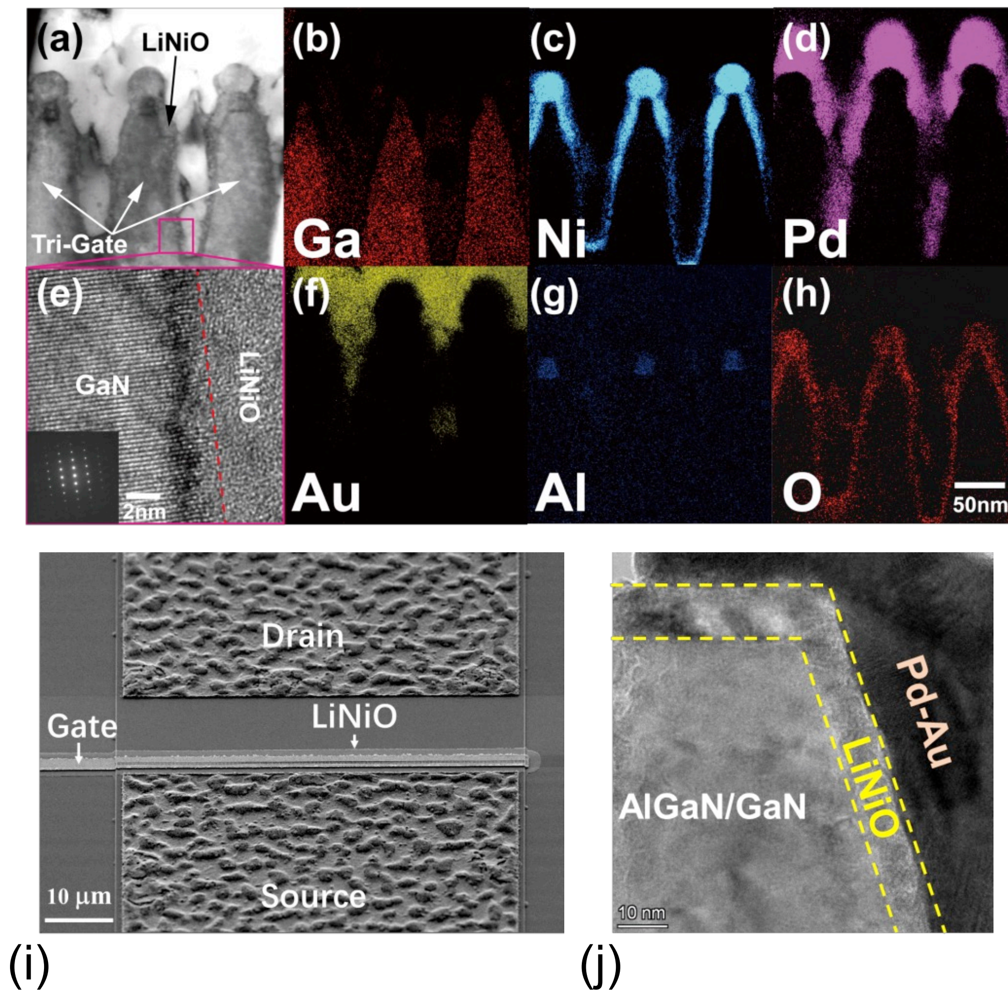

Figure 3-11 (a) Cross-sectional high-angle annular dark field (HADDF) scanning transmission electron microscope (STEM) image. (b)(c)(d)(f)(g)(h) cross-sectional energy dispersive X-ray spectroscopy (EDS) mapping analysis of the LiNiO film on AlGaN/GaN tri-gate structure. (e) high-resolution transmission electron microscope (TEM) of LiNiO/GaN sidewall interface (Insert: Diffraction pattern of GaN region). (i) top view SEM image of finished tri-gate MOSHEMT with LiNiO gate dielectric. (j) cross-sectional HRTEM image at the top of the fin region, good coverage can be observed.

To examine the cross-section of the tri-gate fin, the tri-gate structure was prepared for TEM by focused ion beam (FIB) milling of a cross-sectional lamella (Zeiss NVision 40). STEM was performed at 200 kV with Talos F200S TEM equipped with a high-brightness source and an energy-dispersive X-ray spectrometer, double tilted sample holder was used to align the correct crystal plan. Imaging was performed by collecting incoherently scattered electrons with the HAADF detector. Incoherently scattered electrons are sensitive to the atomic number, and thus the contrast in the HAADF STEM images reflects compositional information. A cross-sectional TEM image of three fins is shown in Figure 3-11. After low-temperature PLD deposition, no interface degradation was found between GaN and LiNiO (Figure 3-11 (e)), along with a clear crystalline AlGaN/GaN sidewall, which is hard to achieve in high-temperature film deposition

processes. From the energy-dispersive X-ray spectroscopy (EDS) mapping (Figure 3-11 (b)-(h)) the conformal LiNiO film step coverage was confirmed. The transistor dimensions were L_{GS} = 2 µm, L_G = 1 µm and L_{GD} = 15 µm.

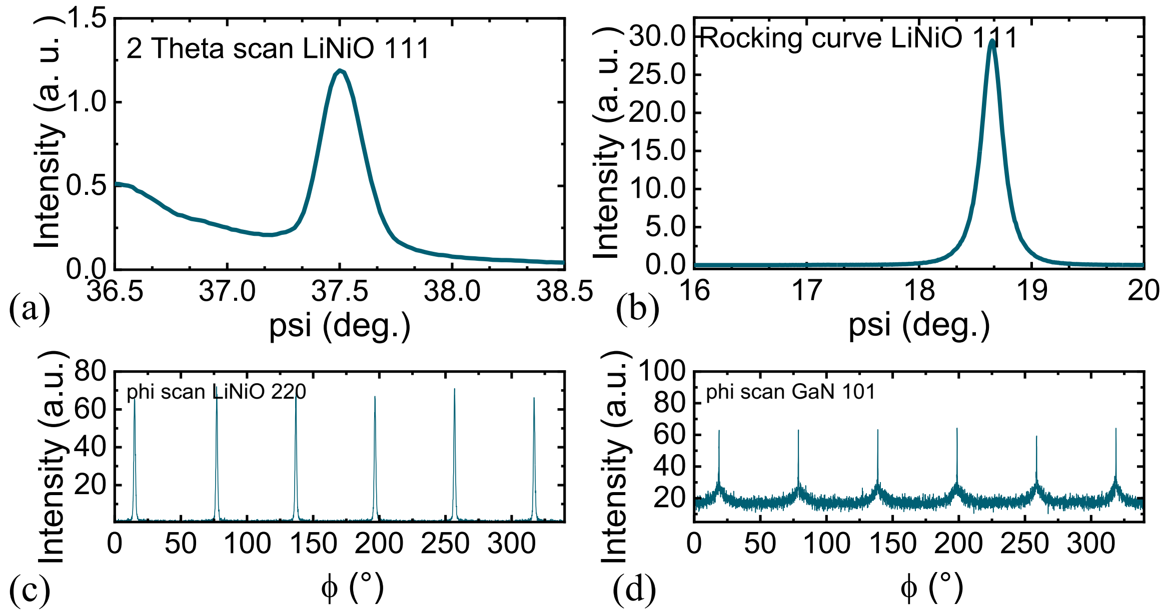

Figure 3-12 X-ray diffraction patterns of LiNiO on AlGaN/GaN/Si substrate. (a) θ-2θ scan and (b) rocking curve of LiNiO (111). Φ-scan on (c) LiNiO (220) and (d) GaN (101)

Device characteristics were normalized by the entire device width and unless otherwise indicated and 15 % Li concentration LiNiO gate oxide was used. The LiNiO patterning method is the essential step in the LiNiO junction gate device process. Unlike the NiO_X film which can be easily patterned by normal photoresist [70, 91], the 400 °C deposition temperature hinders the use of any organic photoresist. As discussed previously, LiNiO is a perfect acid-resistant material, which makes the high-quality pattern of LiNiO difficult. The detailed process method has been discussed previously.

HRXRD tests were done on PLD LiNiO film grow on AlGaN/GaN to verify the epitaxy relationship. An 80 nm thick sputter LiNiO was deposited on a planar AlGaN/GaN substrate, only 111 diffractions are detected, and the rocking curve shows a quite narrow full-width half-maximum (FWHM) value of 0.22°, and the *Φ* scan of LiNiO 220 angles (positions) are the same as GaN 101. So, the epitaxy relationship could be determined as $(111)\left[1\bar{1}0\right]\mathrm{Ni}_{1-x}\mathrm{Li}_x\mathrm{O}//$ $(0002)\left[11\bar{2}0\right]$. This result well matches other work on PLD LiNiO on AlGaN epitaxy relationship [76]. It means LiNiO is a single crystalline layer, which could result in better interface quality over ALD SiO_2 and any other PECVD and ALD materials.

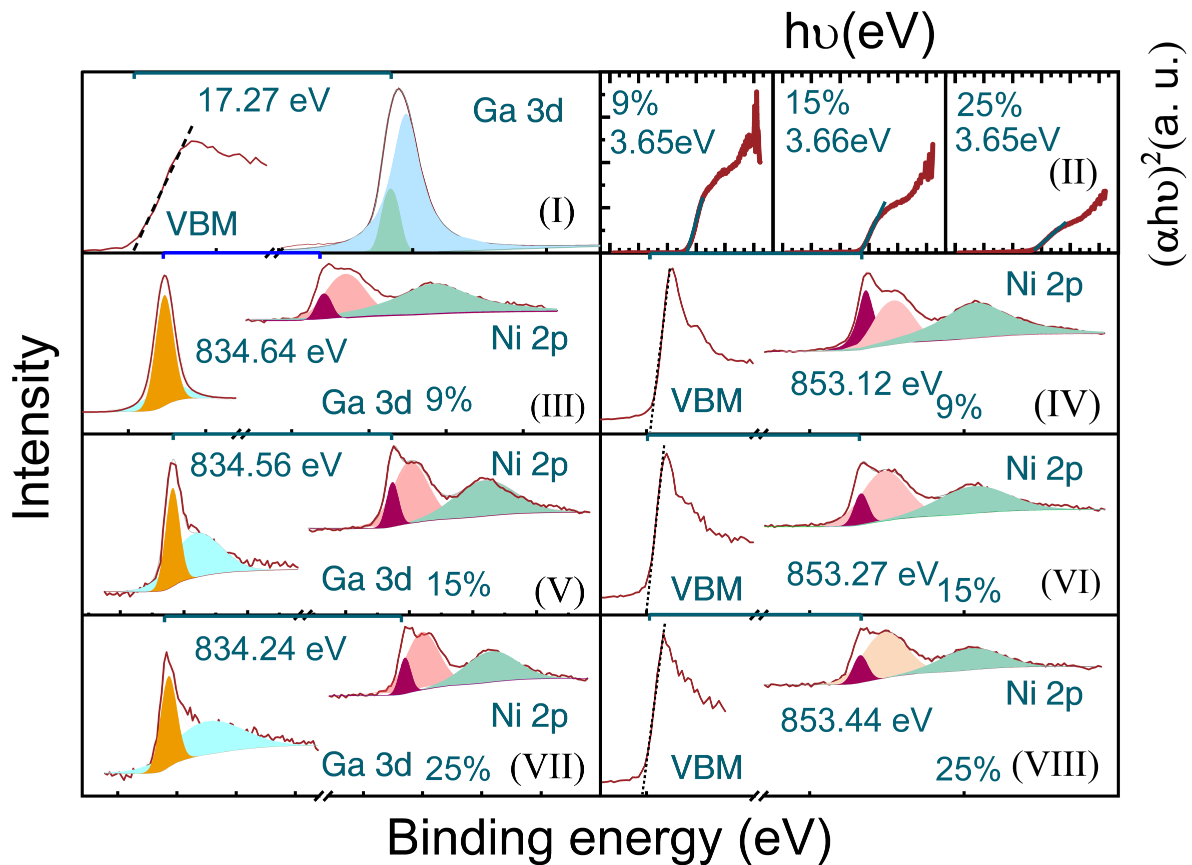

Figure 3-13 X-ray photoelectron spectroscopy (XPS): (I) valence band and Ga 3d core level spectra for AlGaN/GaN. (III)(V)(VII) core level spectra of Ga 3d and Ni 2p from ~3nm thick 9%, 15%, 25% Li doped NiO on AlGaN/GaN. (IV)(VI)(VIII) Ni 2p core level spectra and valence band for ~60nm thick 9%, 15%, 25% Li doped NiO on AlGaN/GaN. (II) $(\alpha h\nu)^2$ versus hν optical transmission spectra plot from ultraviolet-visible spectroscopy (UV-Vis) for different Li doping concentration LiNiO film on fused silica.

The reason of use LiNiO instead of p-GaN is mainly the process difficulty, regrowth p-GaN on tri-gates is very hard to achieve at present time. Because the distance between the fin is very narrow at sub-100 nm scale, the etched sidewall is also not suitable for regrowth for its rough surface. Moreover, the growth and activation of p-GaN were done at high temperature, which also limits the process flow and interface quality (due to atom movement at high temperature). The LiNiO is deposited at a much lower temperature but shows a single crystalline phase, and high hole concentration, which makes it an attractive material for e-mode tri-gate device.

Apart from hole concentration, the band alignment between LiNiO and AlGaN is another major consideration for achieving e-mode. To extract the band alignment between LiNiO and AlGaN different Li-content LiNiO on AlGaN/GaN was measured by X-ray photoelectron spectroscopy (XPS) analysis and ultraviolet-visible spectroscopy (UV-Vis) (Figure 3-13). When the Li atomic percentage varied from 9% to 25% the core level between Ni 2p and VBM increased,

indicating the increase of the Ni^{3+} partial density by replacement Ni to Li. Following the band gap value of LiNiO from UV-Vis measurements, valence band (ΔE_V) and conductive band (ΔE_C) offsets were obtained (Figure 3-14).

In the characterization of band alignment between LiNiO and AlGaN, four samples were needed [92], one clean GaN-on-Si heterostructure chip without any film on top, one thick LiNiO layer (over 50 nm) film deposited on GaN-on-Si heterostructure, one thin LiNiO layer (~5 nm) film deposited on GaN-on-Si heterostructure, and a ~50 nm LiNiO film on glass sample. At first, the band gap of LiNiO was extracted from transmission spectra, this value was got from the LiNiO on glass sample and tested by filmetrics F20 in transmission mode. LiNiO is a direct band gap semiconductor using Tauc model [93]:

$$(ahv)^2 = k\left(hv - E_g\right) \tag{3-1}$$

hv is the photon energy, *k* is a constant and α is the absorption coefficient. In addition, α is determined by equation $\alpha = -(1/d)\ln(T)$, *d* is the thin film thickness and *T* is the optical transmission rate. Band gaps for LiNiO thin films were determined by extrapolating linear regions of plots $(\alpha hv)^2$ versus *hv* where $\alpha hv = 0$[75].

The valence band offset could be determined by using Kraut method [94]:

$$\Delta E_V = \left(E_{Ni2p}^{LNO} - E_V^{LNO}\right) - \left(E_{Ga3d}^{AGN} - E_V^{AGN}\right) - \Delta E_{CL} \tag{3-2}$$

The $E_{\mathrm{Ni2p}}^{\mathrm{LNO}} - E_{\mathrm{V}}^{\mathrm{NNO}}$ disclose the core energy level difference between Ni 2p and valence band maximum value (VBM) of thick LiNiO sample, $E_{\mathrm{Ga3d}}^{\mathrm{AGN}} - E_{\mathrm{V}}^{\mathrm{AGN}}$ is the core energy level difference between Ni 2p and Ga 3d of thin LiNiO sample. And then the conduction band offset (ΔE_{V}) is calculated by:

$$\Delta E_C = E_g^{LNO} - E_g^{AGN} + \Delta E_V \tag{3-3}$$

The $E_{\mathrm{g}}^{\mathrm{LNO}}$ and $E_{\mathrm{g}}^{\mathrm{AGN}}$ are the band gap of LiNiO and AlGaN layer. Based on XPS and UV-Vis results (Figure 3-13), the band alignment relationship between different Li concentration LiNiO can be extracted [75].

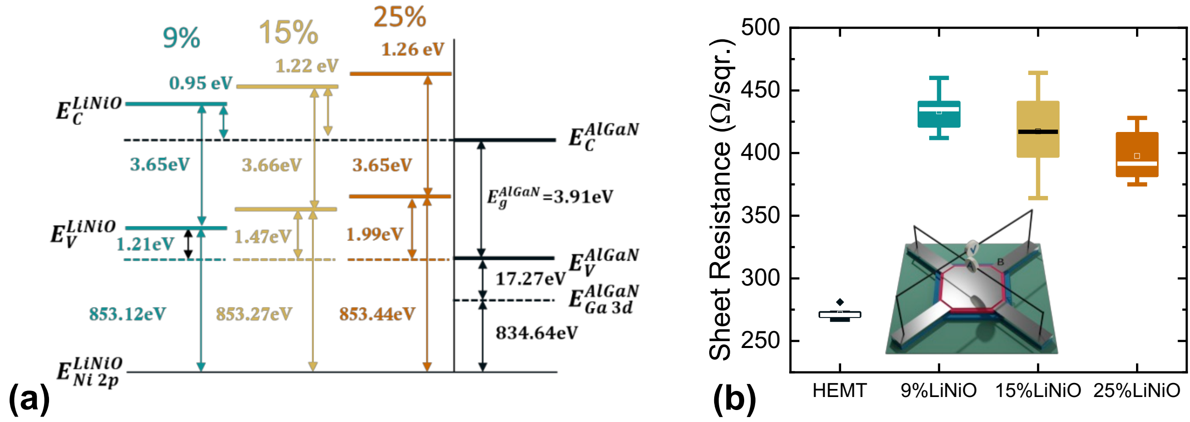

Figure 3-14 (a) Band alignment between LiNiO and AlGaN determined from XPS and UV-Vis measurements, for Li content of 9%, 15%, and 25%. (b) Measured sheet resistance on hall structures patterned on an AlGaN/GaN HEMT structure, and three HEMT structures covered with LiNiO with Li concentrations of 9%, 15%, and 25% and Pd/Au gate. Inset: schematic of gated hall structure.

Three LiNiO films present a similar bandgap ~3.65 eV which is quite close to the GaN value of 3.4 eV. The 9% Li-content sample presents a very small ΔE_V to AlGaN of 1.21 eV which is much smaller than the 2.53 eV [70] of normal magnetron sputtering NiO_X. Even the 25% Li-content LiNiO still presents a small ΔE_V of 1.99 eV. The large ΔE_V of higher Li atom percentage in LiNiO results in a larger band offset, which is not preferred for e-mode operation. This is confirmed from gated hall measurements on HEMT (Figure 3-14). The HEMT hall structure, with LiNiO/Pd/Au gate stack on top, shows statistically higher sheet resistance (R_S) over HEMT epi itself. From the hall measurement of LiNiO on i-GaN with Pd contact, a hole concentration ~ 1×10^{16} cm^{-3} was observed, and mobility below 1 $m^2 \cdot V^{-1} \cdot s^{-1}$, due to the very small mobility, the hall measurement is not suitable for the hole concentration measurement of PLD LiNiO other methods such as Seebeck method is more suitable [75]. The higher Li-content sample is supposed to has a higher hole concentration. However, the planar gate hall measurement of heterostructure shows the 9% Li-content sample has the strongest channel depletion ability. All three samples with LiNiO/Pd on hall square present a 66%-87% increase of the R_S. This results proved the depletion ability of the LiNiO junction gate. The 9% Li-content sample with a small ΔE_V presents the strongest depletion ability on a planar structure. However, on fabricated tri-gate device, 25% Li-content sample presents the most positive V_{TH}. Most of device in the later chapter would use 25% Li-content LiNiO, if not specially mentioned.

3.6 Device performance and optimization

3.6.1 Static performance

Figure 3-15 (a) shows the transfer and (b) output performances, revealing a positive V_{TH} of 0.7 V at I_D = 1 μA/mm (for a device with L_{GS} = 2 μm, L_G = 0.7 μm, and L_{GD} = 15 μm). This was achieved on a low R_S epitaxy (275 Ω/sqr) and a relatively short L_G, which is more challenging to demonstrate e-mode operation. All device characteristics were normalized by a total gate width of 20 μm. A near ideal *SS* of 63 mV/dec was observed, which suggests an excellent gate control of the tri-gate structure and low density of interface traps. A high on/off ratio of 10^9, and peak transconductance (G_m) of 105 mS/mm indicate a small leakage current in off-state and strong gate coupling to the channel.

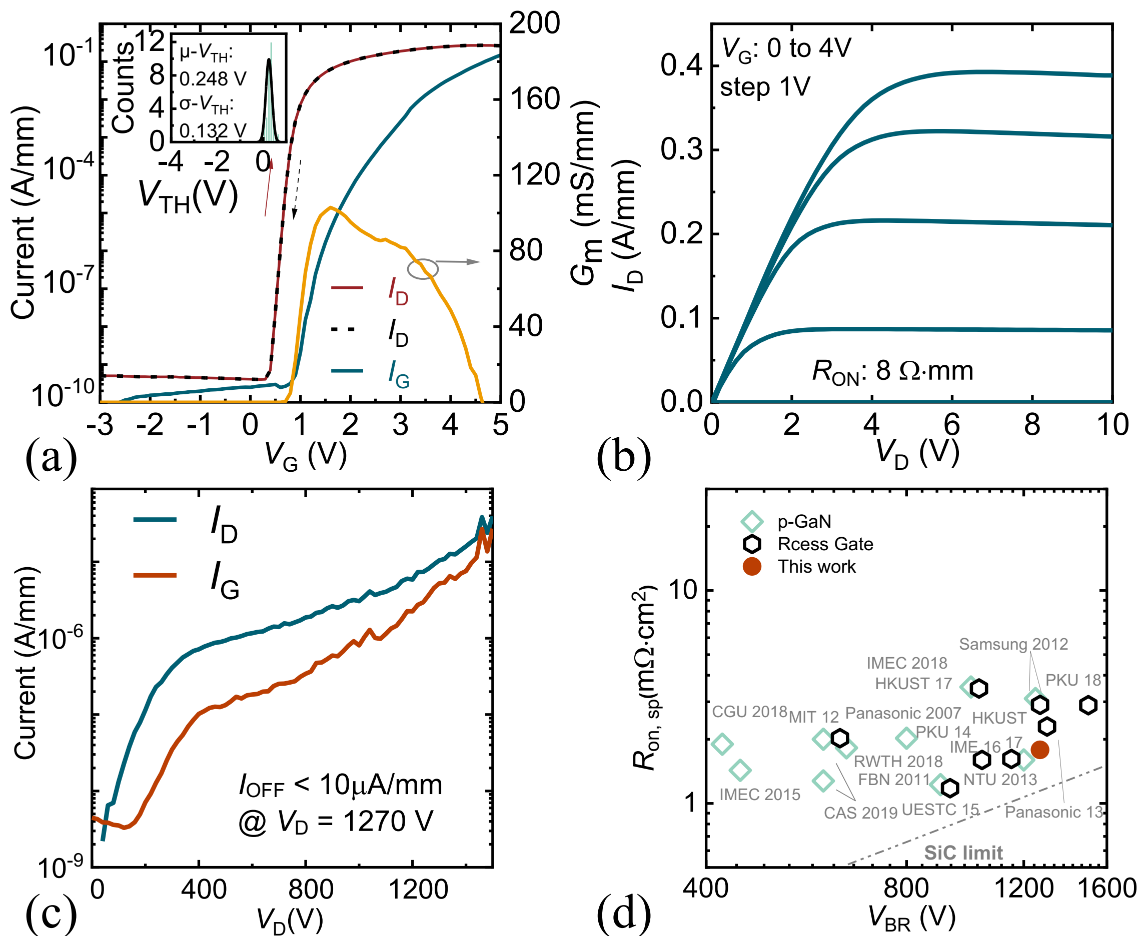

Figure 3-15 (a) Transfer (V_D = 5 V) inset: histograms of V_{TH} distribution among 33 devices (W_{Fin} = 40 nm, 9% Li doping LiNiO gate, and V_{TH} is defined at I_D = 1 μA/mm). (b) Output characteristics of LiNiO tri-gate. R_{ON} is extracted from linear fitting of I_D at V_G = 4 V and V_D = 1V. (d) Three terminal breakdown characteristics of the device at V_G = 0 V (under floating substrate with fluorinert). (d) $R_{on,sp}$ versus V_{BR} by defining V_{BR} at I_{OFF} ≤ 10 μA/mm, for recess gate, floating substrate result was shown for a fair comparison. $R_{on,sp}$ was calculated considering a 1.5 μm of transfer length for each ohmic contact was taken into account for $R_{on,sp}$ calculation. The V_{BR} results in the literature were re-calculated by I_{OFF} ≤ 10 μA/mm.

The ohmic gate (Pd/LiNiO) and junction formed between LiNiO and AlGaN resulted in a gate injection transistor (GIT)-like behavior [32], which is reflected by a second peak in the G_m plot (Figure 2-11 (a)), and results in a larger positive gate current compared to Schottky gate devices. Maximum I_D of 390 mA/mm and R_{ON} of 8 Ω·mm were observed at V_G of 4 V. In addition to the excellent on-state performance, the devices could hold off-state V_D bias of 1270 V (defined at I_{off} < 10 μA/mm, V_G = 0 V floating substrate) due to the well-distributed electric field by the tri-gate structure [14, 60]. Hard breakdown did not happen within the measurement range till 1500 V (Figure 2-11 (c)). When benchmarking the high power FOM of LiNiO junction gate device with the state-of-the-art e-mode device, the device in this work presents a high FOM at the same level of high-performance p-GaN or recess gate MOSHEMT; the V_{BR} is higher than most p-GaN gate devices with the similar junction gate structure. The R_{ON} of the LiNiO hetero-junction gate device is extracted from a relatively low V_G bias point, due to the GIT-like operation mode. Through the optimization of I_G, the gate swing of LiNiO gate device can be further improved.

The large I_G is the natural properties of junction gate devices, which also observed on p-(Al)GaN gate devices. One argument of the drawback of p-GaN gate with ohmic type gate is its high-power consumption and complicated gate driver design. However, from the research of Panasonic, ohmic type junction gate has special safety, current collapse, and reliability advantages. The ohmic type junction gate has already been a major technology route in today's commercial lateral e-mode GaN transistor. In our device design, the large current is not only from the junction gate structure but also from the very thin LiNiO layer on the sidewall, which is due to the non-perfect step coverage capability of the PLD deposition process. And this can be greatly improved by increasing the LiNiO layer thickness, optimizing the disposition condition (higher temperature, higher pressure, or tilted deposition). The on-state performance of our device is at a state-of-the-art level even compared to the MOSHEMT device. Even the R_{ON} and $I_{on, max}$ is weak than the most well-performed MOSHEMT device, it still outperformed the NiO_X or p-GaN gate device in terms of FOM. The limitation of device breakdown is from the gate current, which can be observed from the similar behavior of I_G and I_D during breakdown measurement, due to the junction structure in the proposed device. The device can measure till the measurement range 1500 V, before reaching the power compliance of B1505a. The off-state current is larger than the MOSHEMT tri-gate device. But there is no abrupt breakdown during measurement, which is an advantage over MOSHEMT device for their unpredictable breakdown behavior. This is also shown in the very promising HTRB results.

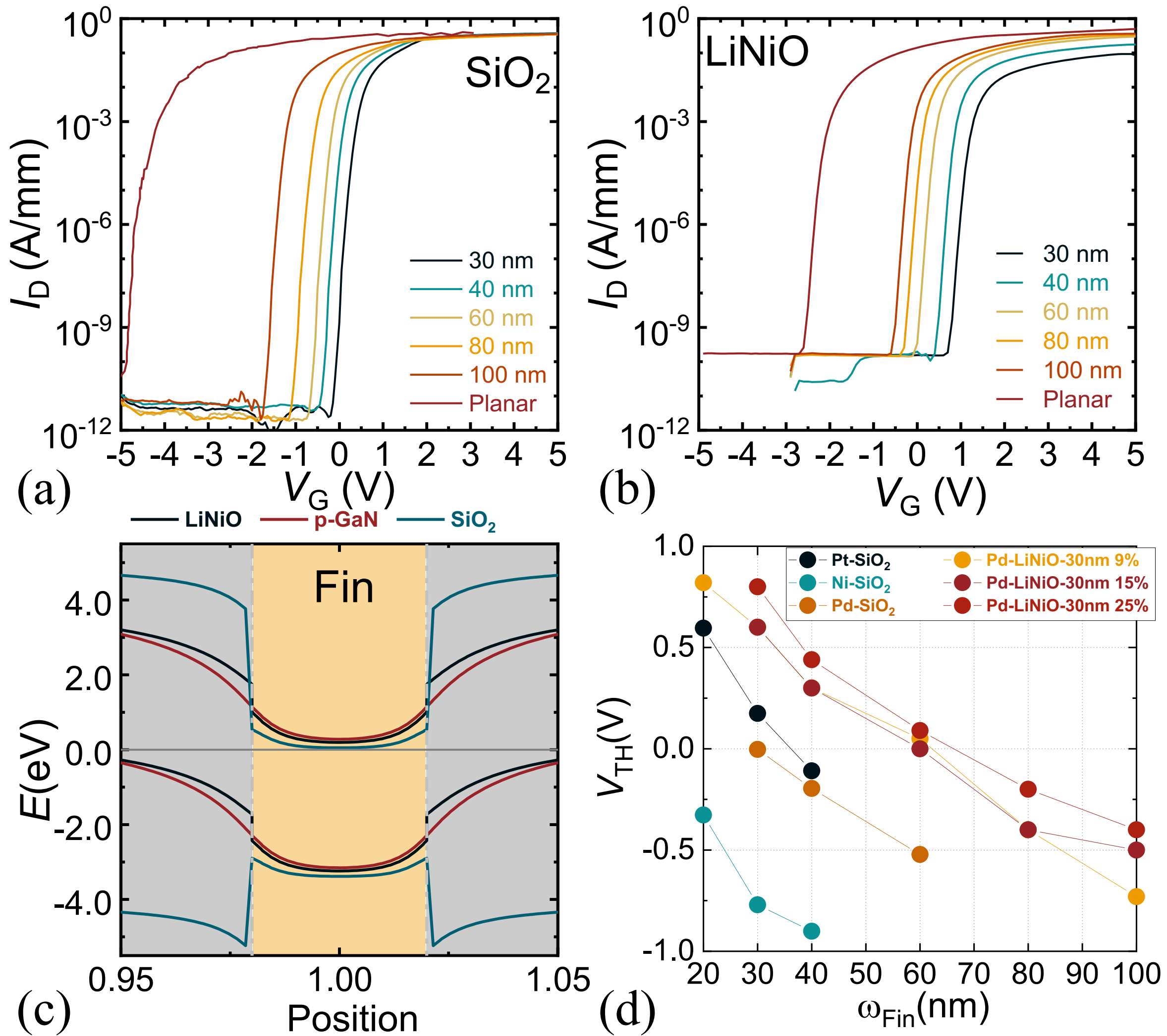

Figure 3-16 Transfer characteristics of different tri-gate fin widths with (a) SiO_2 (Pt gate) and (b) LiNiO (Pd gate) oxide. (c) Simulated band diagram along the fin width direction, at the interface between AlGaN and GaN. Three different gate dielectrics (junction) were used: SiO_2, LiNiO, p-GaN $V_{G,}$ and $V_{Sub.}$ = 0 V. (d) V_{TH} (defined at 1 μA/mm) as a function of W_{Fin} and gate stack, in LiNiO all three doping concentration films are deposited at the same thickness of 30 nm.

Figure 3-16 (a) shows the measured transfer characteristics of different tri-gate fin widths with SiO_2 or LiNiO in gate stacks. LiNiO devices presented a nearly 1 V positive shift in V_{TH} compared to SiO_2 counterparts. E-mode operation was achieved with 60 nm-wide fins with LiNiO (defined at I_D = 1 μA/mm), whereas with SiO_2 this was only possible with 30 nm-wide fins. These results greatly reduce the lithography requirements for defining the tri-gate fins and increase the maximum possible V_{TH}. Figure 3-16 (d) shows the more positive V_{TH} (defined at 1 μA/mm) for the same fin widths achieved with LiNiO compared to SiO_2, and different Li doping concentrations LiNiO (9%, 15%, and 25%) were compared. Unlike the result from gated hall measurement (Figure 3-14 (b)) in which 9 % of film presents the best channel depletion ability. 25% Li-content LiNiO device presents the most positive V_{TH} on tri-gate structure, which is different from the planar case. The limited sidewall depletion of thin oxide layer may result

this. From the latter measurement of PBTI, and the material properties of LiNiO, the trapped charge inside LiNiO is positive. Fabricated device presents a small V_{TH} hysteresis and narrow distribution of V_{TH} during transfer sweep. In Figure 3-16 (c), using Sentaurus TCAD, a 3-dimensional tri-gate fin simulation was performed with three different gate stack: SiO_2, p-GaN, and LiNiO. The band diagram cutting was made at the interface of AlGaN and GaN, along the gate width direction. The results prove the LiNiO has channel depletion ability but is weaker than p-GaN.

3.6.2 Device design optimization

To optimize the device performance, different L_{Fin} devices and different L_{Oxide} devices were fabricated. When the L_{Fin} increases, the V_{TH} shifts weakly towards positive. But this will result in a higher fin resistance, and total device resistance (R_{ON}), which is not favorable. This weak dependence of V_{TH} shows that in 1 μm length fin, the depletion region inside of the fin has already reached the maximum width at this fin width (60 nm). A more apparent V_{TH} dependence was shown at a shorter fin. This result shows that a short fin combined with LiNiO has the ability to pinch off the channel, which is beneficial for the reduction of R_{ON} and RF applications (requiring small gate length for fast operation).

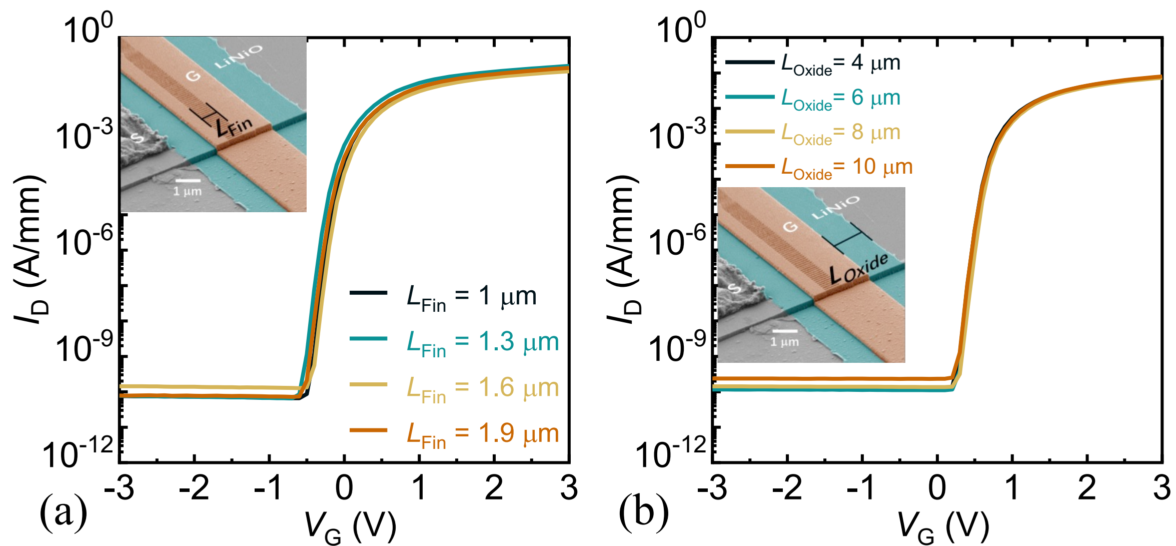

Figure 3-17 (a) Transfer characteristic for different L_{Fin}, devices deposited 9% doped LiNiO, measured at V_D = 5 V, W_{Fin} is fixed at 60nm, and L_{Oxide} is 4 μm (b) Transfer characteristic for different L_{Oxide}, devices deposited 9% doped LiNiO, measured at V_D = 5 V, W_{Fin} is fixed at 60nm, and L_{Fin} is 1 μm.

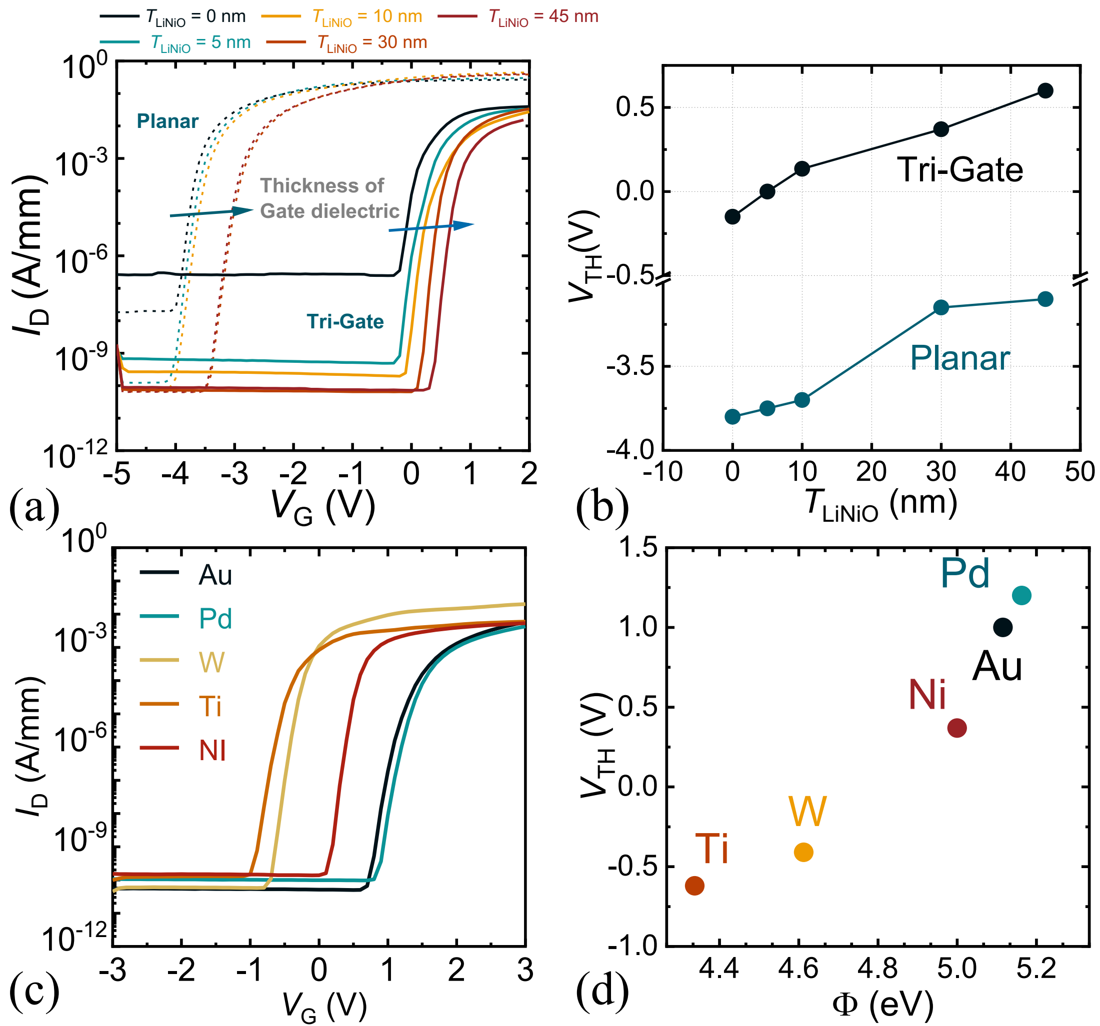

Figure 3-18 (a) Transfer behavior of different T_{LiNiO} devices, both planar and tri-gate devices were fabricated to compare. Devices include 9% doped LiNiO, measured at V_D = 5 V, W_{Fin} is fixed at 40nm. (b) V_{TH} (defined at 1 µA/mm) as a function of T_{LiNiO}. (c) Transfer behavior of different gate metals measured at V_D = 5 V, W_{Fin} is fixed at 30nm. (d) V_{TH} as a function of gate metal work function.

Different thickness of LiNiO film was deposited on both planar and tri-gate structure. Compared to T_{LiNiO} of 0 nm (HEMT structure with Pd gate), inducing LiNiO in device structure results in nearly three orders lower of I_{off}, and more positive V_{TH}. The V_{TH} positive dependence of T_{LiNiO} shows that the existence of LiNiO causes the positive shift of V_{TH} and the thicker LiNiO has stronger shift ability. Pd gate presents the most positive V_{TH}, which is due to its higher work function forms ohmic contact to p-GaN that helps to deplete electrons in the 2DEG in tri-gate structures. This is different from p-GaN whose valence band is deeper than most typical metal [95, 96]. Using Schottky contacts will decrease the positive gate leakage, and increase the turn-on gate voltage, however, it is not beneficial for positive V_{TH}. More importantly, using Schottky gate will results a floating p-GaN layer sandwiched between two junctions, and will induce instability [97], but ohmic gate has successfully demonstrated great reliability [15].

3.6.3 High temperature operation performance

The excellent V_{TH} thermal stability performance is shown in Figure 3-19.The high temperature output behavior is dependent on the epitaxy [98]. There are two sources of conductivity in the HEMT structure: 2DEG and bulk carriers. The bulk carriers are frozen at low temperature, and the bulk carrier density is dependent on temperature, while the 2DEG carrier density is independent of temperature. The scattering mechanism of bulk and 2D carriers has been well described in [99-101]: ionized impurity scattering, polar optical phonon scattering, and acoustic phonon scattering are corresponding to bulk conduction and polar optical phonon scattering, acoustic phonon scattering background impurity scattering, and interface roughness scattering. The off-state current rising is due to the increase of bulk carrier density under high temperature, and the lower of on-current is due to the increase of acoustic scattering in the 2DEG channel. These two mechanism results in the increase in *SS* and negative shift of V_{TH}. which shifted from 0.5 V to 0.28 V at 150 ℃, showing that the device could still maintain e-mode operation even at high temperature.

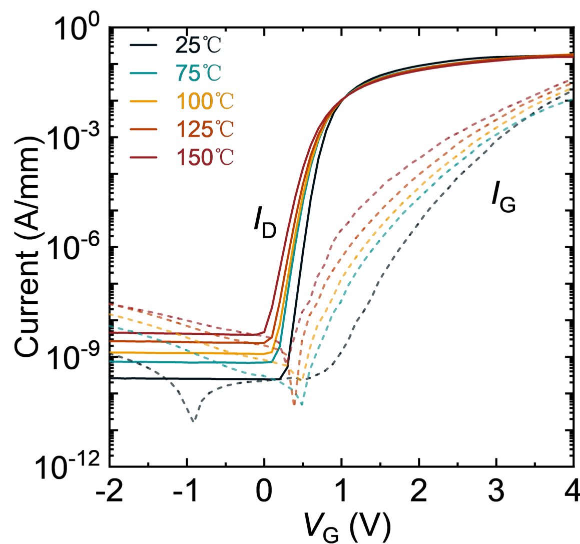

Figure 3-19 Transfer characteristics of the device with measurement temperature from 25 °C to 150 °C (W_{Fin} = 40 nm).

As for I_G behavior, it similar to PN diode's raised temperature behavior. The LiNiO/GaN on- and off-state current are increased with raised temperature. The intrinsic carrier density n_i increases significantly with raised temperature, due to the increase of effective density of states in the conduction band and valence band.

3.6.4 Gate reliability and optimization

The gate structure of our device consists of a p-type layer (LiNiO) and ohmic type gate, which is the same as gate injection transistor configuration (products already available from Infineon and Panasonic). This configuration shows a higher gate current under positive bias over Schottky p-GaN gate devices. These devices operate in the current drive mode gate driver (e.g. Infineon's CoolGaN^{TM} technology). This has been explained by Panasonic: "The device in on state behaves like a diode, this means that there is no breakdown destruction fear in case of voltage spike on the gate. Gate noise will be clamped by the diode and "absorbed" as transitory peak current." [102] In this case, there is no depletion region in the gate metal and LiNiO interface at positive bias. Therefore, the concern of positive reliability in Schottky type Gate p-GaN or normal MOSHEMT is not relevant in ohmic type p-GaN devices [97]. Typically, in p-GaN gated devices (either ohmic or Schottky), the gate bias is relatively small, and the operation point is smaller than normal MOSHEMT. Therefore, the operation gate voltage up to 5 V considered in this work is within a reasonable range. To test the extreme case of high V_G bias device behavior, a large V_G transfer sweep (Figure 3-20 (a)), and step stress test (Figure 3-20 (b)) was performed. During the step stress test, the devices failed at 10.75 V, presenting a lower gate current. This suggests that the failure during high bias is not from the oxide but the degradation of gate metal at high temperatures. Considering the operation point V_G of 3 V, this yields a large gate bias tolerance. Moreover, the gate current can be adjusted by fin width, gate metal, and LiNiO layer thickness.

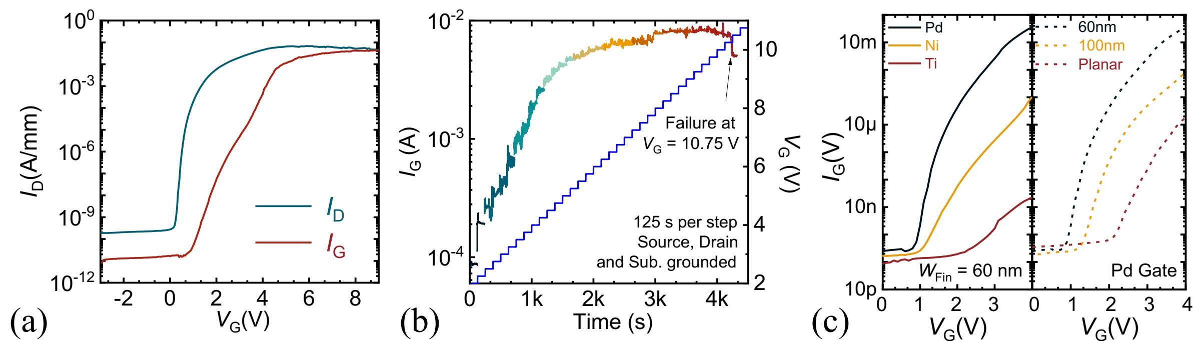

Figure 3-20 (a) Transfer behavior of large V_G sweep (V_D = 10 V). (b) Results of a step-stress test on the gate, by increasing positive gate bias levels. (c) Gate leakage characteristic of devices with different gate metal (left) on W_{Fin} = 60 nm, and with different W_{Fin} (right) with Pd gate.

3.6.5 Reliability performance

We tested negative bias temperature instability (NBTI) at -20 V gate bias, and positive bias temperature instability (PBTI) at 3 V. As previously mentioned, the LiNiO junction gate device is an ohmic gate with a p-type layer device, which is like the GTI device. In Schottky gate p-GaN device, there is a high-field in the depleted region in the p-GaN layer, which generates holes by impact ionization [116] and this is the reason of PBTI' s importance to Schottky type p-GaN device, which is not the case for ohmic type p-GaN device [117]. The voltage drop on the LiNiO layer under positive gate bias is much smaller than normal MOSHEMT or Schottky gate p-GaN device. The degradation of V_{TH} PBTI is not from hole injection in the oxide layer but the stress-induced leakage path due to the very thin oxide on the fin sidewall. A larger V_G PBTI test cannot extract more information from LiNiO itself. A better PBTI performance can be expected for more conformal deposition methods.

NBTI was tested under V_G = -20 V, and there is a high-field depletion region formed in the LiNiO layer in this case. A very small V_{TH} shift present at both room and high temperature proves the good stability of the LiNiO layer itself.

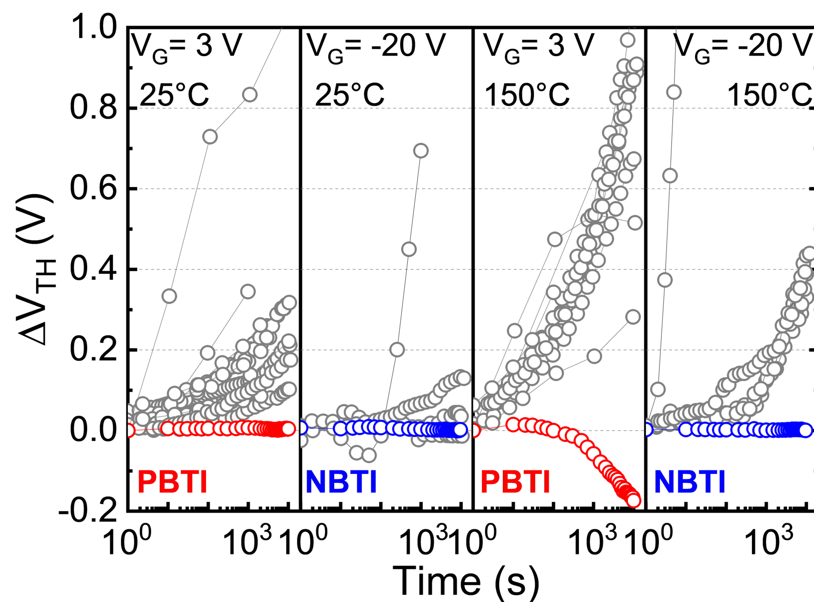

Figure 3-21 (a) Transfer behavior during NBTI stress test. (b) Transfer behavior during PBTI stress test W_{Fin} = 40 nm. (c) PBTI and NBTI test results [83, 103-115].

3.6.6 Dynamic performance

To evaluate the dynamic performance of LiNiO junction gate tri-gate devices, a 100 nm-thick passivation layer was added in the drift region before the device process. The passivation process and test methods are described in Ref [82]. A 100 nm LPCVD SiN passivation layer was deposited on RCA cleaned chip before device fabrication, then SiN was patterned by Cr/Au/Ti hard mask with mixed RIE and 49% HF wet etching. A sharp edge of SiN patterning can be observed in Figure 3-22 (a). Compared with SiO_2 gate oxide, LiNiO junction gate device (both passivated with LPCVD SiN layer in drift region) presented a significantly lower R_{Dyn}/R_{Static} ratio (at $V_D = 200$ V) (Figure 3-22(c)); This behavior confirms the lower interface trap of LiNiO junction gate tri-gate devices.

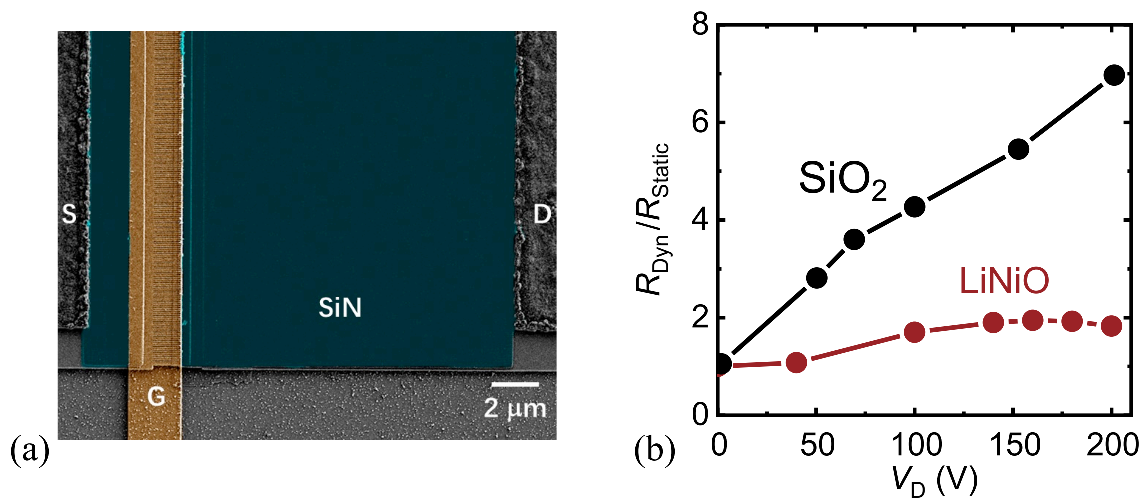

Figure 3-22 (a)Top-view SEM image of LPCVD passivated SiN passivated LiNiO Tri-gate device. (b) Dynamic R_{ON} increase ratio under different static drain bias stress (V_D). Devices with LiNiO and SiO_2 gate stack were compared.

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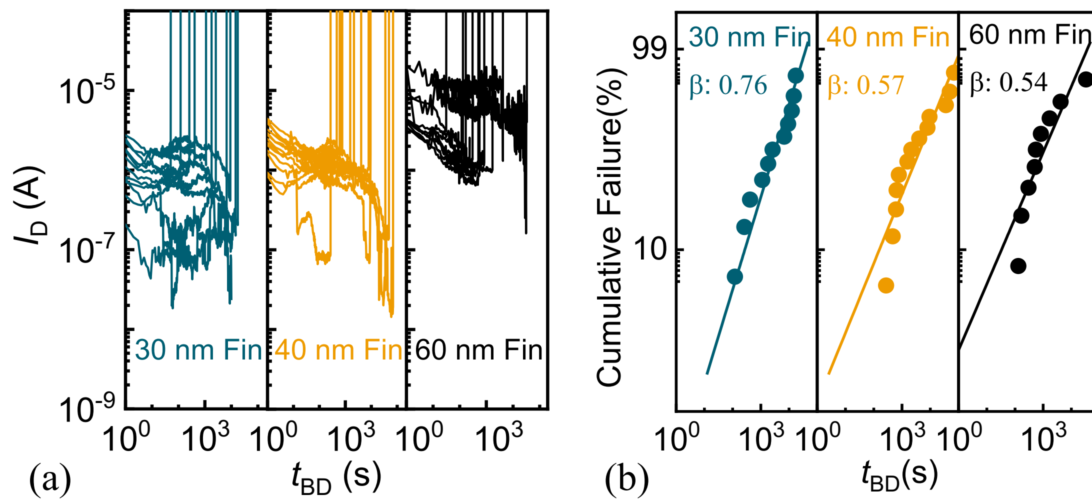

Figure 3-23 (a) Constant voltage stress performed at (V_G = 0V, V_D = 500V, and 150℃) on set of 12 identical devices, (b) Weibull distribution for three sets of devices.

High-temperature reverse bias (HTRB) test was performed to investigate the current-blocking capability at high temperatures. The time-dependent leakage characteristics of devices with different tri-gate fin widths are presented in Figure 3-23 (a). Both devices with 30 nm- and 40 nm-wide fins could be fully turned-off even at 150 ℃ with higher off-state leakage compared to room temperature, while devices with 60 nm-wide fins could not be fully turned off due to its more negative V_{TH}. The Weibull plot could be built from the time-to-breakdown distribution of three device sets (Figure 3-23 (b)). For a narrower fin, a larger fitted parameter β was observed, which indicates a tighter distribution. The possible reason is that the deeper carrier depletion in small fin width devices ensures better device turn-off, which makes the device more immune to process variation-induced punch-through. The ohmic gate formed on LiNiO results in a larger gate current at positive V_G, which is beneficial to on-state reliability, since there is no high electric field region in LiNiO at positive bias [118].

We examined our devices' high temperature blocking ability: we performed a HTRB test under standard: JEDEC JESD22-A108: T_a = 150 °C, V_{DS} = 480 V [15]. The device could survive up to 110 h in off-state. Of course, the off-state leakage current (I_D) increased as the temperature raised, as expected, but it still works in off-state. To our best knowledge, this is the only academic work on e-mode MOSHEMT structure that presented a HTRB result. A much better performance could be expected through better process control and optimization.

3.6.7 LiNiO/AlGaN interface quality characterization

The evaluation of the quality of LiNiO and AlGaN interfaces is based on the conductivity dispersion method. The conductivity dispersion method measures the conductivity change at different frequencies and V_G to determine the depth and amount of interface trapping [120]. The conductance, which is the loss of the trapping process, can indicate the density of the traps. Normally, this test should be performed at the second plateau of the MOSHEMT CV plot. In the conductance dispersion method, the multi-frequency sweep CV limits the frequency points, which can lead to a poor fitting result. Moreover, after the measurement, we need to correct the series resistance and tunnel conductance to extract the actual conductance and capacitance value from the high current C&G measurement [119, 121], leading to the plot of raw CV sweep results misleading [119, 122].

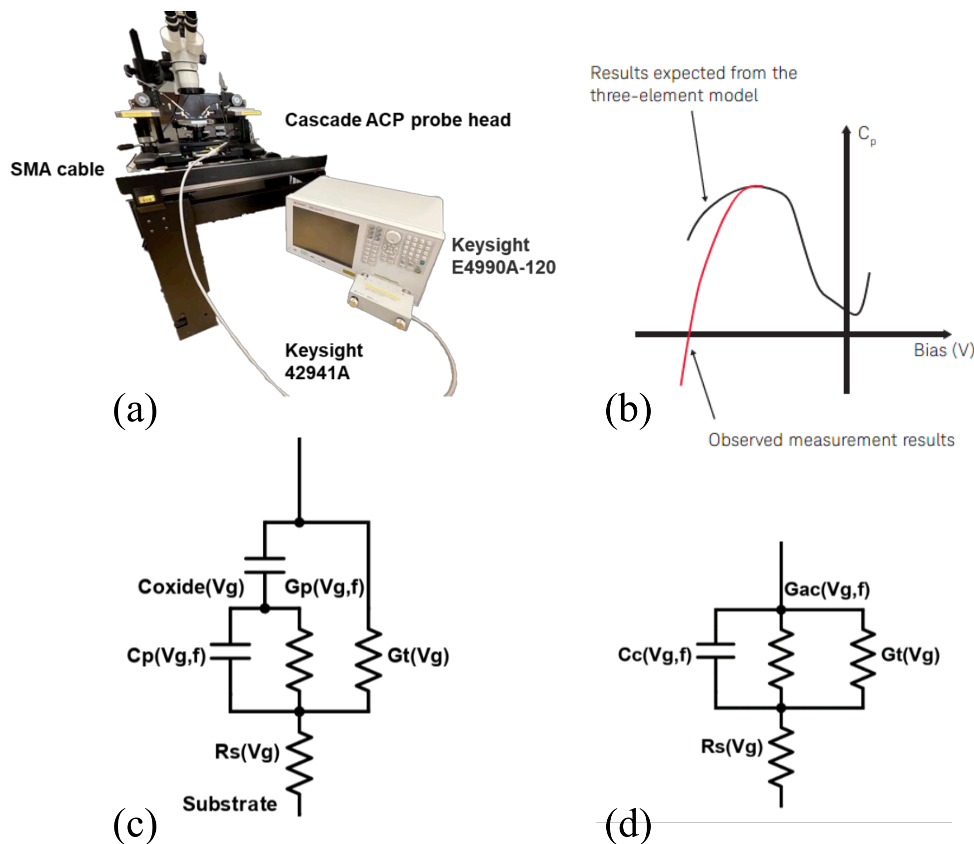

Figure 3-24 (a) RF IV precise capacitance measurement setup, including cascade ACP probe head, Keysight 42941 A adapter, and Keysight E4990A-120 impedance analyzer. (b) negative capacitance behavior during leaky capacitor measurement [119]. (c) C&G model of LiNiO/AlGaN planar junction capacitor device. (d) simplify C&G model of LiNiO/AlGaN planar junction capacitor device.

In our measurement, we sweep the C&G directly using the Keysight E4990A over frequency. The gate structure of our device consists of a p-type layer (LiNiO) and ohmic metal, which

corresponds to the configuration of a gate injection transistor. This configuration exhibits higher gate current under positive bias than Schottky p-GaN gate devices that operate in current drive mode (e.g., Infineon's CoolGaN^{TM} technology). “Gate noise is trapped by the diode and 'absorbed' as transient peak current” [102]. The gate current at positive V_G is high, which is a leaky junction diode. Before the 1990s, it was difficult to extract the C&G value from this type of device (Figure 3-24 (b)). However, during the development of the ultra-thin oxide layer for Si CMOS logic devices, the leaky capacitor characterization method has been fully developed [119, 121]. To accurately characterize the leaky junction diode, several correction methods must be used to remove the negative capacitance due to the large current (1. Three-element model Figure 3-24 (c)(d), 2. Extended RF-IV method instead of auto-balancing methods Figure 3-24 (a), 120 MHz impedance meter and RF probe) [119].

To simplify the measurement, a planar MOS capacitor (MOSC) structure is used. First, the V_G region is extracted from the CV sweep at 1 MHz, then the C&G is swept against frequency at different voltages in the two plateaus. For normal insulating oxide, C_m and G_m are the measured capacitances. C_0 is the static capacitance of the two plateaus, G_p is the trap conductance, $\omega = 2\pi f$ is the radial frequency. (Equation 2-4) is used to calculate the SiO_2 oxide junction device with low leakage SiO_2, while (Equation 2-5) is used to correct the LiNiO junction capacitor (R_{se} is the series resistance; G_t is the tunnel conductance of the oxide).

$$\frac{G_{surf}}{\omega} = \frac{\omega C_0^2 G_m}{\omega^2 (C_m - C_0)^2 + G_m^2} \tag{3-4}$$

$$\begin{gathered}
C_m = \frac{C_c}{(G_c R_{se}+1)^2 + \omega^2 C_c^2 R_s^2} \\
G_m = \frac{G_c (G_C R_{se}+1) + \omega^2 C_c^2 R_s}{(G_c R_{se}+1)^2 + \omega^2 C_c^2 R_s^2} \\
C_c = \frac{C_m}{(1 - G_m R_{se})^2 + \omega^2 C_m^2 R_{se}^2} \\
G_c = \frac{\omega^2 C_m C_c R_{se} - G_m}{G_m R_{se} - 1} \\
G_{ac} = G_c - G_t \\
\frac{G_p}{\omega} = \frac{\omega C_x^2 G_{ac}}{G_c^2 + \omega^2 (C_x - C_c)^2}
\end{gathered} \tag{3-5}$$

After the $\frac{G_p}{\omega}$ versus ω relation was obtained from each device, by fitting with the following equation, the density and time constant of traps can be extracted.

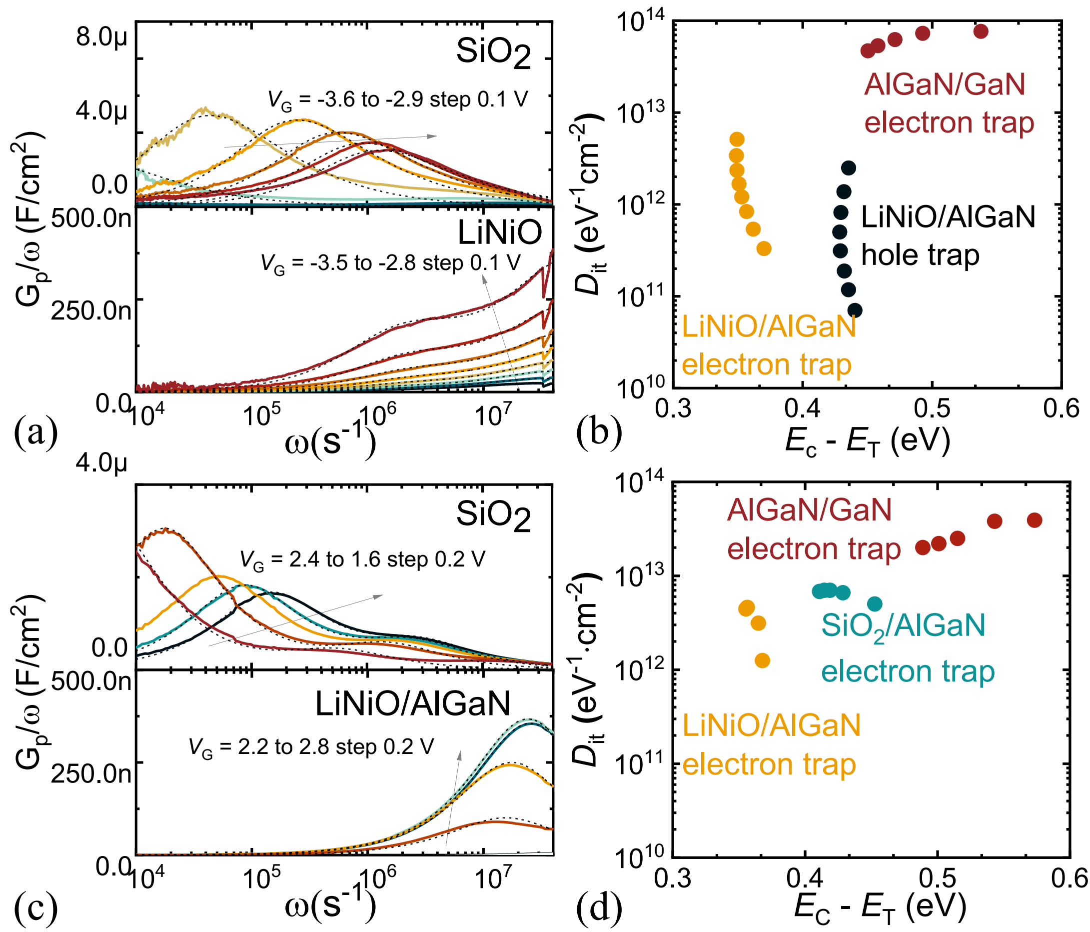

Figure 3-25 Two methods of interface quality characterization through conductance dispersion method: (a)(b) results from the first plateau in CV curve. (c)(d) results from the second plateau in CV curve.

There are two kinds of traps state, discontinue states [120]:

$$\frac{G_{surf}}{\omega} = \frac{q^2 D_{surf}\,\omega\tau_{surf}}{1+\omega^2\tau_{surf}^2} \tag{3-6}$$

And continue state [123]:

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} ln\,[1+(\omega\tau_{it})^2] \tag{3-7}$$

The trap time constant (electron trap) relative distance to the conduction band $E_c - E_{\mathrm{surf}}$ can be estimated from the following expression [120]:

$$\tau_{surf} = (\sigma_T N_c v_t)^{-1} exp\left(\frac{E_c - E_{surf}}{kT}\right) \tag{3-8}$$

And the T is 300 K, σ_T = 4 × 10 $^{-13}$ cm^2 (capture cross-section), v_t = 2.6 × 10^7 cm·s^{-1} (thermal velocity) and N_c = 2.2 × 10 ^{18} cm^{-3} (density states in GaN conduction band) [120].

To perform the correction for leakage in LiNiO device, R_{se} as function of V_G is the |Z| at 100 MHz around the second V_G rising edge. G_t as function of V_G is the G_c measured at 1 kHz. This correction is only used in the second rising edge of LiNiO device. As for the first rising edge of LiNiO and SiO_2 device, no R_{se} and G_t corrections were used. On the second rising edge of the SiO_2 device, only R_{se} correction was applied.

LiNiO is a special material because the hole traps in LiNiO can be extracted at both the first and second rising edges. The first rising edge in CV is a staggered-II type configuration due to the alignment of the LiNiO and AlGaN/GaN bands. The hole at the LiNiO and AlGaN interface is also involved in the trapping process, since the valence band of LiNiO is quite close to the fermi level of AlGaN [124].

Two rising edges are used to determine the LiNiO/AlGaN trap density. In the LiNiO device, two types of traps are observed during the sweep of V_G from -3.5 V to -2.8 V. The shallow one originates from electron traps and the deeper one from hole traps. In the SiO_2/AlGaN/GaN MOSC structure, only the trap states are observed in AlGaN/GaN. However, in the LiNiO device for which the same epitaxy is used, these trap states are not observed. The reason is the same V_G range for testing the two devices, but the SiO_2 MOSC has already turned on in this voltage range. In the GaN channel E_C has already dropped below the Fermi level to form 2DEG, so the trap states can turn on or off. While in the LiNiO device E_C is still above the Fermi level, making the trap states far from the Fermi level and leading to the failure of realizing the trapping-detrapping. For the second rising edge, the SiO_2 device has two trap states. One has the same density and depth as the first rising edge measurement of the SiO_2 device and should be at the AlGaN/GaN interface. For the LiNiO device, only one state is observed to be at the same level as the electron trap in the first rising edge measurement. In this voltage range, only the electron trap at the LiNiO/AlGaN interface can respond to the frequency change. The barrier channel interface trap still cannot be observed in the LiNiO device. This may be attributed to the fact that only the shallowest trap state can respond to a small signal when the gate junction is turned on. LiNiO has a lower density of interface traps than normal NiO_x [124].

3.6.8 Benchmarks

Table 3-3 summarizes the device performance in this work and compares it with other e-mode devices engineered using gate stacks. This work shows high positive V_{TH} on a low R_S substrate and good R_{ON} and V_{BR} were achieved at the same time. Compared with the NiO_x device, the LiNiO device exhibits much higher I_{ON} and achieves higher V_{TH} on a wider fin and a more conductive substrate. This means that LiNiO has much stronger pinch-off capability compared to sputtering NiO_x and exhibits high performance through device optimization. Compared with a tri-gate device using metal with high work function, the required fin width for e-mode operation is reduced from 36 nm to 81 nm, which is much more practical in terms of fabrication. The tri-gate device made of negatively charged oxide cannot perform e-mode operation in log scale. The tri-gate device with electron trap shows high performance with good V_{TH} and small R_{ON}. However, the initialization process and instability at negative gate bias make it difficult to use as a power device. The tri-gate device with recessed gate can also show high performance, but the process of recess and tri-gate make it less attractive; it greatly increases the process difficulty of tri-gate structure (barrier etching of recess-gate structure).

Table 3-3 Comparison of reported high-performance e-mode tri-gate AlGaN/GaN HEMTs

References	This work	[70]	[58]	[67]	[66]	[78]	[56]
Technologies	LiNiO	NiO_X	High Φ metal	Neg. charge	E-trap	Recess	Recess
$V_{TH}{}^{a}$ (V)	0.7	0.45	0.6	0	2.61	1.4	0.53
SS (mV/dec.)	63	63	110	64	64	95	86
$V_{BR}{}^{b}$ (V)	1270	650	1100	150	900	1700	600
R_{ON}(Ω·mm)	8	9.42	7.4	4.5	12	7.32	13.8
R_S(Ω/sq.)	275	480	275	450	256	NA	NA
I_{max}(A/mm)	0.38	0.185	0.58	0.67	0.9	0.62	0.45
W_{Fin} (nm)	40	60	20	130	100	200	160
$W_{Fin,\,max}{}^{c}$(nm)	81	68	36	130	200	NA	NA

[a]Extracted at $I_D = 1\mu A/mm$.

[b]Under floating substrate except for the third work, V_{BR} was taken at $I_D = 10\ \mu A/mm$.

[c]Interpolating from fin width versus V_{TH}, the maximum fin width of e-mode operation (at 1μA/mm).

3.7 Conclusion

In summary, in this thesis we have presented a LiNiO p-type oxide as a heterojunction gate. In combination with a tri-gate structure, e-mode operation with good R_{ON}, V_{BR}, excellent *SS* and $I_{D,\ max}$ is achieved. The tri-gate W_{Fin} requirement to achieve e-mode operation is significantly reduced from 36 nm to 81 nm. In addition, the high stability, flexibility, and interface quality of this low-temperature oxide show great potential for power applications.

Chapter 4 E-mode multi-channel tri-gate device with LiNiO junction gate

4.1 Multi-channel lateral GaN transistor towards ultra-high performance

The lateral GaN (MOS) HEMT is an ideal solution for low/medium voltage rating applications. GaN HEMT structure has a high μ and N_S 2DEG, which is suitable for high power density and high-frequency applications. However, the device performance of GaN lateral device still does not pass the SiC power FOM line. The main challenge of improving the device performance towards material limitation is to reduce the device resistance (R_{ON}) while maintaining high voltage blocking ability (V_{BR}). Traditionally, increasing barrier thickness or increasing the Al content in the barrier can be used to increase the N_S in the channel, however, the large N_S in the channel can reduce the μ, and also hard to pinch-off which is not beneficial for e-mode operation.

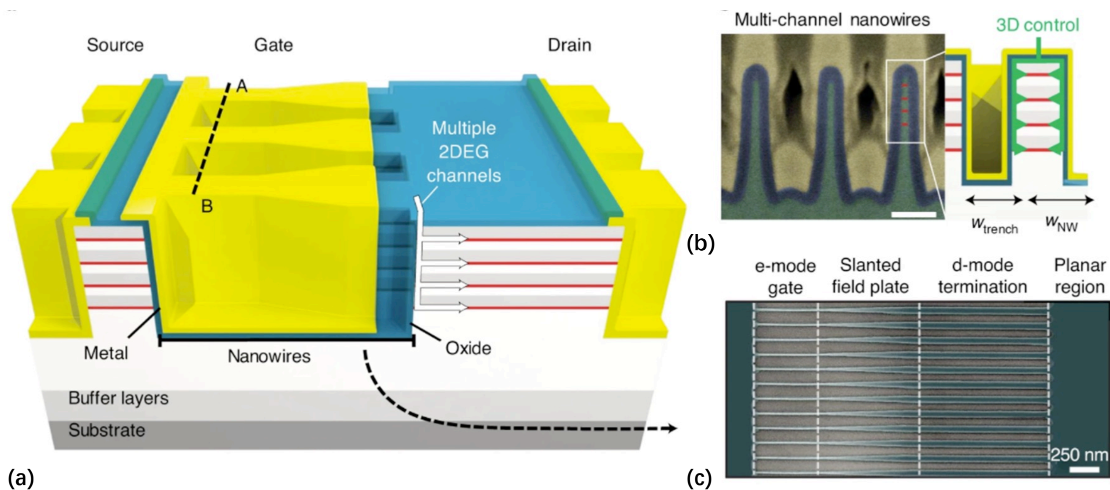

Figure 4-1 Concept of multi-channel tri-gate devices. (a) Three-dimensional schematics of the proposed multi-channel device, featuring multiple parallel channels, to yield extremely low R_{ON}, controlled 3-dimensionally by a tri-gate electrode. The tri-gate is terminated in the nanowire region, rather than on the planar region, to better distribute the electric field and result in high V_{BR}. (b) FIB cross-section and schematics of the multi-channel nanowires covered by the tri-gate structure along the AB line in figure (a). The tri-gate enables simultaneous 3D control over all the multiple channels in the nanowire. The scale bar is 100 nm. (c) Top SEM image of the nanostructured gate area (before the gate oxide and electrode deposition) [73].

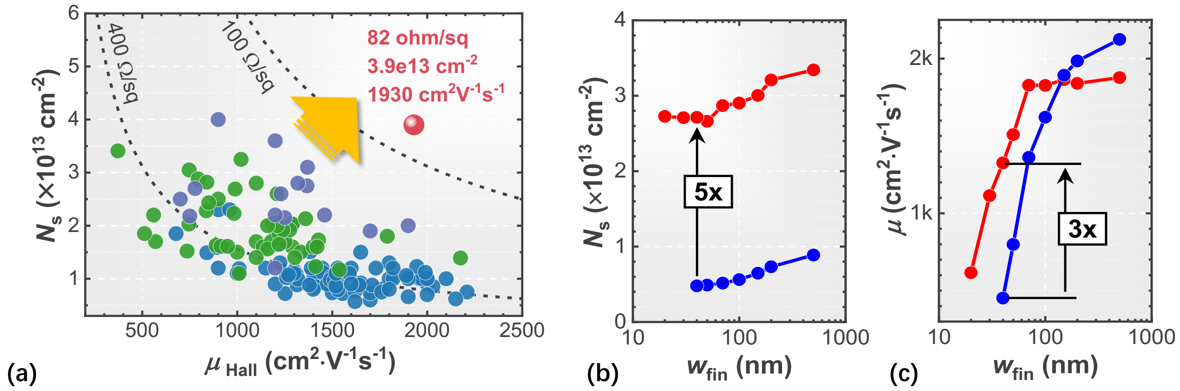

Figure 4-2 (a) Benchmark of the sheet resistance (R_S) of the 4-channel heterostructure in this work against conventional single-channel GaN-based heterostructures in the literature, with AlGaN, InAlN, and AlN barriers. High μ of 1930 $cm^2 \cdot V^{-1}s^{-1}$ was achieved in combination with a large N_s of 3.9 x 10^{13} cm^{-2}, resulting in R_S of 83 Ω/sq. (b)(c) N_s and μ for multi-channel nanowires (red) and single-channel nanowires (blue) with different widths, measured by Hall Bars at room temperature. High μ above 1800 $cm^2 \cdot V^{-1}s^{-1}$ was maintained down to 70 nm-wide nanowires along with a large N_s, in the range of 2.8 – 3 x 10^{13} cm^{-2}. The multiple channels are defined into Tri-gate fin structure in the gate region of the device (Figure 4-1), three-dimensional MOS gate was formed to control the parallel channels from the side gate and top gate. In the Tri-gate fin design, a slanted tri-gate fin was used to regulate the electric fields to high a high V_{BR}. From the multi-channel tri-gate device a very high FOM was successfully demonstrated which surpassed the state-of-the-art result, offering a promising way for future high-performance lateral GaN power devices [73].

Apart from solely increasing N_S in the single 2DEG channel, we stacked multiple heterostructures with 2DEG channels. It allows a large number of N_S distributed in the vertical direction, the μ of the carrier was kept at a high value. And this overcomes the trade-off between N_S and μ with respect to the single 2DEG channel. In the multi-channel epitaxy, the top three channels were formed by 20 nm $Al_{0.25}Ga_{0.75}N$ barrier layers, with Si doping of 1 × 10^{19} cm^{-3}, and 1 nm AlN spacer and 20 nm GaN channel layers. The fourth (bottom) channel has a 10 nm $Al_{0.25}Ga_{0.75}N$ barrier with Si doping of 5 × 10^{18} cm^{-3}. The epitaxy from this design resulted in a very low R_S of 83 Ω/sqr. and large N_S of 3.9 × 10^{13} cm^{-2} which is four times higher than over single-channel epitaxy. And due to the multi-channel spreading carrier in the vertical direction, the μ was kept at a very high value of 1930 $cm^2 \cdot V^{-1} \cdot s^{-1}$. The total channel thickness was ~ 130 nm which is within the design and process capability of the tri-gate structure [73].

Figure 4-3 (a) V_{BR} versus R_{ON} and (d) $R_{ON,\,SP}$ versus V_{BR} benchmarks of the slanted tri-gate multi-channel MOSHEMTs against conventional single-channel GaN (MOS)HEMTs in the literature. Multi-channel devices surpass the material figure-of-merit limit of 4H-SiC, showing a substantial improvement with respect to single-channel devices and a record figure-of-merit of 4.6 GW/cm^2 for d-mode devices and 3.8 GW/cm^2 for e-mode devices. A transfer length of 1 μm from each side has been considered to evaluate $R_{ON,\,SP}$ [73].

The main achievement of the multi-channel tri-gate device is its ability to electrostatically control epitaxy with high conductivity. By using a tri-gate structure around the multi-channel nanowires, gate control occurs from three sides simultaneously.

According to Hall-bar measurements of different fin widths of the multi-channel nanowires, the mobility decreases for narrow nanowires due to roughness scattering and donor-like (positive if empty) states on the sidewalls [125, 126]. A high mobility of over 1200 cm^2·V^{-1}·s^{-1} has been measured for 20 nm nanowires in the on-state. The V_{TH} can also be modulated by W_{Fin} using narrow fin and Pt gate electrodes with high work function. Despite the high N_s of 3.9 x 1013 cm^{-2} of the whole epitaxy, a V_{TH} of 0.85 V (defined by 1μA/mm) has also successfully demonstrated. Moreover, the e-mode is presented together with a very low R_{ON} of 2.5 Ω·mm. This result is more than a two-fold reduction from R_{ON} compared to state-of-the-art single-channel e-mode devices. The same process for e-mode and d-mode devices enables easy integration of e-mode and d-mode devices on the same chip, which is beneficial for GaN power logic switching. Apart from the small R_{ON}, the slanted tri-gate structure also results in good voltage blocking performance. A high V_{BR} of 1300 V (I_D = 1 μA /mm) has been demonstrated with the following three designs: (1) The gate is terminated on the fin instead of the planar region in the single-channel devices, which can avoid early oxide breakdown due to the high electric field at the end of the fin. (2) The slanted tri-gate design balances on-state performance with channel pinch-off performance. It reduces the length of the narrow fin section in the slanted tri-gate structure and distributes the electric field evenly in both vertical and lateral directions (source to drain). (3) A second mesa is used in a multi-channel device to better isolate the devices.

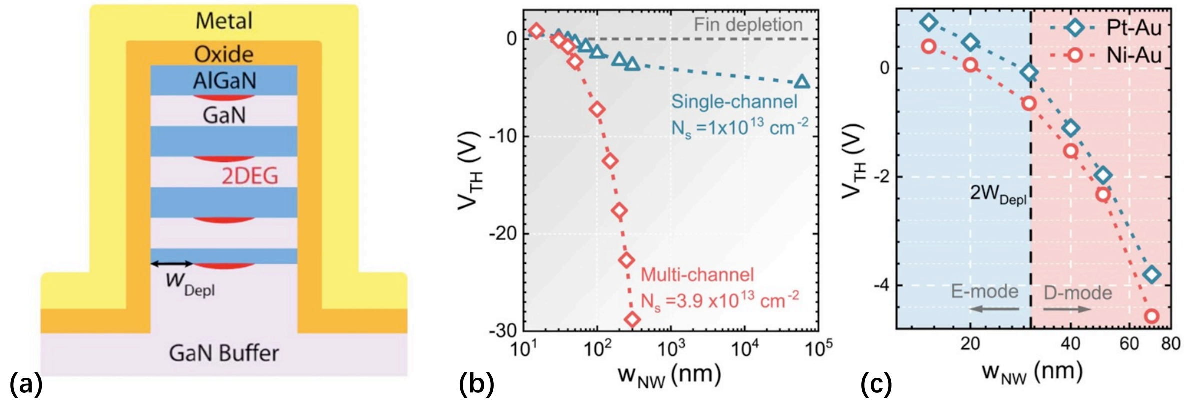

Figure 4-4 (a) The depletion width indicates the minimum nanowire width to achieve e-mode operation since for $W_{NW} < 2\ W_{Depl}$ the depletion regions from the two sidewalls merge in the center and eliminate the 2DEG. (b) It should be noted that while in general a much higher gate voltage is required to turn off a multi-channel nanowire with respect to a single-channel one due to its larger carrier density, for small nanowire widths such difference becomes smaller and multi-channel devices show very similar V_{TH} with respect to single-channel counterpart for W_{NW} below 50 nm, despite the much larger N_s. This is due to the predominant side gate control and to the strong sidewall depletion at such narrow widths, which is similar for multi- and single-channel nanowires. (c) The evaluation of the sidewalls depletion width is consistent with the device transfer curves, which indicate 30 nm as the minimum nanowire width to achieve positive V_{TH}. To further shift V_{TH} to positive values, the conventional Ni-Au gate metal stack was replaced by a Pt-Au gate metal, which resulted in a threshold voltage increase of about 0.5 V. Such improvement, which is consistent for different W_{NW}, derives from the higher work-function of Pt with respect to Ni and allows to increase V_{TH} without any degradation of the channel, resulting in large V_{TH} of 0.85 V for 15 nm-wide nanowires [73].

GaN-based multichannel tri-gate MOSHEMTs have emerged as a promising technology for future high-performance power transistors for low/medium voltage applications [37, 73, 74, 82, 127]. The multiple vertically stacked 2DEG channels offer a way to overcome the trade-off between N_S and mobility (μ). Excellent gate control and modulation of the multiple channels is demonstrated by tri-gate structures, resulting in a significant reduction of the device R_{ON} without sacrificing V_{BR} [73, 74]. Despite this progress, achieving e-mode operation with large V_{TH} in such structures with high N_S is still a major challenge. MOS Tri-gates that rely on sidewall depletion to pinch off multiple 2DEGs in the gate region have achieved e-mode operation with a V_{TH} of ~0.9 V (defined at 1 µA /mm) [73, 74]. But use of gate dielectrics such as SiO_2 and Al_2O_3 (typically deposited by ALD and PECVD) has serious drawbacks in terms of V_{TH} stability and reliability due to their relatively low quality. On the other hand, the high deposition temperature required for a high-quality oxide can degrade the etched GaN surface, which can be detrimental especially for tri-gate structures [30, 81, 82]. Consequently, the most reliable technology available in the market to achieve the e-mode is based on the p-(Al)GaN gate that lifts the conduction band of the GaN channel to locally deplete the 2DEG [32, 118, 128]. Nevertheless, the application of this technology to multi-channel tri-gate structures is challenging due to the difficulty in controlling the p-(Al)GaN growth over the nanoscale structure in tri-gates and degradation of the GaN surface at the high growth temperature. Recently, p-type NiO

[70, 129] and LiNiO [11] have been proved useful for e-mode operation in single-channel tri-gate structures. In particular, LiNiO offers an effective solution due to its low band offset from AlGaN, tunable hole concentration from 1×10^{16} cm^{-3} to 6×10^{21} cm^{-3}, and low deposition temperature of 400 °C [75, 130]. In this chapter, we demonstrate an e-mode multi-channel junction tri-gate AlGaN/GaN HEMTs by successfully integrating a high-quality p-type LiNiO gate layer at low temperature on a multi-channel tri-gate platform. The devices show high performance with large and stable V_{TH} at high temperature.

4.2 Process and optimization

4.2.1 Device design

The epitaxial structure consisting of four AlGaN/GaN channels is the same as that in Ref. [73], which presents a large N_S of 3.9 x10^{13} cm^{-2} and μ of 1,930 cm^2·V^{-1}·s^{-1}, resulting in a low R_S of 83 Ω·sq^{-1}.

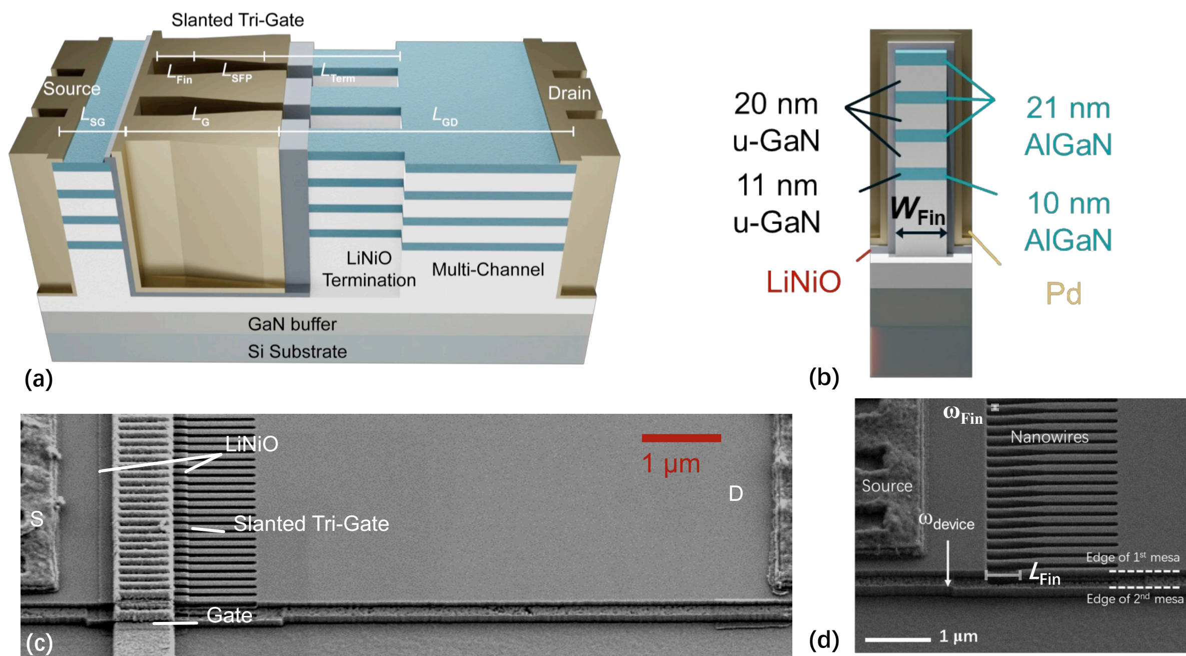

Figure 4-5 (a) 3D schematic of fabricated multi-channel tri-gate HEMT with LiNiO gate oxide, featuring four parallel channels. In the slanted tri-gate region, the Gate metal and LiNiO gate oxide both terminated in the nanowire region. (b) cross-section schematic of single tri-gate structure covered with LiNiO gate oxide and Pd gate metal. (c) Tilted top-view SEM image of the fabricated device, a second mesa structure, and precise pattern LiNiO are included. (d) Tilted top-view SEM image of the device before LiNiO patterning and gate. A clear shrink design of the second mesa can be observed from the image. Apart from the second mesa, sharp results of slanted tri-gate Fin can also be observed. From tilted view. The narrow region of nanowires has the same height as other parts, the AlGaN barrier didn't consumed during the dry etching process of the Fin.

The device fabrication started with mesa isolation and definition of the tri-gate fins by ebeam lithography (EBL), HSQ (2%) was used as ebeam resist. After exposure and development, HSQ will convert into SiO_2 as etching mask. A 2 nm-thick Ti glue layer to enhance the HSQ adhesion to GaN surface [131]. The mesa and fin structures were etched by Ar/Cl_2 inductively coupled plasma etching (ICP) with a depth of 250 nm. 4 cycles of digital etching were used to remove sidewall damages during the dry etching [73, 132] which includes 1min 600 w oxygen plasma etching and 1min dipping in 37% HCl. To better isolate the device, a second mesa was patterned by a thicker HSQ (6%) layer and etched with a depth of 200 nm. The ohmic metal stack composed of Ti/Al/Ti/Ni/Au was defined in the source and drain regions, followed by rapid thermal annealing (780 °C, 30s with N_2 as protective gas).

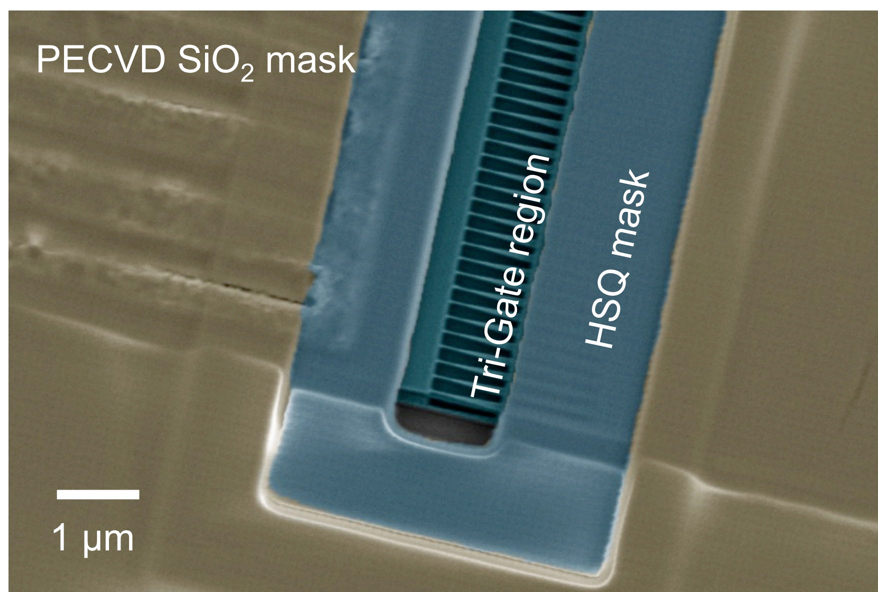

Figure 4-6 Top-view SEM image of additional HSQ mask before LiNiO deposition. HSQ mask and PECVD mask can be observed from the image. Slanted tri-gate and second mesa were also shown.

A 250-nm-thick SiO_2 (300 °C) was deposited by PECVD as an etching stop layer of ion beam etching (IBE) for the LiNiO patterning. To precisely define the LiNiO oxide layer in the gate region, a 180 nm thick HSQ layer was patterned to serve as a lift-off mask. The LiNiO deposition was done by pulsed-laser-deposition (PLD) [75, 76] at 400 °C with a thickness of 70 nm, followed by IBE dry etching. Finally, the gate electrode was defined by EBL followed by deposition of the ohmic gate stack consisting of Pd (50 nm)/Au (250 nm).

4.2.2 Isolation optimization

One difference between multi-channel and single-channel tri-gate devices is the etch depth. For multi-channel (250 nm), the etch depth for the tri-gate fin structure is deeper than for single-channel (180 nm) due to the difference in the overall thickness of the conducting layers. This etch thickness is limited by the consumption of the HSQ mask during dry etching. Especially if the fin width is reduced to 15 nm, the actual thickness of the HSQ on the fin after exposure and development would be less than 60 nm, which will be largely consumed at ICP RIE. 250 nm is already the maximum depth that this process flow could achieve. But it is not deep enough to isolate the device.

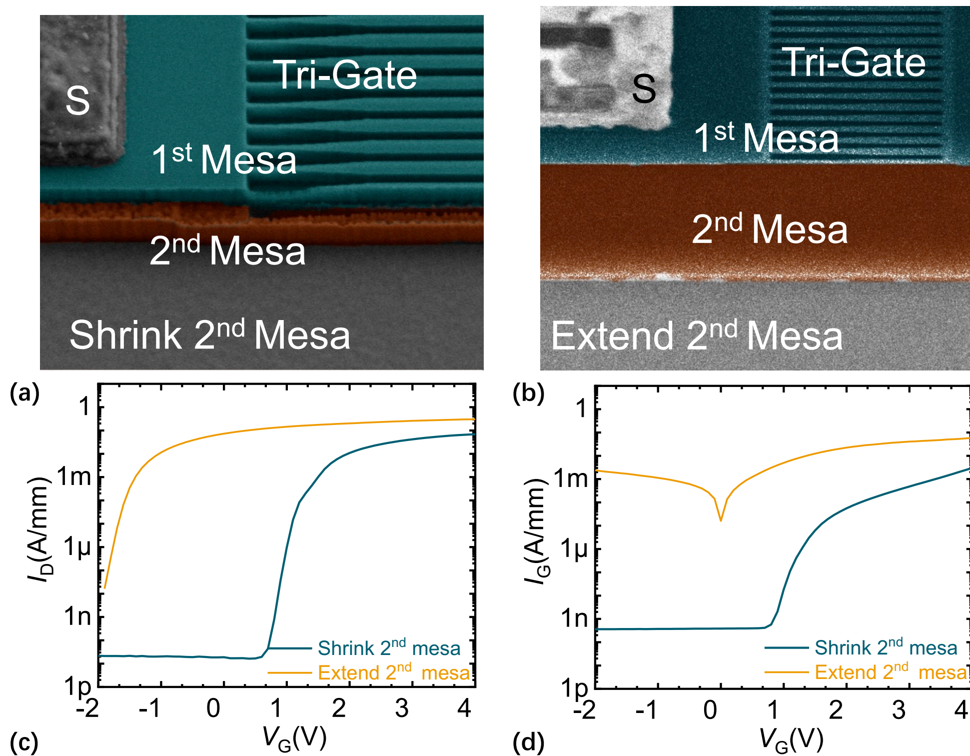

Figure 4-7 (a) Tilted top-view SEM image of shrink second mesa process. (b) Tilted top-view SEM image of extend second mesa process. (c) I_D versus V_G of shrink and extend the second mesa. (d) I_G versus V_G of shrink and extend the second mesa.

For the LiNiO multi-channel gate device, the etch depth of the fin was set at 250 nm to preserve a thicker barrier on the top of the fin without consuming HSQ, to ensure better on-state performance. But the mesa, which is fabricated in the same step as the fin structure, is not enough to isolate the devices; there would be a large cross-mesa leakage between two devices. And the gate can no longer control the device. To break the leakage path, a second mesa method was used (Figure 4-7). When the second mesa is larger than the first mesa and etched before gate deposition, the second mesa becomes a large planar MOSFET, resulting in high leakage and negative V_{TH}. A shrink mesa design can solve this problem and results in low off-state leakage.

4.2.3 LiNiO patterning process optimization

In addition to optimizing the isolation process, a special precise patterning process for LiNiO is also developed to obtain a high-performance multi-channel junction device. Due to the small L_{SG} in multichannel devices (to achieve the lowest possible R_{ON}), the use of the PECVD- SiO_2 lift-off process results in a connection between gate and source through the LiNiO layer. When the device is negatively biased, most of the gate and drain current is caused by the source/LiNiO/gate current path. To pattern the LiNiO more precisely, a second HSQ lift-off mask is used after the first PECVD SiO_2 lift-off mask. IBE during lift-off is performed in the PECVD SiO_2 region to avoid over-etching of the GaN surface on the thin HSQ part. BHF wet etching can lift all the oxide masked LiNiO from below. There are two versions of this second HSQ lift-off mask, which differ at the location of the LiNiO termination. In version 1 (Figure 4-8 (b)), the LiNiO terminates at the planar part in the drift region, while in version 2 (Figure 4-8 (c)), the LiNiO terminates on the fin structure and does not touch the planar part.

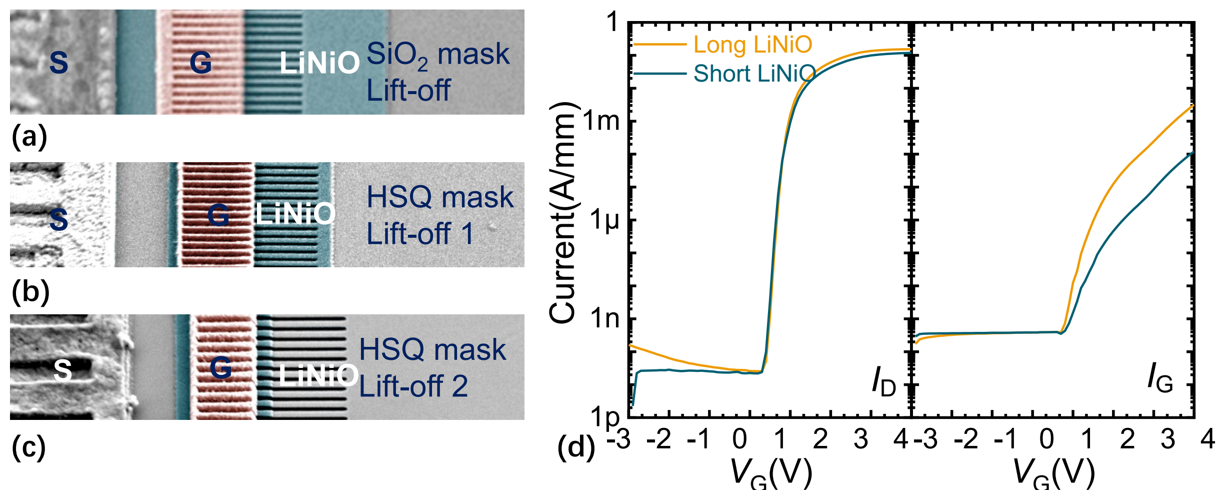

Figure 4-8 (a) Fabricated device with PECVD SiO_2 lift-off mask patterned LiNiO. (b) Fabricated device with additional HSQ patterned LiNiO. LiNiO terminated outside of the Fin. (c) Fabricated device with additional HSQ pattern LiNiO, LiNiO terminated on the Fin. (d) Transfer behavior of two LiNiO termination devices.

Comparing the results of these two designs, we see device with the long termination has higher leakage at reverse V_G and high I_G at positive bias. The long LiNiO termination part would become a leakage path, which is not benefit the on-state performance and leads to leakage in the device. In the fabrication of the second HSQ pattern, the LiNiO layer can be locally deposited with an opening width of less than 1 μm.

4.2.4 Other process optimization

To achieve high resolution, the thin PR is always used. However, our experiment shows that the thin 2% HSQ is not suitable for our junction gate multi-channel device. The thin HSQ in RIE is rapidly consumed, so the 15 nm wide fin top barrier can be strongly etched. The alternative method we resort to is to use thicker HSQ (6%) exposed at a high dose, as well as strong vibrations and a long development time in development process. This method achieves the same resolution but a better-preserved barrier. An interesting effect here is that the V_{TH} of 6% and 2% HSQ devices is the same, while the I_{ON} is increaed. This shows that the multi-channel tri-gate fin is fully exhausted. Even if the gate is partially recessed in the upper channel barrier, the V_{TH} will not shift further.

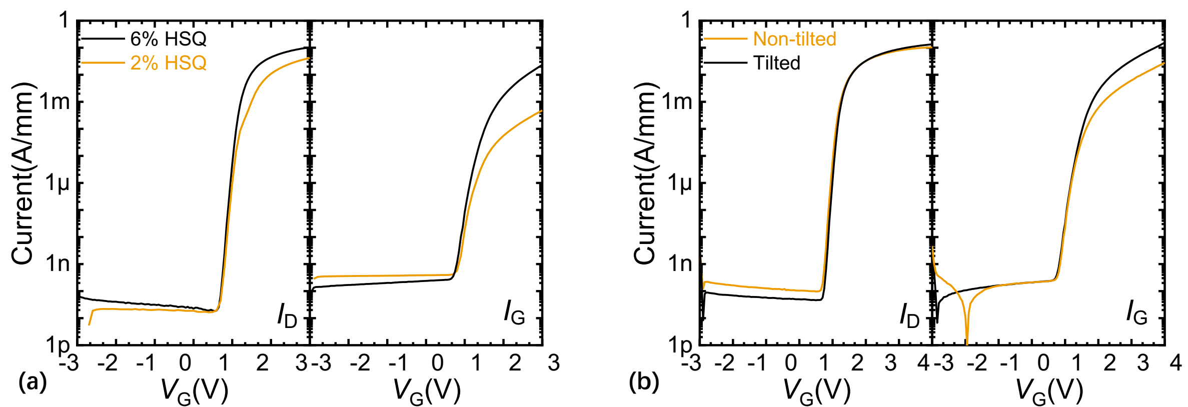

Figure 4-9 (a) Comparison of transfer behavior with two different thicknesses HSQ used for tri-gate nanowire patterning. (b) Comparison of transfer behavior tilted and non-tilted deposition during the PLD deposition process of LiNiO.

The multichannel device has a higher fin, so it is even more difficult to achieve uniform coverage with LiNiO across the fin. To achieve better step coverage, the distance between two fins was increased to more than 100 nm, so that the aspect ratio between fin and cavity is reduced. In addition, the tilted deposition method was tested. Here, the chip was tilted 10 degrees during deposition and deposited twice on each side of the fin. The result (Figure 4-9 (b)) shows that the tilted deposition device has lower gate leakage current at high V_G bias voltage, indicating better step coverage with this technique.

4.3 Static performance

The transfer characteristics of devices with different tri-gate fin widths and the same fin length of 1 μm are shown in Figure 4-10 (a). The decrease of W_{Fin} results in fewer carriers in the channel, thus shifting V_{TH} towards positive values. E-mode operation was possible for all devices with W_{Fin} below 30 nm. All measurements in this work were normalized by the entire width of device width (W_D) (if not otherwise mentioned). Figure 4-10 (b) shows the increase in V_{TH} for longer L_{Fin} and narrower W_{Fin}. P-type LiNiO junction gate resulted in an over 0.5 V shift in V_{TH} compared with the most positive V_{TH} achieved on MOS tri-gate structures with the same W_{Fin}. The maximum V_{TH} achieved on LiNiO multi-channel devices was 1.2 V (for W_{Fin} of 15 nm and L_{Fin} of 1.5 μm), which is very close to the theoretical prediction for e-mode tri-gate device [133]. Figure 4-10 (c) presents the V_{TH} dependency with W_{Fin} and L_{Fin}. And multi-channel and single-channel can achieve a similar level of maximum V_{TH} (Figure 4-10 (d)).

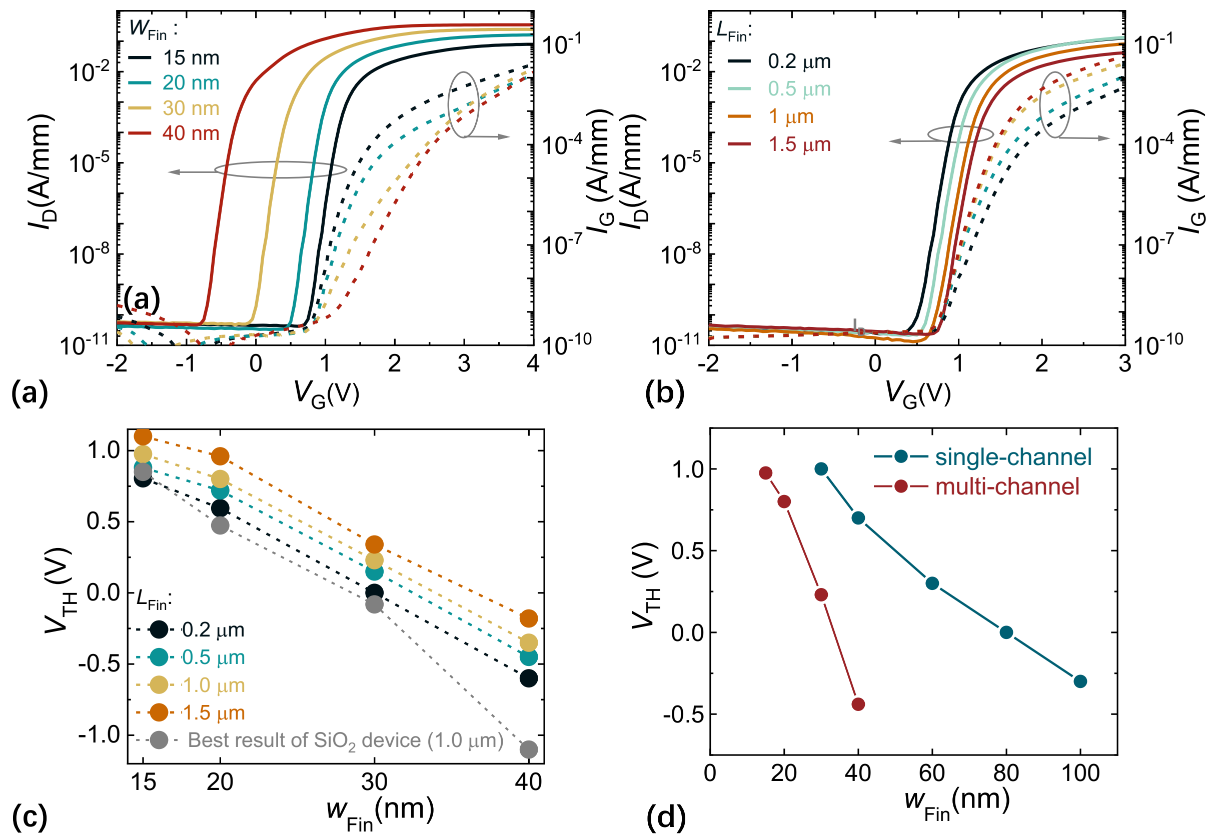

Figure 4-10 (a) Transfer (V_D = 5 V) characteristics of multi-channel tri-gate HEMT with LiNiO. Different tri-gate Fin width (W_{Fin}) devices are included, the length of Fin (L_{Fin}) was set to 1 μm. (b) Transfer (V_D = 5 V) characteristics of multi-channel tri-gate HEMT with LiNiO. Different Tri-gate Fin length (L_{Fin}) devices are included, the width of Fin (W_{Fin}) was set to 15 nm. (c) V_{TH} (defined at 1 μA/mm) versus W_{Fin} and L_{Fin}, compare to the most positive V_{TH} ever achieved on the same epitaxy, with different gate oxide and metal. Using LiNiO/Pd gate combination results in a nearly 0.5 V V_{TH} shift towards positive in small $W_{Fin} \leq 30$ nm and shift nearly 1 V at W_{Fin} = 30 nm. (d) V_{TH} dependence of W_{Fin} of single-channel and multi-channel LiNiO junction gate transistor.

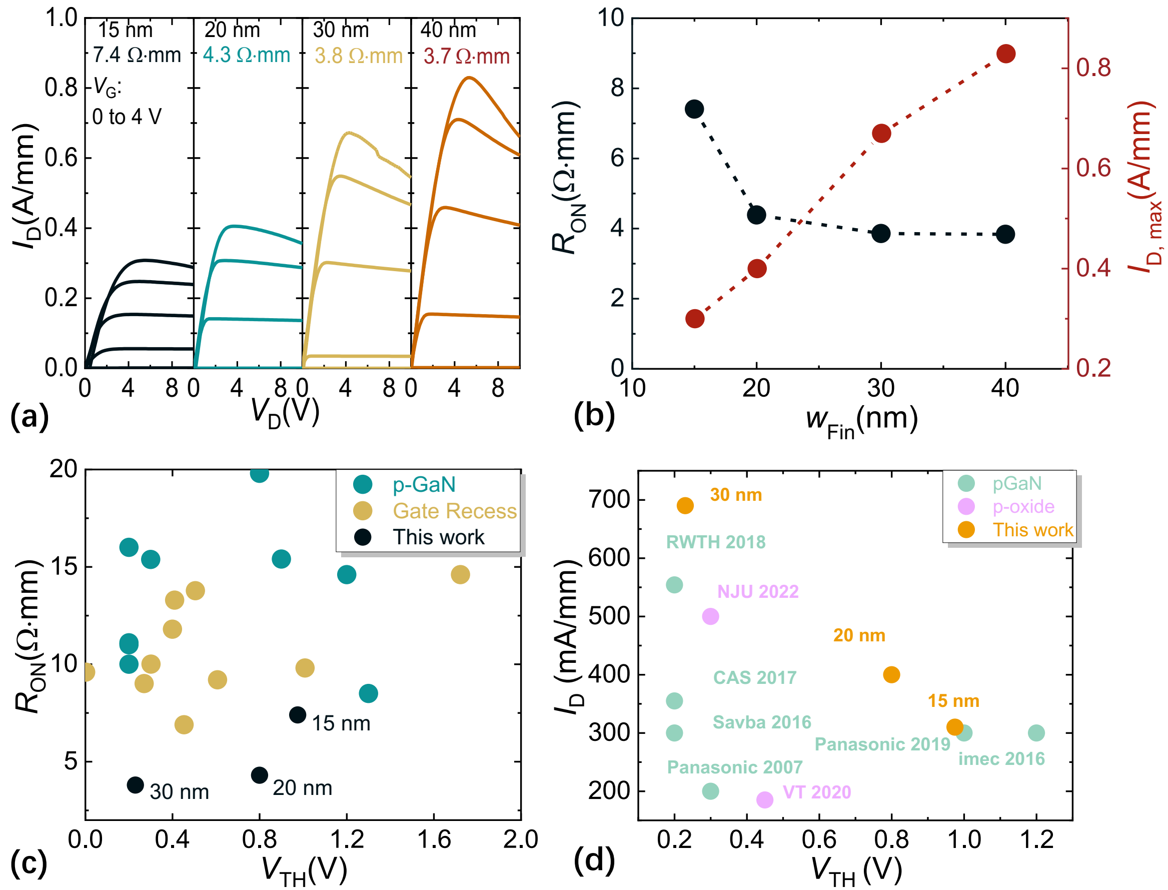

Figure 4-11 (a) Output characteristic of different W_{Fin}, the L_{Fin} was set to 1.0 µm. (b) R_{ON} (extracted at V_G of 4 V) and $I_{D, max}$ versus W_{Fin}. (c) R_{ON} versus V_{TH} benchmark for presented device compared state-of-the-art single-channel e-mode devices through p-GaN gate and gate recess methods from the literature. Multi-channel devices present a more than two times lower R_{ON} for the same V_{TH} with respect to the reported p-GaN gate e-mode devices, and most gate recess e-mode devices. V_{TH} has been defined at 1 µA/mm. Recess gate devices always drive at a much higher V_G.

Figure 4-11 (a) shows the dependence of the output characteristics on W_{Fin}. As summarized in Figure 4-11 (b), devices with smaller W_{Fin} present a higher R_{ON} and lower maximum driving current ($I_{D, max}$), which is due to their increased resistance as well as the over-etching of the fin, especially for the narrower fins (W_{Fin} of 15 nm). In addition, to keep the slanted tri-gate portion constant for a fair study, the number of tri-gate fins was fixed, which resulted in a reduction of $I_{D, max,}$ and increase in R_{ON} with a decrease in W_{Fin}, as they are normalized by the entire W_D. This degradation could be mitigated by increasing the number of fins in the same W_D as well as by improving the etching process for the narrow fins An unprecedented low R_{ON} was achieved at similar V_{TH} when compared to state-of-the-art e-mode devices by the p-GaN gate or p-oxide gate structure (Figure 4-11 (c)), resulting in a $R_{ON, sp}$ of 0.62 mΩ·cm^{-2} (by considering a 1 µm transfer length at each source/drain sides). This corresponded to an excellent FOM of 1.36 GW/cm^2.

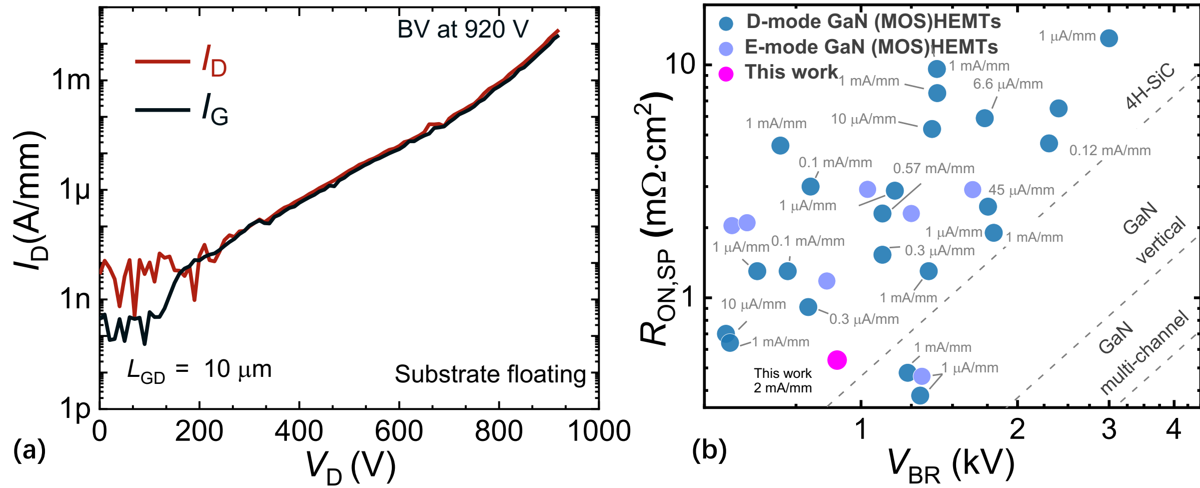

Figure 4-12 (a) Three terminal breakdown characteristics of the device (W_{Fin} = 20 nm, L_{Fin} = 1.0 μm) at V_G = 0 V (under floating substrate with fluorinert). (b) $R_{ON,SP}$ versus V_{BR} benchmarks of the LiNiO multi-channel junction gate transistor against conventional single-channel GaN (MOS)HEMTs in the literature. It shows a very high figure-of-merit of 1.63 GW/cm^2. A transfer length of 1 μm from each side has been considered to evaluate $R_{ON,SP}$. This is the highest FOM ever achieved on junction gate type GaN HEMT device, and only worse than the multi-channel MOSHETM from our previous work.

Figure 4-12 (a) presents the breakdown voltage characteristic of proposed devices (L_{Fin} of 1 μm and W_{Fin} of 20 nm). Owing to the well-distributed electric field by slanted tri-gate structure [14, 56, 60, 74], the device presents V_{BR} (hard breakdown) of 920 V, and most of the off-state current was through the gate ($I_G \approx I_D$). The gate leakage current could be reduced by improving the coverage and thickness of the LiNiO over the tri-gate sidewall, offering a large room for further improvement on V_{BR} [130]. Figure 4-12 (b) benchmark the LiNiO junction gate multi-channel device with state-of-the-art e-mode devices. LiNiO device presents the highest FOM over existing e-mode GaN lateral power transistor using gate recess or p-GaN technology.

4.4 Gate charge and mobility measurements

Gate charge (Q_G) is a major consideration of the switching losses in a high-frequency power circuit. Hence, it is important to monitor the Q_G. The traditional method is to use the integration of I_G over time during the gate turn-on process. However, this method requires a very large test structure and requires an insulating substrate [134].

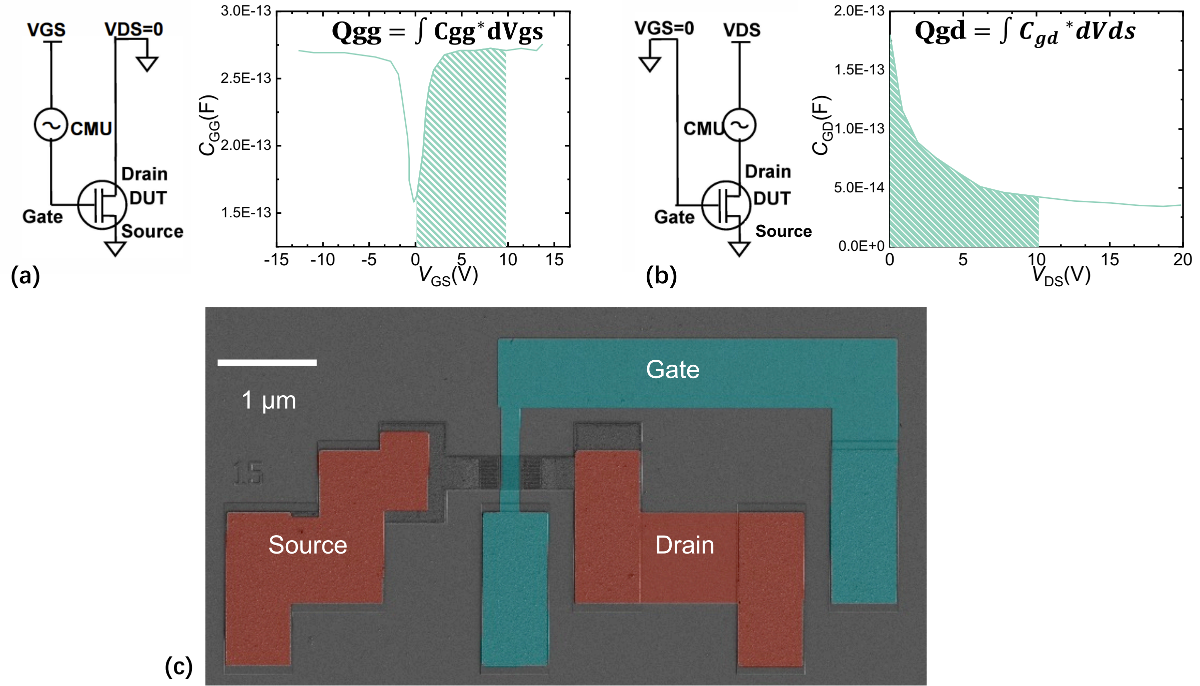

Figure 4-13 CV integration method for measuring gate charge. (a) Plot shows the gate charge component (Qgg). The Qgg is the integration of the shadow part in the curve. (b) Plot shows the gate charge component (Qgd). The Qgd g is the integration of the shadow part in the curve. (c) top-view SEM image of long L_{Fin} (10 µm) for accurate capacitance measurement.

An alternative method to estimate the Q_G was proposed in [134]. The device turn-on process was divided into three steps: (1) Device turns on and the current starts flowing: V_{GS}=0> V_{GP} with V_{DS}-V_D (2) Device is on, the V_{DS} drops from the blocking state (V_{DD}) to V_{ON} (~0): V_{GS} -V_{GP} with V_{DS}=V_{DD}->V_{ON} (3) V_{GS} increases to its final value (V_{GG}): V_{GS}=V_{GP}->V_{GG} with V_{DS}-V_{ON}~0.

$$Qg = \int_0^{Vgp} Cgg * dVgs\Big|_{Vds=Vdd} + \int_{Vdd}^{0} Cgd * dVds\Big|_{Vgs=Vgp} + \int_{Vgp}^{Vgg} Cgg * dVgs\Big|_{Vds=0} \quad (4\text{-}1)$$

It can be approximated by:

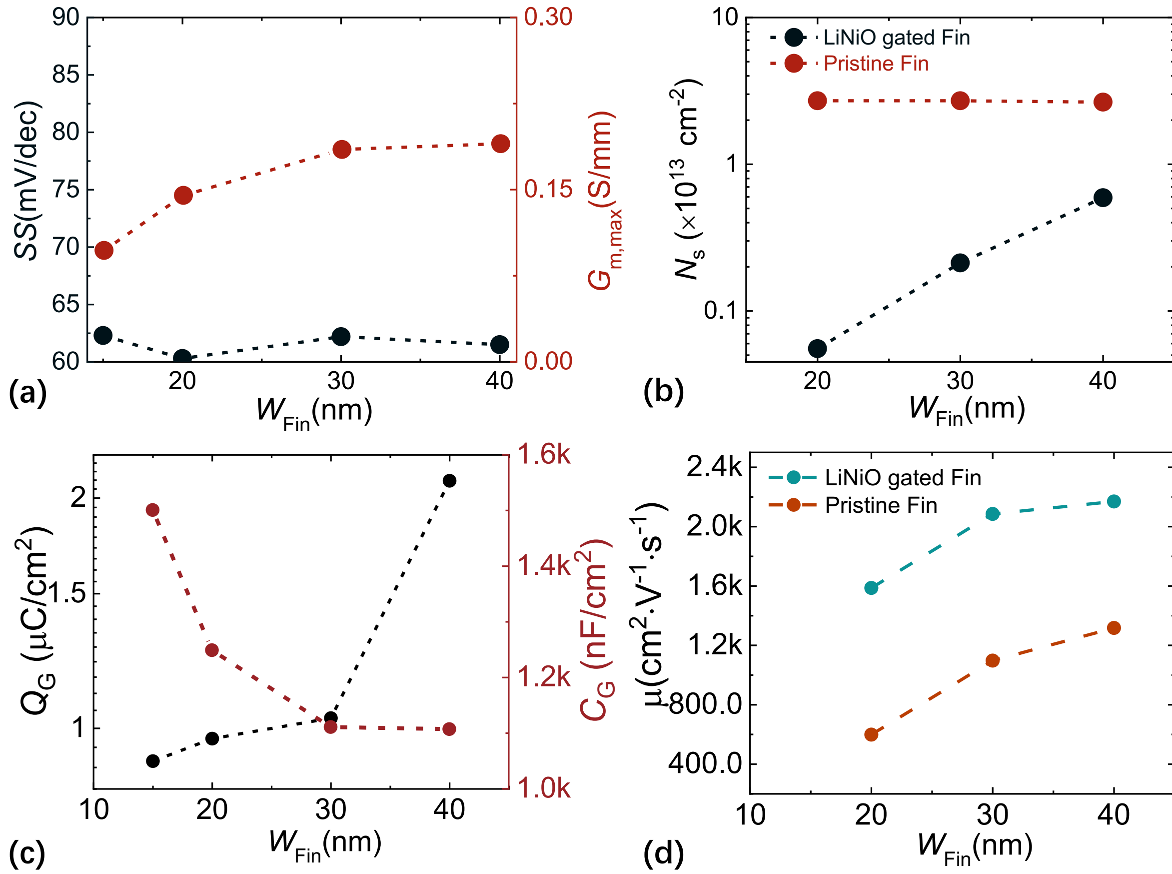

Figure 4-14 (a) *SS* and maximum transconductance ($G_{m,\,max}$) versus W_{Fin}. (b) Carrier density (N_s) of pristine tri-gate Fin without gate oxide and device LiNiO gate stack (normalized on total top surface areas of Fins) versus W_{Fin}. Over 1 order of *N*s was reduced by LiNiO gate stack. *N*s in pristine Fin was extracted by hall measurement, details can be found in [73]. And *N*s in LiNiO gate stack was extracted by CV measurement on large gate length (L_G) device, details in [127]. (c) Q_G (integrated till 0 V) and C_G (V_G = 2 V) dependence on W_{Fin}. (d) Field-effect mobility of LiNiO gated Fin and tri-gate nanowire without any process dependence on W_{Fin}.

$$\begin{gathered}
\int_0^{Vgp} Cgg * dVgs\Big|_{Vds=Vdd} \approx \int_0^{Vgp} Cgg * dVgs\Big|_{Vds=0} \\
\int_{Vdd}^{0} Cgd * dVgs\Big|_{Vgs=Vgp} \approx \int_{Vdd}^{0} Cgd * dVds\Big|_{Vgs=0} \\
Qg \approx \int_0^{Vgg} Cgg * dVgs\Big|_{Vds=0} + \int_{Vdd}^{0} Cgd * dVds\Big|_{Vgs=0}
\end{gathered} \tag{4-2}$$

Using this method, from impedance meter or LCR meter, accurate results could be gotten from measurement at ~pF level accuracy. Thus, this method is very suitable for on-wafer monitoring Q_G for power semiconductors. To extract the capacitance, relate value RF probe compatible device with 10 μm L_{Fin} (Figure 4-13). Compared with that of a pristine fin (without metal/oxide) obtained from hall measurements (Figure 4-14 (b)) [73]. A clear depletion of carriers is observed for smaller fin widths with LiNiO/Pd, which is not the case in pristine fins. The reduced N_S at V_G = 0 V makes it easier to achieve e-mode.

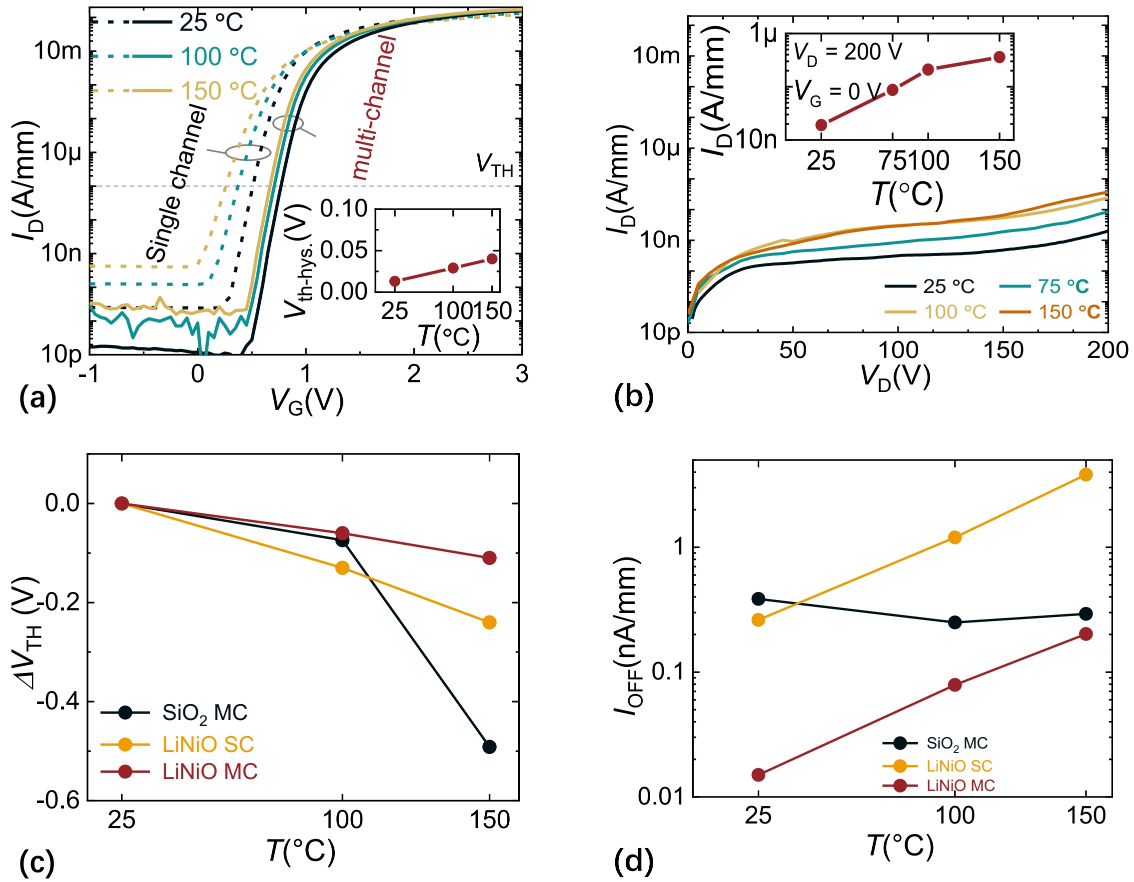

Figure 4-15 (a) Temperature-dependent transfer characteristics of multi-channel (W_{Fin} = 20 nm) and reference single-channel device (W_{Fin} = 40 nm) with measurement temperature from 25 °C to 150 °C, inset presents the V_{TH} hysteresis (defined at 1 μA/mm) of multi-channel device from a double sweep. (b) Temperature-dependent off-state leakage measurement with measurement temperature from 25 °C to 150 °C. V_G was set at 0V with floating substrate, and fluorinert was used. Inset: I_D (V_D = 200 V) versus temperature. (c) Dependence of V_{TH} and I_{OFF} of the SiO_2 MOS gate multi-channel device, LiNiO junction gate single-channel device, and LiNiO junction gate multi-channel device on the temperature. (d) Dependence of I_{OFF} of the SiO_2 MOS gate multi-channel device, LiNiO junction gate single-channel device, and LiNiO junction gate multi-channel device on the temperature

$$\mu_{FE} = G_m L/(W C_{Gate} V_{DS}) \quad (4\text{-}3)$$

Gate charge and gate capacitance are calculated from CV integration to gate operating points (V_G = 2 V) (Figure 4-14 (c)). Field-effect mobility (μ_{FE}) (Equation 4-3) (Figure 4-14 (d)) is extracted from the same measurement point at V_G = 2 V. Compared to the pristine fin, the LiNiO multi-channel nanowire with junction shows much higher mobility (the pristine fin is tested by Hall measurements at V_G = 0 V). Even the direct comparison of mobility by these two methods is limited, the LiNiO epitaxy most likely passivated the GaN surface and leads to better carrier mobility by reducing scattering events.

In addition, these devices presented outstanding stability at high temperatures compared with single-channel devices using LiNiO gate stack (with similar V_{TH} for comparison). As temperature rises from 25 °C to 150 °C (Figure 4-15 (a)), a small V_{TH} shift of -0.11 V was observed. And the leakage level was kept below 1 nA/mm at 150 °C. Moreover, the proposed devices presented a very small V_{TH} hysteresis (from double sweep transfer measurement) of 0.05 V at 150 °C. This small hysteresis reveals the great quality of the LiNiO layer, as evidenced by HRXRD measurements. Considering the high-temperature performance of multi-channel with MOS gate (shown in ref. [74]), we can conclude that the small off-state leakage increment at elevated temperature in transfer measurement s from the good device isolation, while the great quality of LiNiO results in a significant small negative shift of V_{TH} The leakage current in off-state during positive drain voltage (V_D) stress could be maintained below at 1 μA/mm at 150 °C and V_D = 200 V (Figure 4-15 (b)). This superior high-temperature voltage blocking capability is benefited from the depletion from three sides by LiNiO layer, which results in large potential height inside of fin by PN diode type gate [129].

4.5 Conclusion

In this work, we have presented high-performance multi-channel transistors together with LiNiO junction gate. Device show a positive V_{TH} up to 1.2 V (defined at 1 μA/mm), which is the largest V_{TH} achieved on such low R_S multi-channel epitaxy, near-ideal *SS* of 61 mV/dec, high on/off ratio over 9 orders, and excellent FOM of 1.36 GW/cm^2. These results indicate a promising technological path for future high-performance lateral GaN HEMTs through structural, epitaxial and gate material development.

Chapter 5 Exploring the possibility of device-level integration: RC-MOSHEMT

5.1 Introduction

The application area of GaN lateral transistor, the scaling of passive device size is strongly required, which can reduce the system power loss. Considering its application for power conversion, especially in topologies in which transistors are connected to inductive elements, a reverse conduction path for the current is required to release the stored inductor energy at switching events [48]. In traditional Si- and SiC-based vertical power devices, built-in body diodes can be designed using the doped layers to offer a freewheeling path when the transistor is switched off [48, 135, 136].

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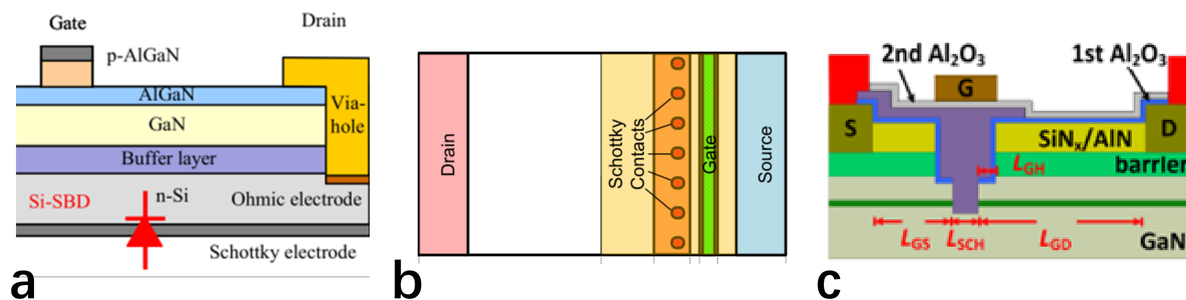

Figure 5-1 (a) Schematic of AlGaN/GaN HEMT integrated with Si Schottky diode, utilized the Si substrate and TSV technology [16]. (b) Schematic of monolithic integration of planar MOSHEMT with Schottky diode [137]. (c) Schematic of monolithic integration of MOSHEMT and Schottky diode utilizing double channel epitaxy [138].

However, such body diodes cannot be formed in lateral GaN HEMTs, due to their unipolar nature and absence of doped layers, and the reverse current of a HEMT, which is dependent on the gate voltage (V_G), is insufficient to offer freewheeling capability [48]. One way to achieve the freewheeling path is by connecting an anti-parallel diode between the source and drain, which provides a path, independent from V_G, for current to flow under reverse drain bias (V_D) [139]. However, using discrete anti-parallel diodes [140] results in extra device area, larger specific on-resistance ($R_{ON,SP}$), and generates additional parasitic components [138].

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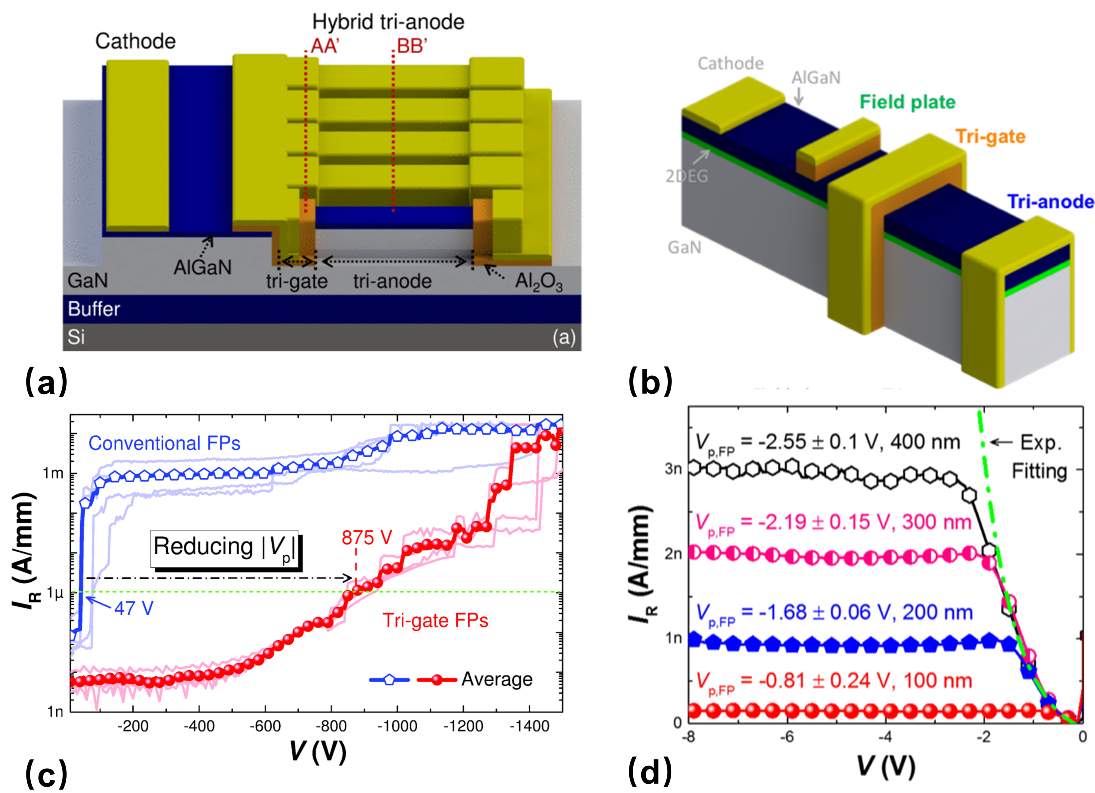

Figure 5-2 (a) (c) Schematic of Tri-Anode Schottky diode, and breakdown behavior over normal SBD. (b) Schematic of single Tri-Anode Fin, and (d) off-state leakage and flat band voltage versus different Tri-Anode fin width.

A compact solution to this issue is to form a SBD on the backside of the GaN-on-Si substrate, which leverages the small V_{ON} of Si SBDs [141]. Nevertheless, this method requires complex Si deep etching process, and the small V_{BR} of Si SBDs hinders the advantage of GaN transistors. Monolithic integration of anti-parallel planar SBDs between drain and gate of HEMT is another area-efficient approach that offers low reverse conduction loss and does not sacrifice the forward performance [142], [137]. But even so, the major limitation of such method is the large reverse leakage current of planar SBDs, which can be a few orders of magnitude higher than the transistors' off-state leakage current (I_{OFF}) [137, 142-145]. The high reverse leakage current issue was addressed in Ref. [138] with an unconventional double-channel heterostructure requiring relatively complex etching processes to demonstrate RC-MOSHEMTs.

In this chapter, we present high-performance reverse-conduction GaN-on-Si metal-oxide-semiconductor high electron mobility transistors (RC-MOSHEMTs) with integrated tri-anode freewheeling diodes. Tri-anode Schottky barrier diode (SBD) presenting small turn-on voltage (V_{ON}), ultra-low reverse leakage current, and high breakdown voltage (V_{BR}) were incorporated at portions of the drift region of AlGaN/GaN MOSHEMTs as freewheeling diodes. The tri-anode RC-MOSHEMTs exhibited outstanding reverse-conduction performance, a small V_{ON} of 0.55 V, along with a high V_{BR} of 1150 V, and a record small ON-resistance (R_{ON}) of 8.83 Ω·mm. These results reveal the potential of the tri-gate/tri-anode technology for future integrated power electronic devices.

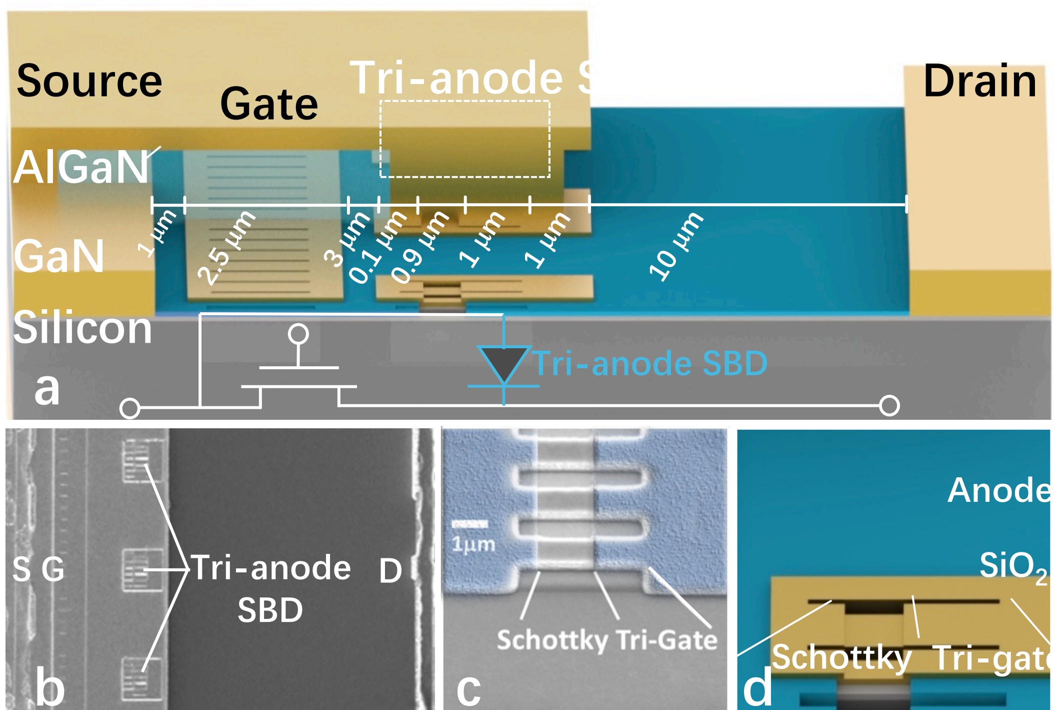

Figure 5-3 (a) Schematic and (b) top–view SEM image of the RC-MOSHEMT, (c) zoomed-in SEM image after Schottky contact opening and (d) schematic of tri-anode region.

5.2 Motivation and approches

Alternatively, we have recently shown the outstanding potential of tri-anode SBDs [146] with small V_{ON}, high V_{BR}, and ultra-low leakage current for high-performance and high-voltage GaN power SBDs [147], [148], and reverse-blocking transistors [149].

In this chapter, we demonstrate RC-MOSHEMT with integrated tri-anode SBDs as freewheeling diodes using relatively simple process. The tri-anode RC-MOSHEMTs presented excellent

reverse-conduction capability (V_{ON} = 0.55 V), strong voltage-blocking ability (I_{OFF} = 25 nA/mm at 200 V and V_{BR} = 1150 V at 1 μA/mm with floating substrate), and a record small forward-conduction R_{ON} (8.83 Ω·mm).

Figure 5-3 (a) and (b) show the schematic and top-view scanning electron microscopy (SEM) image of the tri-anode RC-MOSHEMT. The epitaxy in this work consisted of 5 μm of buffer, 0.3 μm of un-doped GaN channel, 23.9 nm of AlGaN barrier, and 1.8 nm of GaN cap layers. The device fabrication started with e-beam lithography to define the fins in tri-gate and tri-anode regions. Device isolation was done by inductively coupled plasma (ICP) mesa etching, with a depth of ~180 nm. The fin width in the tri-gate and tri-anode regions were 200 nm and 620 nm, along with a spacing of 200 nm and 110 nm, respectively, which were designed based on our previous studies to balance of ON- and OFF-state performances of the device [146], [14]. Source and drain ohmic contacts were formed by alloying Ti/Al/Ti/Ni/Au. A 17 nm thick SiO_2 was deposited by atomic layer deposition (ALD) as the gate dielectric, which was then selectively removed by CHF_3/SF_6-based ICP in the Schottky contact region of tri-anode SBDs (Figure 5-3 (c)). The anode and gate were formed by Ni/Au (Figure 5-3 (d)), followed by the deposition of 50 nm-thick ALD SiO_2 interlayer dielectric (ILD) and the second Ni/Au metal layer (M2) as the source-to-anode connection.

The tri-anode RC-MOSHEMTs consisted of a tri-gate MOSHEMT, and hybrid tri-anode SBDs integrated in its access region between the gate and drain. To equilibrate the forward and reverse current, 33 % of the channel width was occupied by the SBDs, which defines a filling factor (*FF*) as the width of SBDs divided by the width of device footprint, which will be discussed later. All measurement results in this work were normalized by the width of the device footprint, which was 60 μm.

5.3 Device performance

As shown in Figure 5-4 (a), the integrated tri-anode SBDs enhanced significantly the reverse conduction performance of the transistors. The tri-anode RC-MOSHEMTs presented a V_{ON} as small as 0.55 V (at I_D = 1 mA/mm), along with a small reverse forward voltage (V_F) of 1.5 V (at I_D = 50 mA/mm) at V_G = -7 V. In contrast, the V_{ON} and V_F of the reference MOSHEMT were 2.70 V and 4.15 V at the same V_G, respectively. The small V_{ON} is due to the direct contact of the metal to the 2DEG in the tri-anode SBDs [13], [150]. In forward-conduction mode, the tri-anode RC-MOSHEMTs presented a small R_{ON} of 8.83 Ω·mm, which is comparable to the reference device (7.69 Ω·mm) and yields the smallest R_{ON} among reverse-conduction GaN transistors reported in literature. The RC-MOSHEMTs also presented small I_{OFF} and high ON/OFF ratio, which were identical to the reference devices (Figure 5-4 (b)), due to the small reverse leakage current of the hybrid tri-anode SBDs [146], [148], [151].

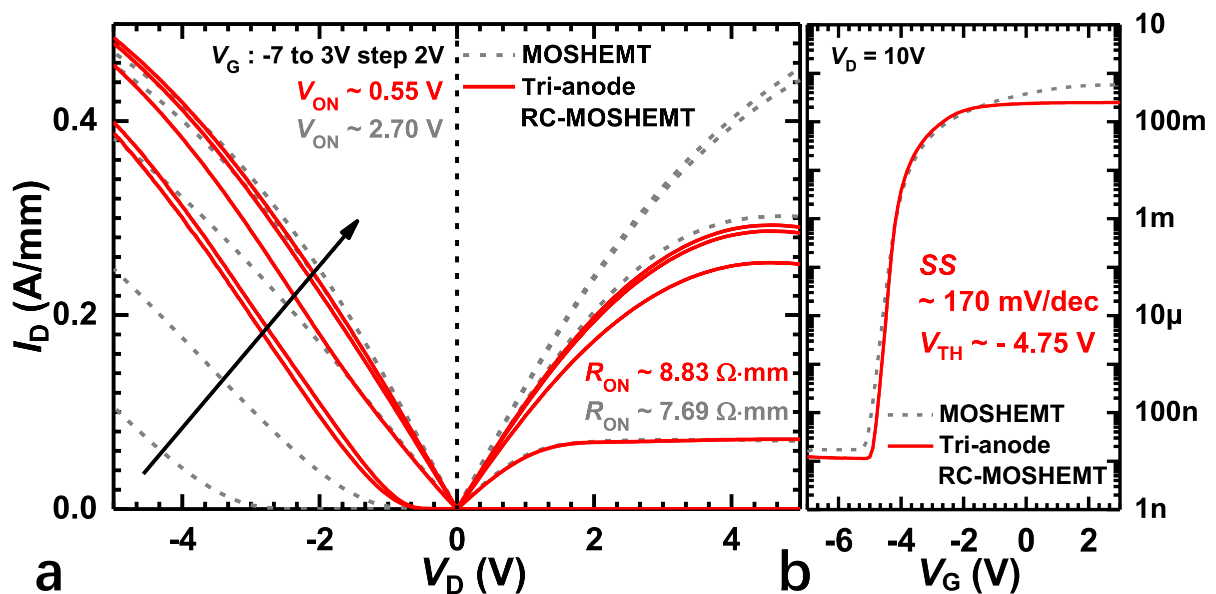

Figure 5-4 (a) Output and (b) transfer characteristics of the tri-anode RC-MOSHEMT and MOSHEMT, normalized by the width of the device footprint.

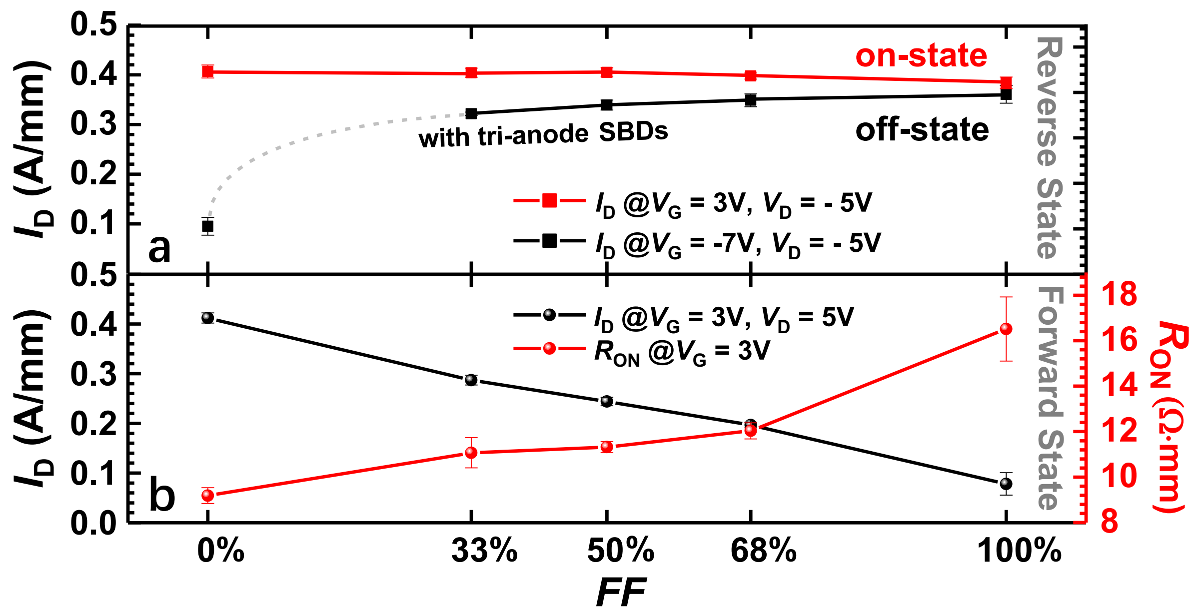

Figure 5-5 (a) Reverse and (b) forward characteristics of the tri-anode RC-MOSHEMT versus different filling factor (*FF*).

The small R_{ON} achieved in the tri-anode RC-MOSHEMTs is mainly attributed to the optimized *FF*, as it determines the percentage of the channel width used for forward and reverse current conduction. Figure 5-5 (a) plots the I_D in reverse-conduction mode of the tri-anode RC-MOSHEMTs (at V_D = -5 V) as a function of their *FF*s. When V_G is higher than V_{TH}, the reverse I_D is independent of the *FF* as the transistor is in ON-state. When V_G is below V_{TH}, *FF* = 33% is already large enough to nearly saturate the reverse I_D. This indicates that a small *FF* value is already enough for tri-anode SBDs to extract most of electrons injected from drain side. In forward-conduction mode, the I_D decreases while the R_{ON} increases with increasing *FF* (Figure 5-5 (b)), which is caused by the smaller effective channel width and higher spreading resistance. Based on these results, *FF* of 33 % was selected, which provided high freewheeling current with small degradation in the forward performance, resulting in a record small R_{ON}, which is highly desirable for efficient power conversion.

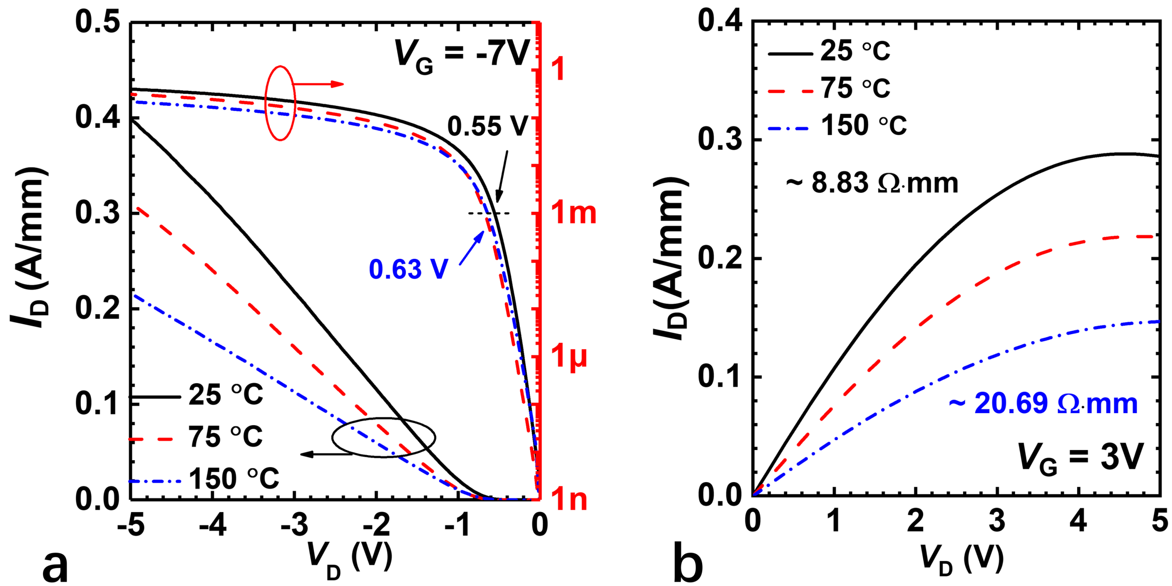

Figure 5-6 Temperature-dependent (a) reverse and (b) forward output characteristics of the tri-anode RC-MOSHEMT at 25°C, 75 ºC and 150 ºC.

The tri-anode RC-MOSHEMT presented a good reverse-conduction performance at high temperatures. From 25 ºC to 150 ºC, the V_{ON} increased to 0.63 V, and the reverse current reduce to 213 mA/mm (at V_D = -5 V) (Figure 5-6 (a)). In forward bias, the R_{ON} was 20.69 Ω·mm at 150 ºC, which is comparable to other integrated devices [138], [149], revealing the great potential for high-temperature applications (Figure 5-6 (b)).

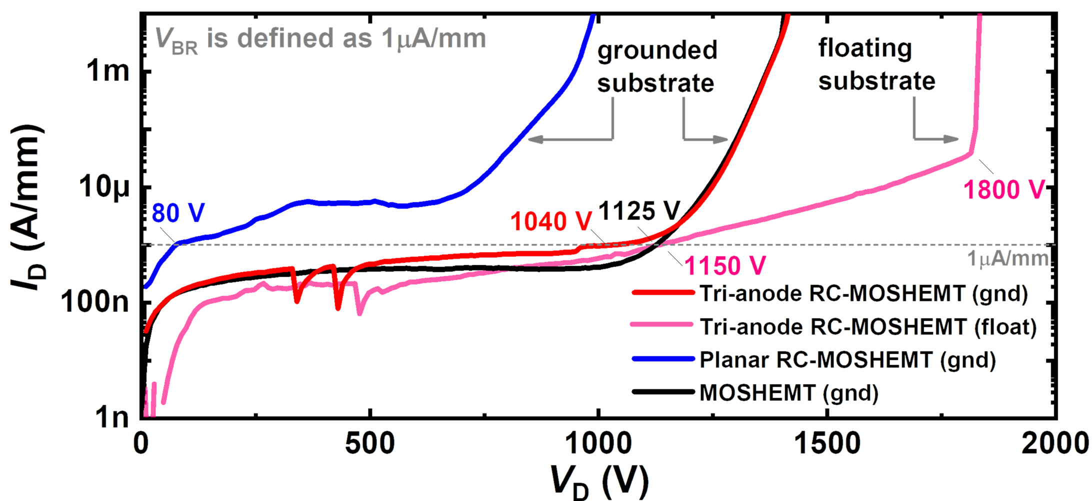

Figure 5-7 Breakdown characteristics of the tri-anode RC-MOSHEMT and MOSHEMT with grounded substrate (gnd) and floating substrate (float).

Figure 5-7 shows the breakdown characteristics of the tri-anode RC-MOSHEMT and reference devices. The V_{BR} of tri-anode RC-MOSHEMT was 1040 V, which is the close to that of the

reference MOSHEMT and significantly improved as compared to MOSHEMT with planar SBDs (RC-MOSHEMT). Such enhancement in V_{BR} is attributed to the better-distributed electric field with the integrated tri-anode SBDs [148], [19-21]. In addition, a very small I_{OFF} of 0.6 μA/mm at 650 V was observed for the tri-anode RC-MOSHEMTs, which is due to the reduced voltage drop at the Schottky junction in the hybrid tri-anode SBDs [148], [151]. With floating substrate, the RC-MOSHEMTs' V_{BR} was as high as 1150 V at 1 μA/mm, and the hard breakdown (HBD) did not occur until 1800 V.

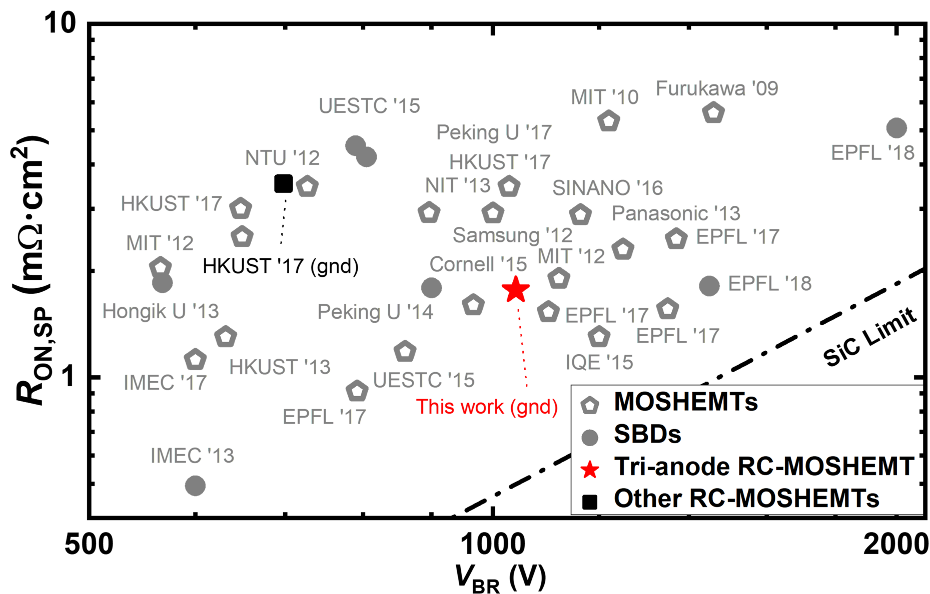

Figure 5-8 $R_{ON,\,SP}$ versus V_{BR} benchmark of the tri-anode RC-MOSHEMT with against GaN-on-Si power MOSHEMTs and lateral SBDs. A 1.5 μm transfer length of source/drain was considered for the calculation of $R_{ON,\,SP}$.

The RC-MOSHEMTs with integrated tri-anode SBDs were compared with other literature results of reverse-conduction GaN transistors in Table 5-1 Comparison of the RC-MOSHEMT with other reverse-conduction transistors., presenting small R_{ON}, V_{ON}, and I_{OFF}, along with the highest V_{BR} of 1040 V. We further benchmarked the tri-anode RC-MOSHEMTs against state-of-the-art discrete lateral GaN-on-Si (MOS)HEMTs, SBDs and other reported RC-MOSHEMTs in Figure 5-8 showing V_{BR} and $R_{ON,\,SP}$ comparable to discrete MOSHEMTs and SBDs, and outperforming other reported reverse-conduction transistors. These results reveal the great potential of the tri-gate/tri-anode technology for highly integrated GaN power devices.

Table 5-1 Comparison of the RC-MOSHEMT with other reverse-conduction transistors.

	This work	**[138]**	**[137]**	**[141]**	**[144]**
Type	D-mode	E-mode	D-Mode	D-mode	E-mode
R_{ON} **(Ω·mm)**	8.83	12.1	10.95	--	26
V_{BR} **(@1μA/mm)**	1040	698	<10	<30	<100
V_{ON} **(@1mA/mm)**	0.55	0.6	--	--	0.8
ON/OFF Ratio	8	7	5	10	--
I_{OFF} **(@200V)**	25 nA/mm	18 nA/mm	>1 μA/mm	--	--

5.4 Conclusion

In this work we presented reverse-conduction GaN-on-Si MOSHEMTs with state-of-the-art performance, by integrating tri-anode freewheeling SBDs. The devices exhibited excellent reverse performance, along with a record small R_{ON}, which can be promising for the next generation of efficient power converters.

Chapter 6 Conclusions

6.1 Results achieved

In this thesis, we explored three directions of future GaN power device: 1) improved device' s FOM, 2) demonstrated high-performance e-mode operation, and 3) device level monolithic integration. The possibility of future high-performance, multi-functional, e-mode GaN transistor was investigated and the performance boundary of GaN device was pushed forward.

We investigated a novel method for e-mode transistors using LiNiO as a junction gate. We have demonstrated a high-performance multichannel junction transistor, proposed a high-performance monolithically integrated free-wheeling diode, and developed a concise method to achieve a slanted field-plate.

We have developed an S-FP technology using grayscale e-beam lithography. This technology reduces the process complexity and dramatically improves the uniformity of the electric field distribution along the channel. The S-FP structure is created in a single step. The angled structure is sharply structured and adjustable. The angle of S-FP can be easily adjusted from the layout design, not during the process. The optimized 30-degree S-FP MOSHEMT exhibited a low R_{ON} of 4.5 Ω·mm while maintaining a high V_{BR} of 832 V. This result shows the great potential of S-FP technology for GaN power devices.

We have presented a LiNiO p-type oxide as a heterojunction gate, combined with a tri-gate structure, leading to e-mode operation with good R_{ON}, V_{BR}, excellent SS and I_{max} at the same time. The requirement of tri-gate W_{Fin} to achieve e-mode operation was significantly alleviated from 36 nm to 81 nm. In addition, the high stability, flexibility, and interface quality of this low-temperature oxide show great potential for power applications.

We have demonstrated high-performance multi-channel transistors with LiNiO junction gate. The transistors exhibited a positive V_{TH} of up to 1.2 V (defined at 1 μA /mm), which is the largest V_{TH} achieved with such a low R_S multichannel epitaxy, a near-ideal SS of 61 mV/dec, and a high on/off ratio of over 9 orders. This resulted in an excellent FOM of 1.36 GW/cm^2. These results indicate a

promising technological path for future high performance lateral GaN HEMTs through structure, epitaxy, and gate material development.

We proposed reverse-conduction GaN-on-Si MOSHEMTs with a state-of-the-art performance by integrating tri-anode freewheeling SBDs. The devices exhibited excellent reverse performance, along with a record low R_{ON}, which is promising for the next generation of efficient power converters.

6.2 Future development

Based on our work, we suggest following possible directions for future research:

High voltage multi-channel tri-gate devices with high V_{TH}: Due to the relatively poor step coverage of the PLD process, the gate current is difficult to control in multi-channel devices, especially at large drain stress. High quality LiNiO based on ALD would be an ideal solution. It can achieve high V_{TH} and very high FOM simultaneously. This technology is very promising for future very high performance low/medium voltages lateral GaN transistors.

Alternative material as junction gate: Besides LiNiO, other p-type TOS have also been developed: Cr-doped TiO_2 and Cu_2O. The advantage of these oxides is their large band gap, which has a positive effect on the gate drive capability and reduces the positive gate current. In addition, Ni is a magnetic material that is unfavorable in standard Si foundry. The TiO_2-based device could solve this problem.

Low-temperature deposition of p-GaN by PLD: Compared with the p-GaN gate, , the carrier pinch-off ability of LiNiO is still weaker due to the band offset between LiNiO and GaN. However, the deposition of p-GaN on tri-gate is a difficult process. It requires special optimization of the deposition to achieve regrowth in the nanoscale structure surface. The high temperature during the activation of p-GaN doping damages the etched surface of the tri-gate structure and leads to unpredictable behavior of the devices. The process method used in this thesis -PLD, can directly transfer the target material to the device surface at low temperature. Reports of PLD deposited n-GaN as regrowth source/drain prove that this method is possible [150, 151]. A more positive V_{TH} shift and better reliability could be expected with this method.

Curriculum Vitae

Wang Taifang

Professional summary

Experienced semiconductor research professional with doctoral level skills &7+ years of experience in deep submicron fabrication, material development and characterization.
Experienced in lateral GaN power electronics device design, epi-design, fabrication, and characterization.

Education

Ecole Polytechnique Federale de Lausanne (EPFL) – Powerlab (Prof. Elison Matioli) Mar. 2017- Apr.2022
Doctor of Philosophy (PhD), Electrical and Electronics Engineering
National Chiao Tung University (NCTU) -NanoST (Prof. Tuo-Hung Hou) Sep. 2014-Oct. 2016
Master's degree in Electronic
Pohang University of Science and Technology (POSTECH) South Korea Sep. 2013-Jan. 2014
Exchange student
University of Electronic Science and Technology of China (UESTC) Sep. 2010- Jun. 2014
Bachelor's degree of Electronic Physics

Projects

Utilizing p-type oxide achieving e-mode GaN Transistor
-Material development of PLD LiNiO towards low leakage, high hole concentration, low interface trap density and small band offset with AlGaN.
-Successfully developed process flow of highly acid resistance LiNiO oxide as a gate dielectric.
-Successfully demonstrated high-performance e-mode GaN MOSHEMTs combined Tri-gate Fin structure with LiNiO: state-of-art V_{BR}, $I_{D,MAX}$, R_{ON}, V_{th}, SS
-Successfully demonstrated multi-channel e-mode tri-gate MOSHEMT by LiNiO with record low R_{ON}.
-Developed interface traps, TDDB, BTI, and switching performance characterization setup and script for measurement and data processing.

High-performance multi-channel LiNiO junction gate Transistor
- Highest FOM ever achieved with junction gate.
- Highest V_{TH} ever achieved on Tri-gate structure.
- Stable operation at high temperature.

Slanted field plate for MOSHEMT using grayscale ebeam lithography on HSQ
-Successfully developed grayscale lithography process by ebeam lithography and a perfect slanted field plate structure was demonstrated.
-Successfully demonstrated a high breakdown voltage planar MOSHEMT structure with slanted field plate.

High-performance MOSHEMTs integrated with freewheeling diode
-Developed self-stop gate dielectric etching process.
-Successfully demonstrated high-performance reverse conducting MOSHEMT, solve the trade-off between forward current and off-state leakage in normal solutions.

Awards

Best student paper award in international workshop on nitride semiconductors (IWN) 2018, Phison Inc. Scholarship, MediaTek Scholarship, twice academic achievement award in Chiao Tung University, and CSC (China Scholarship Council) Exchange Student Scholarship.

Publications

IEEE Electron Device Letter "Enhancement-mode Multi-channel AlGaN/GaN Transistors with LiNiO Junction Tri-gate", **T. Wang**, L. Nela, and E. Matioli, *accepted*
Applied Physics Letters "LiNiO junction Tri-gate for Enhancement-mode GaN Transistors", **T. Wang**, L. Nela, and E. Matioli, *accepted*
Applied Physics Express: "p-NiO junction termination extensions for GaN power devices", R. A. Khadar, A. Floriduz, **T. Wang**, and E. Matioli. 2021. Vol. 14, issue. 7, pp. 071006
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IEDM 2021, "Beyond 8 THz Displacement-field Nano-switches for 5G and 6G Communications", M. S. Nikoo, **T. Wang**, P. Sohi, M. Zhu, F. Qaderi, R. A. Khadar, A. Floriduz, A. M. Ionescu, and E. Matioli, *oral*
ISPSD 2021, "LiNiO Gate Dielectric with Tri-gate Structure for High-performance E-mode GaN transistors", **T. Wang**, M. Samizadeh, L, Nela, and E. Matioli, *oral*
CSW 2019, "Novel Slanted Field Plate Technology for GaN HEMTs by Grayscale Lithography on Flowable Oxide", **T. Wang**, L. Nela, J. Ma, and E. Matioli, *oral*
IWN 2018, "1.1 kV AlGaN/GaN MOSHEMTs with Integrated Tri-anode Freewheeling diode", **T. Wang**, J. Ma, and E. Matoli, *oral, best student paper*

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Appendix-1: Process flow of single-channel junction gate devices

Step	Purpose	Description
1	Wafer dicing	• Substrate: Commercial GaN-on-Si • PR coating as protective layer • Dicing by DISCO DAD321 on backside
2	Defining the alignment marks	• PR: AZ1512 • Coating: 1 min @ 3000 rpm • Baking: 1 min 30 s @ 105 ºC • Exposure parameters: dose 42, defocus 0 (MLA150) • Development: 1 min 10s in AZ726 MIF
3	Etching the alignment marks	• ICP RIE: STS Multiplex ICP • Quick stick glue on Si carry wafer • Etchant: $Ar/Cl_2/BCl_3$ • Time: 2min30s ~300 nm • Check etching depth by profilometers (Bruker Dektak XT)
4	Defining tri-gate nanowires and mesa	• Ebeam lithography (Raith EBPG5000+) • Surface cleaning: RCA-1, O_2 plasma 1 min @ 600 W • PR: HSQ XR1541 002 • Coating: 3000 rpm • Exposure parameters: dose 1650, 100 kV, beta 0.33, eta 0.2 in layout beamer • Development: 2 min 10 s in 25 % TMAH • Rinsing: water tank and CO_2 supercritical point drying (Tousimis Automegasamdri 936C)

5	Etching	• ICP RIE: STS Multiplex ICP • Quick stick glue on Si carry wafer • Etchant: Ar/Cl_2 • Time: 2min ~200 nm
6	PR stripping	• BHF dipping
7	Digital etching to clean the surface	• 1 min 600 W O_2 plasma • 2 min 37 % HCl dipping • Repeat 5 times
8	Defining the ohmic contact region	• Ebeam lithography • PR: PMMA double layer • Coating: PMMA-495-A8 7000 rpm 1 min Baking: 180 ºC for 7 min 30s Cooling: 3min Coating: PMMA-950-A4 4500 rpm 1 min Baking: 180 ºC for 7 min 30s Cooling: 3min • Exposure parameters: dose 750, beta = 0.33, eta = 0.6 • Development: 3 min in MiBK:IPA 1:3, rinsing 1 min in IPA

9	Ohmic formation	• Pre-clean: 20 s O_2 plasma cleaning at 200 W • Metal: Ti/Al/Ti/Ni/Au • Thickness: 20/120/40/60/50 nm • Lift-off: 1165 solvent at 70 ºC • RTA: 780 ºC 30 s
10	Oxide lift-off mask	• PECVD SiO_2 250 nm by Oxford Plasmalab system 100 • PR: AZ1512 • Pre-coating: HMDS standard coating process • Coating: 1 min @ 3000 rpm • Baking: 1 min 30 s @ 105 ºC • Exposure parameters: dose 42, defocus 0 (MLA150) • Development: 1 min 10s in AZ726 MIF • Etching: BHF in 2 min 30 s • PR strip: 1165 solvent, IPA rinsing, water rinsing
11	LiNiO layer deposition	• Solmates SMP 800 pulsed laser deposition
12	LiNiO lift-off	• PR: AZ10XT60 • Coating: 1 min @ 6000 rpm • Baking: 3 min @ 105 ºC • Rehydration: wait 10 min • Exposure parameters: dose 240, defocus 0 (MLA150) • Development: 5 min in AZ400K (1:4 diluted) • Etching: IBE (Veeco Nexus IBE350) low, 0 degree 4min (cooling cycles added) • BHF etching: 5 min • PR strip: 1165 solvent, ultrasound lift-off

13	Gate patterning	• Ebeam lithography • PR: PMMA double layer • Coating: PMMA-495-A8 7000 rpm 1 min Baking: 180 ºC for 7 min 30s Cooling: 3min Coating: PMMA-950-A4 4500 rpm 1 min Baking: 180 ºC for 7 min 30s Cooling: 3min • Exposure parameters: dose 750, beta = 0.33, eta = 0.6 • Development: 3 min in MiBK:IPA 1:3, rinsing 1 min in IPA • Residue clean: 20 s O_2 plasma cleaning at 200 W
14	Gate formation	• Metal: Pd/Au • Thickness: 50/150 nm • Lift-off: 1165 solvent at 70 ºC

Appendix-2: Process flow of multi-channel junction gate devices

Step	Purpose	Description
1	Wafer dicing	• Substrate: Commercial GaN-on-Si • PR coating as protective layer • Dicing by DISCO DAD321 on backside
2	Defining the alignment marks	• PR: AZ1512 • Coating: 1 min @ 3000 rpm • Baking: 1 min 30 s @ 105 ºC • Exposure parameters: dose 42, defocus 0 (MLA150) • Development: 1 min 10s in AZ726 MIF
3	Etching the alignment marks	• ICP RIE: STS Multiplex ICP • Quick stick glue on Si carry wafer • Etchant: $Ar/Cl_2/BCl_3$ • Time: 2min30s ~300 nm • Check etching depth by profilometers (Bruker Dektak XT)
4	Defining tri-gate nanowires and mesa	• Ebeam lithography (Raith EBPG5000+) • Surface cleaning: RCA-1, O_2 plasma 1 min @ 600 W • Glue layer deposition: 2 nm Ti (DP650 sputter) • PR: HSQ XR1541 006 • Coating: 7000 rpm • Exposure parameters: dose 1750, 100 kV, beta 0.33, eta 0.2 in layout beamer • Development: 4 min in 25 % TMAH • Rinsing: water tank and CO_2 supercritical point drying (Tousimis Automegasamdri 936C) • Post-process: O_2 plasma 10 min @ 600 W

5	Etching	• ICP RIE: STS Multiplex ICP • Quick stick glue on Si carry wafer • Etchant: Ar/Cl_2 • Time: 2 min 30 s ~250 nm
6	PR stripping	• BHF dipping
7	Digital etching to clean the surface	• 1 min 600 W O_2 plasma • 2 min 37 % HCl dipping • Repeat 5 times
8	Second mesa	• Ebeam lithography (Raith EBPG5000+) • Surface cleaning: RCA-1, O_2 plasma 1 min @ 600 W • PR: HSQ XR1541 006 • Coating: 3000 rpm • Exposure parameters: dose 1250, 100 kV, beta 0.33, eta 0.2 in layout beamer • Development: 4 min in 25 % TMAH

9	Etching of 2nd mesa	• ICP RIE: STS Multiplex ICP • Quick stick glue on Si carry wafer • Etchant: Ar/Cl_2 • Time: 3 min ~300 nm
10	PR stripping	• BHF dipping
11	Defining the ohmic contact region	• Ebeam lithography • PR: PMMA double layer • Coating: PMMA-495-A8 7000 rpm 1 min Baking: 180 ºC for 7 min 30s Cooling: 3min Coating: PMMA-950-A4 4500 rpm 1 min Baking: 180 ºC for 7 min 30s Cooling: 3min • Exposure parameters: dose 750, beta = 0.33, eta = 0.6 • Development: 3 min in MiBK:IPA 1:3, rinsing 1 min in IPA

12	Ohmic formation	• Pre-clean: 20 s O_2 plasma cleaning at 200 W • Metal: Ti/Al/Ti/Ni/Au • Thickness: 20/120/40/60/50 nm • Lift-off: 1165 solvent at 70 ºC • RTA: 780 ºC 30 s
13	Oxide lift-off mask	• PECVD SiO_2 250 nm by Oxford Plasmalab system 100 • PR: AZ1512 • Pre-coating: HMDS standard coating process • Coating: 1 min @ 3000 rpm • Baking: 1 min 30 s @ 105 ºC • Exposure parameters: dose 42, defocus 0 (MLA150) • Development: 1 min 10s in AZ726 MIF • Etching: BHF in 2 min 30 s • PR strip: 1165 solvent, IPA rinsing, water rinsing • Ebeam lithography (Raith EBPG5000+) • Surface cleaning: RCA-1, O_2 plasma 1 min @ 600 W • PR: HSQ XR1541 006 • Coating: 6000 rpm • Exposure parameters: dose 1250, 100 kV, beta 0.33, eta 0.2 in layout beamer • Development: 4 min in 25 % TMAH
14	LiNiO layer deposition	• Solmates SMP 800 pulsed laser deposition
15	LiNiO lift-off	• PR: AZ10XT60 • Coating: 1 min @ 6000 rpm • Baking: 3 min @ 105 ºC • Rehydration: wait 10 min • Exposure parameters: dose 240, defocus 0 (MLA150) • Development: 5 min in AZ400K (1:4 diluted) • Etching: IBE (Veeco Nexus IBE350) low, 0 degree 4min (cooling cycles added) • BHF etching: 5 min • PR strip: 1165 solvent, ultrasound lift-off

16	Gate patterning	• Ebeam lithography • PR: PMMA double layer • Coating: PMMA-495-A8 7000 rpm 1 min Baking: 180 ºC for 7 min 30s Cooling: 3min Coating: PMMA-950-A4 4500 rpm 1 min Baking: 180 ºC for 7 min 30s Cooling: 3min • Exposure parameters: dose 750, beta = 0.33, eta = 0.6 • Development: 3 min in MiBK:IPA 1:3, rinsing 1 min in IPA • Residue clean: 20 s O_2 plasma cleaning at 200 W
17	Gate formation	• Metal: Pd/Au • Thickness: 50/150 nm • Lift-off: 1165 solvent at 70 ºC