A Generalized Phase-Shift PWM Extension for Improved Natural and Active Balancing of Flying Capacitor Multilevel Inverters

Georgios Kampitsis, *Member, IEEE*, Efstratios Batzelis, *Senior Member, IEEE*, Antonis Kolokasis, *Member, IEEE*, Elison Matioli, *Senior Member, IEEE* and Bikash C. Pal, *Fellow, IEEE*

Abstract The emergence of wide bandgap power devices has brought the attention back to the flying capacitor (FC) multilevel inverters with a large number of stages, in an effort to increase the power density by minimizing the passive components. The main challenge that such systems face, particularly the ones based on high-frequency Gallium-Nitride devices and small-value ceramic capacitors, relate to the stringent requirements for precise and fast capacitor balancing. Conventional *natural balancing* techniques exhibit poor settling times, while most improved natural balancing methods are not easily scalable to more than five levels. The alternative of *active balancing* normally requires one isolated sensor per FC which increases the overall system cost and footprint, or a single ac-side sensor that is more compact but calls for sophisticated PWMs that again are not available for multiple levels. In this paper we introduce a generalized pulse width modulation (PWM) strategy based on the phase-shift and carrier swapping principles for an arbitrary number of levels. We provide an easy and intuitive method for the extraction of the PWM pattern, the switching states, and their sequence. Simulations were carried out in Matlab/Simulink and experimental tests were conducted on a single-phase 7-level GaN inverter prototype. Not only is the extended PWM advantageous in natural balancing, but it also provides the right zero switching states for ac-side FC sensing in active balancing.

Index Terms— **Active balancing, flying capacitor, gallium nitride, multilevel inverters, natural balancing, pulse width modulation, switching states, wide band gap semiconductors.**

I. INTRODUCTION

IN recent years, there has been an increasing number of power transfer applications that pose strict volume and weight constrains on the energy conversion systems. The most demanding applications are found in the transportation sector, including electric and hybrid aircraft propulsion systems [1], [2] and electric vehicle charges [3]. Stationary applications, such as PV generators [4], power factor correction (PFC) systems [5] and various medium voltage applications [6] also benefit from more compact and lightweight converters, as this is translated to lower installation cost.

A potential answer to this need can be provided by wide bandgap (WBG) power semiconductors in multilevel inverter (MLI) topologies. The high switching frequency capabilities of

G. Kampitsis, A. Kolokasis and B. Pal, are with the Department of Electrical and Electronic Engineering, Imperial College London, SW7 2AZ, U.K. (e-mail: g.kampitsis@imperial.ac.uk, antonis.kolokasis@cytanet.com.cy, b.pal@imperial.ac.uk). Efstratios I. Batzelis is with the School of Electronics and Computer Science, University of Southampton, SO17 1BJ Southampton, U.K. (e-mail: e.batzelis@soton.ac.uk). E. Matioli is with the Power and Wide Bandgap Electronics Research Laboratory, École Polytechnique Fédérale de Lausanne, 1015 Lausanne, Switzerland (e-mail: elison.matioli@epfl.ch).

these devices (in the hundreds of kHz to a few MHz range) allow the minimization, even elimination, of the magnetic components and the replacement of electrolytic capacitors with lightweight and reliable ceramic capacitors [7]. Moreover, the overall efficiency and power density gain brings a further reduction to the physical dimensions of the cooling system [8].

Miniaturized multilevel converters have lately gained more attention with advancements on the monolithic integration of several Gallium Nitride devices on a single chip, as has been demonstrated in [9]–[11]. The flying capacitor (FC) inverter with a large number of stages is the most appropriate topology for such applications, due to the high energy density of ceramic capacitors, the absence of clamping diodes and the requirement for a single input DC source. Authors of [3] and [5] have demonstrated 7-level FC inverters for PFC and PV applications and have competed in the *Google/IEEE Little box challenge* for the world's smallest 2 kW grid connected converter. Further, a 9-level and a 13-level GaN-based FC MLIs were designed and developed in [2] and [4], respectively, that have demonstrated record-braking power densities for aviation and renewable energy applications. Another reason for the increased attention to the GaN-based FC topologies is the limited breakdown voltage capabilities of the GaN transistors. More specifically, state-of-the-art GaN devices are typically characterized by low to medium voltage capabilities (200 to 600 V breakdown), hence the series connection of FC topology and its voltage

sharing properties prove to be beneficial for utilizing GaN transistors.

However, as the total inverter capacitance gets lower with miniaturization, regulating the FC voltage becomes more challenging. Internal non-idealities, such as the transistors' voltage drop and timing mismatches, caused by the dead-time and the drivers' propagation delay [12], [13], may cause the FC to drift from their nominal voltage. Additionally, external conditions, such as load disturbances [21], [22] or input source nonidealities [23] may also lead to FC voltage drift. Such non-nominal FC voltage variations need to be contained quickly to avoid operation of the transistors in non-rated conditions and the risk of system failure. Therefore, a fast and reliable capacitor balancing technique, either natural (passive) or active, is particularly important for future GaN-based MLIs.

Natural balancing is the most widely used and cost-effective solution and is based on pulse width modulation (PWM) techniques that ensure that the average current of all FC over a fundamental cycle is zero [14]. Among the different PWM strategies, the conventional level-shifted PWM techniques, namely the phase disposition (PD), phase opposition disposition (POD) and alternative phase opposition disposition (APOD), fail to properly balance the FC due to the insufficient number of generated switching state around zero crossing, which we will later prove that is key for optimal natural balancing. In fact, only a single independent state is produced, which is attributed to the inherent structure of these PWM techniques that require a level shift of the carriers only in the Y-axis, thus keeping the two sets of carriers separated at either sides of the reference around zero crossing. On the other hand, the phase shifted PWM (PSPWM) can successfully balance the FC, while maintaining a low implementation cost. However, it exhibits a very slow balancing response in low modulation indices. Authors of [15]–[18] introduced modified phase disposition PWMs (MPDPWM) based on discontinuous reference waveforms or multiple trapezoidal-shaped carriers that combine improved natural balancing performance with low output harmonic content. Even though this technique is expandable to any number of levels, N, it generates the same switching states around zero crossing as the PSPWM and is thus characterized by similarly poor natural balancing performance.

To address this problem, a finite state machine executed in cyclical fashion has been proposed in [19]. This methodology is generated by decoding the conventional Phase Disposition (PDPWM) and the Centered Space Vector PWM (CSVPWM) [20], [21] to identify the target voltage level for each phase leg. Although flexible, this approach is not applicable with a common microcontroller unit (MCU), but it rather requires a fast field-programmable gate array (FPGA) device. Additionally, the computational cost needed for calculating the next state might be a limiting factor for high-switching-speed GaN inverters.

A promising alternative proposes the modification of the traditional PSPWM technique (MPSPWM) by swapping a subset of the carrier signals either at their intersecting point [22] or at the lowest carrier level (zero level) [23]. This method

leads to optimal utilization of the redundant zero switching states (ZSS), i.e. the states that correspond to zero output voltage, at negligible extra computational cost. Unfortunately, however, the MPSPWM strategy has not been scaled for inverters with more than five levels to this day. As the number of levels increases, the swapping combinations increase exponentially with unpredictable switching sequences and no guarantee for natural balancing. It remains today an unresolved issue to generalize the MPSPWM to an arbitrary number of levels with a clear carrier swapping mechanism and deterministic pulse sequence.

The natural balancing limitations can be overcome by adopting a closed-loop *active balancing* strategy that regulates the FC voltages at the right level regardless of the disturbance. However, most such methods rely on galvanic isolated measurements across each FC [24]–[28], thus increasing significantly the total system cost and footprint, especially in MLIs with a large number of stages. Real-time state estimation algorithms have been proposed in [13], [29]–[31], which require the knowledge of just the inverter output current, but are characterized by high computational burden and low response speed, rendering them not-applicable in fast GaN-based MLIs.

A viable alternative for accurate FC measurements with minimum component count adopts the concept of *ac-side monitoring*, which involves sampling the inverter output voltage at specific switching states and extracting the FC voltages from these measurements [32]–[35]. Particularly, we have demonstrated in [32] increased measurement bandwidth and accuracy by combining the MPSPWM of [22] with a bidirectional clamping circuit, making the approach ideal for high-frequency GaN MLIs. Yet, this measurement method requires the production of all ZSS from the PWM, which is feasible for up to 5-level inverters with MPSPWM. It is therefore apparent that a generalized PWM strategy with maximum utilization of the redundant switching states is equally favorable for both natural and active balancing, and such a PWM for more than 5 levels is currently missing from the literature.

In this study, we aim to address this emerging need by extending the MPSPWM to any number of levels. The key contribution is the *derivation of an intuitive and deterministic pattern* for the carrier swapping, applicable to an *arbitrary number of levels*, which allows for generalization of that PWM to what we denote hereinafter as *carrier–swapping PWM* (CSPWM).

We also provide guidelines for the extraction of the generated switching states and their sequence, which lead directly to the system of linear equations to be solved in ac-side monitoring applications, avoiding additional analysis and simulations. The proposed carrier pattern exhibits a series of merits such as switching state symmetry, smooth carriers' transition, implementation simplicity allowing the use of an MCU, and straightforward FC voltage extraction in ac-side monitoring systems.

To the best of the authors knowledge, this is the first time to introduce a generalized PWM strategy for FC MLI that
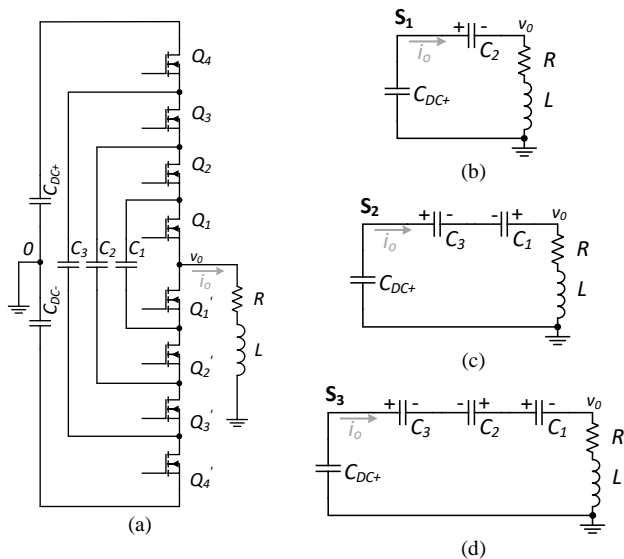
Fig. 1. (a) Schematic diagram of a single phase 5-level FC inverter feeding an R-L load. (b-d) Equivalent circuits that correspond to the three zero switching states S_1-S_3.

produces the right ZSS and is scalable to any number of levels, thus ensuring optimal natural balancing and allowing application of a fast and precise ac-side voltage monitoring for active balancing.

The rest of the paper is structured as follows: the balancing mechanisms in a FC MLI are discussed in Section II, followed by the proposed CSPWM in Section III. Switching model simulation and results from the analytical approach are given in Section IV. Section V is dedicated to the experimental verification of the extended PWM and Section VI summarizes the concluding remarks.

II. BALANCING MECHANISMS IN FC MLIs

The goal of this section is to introduce the balancing mechanisms in FC MLIs using a 5-level inverter as a benchmark, demonstrate how the proposed CSPWM is favorable for both natural and active balancing, and explain the extension challenges.

A. Natural Balancing

The way that natural balancing PWMs help reduce the FC voltage error is though harmonic current injection over the inverter output load by means of dissipation of the imbalanced energy [36]–[39]. The analysis that follows considers a simple R-L load to illustrate the phenomenon (Fig. 1), but parasitic losses (e.g. in the semiconductor devices, eddy currents, high frequency skin effect) further speed-up the balancing process in practice [38].

Well established algorithmic methods based on frequency domain transformation [40]–[42] and more recent average-value models in time domain [36], [37] have shown that the FC voltage dynamics under natural balancing contain two exponential decay components: (i) a minor fast component that depends on the load level, and (ii) a dominant slower component that relates to the amplitude modulation index, m_a. According to [23], the worst-case scenario holds for zero m_a, when the theoretical natural balancing time constant becomes
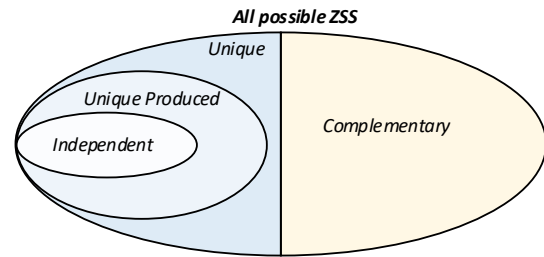

Fig. 2. Venn diagram describing the classification of the ZSS.

infinite, as the damping factor and the common mode term tend to zero. Therefore, fast natural balancing under $m_a = 0$ ensures a satisfying performance for all other operating conditions as well, which indicates that ZSS are of primary importance for any such PWM.

Before we continue with the natural balancing analysis, it is important to introduce a classification of the different ZSS with the help of the Venn diagram in Fig. 2. The number of *all possible* ZSS that can be produced with the switching combinations depends only on the number of levels of the FC inverter and is unrelated to the PWM strategy. These ZSS can be divided into two non-overlapping groups, the *unique* ZSS, involving the conduction of the top-side dc-link capacitor C_{DC+}, and their *complementary* states, corresponding to the conduction of the low-side C_{DC-}. A PWM strategy will produce only a subset of the available *unique* ZSS, namely the *unique produced* ZSS. In general, every ZSS involves a combination of FCs which may be different from other ZSSs or may be the same as the synthesis of other ZSSs. Only a subset of the *unique produced* ZSS involves independent combination of FCs, i.e., the expression of the FCs in the output voltage is different in every ZSS. This group is denoted here as *independent* ZSS and has particular importance, as shown next.

Let us consider the 5-level FC inverter benchmark of Fig. 1. The inverter has six possible ZSS in total, the *unique* S_1-S_3 referring to the top-side dc-link capacitor (see Fig. 1(b-d)) and their *complementary* $S_1{'}$- $S_3{'}$ corresponding to the low-side conduction path. TABLE I shows how the inverter output voltage relates to the FC voltages, $v_{Ci} = v_{DC}·i/(N-1)$ - v_{Ci} ($i = 1,…, N$-2), or more conveniently to the respective voltage deviations from their nominal value Δv_{Ci}. The *complementary* ZZS are omitted in TABLE I for conciseness.

The conventional PSPWM generates only two *unique produced* ZSS (S_1 and S_2), according to Fig. 3(a), in the following sequence: S_1(0011)–S_2(1001)–$S_1{'}$(1100)–$S_2{'}$(0110). The corresponding equations (rows 1 and 2 in TABLE I) show that C_2 contributes to the output voltage independently (row 1) and hence Δv_{C2} will quickly get to zero. On the other hand, C_1 and C_3 jointly participate in the generation of the output voltage (row 2) that entails that the difference (Δv_{C3}-Δv_{C1}) will converge to zero, but not the individual Δv_{C3} and Δv_{C1}, as explained in [36]. In other words, the three FCs do not get

TABLE I
ZERO SWITCHING STATES FOR A 5-LEVEL FC INVERTER.

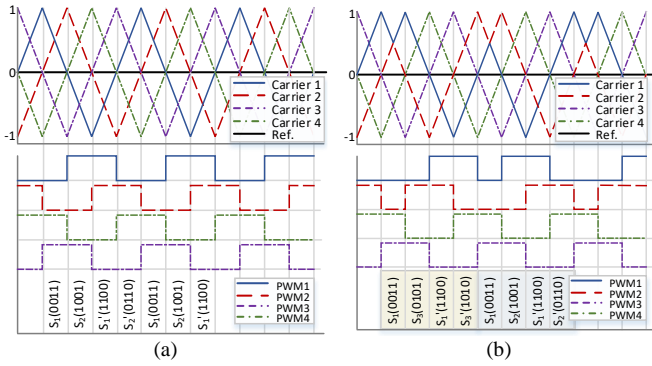| State	Fig.1	Q_{x1}	Q_{x2}	Q_{x3}	Q_{x4}	v_0	
S_1	(b)	0	0	1	1	$v_{DC}/2$-v_{C2}	$= \Delta v_{C2}$
S_2	(c)	1	0	0	1	$v_{DC}/2$-v_{C3}+v_{C1}	$= \Delta v_{C3}$-Δv_{C1}
S_3	(d)	0	1	0	1	$v_{DC}/2$-v_{C3}+v_{C2}-v_{C1}	$= \Delta v_{C3}$-Δv_{C2}+Δv_{C1}

Fig. 3. Carrier waveforms and respective PWM signals for zero output voltage of a 5-level FC inverter with (a) PSPWM and (b) CSPWM strategies.

exposed to the output current independently (number of *independent* ZSS < number of FC), which results in suboptimal natural balancing.

On the contrary, the CSPWM generates all *unique* ZSS (S_1-S_3) as demonstrated in [22] and shown graphically in Fig. 3(b). This method is based on swapping two carriers at their meeting point. In this example, carriers 1 and 2 swap direction when they simultaneously reach the 0.5 mark in every period. A complete switching sequence is now comprised by 8 ZSS: $S_1(0011)$–$S_3(1001)$–$S_1'(1100)$–$S_3'(0101)$–$S_1(0011)$–$S_2(1010)$–$S_1'(1100)$–$S_2'(0110)$. Here, the sets of *unique*, *unique produced* and *independent* ZSS fortunately coincide, and more importantly the number of *independent* ZSS is equal to the number of FC. This means that all FC contribute to the output voltage in an independent manner within two switching cycles, which is translated to fast and symmetrical natural balancing.

An effective mathematical formulation of this independence is via the relation of the FC voltage deviations Δv_{Ci} with the inverter output voltage during the state S_j, $v_o(S_j)$, given in matrix form in (1) for this example. This system of equations, referred to hereinafter as $v_o = P \times \Delta v_C$, can show whether the considered ZSS are independent or not: the FCs are independently expressed in the output voltage if, and only if, the system of equations has a unique solution $\Delta v_c = P^{-1} \times v_o$ expressed in (2), i.e. when the P matrix is invertible.

$$\begin{bmatrix} v_0(S_1) \\ v_0(S_2) \\ v_0(S_3) \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ -1 & 0 & 1 \\ 1 & -1 & 1 \end{bmatrix} \times \begin{bmatrix} \Delta v_{C1} \\ \Delta v_{C2} \\ \Delta v_{C3} \end{bmatrix} \leftrightarrow v_o = P \times \Delta v_C \quad (1)$$

$$\begin{bmatrix} \Delta v_{C1} \\ \Delta v_{C2} \\ \Delta v_{C3} \end{bmatrix} = \begin{bmatrix} 0.5 & -0.5 & 0.5 \\ 1 & 0 & 0 \\ 0.5 & 0.5 & 0.5 \end{bmatrix} \times \begin{bmatrix} v_0(S_1) \\ v_0(S_2) \\ v_0(S_3) \end{bmatrix} \leftrightarrow \\ \Delta v_c = P^{-1} \times v_o \quad (2)$$

This analysis shows that fast natural balancing is achieved when the PWM produces a number of *independent* ZSS equal to the FC count, and that this condition holds true when $v_o = P \times \Delta v_C$ has a unique solution. The objective of this paper is to derive a PWM that satisfies just that for any number of levels.

B. Active Balancing

Such a PWM that generates the "right" amount of independent ZSS is also a requirement for active balancing that employs ac-side monitoring. For example, in [32] we show that

the FC voltages can be extracted by clamping (i.e., saturating) and sampling the inverter voltage solely during the ZSS. This method increases the resolution and accordingly broadens the measurement bandwidth to more than 200 kHz, allowing its application in high frequency GaN-based inverters. At the same time, the circuit complexity and cost are kept to a minimum, by using a single, non-isolated sensor per phase.

The only prerequisite is to apply a PWM strategy that relates the output voltage with the FC voltages $v_o = P \times \Delta v_C$ in a way that we can extract the latter from the former, i.e. the system is fully observable and has a unique solution $\Delta v_c = P^{-1} \times v_o$. Interestingly, this is the same condition for optimal natural balancing, that is to produce a number of *independent* ZSS equal to the FC count. Although this has been established for N = 5 in [32], it remains an open challenge for an arbitrary number of levels *N*.

The main conclusion here is that both natural and active balancing benefit from a PWM that produces *independent* ZSS of equal number to the FC count. This observation is further elaborated next and utilized to assess whether a PWM satisfies that condition by checking the rank of matrix P in $v_o = P \times \Delta v_C$.

C. Extension Challenges

In a 5-level inverter, the MPSPWM method dictates that a single carrier swapping of any neighboring carriers at their intersecting point is sufficient for introducing the missing ZSS, i.e., S_3. However, in higher order MLIs, there is no guideline in literature for which carrier pairs should be exchanged nor details on the correct number of swaps in one period. This leads to hundreds, even thousands of possible carrier swapping combinations. For instance, a 9-level FC inverter has 8 carrier signals that can be arranged in more than 750 swapping combinations. Most of them, however, still produce an insufficient number of switching states or do not result in an adequate number of *independent* ZSS.

The first task for breaking down the PWM extension complexity is to identify *all possible* ZSS for any number of levels. In this study, we introduce an intuitive representation of the degree of redundancy of each generated voltage level in a FC MLI through the Pascal's Triangle, shown in Fig. 4. Each element in the triangle shows the number of states that produce the voltage level that is indicated in the base of the triangle for the number of levels given in the row. For example, the outer
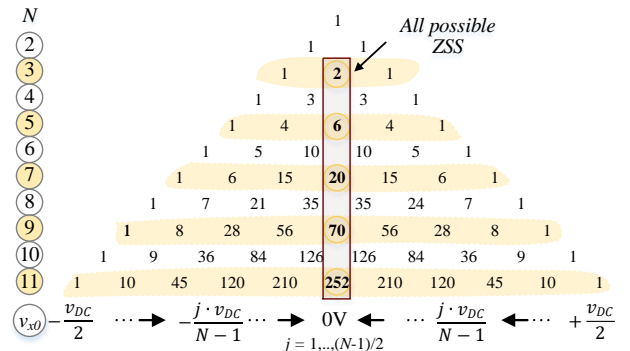

Fig. 4. Pascal's triangle representing the redundant switching states in an FC MLI with arbitrary number of levels.

edges always correspond to the maximum output voltage $\pm v_{DC}/2$, whereas the central column corresponds to 0 V, i.e. the number of *all possible* ZSS. It is evident that only MLIs with odd number of levels can produce zero output voltage, which is why these are the most widely used MLIs, both commercially and in academic reports.

The number of *all possible* ZSS shown in the central column can be calculated via the central binomial coefficient, P_b, given in (3), while the number of the *unique* ZSS is $P_b/2$.

$$P_b = \frac{(2 \cdot n)!}{(n!)^2}, where \; n = \frac{N-1}{2} \tag{3}$$

In the general case of an N-level inverter, there are $N_{FC} = N-2$ flying capacitors, meaning we need at least $N-2$ *independent* ZSS for a unique solution in $\boldsymbol{v_o} = \boldsymbol{P} \times \boldsymbol{\Delta v_C}$. However, the phase-shift switching pattern produces only $n=(N-1)/2$ unique ZSS. This is because in one switching period there are $N-1$ switching states, half of which are unique, and the other are the complementary ones. However, n is always smaller than N_{FC}, with the exception of $N = 3$. This means that an increasing number of additional ZSS, proportional to the number of levels, are required for an independent system of equations. The amount of extra switching states N_{ex} is given by (4).

$$N_{ex} = N_{FC} - n = \frac{N-3}{2} = n-1 \tag{4}$$

TABLE II summaries the number of unknown variables, N_{FC}, the maximum possible ZSS, $P_b/2$, the *independent* ZSS produced by the PSPWM, n, and the additional ZSS needed, N_{ex}, for various levels. It is evident that the PSPWM is appropriate only for a 3-level inverter and a 5- level inverter indeed requires one extra state as already demonstrated earlier.

A key observation regarding the CSPWM is that a single swapping of two carriers generates one new pair of switching states (a unique one and its complementary) while, all the original states are still produced. This is because every swapping splits the switching sequence into two distinct periods, as shown in Fig. 3(b):

- the original carrier sequence {1,2,3,4}, marked with the gray area, and
- the new sequence with swapped carriers {2,1,3,4} highlighted with the yellow area.

This reveals that the minimum number of swapping actions, N_{sw}, should be equal to N_{ex}, e.g. 2 swaps for a 7-level inverter, 3 swaps for 9-level and so on. Yet, depending on the selection of the carrier pairs to be swapped, the resulting system of equations can be independent, overdetermined, or inconsistent. The following section is dedicated in identifying the PWM strategy with the right swapping actions that lead to the desired independence condition for any number of levels.

TABLE II
ZERO SWITCHING STATES FOR A 5-LEVEL FC INVERTER.

Number of levels (N)	Number of FC (N_FC)	Unique ZSS (P_b/2)	Independent ZSS from PSPWM (n)	Extra ZSS required (N_ex)
3	1	1	1	0
5	3	3	2	1
7	5	10	3	2
9	7	35	4	3
11	9	126	5	4

III. PROPOSED CARRIER SWAPPING PWM EXTENSION

Here we present the analytical methodology to produce the generalized PWM strategy with optimal ZSS utilization. The guidelines given in the following subsections aim to provide the reader with a single and straightforward modulation pattern, thus addressing the almost-chaotic carrier swapping combinations. The generated pattern shall hold true for any number of stages and shall coincide with the already existing MPSPWM when $N=5$.

The following analysis considers a 7-level inverter as an example, therefore, it is useful to introduce all possible ZSS of the 7-level inverter in TABLE III.

A. Unique ZSS Matrix from PSPWM

The first step is to identify the original ZSS produced by the conventional PSPWM for N levels and capture them in a binary matrix format, $S_{PS(N)}$, the size of which is $n \times (N-1)$. This matrix has an insufficient number of states (see TABLE II), but it forms the basis for the steps that follow. The so-called *unique ZSS matrix* for a 7-level inverter is given in (5), corresponding to S_1-S_3. In the general case of N levels:

- The 1st row (S_1) comprises of '0' in the half leftmost elements and '1' in the other half, i.e., the n top transistors in the high-side of the bridge leg conduct (e.g., Q_4-Q_6 for 7 levels).
- Every other state can be found by performing the logical operation of *circular right shift* on the previous state [43], i.e. shifting the bit-series to the right by one bit and filling in the leftmost position with the rightmost bit that was shifted out (e.g., S_2 is produced by shifting S_1, and S_3 from shifting S_2).
- This is performed n-1 times, so that all n unique ZSS that can be produced by PSPWM are captured in $S_{PS(N)}$.

$$\boldsymbol{S_{PS(7)}} = \begin{bmatrix} S_1 \\ S_2 \\ S_3 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 1 & 1 & 1 \\ 1 & 0 & 0 & 0 & 1 & 1 \\ 1 & 1 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{5}$$

B. Carrier Swapping

The next step requires the identification of the carriers that are good candidates for swapping. A pair of carriers that guaranties the production of new unique switching states are the neighboring ones with adjacent "01" or "10" pairs in every line of the S_{PS} matrix. In the 7-level inverter example, carriers 2 and 3 correspond to adjacent "01" bits in the 1st line in (5)

TABLE III
ZERO SWITCHING STATES FOR A 7-LEVEL FC INVERTER

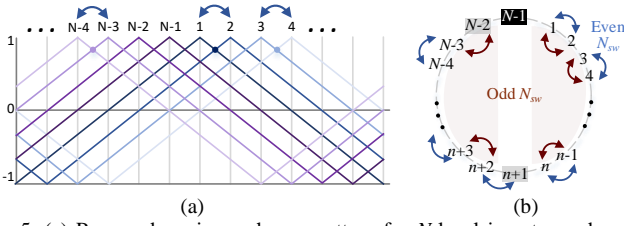| State	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	v_0
S_1	0	0	0	1	1	1	Δv_{C3}
S_2	1	0	0	0	1	1	$\Delta v_{C4} - \Delta v_{C1}$
S_3	1	1	0	0	0	1	$\Delta v_{C5} - \Delta v_{C2}$
S_4	0	0	1	1	0	1	$\Delta v_{C5} - \Delta v_{C4} + \Delta v_{C2}$
S_5	0	1	1	0	0	1	$\Delta v_{C5} - \Delta v_{C3} + \Delta v_{C1}$
S_6	0	0	1	0	1	1	$\Delta v_{C4} - \Delta v_{C3} + \Delta v_{C2}$
S_7	0	1	0	0	1	1	$\Delta v_{C4} - \Delta v_{C2} + \Delta v_{C1}$
S_8	1	0	0	1	0	1	$\Delta v_{C5} - \Delta v_{C4} + \Delta v_{C3} - \Delta v_{C1}$
S_9	1	0	1	0	0	1	$\Delta v_{C5} - \Delta v_{C3} + \Delta v_{C2} - \Delta v_{C1}$
S_{10}	0	1	0	1	0	1	$\Delta v_{C5} - \Delta v_{C4} + \Delta v_{C3} - \Delta v_{C2} + \Delta v_{C1}$

Fig. 5. (a) Proposed carrier exchange pattern for *N*-level inverter and even number of N_{sw}. (b) Representation of the proposed swapping pattern for both odd and even number of exchanges.

while carriers 6 and 1 correspond to adjacent "10" bits. All the potential carrier exchanges are reported in (6). However, the two carrier pairs in the same row are 180° phase shifted and should not be swapped simultaneously; exchanging a second pair of the same line within the same fundamental period would cancel out the effect of the first pair, meaning that fewer *unique* ZSS will be generated.

$$Potential\ Swaps\ (7) = \begin{bmatrix} \{3,4\}\ and\ \{1,6\} \\ \{4,5\}\ and\ \{1,2\} \\ \{5,6\}\ and\ \{2,3\} \end{bmatrix} \quad (6)$$

From the remaining *n* potential swaps (one per row), a combination of $N_{SW} = N_{ex} = n-1$ should be selected. Given that any carrier can be part of only one swapping pair, we end up with an easy and intuitive swapping pattern that meets the aforementioned requirements, as explained below and illustrated in Fig. 5:

- The triangle carriers are swapped sequentially in pairs of 2, except for two carriers, that is $N_{SW} = n-1$ swaps in total.
- If N_{SW} is even, the exchange sequence will be {1,2}, {3,4}, …, {N-4,N-3}, whereas the last two carriers (*N*-2 and *N*-1) are not swapped (e.g. {1,2} and {3,4} in the 7-level example). This is graphically shown in Fig. 5(a), where the respective carriers change direction whenever they meet.
- If N_{SW} is odd, the exchange sequence will be {1,2}, …, {n,n-1} and {n+2,n+3}, …,{N-3,N-2} (e.g. {1,2}, {3,4} and {6,7} for 9 levels). In other words, the first *n* consecutive carriers are swapped, leaving the carrier *n*+1 unaffected and then swapping the following *n*-2 carriers.

The complete swap pattern is depicted in Fig. 5(b), where the carrier labels are placed onto a circle and the proposed exchanges are shown with blue arrows for even N_{SW} and red arrows for odd N_{SW}. This pattern satisfies all the set requirements and holds for FC MLIs of any number of levels. Implementation of this swap mechanism is quite straightforward in any MCU and constitutes essentially the proposed CSPWM.

For natural balancing applications, realizing this swap pattern is the sole step required. For active balancing employing ac-side monitoring, the additional step of extracting the FC voltages from the output voltage remains; the following sections explain how this is done.

C. The Extended ZSS Matrix

Calculation of the FC voltages implies forming the $v_o = P \times \Delta v_C$ relation, which in turn entails composing the coefficients matrix P. To do that, we first need to derive the

independent ZSS matrix $S_{I(N)}$ that is produced with the proposed swapping pattern. $S_{I(N)}$ will incorporate the standard states generated by the PSWPM $S_{PS(N)}$ plus the additions $S_{SW(N)}$ introduced by the carrier swapping.

The new switching states $S_{SW(N)}$ can be extracted from the original state matrix $S_{PS(N)}$ once we identify *which* states are affected by the carrier swap and *how*:

- Swapping a set of carriers {*i*, *i*+1} will affect a single state, that is the one with different bits at these positions, i.e. "01" or "10" bit sequence in the columns (*i*, *i*+1). In the 7-level example, the exchange {1,2} will act upon $S_2 = \mathbf{10}0011$, while the {3,4} swap will affect $S_1 = 00\mathbf{01}11$.
- Each state affected gets the respective bits swapped, so that a new ZSS is generated. In the 7-level example, S_2 is transformed into $S_7 = \mathbf{01}0011$, and S_1 into $S_6 = 00\mathbf{10}11$.

The matrix form of the newly generated states $S_{SW(N)}$ is of $N_{sw} \times (N-1)$ size. For the 7-level inverter, $S_{SW(7)}$ is given in (7), where the exchanges are marked with bold text.

$$S_{SW(7)} = \begin{bmatrix} S_6 \\ S_7 \end{bmatrix} = \begin{bmatrix} 0 & 0 & \mathbf{1} & \mathbf{0} & 1 & 1 \\ \mathbf{0} & \mathbf{1} & 0 & 0 & 1 & 1 \end{bmatrix} \quad (7)$$

Now the matrix that incorporates all independent switching states, $S_{I(N)}$, can be derived by concatenating matrices $S_{PS(N)}$ and $S_{SW(N)}$, leading to a (*N*-2) × (*N*-1) matrix. An example of the $S_{I(7)}$ is presented in (8).

$$S_{I(7)} = \begin{bmatrix} S_{PS(7)} \\ S_{SW(7)} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 1 & 1 & 1 \\ 1 & 0 & 0 & 0 & 1 & 1 \\ 1 & 1 & 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 & 1 & 1 \\ 0 & 1 & 0 & 0 & 1 & 1 \end{bmatrix} \quad (8)$$

D. Solution to the System of Equations $v_o = P \times \Delta v_C$

The final step of this analytical methodology is to solve $v_o = P \times \Delta v_C$, which requires determination of the coefficient matrix P. This calculation is based on the principle that the conduction and current direction of a FC is determined by the state of the two neighboring transistors between which the FC positive terminal is connected to. More specifically, the capacitor C_j

- does not conduct when the devices Q_j and Q_{j+1} are both on (1) or both off (0),
- contributes to the output voltage with a positive sign (+1) when Q_j is off (0) and Q_{j+1} is on (1) and
- contributes to the output voltage with a negative sign (-1) when Q_j is on (1) and Q_{j+1} is off (0).

Thus, the contribution of capacitor C_j in the output voltage during the state S_i can be modeled by subtracting the *j* bit from the *j+1* bit in *i* row of $S_{I(N)}$, as described in (9).

$$P_{(N)}(i,j) = S_{T(N)}(i,j+1) - S_{I(N)}(i,j), \\ i, j = 1,..,N\text{-}2. \quad (9)$$

Since $S_{I(N)}$ holds a set of *independent ZSS* equal in number to the FC count, the resulting $P_{(N)}$ matrix will always be of square size (*N*-2) × (*N*-2) with a rank equal to the FC count and will *always be invertible*. $P_{(7)}$ of the 7-level example is given in
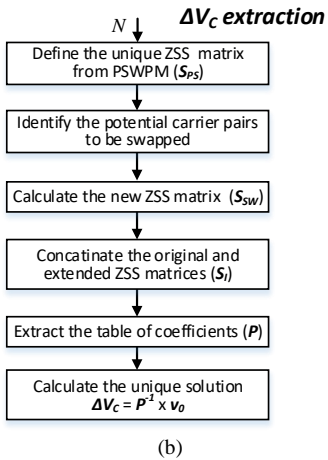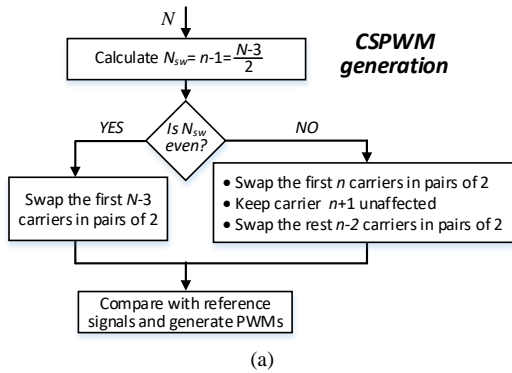
Fig. 6. Flowcharts presenting (a) the generation of the CSPWM pattern for enhanced natural balancing and (b) the extraction of the ΔV_C measurements for the ac-side monitoring and for an arbitrary umber of levels.

(10). The flying capacitor's voltage deviation can now be extracted by finding the inverse of the coefficient matrix, P^{-1}, and solving $\Delta v_c = P^{-1} \times v_o$.

$$P_{(7)} = \begin{bmatrix} 0 & 0 & 1 & 0 & 0 \\ -1 & 0 & 0 & 1 & 0 \\ 0 & -1 & 0 & 0 & 1 \\ 0 & 1 & -1 & 1 & 0 \\ 1 & -1 & 0 & 1 & 0 \end{bmatrix} \tag{10}$$

The previous analysis is summarized in the flowcharts of Fig. 6 and is implemented in the Matlab code that accompanies this paper.

An important feature of the proposed PWM extension methodology is that it always generates fully symmetrical switching states within one full period, i.e., double of the switching period. This is a key requirement for achieving fast natural balancing, as explained in [22]. An additional benefit of this approach is that the produced ZSS and their sequence in time are generated analytically without the need for complex or time-consuming simulations. This feature, along with the straightforward derivation of the solution to the system of equations for the FC voltages allows the direct application of the precise measurement system of [32] for active balancing. It is worth noting that in case this ac-side monitoring system is to implemented, the inverter switching frequency should be bounded by the limits of (11), according to [32], where ω is the angular fundamental frequency and T_{ADC} is the sample and hold time of the analogue-to-digital converter (ADC) module that captures the inverter switching node.

$$F_{sw\,min}^{\,max} = \frac{1 \pm \sqrt{1 - 2 \cdot T_{ADC} \cdot \omega \cdot (N-1)^2}}{2 \cdot T_{ADC} \cdot (N-1)} \tag{11}$$

On the contrary, if the application relies only on the improved natural balancing provided by the CSPWM, there is no practical limitation for the switching frequency. The proposed CSPWM hardly adds any computational cost, compared to the traditional PSPWM, allowing its implementation in a conventional microprocessor, as will be verified in Section V.

Overall, the proposed modulation method is an improved alternative to the traditional PSPWM any FC, with better natural balancing response, possibility to easily measure the FC voltages from a single point, with minimal added computational complexity but at the cost of slightly higher THD, as will be shown in the following Section

IV. SIMULATION RESULTS

The purpose of this section is to evaluate the scalability of the proposed PWM pattern and its dynamic performance for natural balancing against other conventional and state of the art PWMs. To this end, we have implemented the described analytical models along with detailed switching models of the entire 7-level FC inverter in Matlab/Simulink.

A. Analytical Approach

This analysis aims to validate that the prosed swapping pattern generates the right set of independent ZSS for any level and compare that to other PWMs in literature. The process starts with the generation of the triangle waveforms, followed by the calculation of the crossing points between carriers and the extraction of the ZSS for the selected carrier exchange option.

To highlight the complexity of extending the CSPWM *without a known pattern*, we have implemented an exhaustive search for the optimum solution when two pairs of carriers are swapped in a 7-level inverter. The criteria for selecting the best combination are:

1) The system of equation should have a unique solution, i.e. all ZSS are *independent*.
2) The PWM sequence should have fully symmetrical ZSS, which means that a complete sequence is comprised by an equal number of *unique* and *complementary* ZSS.
3) The system should not be overdetermined i.e., the number of *independent* ZSS is equal to the FC count.

Fig. 7 summarizes all the possible swapping combinations in a color-coded 2D table format. Every row has the same first pair of triangles and the second pair changes with different columns. Every cell contains two pieces of information: the carrier swapping combination and the number of unique ZSS. We can group the cells in four categories:

- The cells with gray background indicate that the ZSS are not *independent* even if the number of the *unique produced* ZSS is greater than $N_{FC} = 5$ (i.e., the system $v_o = P \times \Delta v_C$ is underdetermined).

1-2 & 3-4 (5)	1-2 & 3-5 (5)	1-2 & 3-6 (4)	1-2 & 4-5 (4)	1-2 & 4-6 (5)	1-2 & 5-6 (5)
1-3 & 2-4 (6)	1-3 & 2-5 (6)	1-3 & 2-6 (6)	1-3 & 4-5 (5)	1-3 & 4-6 (5)	1-3 & 5-6 (5)
1-4 & 2-3 (4)	1-4 & 2-5 (4)	1-4 & 2-6 (5)	1-4 & 3-5 (6)	1-4 & 3-6 (3)	1-4 & 5-6 (4)
1-5 & 2-3 (5)	1-5 & 2-4 (5)	1-5 & 2-6 (6)	1-5 & 3-4 (5)	1-5 & 3-6 (5)	1-5 & 4-6 (6)
1-6 & 2-3 (5)	1-6 & 2-4 (5)	1-6 & 2-5 (4)	1-6 & 3-4 (4)	1-6 & 3-5 (5)	1-6 & 4-5 (5)
2-3 & 4-5 (5)	2-3 & 4-6 (5)	2-3 & 5-6 (4)			
2-4 & 3-5 (6)	2-4 & 3-6 (5)	2-4 & 5-6 (5)			
2-5 & 3-4 (4)	2-5 & 3-6 (4)	2-5 & 4-6 (5)			
2-6 & 3-4 (5)	2-6 & 3-5 (5)	2-6 & 4-5 (5)			
3-4 & 5-6 (5)					
3-5 & 4-6 (6)					
3-6 & 4-5 (4)					

Fig. 7. All possible combinations of exchanging two pairs of carriers in a 7-level inverter. The color coding indicates underdetermined systems (in gray), overdetermined systems (in yellow), independent systems with non-symmetrical states (in light red) and independent systems and symmetrical ZSS (in dark-green, proposed pattern).

- The cells in light-red shading have an equal number of *independent* ZSS and FC count, but some states do not come into complementary pairs, i.e., the ZSS are non-symmetrical.

- The combinations in yellow color give a set of *independent* ZSS which are more in numbers than the FC count, i.e., overdetermined system. This hinders the ac-side monitoring system implementation, since it is not straightforward to form and solve the system of equations.

- Lastly, the cells in dark-green color satisfy all the set criteria by producing exactly as many *independent* ZSS as the FC count. Simultaneously, the natural balancing is optimal, while the FC voltages extraction in ac-side monitoring is easier. The proposed pattern corresponds to the top-left cell (1,1), but a close look reveals that all green cells are essentially the same pattern but with different carrier numbering. In fact, all of them can be generated from the proposed pattern by selecting an arbitrarily carrier as the starting point, i.g., starting the swapping sequence with the carrier 1, or 2, or…6. The main conclusion here is that the set requirements are met only with the proposed pattern.

Further to the exhaustive search, we validated the expandability of the proposed pattern using the Matlab code that accompanies this paper. The provided code generates the matrices S_{SP}, S_{SW} and S_I, it calculates the coefficient table P and solves the system of equations $\Delta v_c = P^{-1} \times v_o$, by computing the inverse P^{-1}, for any number of levels N (input). Repetitive execution of the Matlab script for a wide range of levels proves that the CSPWM pattern always generates an independent system of equation with symmetrical states. This is graphically illustrated in Fig. 8 that shows the rank of the equation matrices for the CSPWM (blue circle markers), the PSPWM and the MPDPWM (both in red square markers) for $N = 3,…,51$. The rank of these matrices represents the number of independent
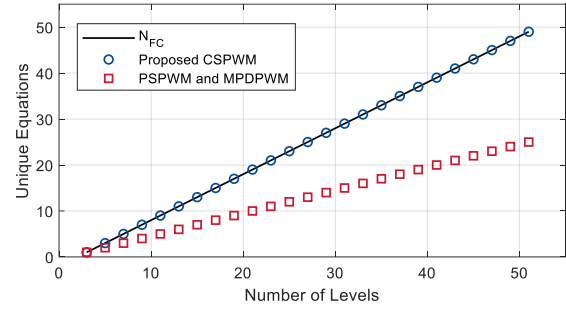

Fig. 8. Number of independent equations generated by the CSPWM, the PSPWM and the MPDPWM for a wide range of levels.

equations. It is evident that only the proposed PWM pattern produces an adequate number of independent equations, equal to the number of FC, marked with black sold line. This in turn means that, contrary to alternative methods, the CSPWM allows all FC to be independently expressed at the inverter output voltage for any number of levels, leading to optimal natural balancing.

B. Switching Model Simulations

Here we investigate the natural balancing performance for the proposed CSPWM pattern against the conventional PSPWM and the modified PDPWM, during an instantaneous imbalance. Such imbalance can be caused by load disturbances or grid-side asymmetries and will be reflected to the capacitor voltage levels. Yet, the most representative short-term imbalance condition, that is also implementable and reproducible in the experimental setup, is the step change to the DC voltage. It is expected that the implemented PWMs will compensate for the voltage imbalance, leading the system back to stability. The simulation parameters are listed in TABLE IV.

For the first test we simulated a 3-phase 7-level FC inverter operating at 16.67kHz and feeding a symmetrical resistive load of 10 Ω through an inductive filter of 270 μH. The star neutral was connected to the dc-link mid-point. We investigated the worst-case scenario of $m_a = 0$, which corresponds to the maximum balancing time, as mentioned in Section II, and thus, it best highlights the strength or weakness of a PWM scheme. Fig. 9 shows the FC voltages during a step change of the dc-link from 0 V to 300 V. It is evident that the CSPWM pattern exhibits the fastest natural balancing response for all FC compared to the conventional PSPWM and the MPDPWM. The only exception is the middle capacitor (C_3 for the 7-level inverter) for which the PSPWM and MPDPWM are marginally faster. This is attributed to the fact that C_3 is contributing independently to the inverter output voltage (state $S_1 = 000111$) twice as many times as in the CSPWM.

It is worth noting that the natural balancing settling time is affected by the switching frequency, as formulated in [36], [37] for the PSPWM. However, the CSPWM performs better

TABLE IV
MATLAB/SIMULINK SIMULATION PARAMETERS

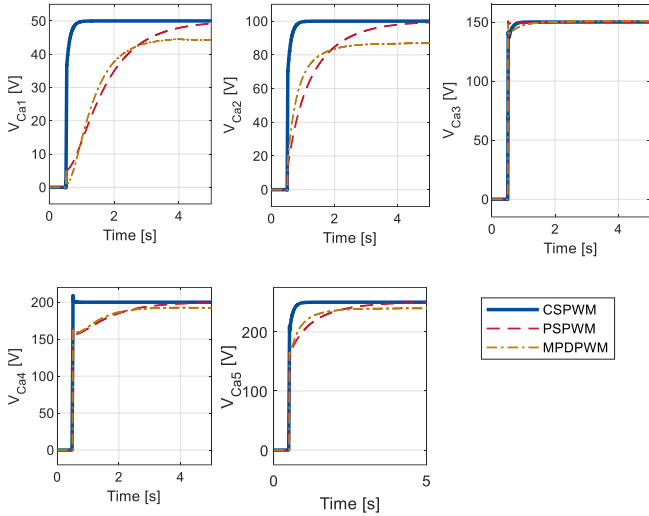| Parameter	Levels	R_{load}	v_{DC}	F_{sw}	C_{DC+}, C_{DC-}	C_{FC}	L_F
Value	7 to13	10 Ω	300 V	16.67 kHz	50 μF	10 μF	270 μH

Fig. 9. Natural balancing response of a 7-level FC inverter operated with the CSPWM, the PSPWM, the MPDPWM, during a step change of the dc-link voltage from 0 V to 300 V. The worst-case scenario of $m_a = 0$ is simulated.

Fig. 11. FC voltage deviation during a step change of the dc-link voltage from 200 V to 300 V. The ac-side measurements are plotted against the actual ΔV_C signals.

compared to other PWM methos, and the settling time is the smallest possible for the given switching frequency.

Further to the 7-level MLI results, we have developed the switching models of a 9-, 11-, and 13-level inverter to validate the performance of the generalized CSPWM for a larger number of levels and thus prove the extension effectiveness of the proposed pattern. The rest of the simulation parameters are kept the same as the 7-level test, tabulated in TABLE IV. For presentation coherence, we only plot the response of C_3 during natural balancing in Fig. 10. This graph highlights the advantages of the CSPWM for faster natural balancing and more precise capacitor level compared to the commonly used PSPWM and the state-of-the-art MPDPWM.

Further to the natural balancing simulations we investigated the performance of the ac-side monitoring system with an analytical calculation of the ΔV_C signals [32]. To record a sharp FC voltage variation, the inverter was subjected to a step dc-link change from $v_{DC} = 200$ V to $v_{DC} = 300$ V while the modulation index was fixed at $m_a = 0.8$. The measurements extracted from the ac-side sensing are plotted against the actual FC voltage deviation signals in Fig. 11. Although the sampling rate is very high (one sample per ZSS, i.e., the sampling frequency is $F_{SW}/(N\text{-}1)$) the measurements are updated once every zero crossing of the inverter output voltage, thus twice in one fundamental period, as can be seen from the zoomed view in Fig. 11. This is a typical feature of an ac-side monitoring
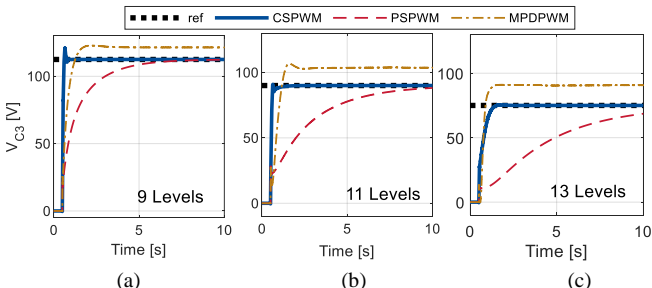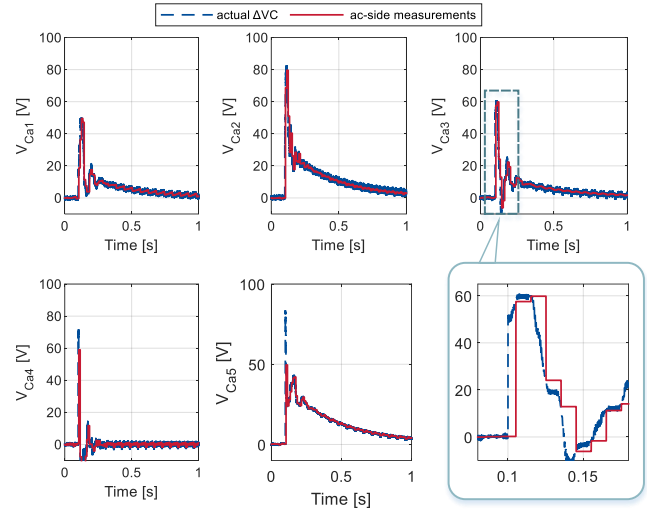
approach which, despite the relatively small update frequency, is proven to be effective for active balancing [32]–[35].

Even under such harsh conditions, the analytical extraction of the ΔV_C values is accurate allowing the application of an active balancing scheme.

Another important characteristic of any PWM strategy is the total harmonic distortion (THD) of the generated output current. To quantify the THD of the PWMs under investigation, we simulated the MLIs for a wide range of levels (from 7 to 13 levels) with the parameters of TABLE IV and a fixed amplitude modulation index of 0.8, under steady state conditions. All simulations were executed with a discrete step of 200 ns and the THD was calculated during 4 fundamental cycles. The results tabulated in TABLE V show that the PSPWM generates the lowest harmonics followed by the MPDPWM and then the CSPWM. However, the difference in THD between the proposed PWM and the conventional PSPWM falls with the number of levels from 0.57% to only 0.2%. This could be considered a small price to pay for an improved natural balancing and a very cost-effective and compact measurement system that results from the direct expression of all FC at the inverter switching node.

The simulation results have demonstrated that the proposed PWM extension pattern generates an adequate number of independent equations with symmetrical switching states for any number of levels at the cost of slightly higher THD of the output current. The CSPWM leads to fastest natural balancing response with accurate steady state FC voltages and direct expression of all FC to the inverter switching node for a precise voltage measurement through a simple, cost effective and compact ac-side circuit.

Fig. 10. Natural balancing response of C_3 in a (a) 9-level, (b) 11-level and (c) 13-level FC inverter with different modulation strategies, during a step change of the dc-link voltage from 0 V to 300 V

TABLE V
OUTPUT CURRENT THD FOR DIFFERENT NUMBER OF LEVELS AND MODULATION STRTEGIES

Levels	PSPWM	MPDPWM	CSPWM
7	1.29 %	1.66 %	1.86 %
9	0.72 %	1.34 %	1.11 %
11	0.67 %	0.95 %	0.86 %
13	0.57 %	0.93 %	0.77 %

V. EXPERIMENTAL VERIFICATION

For the experimental evaluation of the proposed CSPWM extension we have designed and developed a 7-level all-GAN inverter depicted in Fig. 12, with the components and parameters listed in TABLE VI. The DC-link is located in the main printed circuit board (PCB) and each of its capacitors, C_{DC+} and C_{DC-}, is comprised by 12 parallel connected polypropylene film capacitors, with a total capacitance of 12 · 4.7µF = 56.4 µF. The main board also holds the DC and AC input and output measurement sensors and the microcontroller.

A single phase-leg PCB, shown in Fig. 12(b) in white solder mask, holds the twelve EPC2034 transistors, their gate drivers (UCC27611), and the accompanying power and digital isolators (MTU1S1205MC and Si8610BC-B-IS, respectively). Each FC, mounted on the back side of this PCB, consists of several parallel connected multi-layer ceramic capacitors (MLCC), to reach 10µF. The number of parallel MLCCs is proportional to the voltage stress of every FC, as the selected components (C5750X6S2W225K250KA) exhibit a sharp decline of their capacitance with the applied DC bias [44].

The measurement module, shown in Fig. 12(b) in black solder mask, is dedicated for monitoring the FC voltages with two methods: i) the conventional galvanically isolated voltage divider and ii) the ac-side monitoring system proposed in [32].

The switching frequency was set to F_{sw} = 66.667 kHz, which corresponds to a ZSS pulse-width of 2.5 µs. The implemented CSPWM is presented in Fig. 13(a). Carriers {1,2} and {3,4} switch positions at their intersecting point, while carriers 5 and 6 remain unaffected, as can be seen from the zoomed view on the right. The black trace indicates a region close to the output
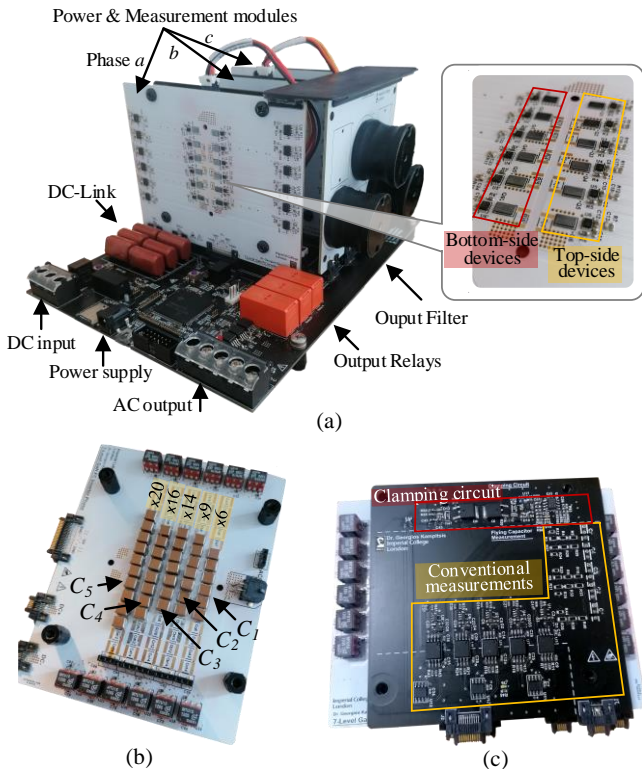
TABLE VI
LIST OF COMPONENTS OF THE 7-LEVEL INVERTER PROTOTYPE

Main and Filter Board		Clamping Circuit	
Component	*Part No*	*Component*	*Part No*
DC-link Capacitors	ECW-FD2W475KC 12p2s configuration	MOSFETs	STD8N60DM2
microcontroller	F28384D	Instrumentation Amp	AD8421ARMZ
Current sensor	MLX91221	Operation Amp	OPA2189
Voltage isolator	ACPL-C87A	Zener Diodes	KDZVTFTR20B
ADC module	ADS7953	R_S	200 Ω
Filter Inductors	1140-271K-RC	v_{DD}	12V

Power Board					
Component	*Part No*				
Flying Capacitors	C5750X6S2W225K250KA				
	C_1	C_2	C_3	C_4	C_5
	6p1s	9p1s	14p1s	16p1s	20p1s
GaN Devices	EPC2034				
Gate Driver	UCC27611DRVT				
Digital isolator	Si8610BC-B-IS				
Power isolator	MTU1S1205MC				
F_{sw}	66.667 kHz				

voltage zero crossing, where the ZSS are manifested with the longest possible pulse width. More details for this ac-side monitoring method may be found in [32]. The gray peaks represent the instances of the different ZSS and can be used for sampling the inverter switching node to obtain $v_o(S_I)$. The system was initially tested in steady state conditions under v_{DC} = 140V, as demonstrated in Fig. 13(b). In this graph the input and output voltage waveforms are plotted, along with transistor's Q_2 drain-source voltage.

A. Natural Balancing under Disturbances

The natural balancing response of the proposed CSPWM was initially evaluated against the conventional PSPWM under a sharp voltage change on the dc-link. More specifically, v_{DC} was originally set to zero and subsequently was increased to 140 V in a step manner. At the same time, the modulation index was set to zero, $m_a = 0$, so that only the ZSS contribute to the natural balancing. The FC voltage measurements were

Fig. 12. (a) GaN MLI prototype used for the experimental validation. (b) Bottom view of a single phase-leg board. (c) FC measurement module.
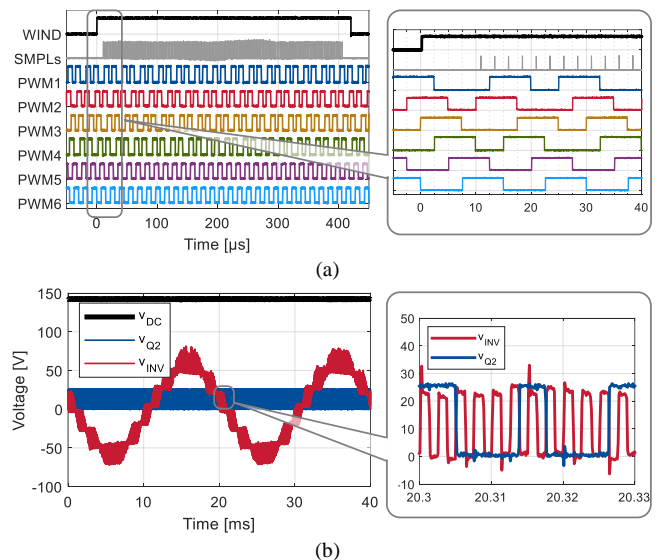

Fig. 13. (a) Experimental measurements of the proposed CSPWM sequence for a 7-Level inverter. The gray trace indicates the sampling timing of the inverter output voltage close to the zero-crossing point, marked with a black trace. (b). Input and output voltage waveforms for the 7-level inverter when v_{DC} = 140V. The transistor's Q_2 drain-source voltage is also included in the same graph.
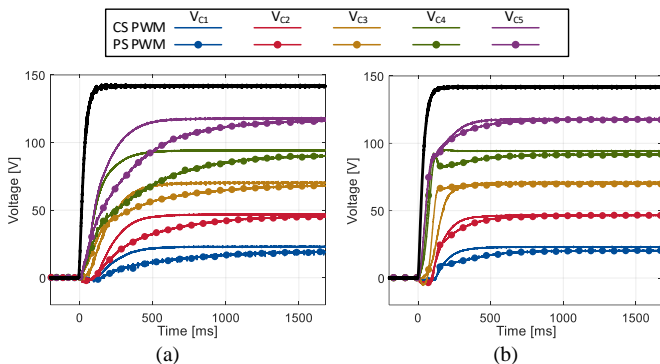
Fig. 14. Natural balancing response of the CSPWM against the PSPWM during a step change of the dc-link (black trace) and (a) no-load conditions and (b) the inverter feeding an RL load.

recorded for two scenarios: a) no-load conditions and b) the inverter feeding an RL load with $R = 10\ \Omega$ and $L = 270\ \mu H$. The results are plotted in Fig. 14, where the CSPWM is shown in solid lines and the PSPWM with circle marks. Comparing (a) with (b), we observe faster response in high loads as the imbalance energy is dissipated more rapidly. But in both scenarios the CSPWM has enhanced natural balancing response with 3 times lower settling time (10% to 90%) than the PSPWM (calculated as an average over all FC). It is only C_3 voltage that exhibits slightly faster response with the PSPWM and RL load, as explained in Section IV.

B. Natural Balancing at Permanent Asymmetries

With the second experiment we evaluate the performance of the CSPWM in an inherent/permanent system asymmetry. To this end, we introduced an abrupt imbalance at $t_0 = 0$, with the form of a resistor, $R_{asym} = 47\ k\Omega$, connected across C_4. The oscilloscope waveforms for the FC voltages are plotted over time in Fig. 15, where the solid lines correspond to the proposed CSPWM and the traces with circle marker to the PSPWM. The results highlight that the CSPWM helps the FC maintain a smaller voltage deviation especially C_1 and C_4, compared to the PSPWM.

C. Ac-side Monitoring

Lastly, the same test conditions are applied to demonstrate the extraction of the FC voltage deviation, ΔV_C, through the ac-side monitoring system of [32]. Please also note that the introduction of the clamping circuit on the switching node of the inverter will not affect the natural balancing response, due to the minimal added parasitic components.
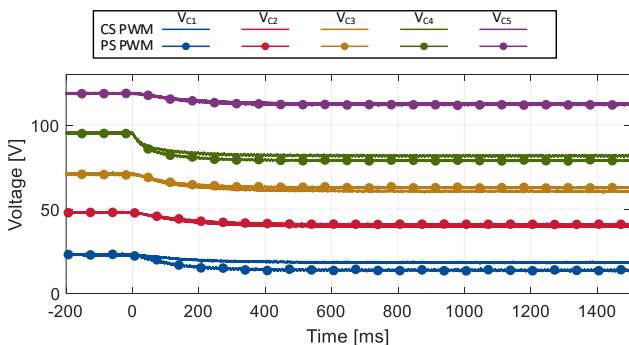

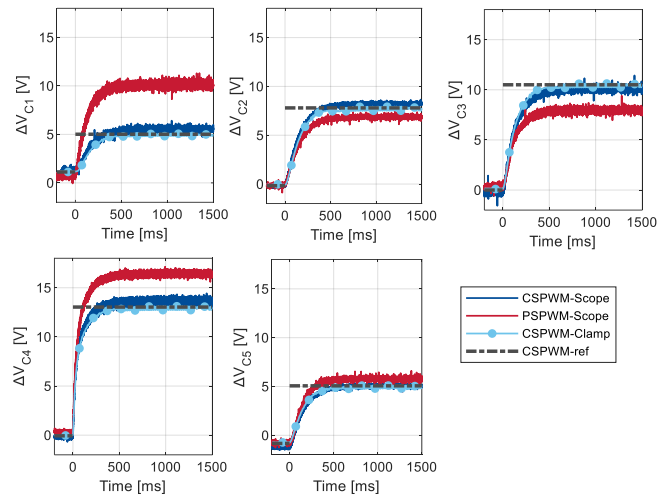Fig. 15. FC voltages measured under step-wise asymmetry introduced on C_4.

Fig. 16. Voltage variation the FC (a) Δv_{C1}, (b) Δv_{C2}, (c) Δv_{C3}, (d) Δv_{C4} and (e) Δv_{C5}, when a step-like asymmetry is introduced in C_4 of a 7-level inverter at $t_0 = 0$ and $v_{DC} = 140$ V. Comparison between traditional voltage devider sensor and analytical extraction method.

Having the coefficient table of the 7-level inverter from the analytical method (10), we can solve the system of equations (1) just by sampling the inverter output on every ZSS. Fig. 16 shows the results of the analytical solution with light-blue traces and round markers in comparison to the respective oscilloscope measurements (in dark blue color). The gray dash-dotted lines correspond to the true-RMS measurements via a digital multimeter, before and after the asymmetry. For sake of completeness, we have also included the FC voltage deviation when the PSPWM strategy is applied (red traces), which of course cannot lead to an analytical solution.

The analytical extraction of the FC voltages always gives a valid solution that perfectly coincides with the reference (multimeter) measurements. In fact, it approximates the ΔV_C values even better than the oscilloscope, whose samples deviate slightly from the true RMS measurements as the oscilloscope needs to contain the entire V_C waveform with finite resolution within the screen, to avoid the overdrive phenomenon [45].

The experimental results showed that the proposed PWM extension is advantageous not only in natural balancing but also helps with the calculation of the FC voltage levels in a simple, accurate and compact method, ideal for the next generation GaN-based MLIs.

VI. CONCLUSION

In this work we have introduced a generalized PWM strategy for FC MLIs, that ensures enhanced natural and active balancing. The methodology is based on swapping a predefined set of neighboring carriers within two consecutives switching cycles and the pattern is applicable to any number of levels. The result of this analytical method is the extraction of the *independence* ZSS, their sequence in time and system of equations that relates the FC voltages to the inverter output voltage. The proposed PWM always generates fully symmetrical switching states and the unique solution to the system of equations allows direct application of a compact and fast ac-side FC monitoring system that can subsequently be

used for active balancing. The implementation simplicity of the generalized CSPWM hardly adds any computational cost, thus favouring the use of a readily available and cost-effective microprocessors instead of sophisticated FPGAs. The advantages of the CSPWM come at a cost of slightly higher THD of the inverter output current. Simulation and experimental results on a 7- to 13-level GaN-based inverter validate the improved natural balancing response of the CSPWM during sudden dc-link voltage variations and its enhanced performance in system asymmetries. The extended CSPWM pattern can be a very useful tool for the next generation high-power density and high-frequency GaN MLIs.

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Georgios Kampitsis (Member, IEEE) received the Diploma and Ph.D. degrees in electrical and computer engineering from the National Technical University of Athens (NTUA), Greece, in 2011 and 2016, respectively. In 2017, he joined the Power and Wide-Band-Gap Electronics Research Laboratory, École Polytechnique Fédérale de Lausanne, Switzerland, as a Post-Doctoral Researcher (2017-2019), working on efficient GaN power converters. Since 2020 he has been a Research Fellow with Imperial College London, U.K., holding an EU Marie-Curie individual Fellowship on high power density converters for distributed energy resources**.** His research interests include the development and control of compact power converters based on wide-band-gap (WBG) semiconductor devices (SiC and GaN) for renewable energy source (RES) applications.

Efstratios I. Batzelis (Senior Member, IEEE) received the Ph.D. degree from the National Technical University of Athens (NTUA), Athens, Greece, in 2016. Since 2021, he has been a Lecturer with the University of Southampton, Southampton, U.K. and a Research Fellow with the Royal Academy of Engineering, London, U.K., working on solar integration in developing countries. Prior to that since 2019, he was a Research Fellow with Imperial College London, London, U.K., and before that he held an EU Marie-Curie individual Fellowship on photovoltaic control & integration in 2017–2019 also with Imperial College London. His research interests include renewable energy technologies and distributed energy resources, mainly solar photovoltaics, power electronics control, and power system dynamics and stability. He is currently an Associate Editor for IEEE Transactions on Sustainable Energy.

Antonis Kolokasis (Member, IEEE) received the MSc. Degree Future Power Networks from Imperial College London, England, and the B.Eng. Degree in electronic and electrical engineering from the University of Huddersfield, England, in 2021 and 2020, respectively. In 2021, he joined Energy & Beyond LTD electricity supply company of Green Energy Group, Limassol, Cyprus, as an electricity market operator (2021-2022), working in solar power plant design and renewable energy trading. Since 2022 he has joined the Cyprus Energy Regulatory Authority (CERA), working as an energy engineer, conducting research on the EU programs undertaken by the authority as part of its commitments for Research, Technological Development, and Innovation. The programs include development of emission reduction technologies, enabling smart grid technologies and increasing penetration of RES and storage in Cyprus.

Elison Matioli (Senior Member, IEEE) received the double B.Sc. degrees from École Polytechnique, Palaiseau, France, and Escola Politecnica—Universidade de São Paulo (USP), São Paulo, Brazil, in 2005, and the Ph.D. degree from the Materials Department, University of California at Santa Barbara (UCSB), Santa Barbara, CA, USA, in 2010. He was then a Postdoctoral Fellow with the Massachusetts Institute of Technology (MIT), Cambridge, MA, USA, from 2010 to 2014. He is currently an Associate Professor with the Institute of Electrical Engineering, École Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland. His research interests include the fields of wide-band-gap semiconductor devices for power electronics and ultrafast RF devices, thermal management of electronics based on microfluidic cooling, and high-efficiency high-power-density power converters.

Bikash C. Pal (M'00-SM'02-F'13) received B.E.E. (with honors) degree from Jadavpur University, Calcutta, India, M.E. degree from the Indian Institute of Science, Bangalore, India, and Ph.D. degree from Imperial College London, London, U.K., in 1990, 1992, and 1999, respectively, all in electrical engineering. Currently, he is a Professor in the Department of Electrical and Electronic Engineering, Imperial College London. His current research interests include renewable energy modelling and control, state estimation, and power system dynamics. He is Vice President Publications, IEEE Power & Energy Society. He was Editor-in-Chief of IEEE Transactions on Sustainable Energy (2012-2017) and Editor-in-Chief of IET Generation, Transmission and Distribution (2005-2012) and is a Fellow of IEEE for his contribution to power system.