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Medipix4, a high granularity four sides buttable pixel readout chip for high resolution spectroscopic X-ray imaging at rates compatible with medical CT scans

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Viros Sriskaran

Abstract

Medipix4 is the latest member in the Medipix/Timepix family of pixel detector chips aimed at high rate spectroscopic X-ray imaging using high-Z materials. The chip address the limitations of conventional hybrid pixel detectors for X-ray imaging. Its predecessor, Medipix3RX, covered some of those limitations and demonstrated the possibility of spectroscopic X-ray imaging at a fine pitch while keeping the spectral fidelity using a charge-sharing correction algorithm. However, its use in medical imaging, synchrotron applications, material analysis, and other applications highlighted some limitations. Indeed, the 3-side buttable architecture in Medipix3RX and other actual X-ray imaging systems introduces a dead zone in the imaging that closes the door to constructing large-area detectors. Moreover, the improvement in the dynamic energy range, the count-rate capability, and the energy resolution will benefit those applications.

This thesis describes the Medipix4 chip implementation and discusses the proposed new pulse processing electronics in the analog pixel. The readout architecture relies on single photon counting with charge sharing correction for the energy binning of incoming hits. The chip consists of 320 x 320 pixels of 75 µm x 75 µm. It can work in Fine Pitch Mode (FPM) with 75 µm pixel pitch and two threshold bins per pixel or in Spectroscopic Mode (SM) with 150 µm pitch and up to eight energy threshold bins. Unlike its predecessor, Medipix3RX, it will be possible to tile the ASIC fully in both x and y directions, permitting seamless large area coverage. The chip size is 24 mm x 24 mm and covers 99.37% active area when using TSV connections only.

The ASIC is designed in a commercial CMOS 130 nm process technology with a power supply of 1.2 V. The new analog front-end architecture improves the energy dynamic range, the count-rate capability, and the energy resolution compared with Medipix3RX while the charge sharing correction is still supported. Those improvements come at the expense of power consumption and spatial resolution. The latter should not be a problem since studies have shown that the optimal pixel pitch for CdTe or CdZnTe should be slightly larger than the Medipix3RX pixel in order to account for a larger fraction of fluorescence photons.

Each analog pixel contains a Charge Sensitive Amplifier with a DC leakage compensation network up to 50 nA. Two pulse-shaping circuits in the second stage implement the charge sharing correction mode. The new shaper amplifier has a reduced baseline drift at high flux compared to the amplifier implemented in the previous Medipix/Timepix chips. The implemented ASIC has three modes of operation: High Dynamic Range Mode (HDRM), Low Noise Mode (LNM), and Ultra-Fast Mode (UFM). In HDRM, the chip can process X-ray photons with energies up to 154 keV with a CdTe sensor, implying 40% improvement compared to Medipix3RX. In LNM, the expected energy resolution has been improved by 55 %. In UFM, the post-layout simulated count-rate capability of the front-end is 19×10^6 photons.mm^{-2}.s^{-1} at 10% hit loss for a 150 µm pixel pitch and not affected by charge sharing effect, showing an improvement by a factor of 5. In addition, the pixel includes a digital pile-up filtering method that improves spectral fidelity at high rates.

Keywords

Front-end electronics, Charge sharing, Photon counting, Photon processing, Hybrid pixel detectors, Medipix, Timepix, X-ray imaging, Pile-up.

Résumé

Medipix4 est le dernier détecteur hybride de pixels conçu dans la famille Medipix/Timepix destiné pour la spectroscopie avec rayons X à haut taux de comptage. Cette puce est compatible avec les semi-conducteurs avec un numéro atomique élevé et résout les limitations des détecteurs hybrides de pixels utilisés pour l'imagerie par rayons X. Son prédécesseur, Medipix3RX, avec l'algorithme pour corriger le partage de charges, a permis de résoudre quelques limitations et a démontré que la spectroscopie par rayons X était possible en utilisant des pixels de très petites tailles tout en conservant la fiabilité spectrale. Cependant, ses utilisations dans les applications médicales, synchrotrons, analyse de matériaux, et autres applications ont signalés quelques limitations. En effet, Medipix3RX mais aussi les autres systèmes d'imagerie par rayons X actuels permettent seulement la butée des puces contre trois côtés, ce qui limite la construction des détecteurs de grandes surfaces. De plus, une amélioration du gamme d'énergie, du taux de comptage, et de la résolution d'énergie peuvent bénéficier ces applications.

Cette thèse explique l'architecture de Medipix4 et décrit une nouvelle électronique pour le traitement de photons dans la partie analogique du pixel. L'architecture de lecture utilise le comptage de photons avec un algorithme de correction du partage de charges pour la répartition des évènements en fonction de leurs énergies. La puce est une matrice de 320 x 320 pixels ayant une taille de 75 µm x 75 µm. Deux seuils sont disponibles en Fine Pitch Mode (FPM) pour un capteur dont le pas de pixel est de 75 µm. En Spectroscopic Mode (SM), pour un capteur avec un espacement entre les pixels de 150 µm, on dispose de huit seuils. Contrairement à Medipix3RX, la puce est apte à venir en butée contre les quatre côtés, cela permet la construction des détecteurs couvrant une grande surface sensible. La taille de la puce est de 24 mm x 24 mm et a une zone sensible de 99.37% lorsque les connections TSV sont utilisées.

Medipix4 a été conçu avec une technologie commerciale CMOS 130 nm à partir d'une alimentation d'entrée de 1.2 V. La nouvelle architecture pour l'électronique analogique du pixel améliore la gamme d'énergie, le taux de comptage, et la résolution d'énergie par rapport à Medipix3RX tout en conservant la correction pour le partage de charges. Ces améliorations ont été possibles aux dépens d'une petite augmentation de la consommation de puissance et de la résolution spatiale. Une plus grande taille du pixel permettrait de capturer les photons de fluorescences qui déposent leurs énergies loin du point initial d'interaction dans les capteurs de CdTe ou CdZnTe.

Chaque pixel analogique comporte un amplificateur sensible à la charge avec un mécanisme de compensation du courant de fuite jusqu'à 50 nA. Deux circuits de mise en forme d'impulsions permettent d'assurer la correction du partage de charges. Ces deux circuits ont une faible dérive de la ligne de base à haut taux de comptage par rapport aux précédents amplificateurs des puces Medipix/Timepix. On propose trois modes de fonctionnement pour la puce : High Dynamic Range Mode (HDRM), Low Noise Mode (LNM), et Ultra-Fast Mode (UFM). Avec HDRM, la puce peut détecter des rayons X avec une gamme d'énergie allant jusqu'à 154 keV pour un capteur de CdTe, suggérant une expansion de 40% par rapport à Medipix3RX. Avec LNM, on prévoit une amélioration de 50% sur la résolution d'énergie. Après la disposition du layout, les simulations indiquent un taux de comptage de photons jusqu'à 19 x 10^6 photons.mm^{-2}.s^{-1} avec 10% de perte d'évènements lorsque l'électronique est configurée pour les pixels de 150 µm et avec correction du partage de charges. Le taux de comptage est cinq fois élevé qu'avec Medipix3RX. Et enfin, la partie digitale du pixel comporte un mécanisme de filtrage des évènements qui s'empilent. Ce procédé de filtrage permet d'améliorer la fiabilité spectrale à haut taux de comptage.

Mots-clés

Electronique Frontale, Partage de charge, Comptage de photon, Traitement de photon, Détecteur hybride de pixels, Medipix, Timepix, Imagerie par rayons X, Pile-up.

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Chapter 1 Introduction

The idea of using pixel detectors to identify the nature of incident particles by detecting their characteristic patterns in the pixel matrix is proposed in [1]. In 1988, a CERN team design introduced hybrid pixelated devices in which a sensor matrix is connected to a readout chip on different substrates. The hybrid pixel technology became a candidate for particle tracking along with the monolithic pixel detectors [2], which were developed under the RD19 collaboration at CERN. The first pixelated chip with 9 x 12 pixels, manufactured in a 3 µm CMOS process, was designed at CERN in collaboration with the microelectronics group at EPFL (the designers are Enz, Krummenacher, and Vittoz), and with the support of the particle physics group at the ETHZ and the Swiss National Fund [2]. The first measurements with wire-bonded instead of external connections between the sensor and the readout pixels are published in [3]. Using bump bonded connections allowed exact matching of the readout matrix to the sensor matrix.

Many chips followed the hybrid pixel design and allowed the collaboration to gain experience in designing such detectors. The WA97 heavy-ion experiment implemented a detector called Omega2, with a large sensitive area of 13 x 63 pixels and with a pixel dimension of 75 x 500 µm². Total area coverage of 5 cm² was obtained by connecting six ladders of 6 chips. Figure 1.1 shows the tracking capability of this hybrid pixel detector with an excellent spatial resolution. The figure shows that every dot is associated with a track. This experiment demonstrated the unique features of hybrid pixel detectors: the ability to take noise hit free tracks at a high rate.

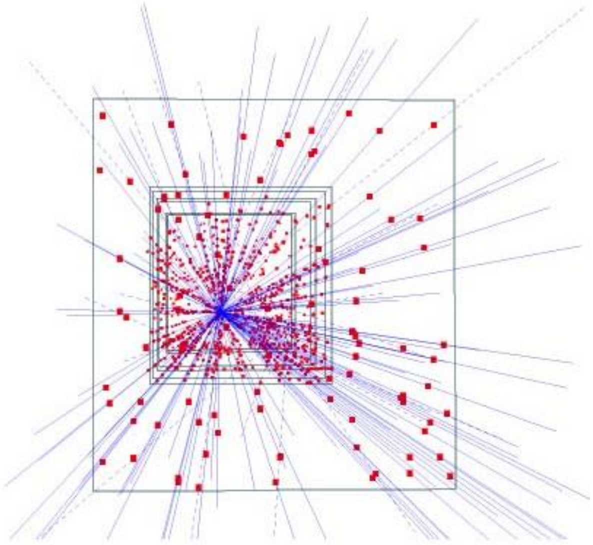


Figure 1.1. A fixed target Pb-Pb event reconstruction with 153 tracks, using a seven-plane pixel telescope in WA97. Each 'Window' represents 5 x 5 cm², having 72000 pixels. The pixel dimension is 75 x 500 µm². The tracks have been reconstructed with a trigger precision of 1 µs and a radiation tolerance of around 30 kRad. The red dots on the figure represents the detected hits in the silicon detectors [4].

The Medipix collaborations have been created to transfer the technology of hybrid pixel detectors, from the original use in High Energy Physics (HEP) applications, into other fields of science like medical imaging, synchrotron applications, material analysis using X-ray sources, electron microscopy, and others [5].

Trends in the microelectronics industry and the need for increased functionality and performances concerning the state-of-the-art pixel circuits oblige the radiation instrumentation community to continue following Moore's Law in developing pixelated front-end electronics [6]. However, each new technology node requires a significant effort to understand how high-performance (low-power, low-voltage, and small-area) analog designs can be implemented. A particular challenge is how to design circuits that perform consistently when implemented in large arrays.

This thesis focuses on the implementation and design of Medipix4 ASIC (Application-Specific Integrated Circuit) using a CMOS 130 nm process and 9-metal layers. Medipix4 is the latest member of the Medipix family of pixel detector readout chips aimed at high rate spectroscopic X-ray imaging. The author, throughout this thesis, provides a guideline to the reader on the design of a large area pixel detector. In addition, the author emphasizes the technical challenges encountered in the design phase and the strategies developed to overcome those difficulties. This thesis is structured as follows:

- Chapter 2 is an introduction to X-ray imaging. The first part reviews the interaction of photons with matter. The second part presents a classification of imaging systems according to the energy conversion method and processing electronics. Finally, the ideal X-ray image detector requirements are examined, and the advantages of a hybrid photon counting system in X-ray imaging are presented.

- Chapter 3 is a review of hybrid pixel detectors for X-ray imaging. The signal formation in the sensor volume is analyzed in section 3.1.1. Section 3.1.2 emphasizes the limiting factors that have to be considered when designing sensor pixels. The absorption efficiency, charge sharing, generation of fluorescence photons, charge trapping and recombination, and polarization effects are discussed. The flip-chip process to connect the sensor pixel to its readout electronics is briefly described in section 3.2. The pulse processing electronics are detailed in section 3.3.1. The limiting factors in the analog processing chain, such as electronic noise, threshold mismatch, gain mismatch, ballistic deficit, and pulse pile-up, are presented in section 3.3.2. The performances of existing hybrid pixel detectors are also compared in this chapter.

- Chapter 4 presents the Medipix family of chips and the Medipix readout applications. First, X-ray imaging using single-photon processing architecture was demonstrated with the Medipix1 chip (section 4.1). Later, the Medipix2 was developed to explore spectroscopic imaging at a very fine 55 µm pixel pitch (section 4.2). Degradation of the energy spectrum was measured with Medipix2 due to charge sharing between pixels and the generation of fluorescence photons in high-Z materials. A charge sharing correction algorithm was implemented in the Medipix3RX chip (section 4.3). The latter's limitations are analyzed in view of the design of Medipix4 ASIC, which proposes solutions.

- Chapter 5 focuses on the Timepix family of chips and summarizes its applications. Timepix chip is derived from the Medipix2 readout and can detect the energy or arrival time of the incoming particles (section 5.1). Timepix3 is the second chip produced in the Timepix family. Timepix3 provides the energy and the time of arrival information simultaneously and with a better time resolution than Timepix chip (section 5.2), time bin being 1.56 ns. Another innovation in Timepix3 is its data-driven readout. Timepix2 was designed and produced later for the applications requiring measurements in mixed radiation fields (section 5.3). In the framework of the design of the Timepix2 chip, the author implemented a rail-to-rail buffer using the CMOS 130 nm process to monitor the output signal of the front-end. He then contribute to the design of the analog periphery of the chip containing the Digital-to-Analog Converters (DACs) to bias the analog pixel. The chip was fabricated in silicon and was characterized electrically. Timepix4 is the last ASIC in the Timepix family of chips manufactured using the CMOS 65 nm process (section 5.4). The chip can be tiled seamlessly on four sides and provides a time bin of 200 ps. The author implemented a slow Rail-to-Rail (RtR) buffer for the biasing of the DACs and a fast one to monitor the high-speed signals.

- Chapter 6 focuses on the design and implemention of the last ASIC in the Medipix family called Medipix4, which is the core of this thesis. The chip is 4-side buttable like Timepix4 and targets high-rate applications using high-Z materials. The chapter highlights the importance of a top-to-bottom methodology in large-area chip design. The Medipix4 chip results from a collaboration between engineers and physicists teams. The author will mainly discuss his contribution, which is the design of the analog front-end of the chip, and briefly report the other work for completeness. The author studied the power distribution and the redistribution layer to achieve the 4-side buttable feature (section 6.2). He then implement a new architecture in the analog pixel to overcome the limitations observed with Medipix3RX and other photon-counting detectors (section 6.3). In the digital pixel, a new approach deals with pile-up events (section 6.4).

- Chapter 7 concludes this thesis and shows the main results.

The publications generated by this work are listed at the end of this manuscript.

Chapter 2 Introduction to X-ray imaging

A new era started after the discovery of X-rays by the physicist and engineer Wilhelm Conrad Röntgen in 1885. Many applications benefit from their use, especially in medical applications. Indeed, X-rays can pass through various materials without significant scattering and enables interior objects imaging. X-ray detection systems were based on a phosphorous screen and a light-sensitive film resulting in an analog image. The digital format is preferred for storage and image post-processing [7], [8]. This chapter presents the X-ray imaging systems, which convert X-ray photons into electrical signals written in a digital format. The interactions between X-ray photon and matter are described in section 2.1. The X-ray detector uses a material capable of absorbing the incident photon and converting its energy directly or indirectly into a measurable electrical signal. Readout electronics are used to process this signal. There are two architectures to achieve this operation: energy integrating or pulse processing architectures. Section 2.2 presents the two processing methods and details their advantages and drawbacks. Section 2.3 describes an ideal X-ray detector and introduces the hybrid pixel detector.

2.1 Interaction of X-rays with matter

Four processes describe the interaction of X-ray photons in the semiconductor material: photoelectric absorption, pair production, Compton scattering, and Rayleigh scattering.

2.1.1 Photoelectric absorption

In the photoelectric absorption effect, the incident photon interacts with an atom of the sensor material and disappears. A photoelectron is ejected from the atomic shell during this process. The energy of the photoelectron is given by:

$$E = hv - E_b \tag{2-1}$$

Where hv is the energy of the incoming photon, and E_b is the binding energy of the ejected electron. This interaction leaves a vacancy in the shell of the ionized atom. The vacancy is filled by the capture of a free electron or through the rearrangement of the electrons in the outer shells. During this process, characteristic fluorescence X-rays can be emitted or not. The energy of the X-ray fluorescence photons depends on the difference between the two shells' binding energies. The excess energy can also kick out other electrons from their outer shells, called Auger electrons. Complete absorption of the incoming photon energy is desired for ideal X-ray detection. This means that ideal spectroscopic imaging requires the capture of the photoelectron and its secondary products by the same sensor element unit, resulting in a single energy peak in the measurement [9].

Table 2-1 provides the fluorescence properties of some materials used for radiation detection. $d_{\alpha1}$ and $d_{\alpha2}$ indicate the mean free path of the fluorescence photons, $K_{\alpha1}$ and $K_{\alpha2}$ give their associated energies, and η is the probability of creating a fluorescence photon after a photoelectric interaction. For a silicon sensor, the probability of generating a fluorescence photon after an interaction is 4.1%, and the mean free path of those photons is around 12 µm. High-Z materials have a fluorescence yield of more than 50%. For instance, CdTe has more than 80% chance to generate fluorescence photons, and the mean free path of those photons is large: 58 µm for Te and 111 µm for Cd. Those mean free paths are comparable or larger than the pixel sizes commonly used in radiation detection.

Material		**N**	**K_1 [keV]**	**L_2 [keV]**	**L_3 [keV]**	**$K_{\alpha1}$ [keV]**	**$K_{\alpha2}$ [keV]**	**$d_{\alpha1}$ [µm]**	**$d_{\alpha2}$ [µm]**	**η[%]**
Si		14	1.84	0.10	0.10	1.74	1.74	11.86	11.86	4.1
Ge		32	11.1	1.26	1.23	9.89	9.86	50.85	50.40	54.8
GaAs	Ga, 48.20%	31	10.36	1.14	1.11	9.25	9.22	40.62	40.28	50.5
	As, 51.80%	33	11.87	1.36	1.32	10.54	10.50	15.62	15.47	56.6
CdTe	Cd, 46.84%	48	26.71	3.73	3.53	23.17	22.98	113.20	110.75	83.6
	Te, 53.16%	52	31.81	4.61	4.34	27.47	27.20	59.32	57.85	87.3

Table 2-1: fluorescence properties of some semiconductor detector materials [10]. The atomic number N, K and L –edges are indicated along the $K_{\alpha1}$ and $K_{\alpha2}$ energies of the generated fluorescence photons. $d_{\alpha1}$ and $d_{\alpha1}$ give the mean free path of those generated photons. η [%] is the fluorescence yield.

2.1.2 Compton (or incoherent) scattering

In Compton scattering (or incoherent scattering) process, the X-ray photon is scattered inelastically after interacting with an orbital electron loosely bound to the atom. The incident photon energy exceeds the binding energy of the free electron. The photon transfers part of its energy to the free electron but does not disappear during the collision. Subsequently, the photon is scattered from its initial trajectory through an angle θ, while the recoil electron is emitted at another given angle. The energy of the recoil electron E_{recoil} is given by:

$$E_{recoil} = hv - \frac{hv}{1+\frac{hv}{m_e c^2(1-\cos\theta)}} \qquad (2\text{-}2)$$

Where m_e is the electron's mass and c is the speed of light in vacuum.

The recoil electron receives maximum kinetic energy at θ= 180°. In this case, the photon is backscattered in its initial trajectory.

2.1.3 Electron-Positron pair production

Pair production occurs for a photon with an energy higher than $2m_e c^2 \approx 1.022\ MeV$ in an electric field of the atom nucleus or the orbital electron. The incoming photon disappears during this process, and its excess energy creates a positron-electron pair. The sum of the kinetic energy of the positron and the electron is the difference between the incident photon energy and 1.022 MeV. The positron slows down and subsequently annihilates, creating two photons. The latter has an energy equal to 0.511 MeV and travels in the opposite direction.

2.1.4 Rayleigh (or coherent) scattering

Rayleigh scattering or coherent scattering involves the interaction of the whole atom with the incoming photon. Only minimal energy is absorbed by the atom, resulting in a deflection of the photon. This mechanism has little importance in X-ray imaging because the energy transfer from the photon to the matter is negligible and its cross-section is very low, as illustrated in Figure 2.1.

Figure 2.1 plots the cross-section of the silicon versus the incoming X-ray photon energy. The cross-section is a parameter that indicates the probability for a process to occur [11]. The photoelectric absorption is the dominant mechanism below 57 keV. The sharp increase of the cross-section value around 1.8 keV corresponds to the binding energy of the electrons in the K-shell. Between 57 keV and 1.022 MeV, the Compton scattering is the dominant mechanism. Above 1.022 MeV, the pair production becomes the most likely interaction. The Rayleigh scattering is present at low energies below 50 keV but has no significant effect on the overall measurement.

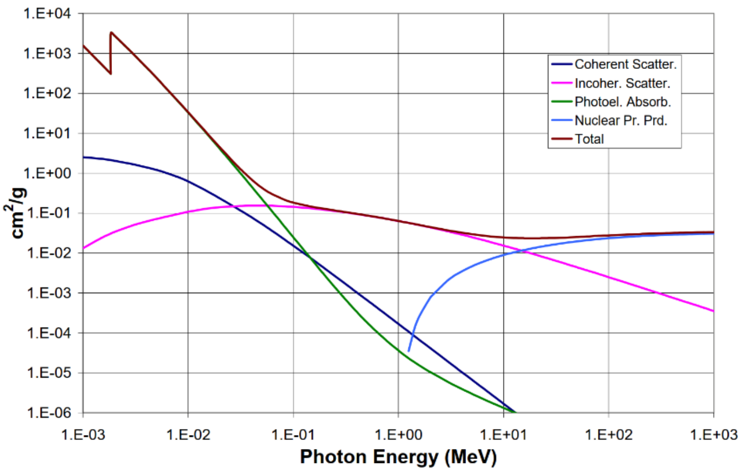


Figure 2.1. The cross-section in a silicon sensor versus the energy of the incoming X-ray photon. The four interactions with the material are highlighted [11].

2.2 Detectors for X-ray imaging

An X-ray imaging system is classified on how the X-ray photon is converted into a measurable electrical signal. The direct and indirect conversions are analyzed in the first part. The X-ray detector is also categorized accordingly to the architecture implemented for signal processing. The second part reviews the photon counting system versus the integrating energy system. Finally, the concept of the ideal detector will be presented, and more information can be found in [12].

2.2.1 Direct versus indirect conversion

The principle of the operation of an indirect detection system is illustrated on the left-hand side in Figure 2.2. There are two processes involved in converting an X-ray photon into a measurable electrical signal. First, the photon is converted into visible light using a scintillator element. The amount of light is proportional to the energy of the incoming X-ray. Subsequently, the visible light is converted into an electrical signal through readout electronics using photodiodes. In this illustration, a thin layer of septa suppresses the crosstalk between adjacent channels in the segmented scintillator [12]. Depending on the material used for the scintillator, between 100 e- and 1000 e- are generated in the photodiode. Indirect detection systems are cheaper than direct conversion systems but suffer from lower energy and spatial resolution due to the two-step conversion.

The direct detection systems rely on a one-step process, for which the principle is illustrated on the right-hand side in Figure 2.2. The X-ray photon interacts with the detector material, and creates electron-hole pairs that drift towards the collection electrode under the influence of an electric field. The movement of the cloud of charges in the material induces an electrical signal measured using dedicated readout electronics. The formation of the electrical signal in the sensor is examined in the next chapter. The X-ray energies used in medical applications can go up to 120 keV, which means that each incoming X-ray photon releases a charge of around 27000 electrons in a CdTe semiconductor material. The detected signal in indirect conversion technology is highly reproducible.

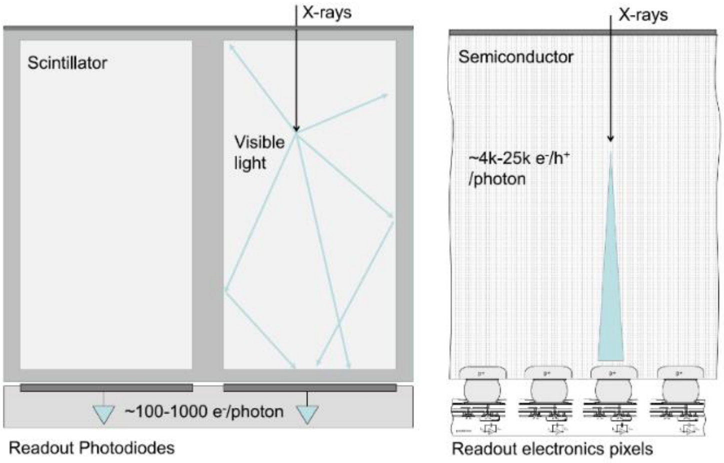


Figure 2.2. Illustration of an indirect detection system on the left and direct detection on the right [12].

2.2.2 Integrating versus pulse processing architecture

An X-ray imaging system is named *integrating energy system* when the energy of the detected photons is integrated over the exposition time. The operation principle of an integrating system is illustrated in the middle plot in Figure 2.3. Five events are sent to the detector at a different time of arrival. The readout electronics integrates the signal over the total exposure time. The contribution of each photon to the signal is proportional to its energy. High-energy photons contribute more than low energy photons. An integrating energy system can process photons that arrive very close in time, for example, the events ‘4’ and ‘5’ in Figure 2.3. However, the noise is also integrated with the signal during this operation. Therefore, the signal-to-noise ratio and the dynamic range of integrating systems are limited.

The signal from each photon is treated on an event-by-event basis in *single pulse processing architecture*. The latter contains a Charge Sensitive Amplifier (CSA) to amplify the current at its input. In some topologies, a pulse shaping circuitry further improves the signal-to-noise ratio. The signal’s amplitude at the output of the CSA or the shaping amplifier is proportional to the energy of the impinging X-ray photon. The operation principle is illustrated in the bottom plot in Figure 2.3. A discriminator, generally implemented with multiple thresholds, is the last stage amplifier in pulse processing architecture.

Multiple thresholds and energy weighting techniques significantly improves the image quality in pulse processing systems [13]. Moreover, setting the threshold above the random electronic noise enables a total noise rejection. However, unlike integrating operation, pulse processing requires a minimum time to process two consecutive events. This time limitation is referred to as 'dead time.' For instance, the events '4' and '5' in Figure 2.3 are recognized wrongly as a single event, leading to the non-linear behaviour.

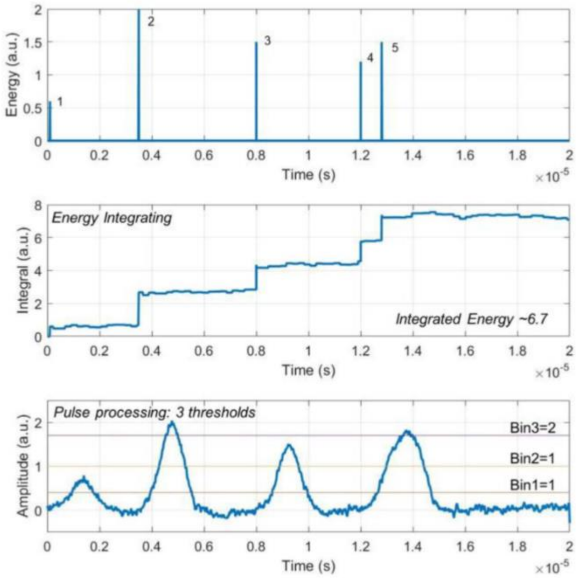


Figure 2.3. Operation principle of an integrating energy system in the central plot and a pulse processing architecture in the bottom plot. The time of arrival of 5 photons having different energies is shown in the top plot. Three thresholds are applied in the case of the pulse processing system. The 4th and 5th events suffer from pile-up in the pulse processing architecture and recognized wrongly as a single event [12].

2.3 Towards an ideal X-ray imaging detector system

2.3.1 Ideal X-ray spectroscopic imaging system?

We stated that direct detection systems provide better energy and spatial resolution than indirect conversion systems. Moreover, single pulse processing architecture allows the measure of individual events on an event-by-event basis. On the other hand, individual information about each photon is lost in an integrating architecture. To achieve an ideal X-ray spectroscopic imaging system, a direct conversion and pulse processing architecture with multiple thresholds in the readout electronics are desired. More constraints are required in some cases. For instance, the requirements for biomedical imaging systems presented in [14] and [15] are:

- High efficiency for a lower radiation dose to the patient. The ideal system must extract the maximum of information from the incoming flux by measuring the energy and position of each X-ray photon. The dead time of the pulse processing architecture should be as short as possible to process the input photon flux correctly.
- Good spatial resolution for high-resolution imaging. For instance, around 50 µm resolution is desired in mammography, between 100 µm and 150 µm in radiography, or in the range 150 µm - 200 µm in fluoroscopy applications [7].
- The sensitive area should be as large as the imaged object. For instance 35 cm x 43 cm in radiography or 18 cm x 24 cm in Mammography [7]. The actual X-ray imaging systems introduce a dead zone in the imaging. An ideal X-ray system extends in both the x-axis and y-axis without any dead region between the adjacent sensitive devices.
- Low noise to clarify the imaging. Pulse processing architecture allows long acquisition time imaging with complete noise rejection. The threshold set above the random electronic noise removes the false hits in measurement. However, increasing the threshold level means a lower efficiency. The random electronic noise must be minimized for this purpose.
- Linear dynamic range from low dose to high dose. The counter depth in the readout electronics must be sufficient to ensure a linear behavior. In addition, the minimum detectable charge depending on the random electronic noise must be minimized. Finally, the loss of counts due to pulse pile-up must be avoided for high incident photon flux.

2.3.2 Hybrid pixel detectors for X-ray imaging

A hybrid pixel detector is a 2-dimensional array of microscopic radiation-sensitive elements, each of which is connected to its signal-pulse processing. The hybrid pixel detectors are a direct detection system read out by single-pulse processing electronics. Indeed, the semiconductor material converts the X-ray photons directly into an electrical signal to be measured by the readout electronics.

The radiation-sensitive elements are called “sensor pixels,” the associated electronics are “readout pixels.” Flip-chip technology permits connecting the semiconductor sensor material to the readout electronics, as shown in Figure 2.4. This separation allows independent optimization of the readout and sensor parts. Different materials can be used for the sensor while keeping the same readout circuit. The composition of the semiconductor material is chosen for its sensitivity to detect a specific range of energies. Synchrotrons applications use Silicon (Si) to detect low-energy photons. Medical applications target high-energy photons, materials like Cadmium Telluride (CdTe) or Galium Arsenides (GaAs) are more appropriate. The digital part of the readout takes advantage of the scaling down of the CMOS technology every two years to implement complex pulse processing circuitries needed for each application [6].

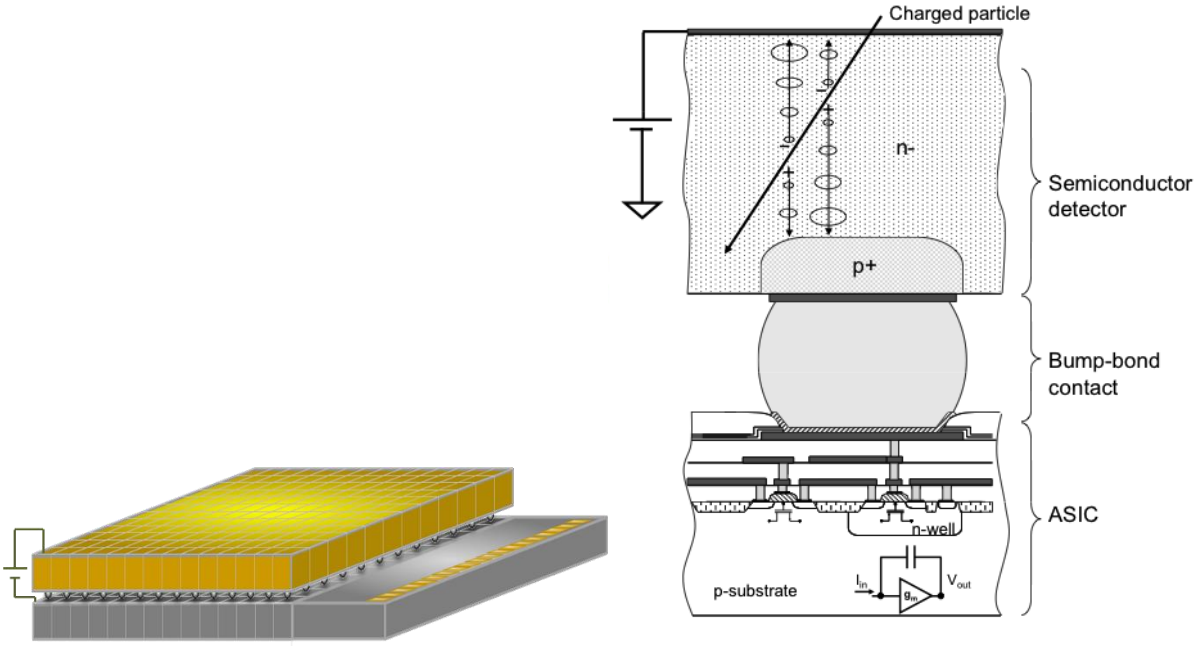


Figure 2.4. 3-Dimensional view of the architecture of a hybrid pixel detector in the left plot. The yellow array at the top represents the semiconductor sensor. The grey array at the bottom is the readout pixels. The connection between both parts is made with flip-chip technology. The 2-Dimensional view is shown in the right plot [11].

2.4 Summary

In this chapter, the interactions of X-ray photons with the matter have been summarized. Photoelectric absorption is desired for high-quality X-ray imaging. An ideal X-ray detector system will rely on direct detection for better energy and spatial resolution. In addition, a single photon processing architecture in the readout electronics measures the information of individual X-ray photons on an event-by-event basis allowing to sample different regions of the incoming spectrum. Combined with a polychromatic beam, this might lead the detector to achieve material identification in the sample. The hybrid pixel detector fulfills those conditions and its limiting factors are analyzed in the next chapter.

Chapter 3 Pulse processing for X-ray imaging

This chapter reviews the design of hybrid pixel detectors for X-ray imaging. Section 3.1 describes the charge transport in the sensor volume, and highlights the limiting factors of the sensor material for X-ray imaging. Section 3.2 briefly presents the micro-bumps to connect electrically the sensor to the readout electronics. Finally, section 3.3 studies the pixel electronics for X-ray imaging and its limiting factors.

3.1 Semiconductors detectors

3.1.1 Charge transport in semiconductors

The interaction of a charged particle or photon in the semiconductor material creates electron-hole pairs. The free carriers are separated by an applied electric field. Two mechanisms are involved in the transport of carriers in the semiconductor material: the drift and the diffusion. As predicted by the Shockley-Ramo theorem, the motion of these carriers induces a current which is the input of the readout pixel [16].

3.1.1.1 Drift

An applied electric field to the semiconductor material makes the charges drift along the field lines. Random collisions accompany the acceleration of the free carriers with the semiconductor lattices. The drift current density for electrons and holes under an applied field E are given by:

$$\begin{cases} J_{e,drift} = -qn\mu_e E \\ J_{h,drift} = qp\mu_h E \end{cases} \tag{3-1}$$

With q the elementary charge, n and p the electron and hole concentration respectively and, μ_e and μ_h their mobility. The mobility holds for scattering mechanisms that depend on temperature, concentration of impurities, material, and on the electric field. Table 3-1 shows the mobility of electrons and holes in different semiconductors at 300 K. The mobility of electrons is significantly higher than holes in most semiconductor materials. For instance, it is ten times higher in CdTe and CdZnTe. Other physical properties are indicated in Table 3-1, like the material's atomic number, bandgap energy, pair creation energy, and resistivity.

The drift current does not increase linearly with the electric field and saturates at a 'velocity saturation' value. In case of silicon, the velocity saturation is around 1 x 10^7 cm/s for an applied field around 10^5 V/cm.

Material	**Si**	**Ge**	**GaAs**	**CdTe**	**CdZnTe**	**Perovskites ($MAPbI_3$)**	**Perovskites ($CsPbBr_3$)**
Atomic number	14	32	31,33	48,52	48,30,52	66.8	65.9
Bandgap (eV)	1.12	0.67	1.43	1.44	1.57	1.51	2.28
Pair creation energy (eV)	3.62	2.96	4.2	4.43	4.6	4.63	3.3
Resistivity (Ωcm)	10^4	50	10^7	10^9	10^{10}	> 10^8	10^9
μ_e (cm^2/Vs)	1400	3900	8000	1100	1000	70	
μ_h (cm^2/Vs)	480	1900	4000	100	100	48	52

Table 3-1: Physical properties of semiconductors frequently used for radiation detection [12] at 300 K.

3.1.1.2 Diffusion

The difference in free carrier concentration in the sensor causes diffusion of carriers along the concentration gradient. In this case, a current flows from the high to lower carrier concentrations. This mechanism happens simultaneously with the drift. The current density due to electron and hole diffusion are given by:

$$\begin{cases} J_{e,diffusion} = qD_e \nabla n_e \\ J_{h,diffusion} = -qD_h \nabla n_h \end{cases} \tag{3-2}$$

Where D_e and D_h are the diffusion coefficient of electron and hole, and ∇n_e and ∇n_h are the gradients in concentrations.

Einstein's equation relates the diffusion coefficient to the mobility of the carriers [17]:

$$\frac{D_e}{\mu_e} = \frac{D_h}{\mu_h} = \frac{k_B T}{q} \tag{3-3}$$

Where k_B is the Boltzmann constant equal to 1.38.10^{-23} J/K, and T is the absolute temperature.

3.1.1.3 Shockley-Ramo Theorem

The charge carriers generated from the absorption of a particle in radiation detectors will induce an electrical signal at the electrodes. It is essential to associate the signal waveform to the velocity of the carriers in the sensor material, and not to the charge reaching the collection electrode, since the electrical signal disappears if the charges stop moving or reach the electrode. The Shockley-Ramo theorem expresses the current due to the drift movement of the carriers under the effect of the electric field [16], [18]:

$$i(t) = q\,\overrightarrow{V_{drift}}\ \overrightarrow{E_w} \tag{3-4}$$

Where $\overrightarrow{V_{drift}}$ is the average velocity of the carriers, and $\overrightarrow{E_w}$ is the weighting electric field. The latter quantifies the coupling of the moving charge to a specific terminal that is kept at a unity potential, while the other terminals are grounded. The weighting field is obtained by solving the Laplace equation:

$$\nabla^2 \varphi_w = 0 \tag{3-5}$$

A basic configuration of a sensor having an infinite parallel plate geometry shown in Figure 3.1 is analyzed in this section. We consider a CdTe sensor with a thickness d=2 mm biased under V_{BIAS} = 500 V. In the case of photoelectric absorption and in the absence of fluorescence photons, an X-ray photon crossing this sensor generates hole-electron pairs at the y-ordinate axis. The electrons drift towards the anode under the electric field V_{BIAS}/d and induce a current i_e during the collection time t_e. Similarly, the holes induce a current i_h during t_h. In the CdTe sensor, the mobility of the electrons is eleven times higher than that of holes. Therefore, the time required for collecting those carriers is much shorter. The collection time of the carriers is given by:

$$t_e = \frac{y}{\mu_e * \frac{V_{BIAS}}{d}} \tag{3-6}$$

$$t_h = \frac{d-y}{\mu_h * \frac{V_{BIAS}}{d}} \tag{3-7}$$

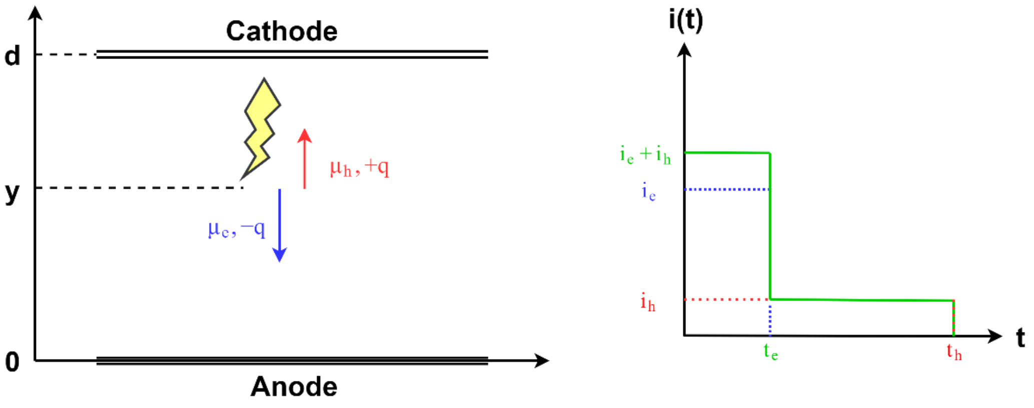


Figure 3.1. Parallel plate geometry sensor, the carriers induce a current during the drift movement towards the electrode. The right plot represents the induced current as a function of time.

By applying the Shockley-Ramo theorem and fixing the collection electrode at 1 V, the weighting field is given by 1/d. The current induced by electrons and holes are given by:

$$i_e = q\mu_e * \frac{V_{BIAS}}{d} * \frac{1}{d} \tag{3-8}$$

$$i_h = q\mu_h * \frac{V_{BIAS}}{d} * \frac{1}{d} \tag{3-9}$$

The induced charge at the time t=t$_e$ by taking $\mu_h = \mu_e/11$ is simplified to:

$$q(t = t_e) = (i_e + i_h)t_e = q\frac{12}{11} * \frac{y}{d} \tag{3-10}$$

For instance, an interaction at the d/2 ordinate axis gives a time collection of 36 ns for electrons and 400 ns for holes. For a front-end having an integration time around t$_e$, only 55% of the total deposited charge will be measured by the system. This incomplete charge collection is called loss by "ballistic deficit." Later in this chapter, we will see that ballistic deficit can be avoided using an optimal integrating time for the front-end electronics. This analysis conducted for the parallel plate geometry with the uniform weighting field provides a simple understanding of the formation of the signal in the sensor. However, it cannot be extended to segmented sensors. The signal formation in a segmented detector is developed in [19]–[21]. When the electrode size is smaller concerning the thickness of the sensor, the weighting potential decreases a lot along with the sensor depth. This is illustrated in Figure 3.2, showing the weighting potential as a function of the sensor depth in a segmented 2 mm thick CdTe sensor and for a pixel pitch of 110 µm and 500 µm. Most of the induced current will come from the charge carriers close to the collection electrode when decreasing the pixel size. In Figure 3.2, the contribution of the slow carriers, which are holes for the CdTe sensor, can be deduced. For an interaction happening at mid-way between the two electrodes, the motion of the holes contributes to 3% of the total deposited charge for the pixel pitch of 110 µm and around 13 % for the 500 µm pixel [12]. This is referred to as the "small pixel effect." In addition, the gradient of the weighting potential is higher for smaller pixel dimensions, leading to a shorter induced signal pulse than with larger pixels. A short signal pulse is desirable to design fast front-end electronics with a short shaping time.

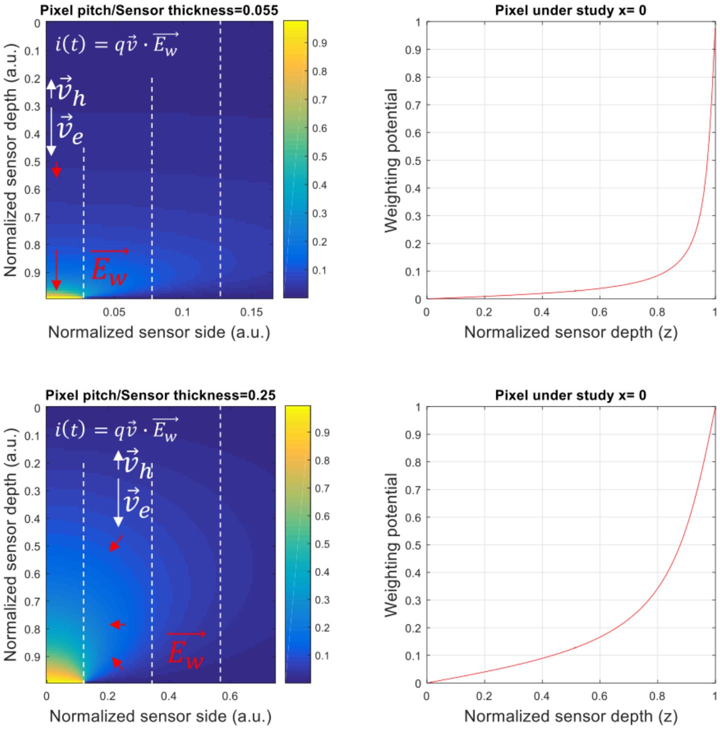


Figure 3.2. Illustration of the weighting potential in a 2 mm thick segmented sensor with a pixel pitch of 110 µm (top) and 500 µm (bottom) [12].

3.1.2 Limiting factors in sensors for X-ray imaging

Few mechanisms must be taken into account when designing the sensor for the hybrid pixel detector. The choice of the semiconductor material, pixel size, sensor thickness, and applied voltage will influence the system's overall performance. The limiting factors in the sensor material for X-ray imaging are summarized in the following section.

3.1.2.1 Absorption efficiency

When an X-ray photon interacts with the sensor material, the energy deposition in the initial impact point can be total (photoelectric with the emission of Auger Electrons) or partial (photoelectric with the emission of fluorescence photons, Compton). If there is no interaction with the sensor, the photon will pass through without leaving any trace. The X-ray absorption efficiency in silicon decreases rapidly for photon energy above 20 keV. Replacing the silicon sensor with a semiconductor with a higher atomic number, called “high Z materials”, extends the absorption efficiency at higher photon energies [22]. For this reason, compound semiconductor materials have become very attractive in X-ray imaging [23]. Figure 3.3 shows the absorption efficiency of 500 µm thick sensors: Si (Z=14), Ge (Z=32), GaAs (Z=31 for Ga & Z=33 for As), and CdTe (Z=48 for Cd and Z=52 for Te). Ge and GaAs have their plots overlapping due to their very close atomic number. In addition, the efficiency of the sensor depends on the thickness of the sensor material; a thicker sensor increases the chance of capturing the X-ray photon.

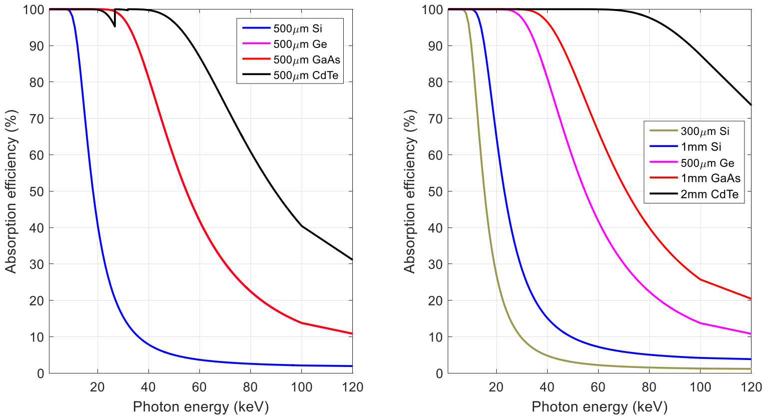


Figure 3.3. Absorption efficiency of different semiconductor materials (Si, Ge, GaAs and CdTe) (left), and for different thicknesses of the sensor (right) [13] [22].

A strategy to improve the absorption efficiency consists of placing silicon strip detectors along the direction of the X-ray source [24]. The technique is called “edge-on” and illustrated in Figure 3.4, where the photon impinges from the edge side of the detector, leading to an excellent absorption efficiency for X-rays up to 200 keV [25]. However, the Compton scattering effect in silicon for the energies of interest in medical X-ray imaging degrades the system energy response [12].

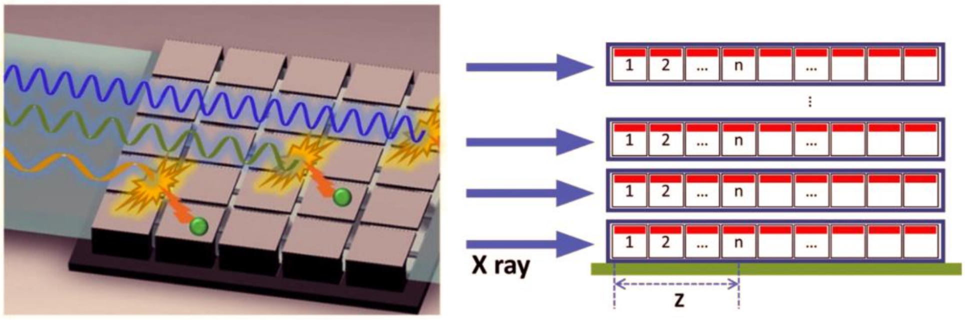


Figure 3.4. In edge-on detectors, the photon comes from the edge-side of the detector. The long active distance gives a higher chance of absorbing a high-energy X-ray photon than conventional face-on geometry [25].

3.1.2.2 Fluctuations in the number of generated charge carriers

A discrete number of charge carriers are generated when a photoelectron interacts with the surrounding atoms. During the generation of carriers, a part of the energy is dissipated through the excitation of the crystal lattice [17]. Therefore, the energy to create an electron-hole pair is greater than the minimum ionization energy, defined by the bandgap energy. The fluctuations in the number of generated charge carriers are Gaussian and are expressed in Full-Width at Half-Maximal (FWHM) [11]:

$$FMHW = 2.35 * \sqrt{F\varepsilon E} \tag{3-11}$$

Where F is the Fano factor [26], ε is the conversion efficiency of the sensor, E is the absorbed energy. For instance, for silicon sensors, ε is equal to 3.6 eV/electron-hole pair, and the fano factor is around 0.12. The energy resolution of the hybrid detectors depends on the random fluctuation of the carriers in the induced charge and the electronic noise, which is the dominant factor.

3.1.2.3 Charge diffusion

The diffusion mechanism described earlier leads to a broadening of the charge cloud along with the drift motion. A Gaussian distribution characterizes this spread of charges with a standard deviation given by:

$$\sigma_e = \sqrt{2D_e t} \tag{3-12}$$

Where t is the lapse of time between the deposition and the collection of the charges by the electrode.

Figure 3.5 shows the charge deposition by a 50 µm depth interaction in a 300 µm thick sensor. The diffusion leads to broadening the charge cloud's length and width during the drift. That means decreasing the pixel size or increasing the sensor thickness leads to the charge deposition between adjacent pixels. This phenomenon is referred to as “charge sharing”. Charge sharing means that a single-pixel element does not detect the total induced charge, which distorts the measured energy spectrum.

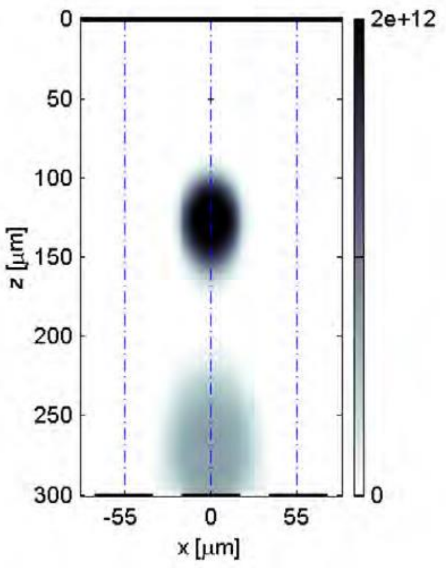
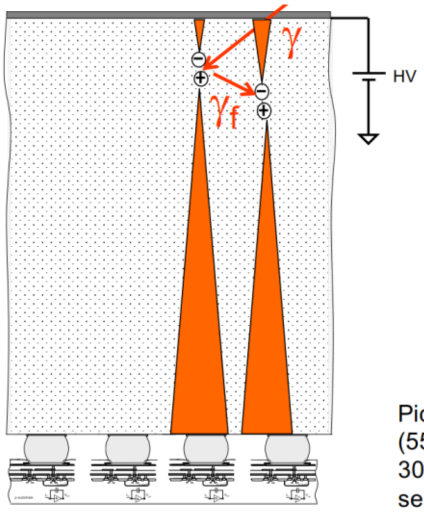


Figure 3.5. Simulation of the charge deposition in a pixelated silicon sensor of a 10 keV photon after deposition at 50 µm depth. The black cloud represents the charges after 4 ns of drift (and diffusion), and the gray cloud after 14 ns of drift motion [10].

Some applications use the charge sharing between small pixels to improve the spatial resolution at a sub-pixel resolution [27] [28]. For instance, using the hybrid pixel detector Timepix bonded to a 300 µm thick silicon sensor, a spatial resolution around 300 nm with 55 µm pixel pitch is reported [29]. For spectroscopic applications that require an excellent energy resolution, the charge sharing between pixels must be avoided using large pixels, or corrected for small pixels. The Medipix4 ASIC is a target for spectroscopic applications; therefore, it requires a scheme for addressing the distortion in the energy spectrum of charge sharing between pixels. Later in this thesis, architectures for charge sharing correction will be presented.

3.1.2.4 Fluorescence photons

During the photoelectric effect, the incident photon interacts with an atom. This process liberates a photoelectron from one of the atomic shells. The vacancy created from the emitted electron will be refilled with an electron from the surrounding or an upper atom-shell [9]. The rearrangement of the electrons can lead to the emission of one or more characteristic fluorescence photons, with energy depending on the potential energy difference between the shells involved in the process. The excess energy can also free other electrons from their shells through Auger emission. Figure 3.6 shows the emission of a fluorescence photon. The later travels some distance away from the initial interaction point before depositing its energy. We have seen in 2.1.1 that the fluorescence travel distance is comparable or larger than the pixel sizes used in radiation detection. This means that the measured energy spectrum will be distorted due to an incomplete collection of the charge by a single unit pixel [13].



Picture to scale (55µm pixel pitch, 300µm thick sensor)

Figure 3.6. Illustration of a fluorescence photon emitted after de-excitation of an atom. The fluorescence photon travels away from the initial interaction point; small pixels may not detect the full-deposited charge (courtesy R. Ballabriga).

3.1.2.5 Charge trapping and recombination

The semiconductor material might have a low level of impurities like gold, zinc, or other metallic atoms, which act as trapping centers for the charge carriers drifting under the influence of the electrical field [30]. The captured electron or hole will not contribute to the signal induced on the collection electrode. The impurities can also act as a recombination center, where one of the charge carriers is first captured, then annihilated by capturing the complementary charge carrier. Both trapping and recombination lead to a degradation of the measured energy spectrum. The trapping length L_{te} is the mean value of the distance traveled by a charge carrier before trapping or recombination. It can be calculated by the product of the mobility (μ_e or μ_h), to the lifetime of the carrier (τ_e or τ_h) and the electrical field value in the sensor. The probability that a charge carrier is trapped or recombined is given by [12]:

$$P_{loss} = 1 - e^{\frac{-y}{L_t}} \tag{3-13}$$

Where y is the travel distance of the charge carrier until the collection electrode.

Table 3-2 indicates the trapping length and the probability of trapping/recombination of electrons and holes (L_{te}, L_{th}) in the semiconductor materials for a constant electrical field of 300 V/mm and a sensor thickness of 1 mm. The probability of trapping and recombination is nearly zero in the case of Si and Ge but increases for compound materials. In the case of CdTe, the probability of charge loss is around 1% for the electrons and 15% for the slow carrier holes.

Material	**Si**	**Ge**	**GaAs**	**CdTe**	**CdZnTe**	**Perovskites ($MAPbI_3$)**	**Perovskites ($CsPbBr_3$)**
$\mu_e\tau_e$ (cm^2/V)	> 1	> 1	8 x 10^{-5}	3.3 x 10^{-3}	1 x 10^{-3}	> 7 x 10^{-4}	> 8 x 10^{-4}
$\mu_h\tau_h$ (cm^2/V)	~ 1	> 1	4 x 10^{-6}	2 x 10^{-4}	3 x 10^{-4}	> 8 x 10^{-4}	> 1 x 10^{-3}
L_{te} (cm) *for E= 300 V/mm*	3000	3000	0.24	9.9	3	2.1	2.4
L_{th} (cm) *for E= 300 V/mm*	3000	3000	0.012	0.6	0.9	2.4	3
$P_{loss,e}$ (%) *for 1 mm thick sensor*	0.0033	0.0033	34.1	1	3.3	4.65	4.1
$P_{loss,h}$ (%) *for 1 mm thick sensor*	0.0033	0.0033	100	15.4	10.5	4.1	3.3

Table 3-2: Electron and hole trapping length for different semiconductor materials under 300 V/mm electrical field. The probability of the charge trapping/recombination is given for a 1 mm thick sensor.

Charge trapping and recombination can be minimized by reducing the sensor thickness (at the cost of a lower absorption efficiency), increasing the electric field in the material (at the cost of a higher leakage current in the sensor), and using materials with high mobility for both carriers [13]. Another solution for dealing with the charge trapping/recombination is to take advantage of the small pixel effect described earlier in this chapter. For small pixel dimensions compared to the sensor thickness, the fast carriers drifting to the sensing electrode contribute to most of the sensor's induced signal. The small pixel effect is beneficial for the materials like CdTe or CdZnTe, where the hole trapping is dominant.

3.1.2.6 Polarization of the sensor

In some high-Z materials like CdTe or CdZnTe, the low mobility of holes added to the defects in the crystal can create a dynamic space charge buildup when the sensor is exposed to a high flux of X-ray [30]. The resulting buildup space charge leads to a lateral electric field perpendicular to the irradiation direction, which in turn causes the lateral drift of charge carriers [31]. This phenomenon is called polarization of the sensor and, leads to a time-dependent decrease of the count-rate of the system. The polarization effect in a sensor can be minimized at low-temperature operation, or by increasing the bias voltage of the sensor [13]. However, the increase of the bias voltage leads to a higher leakage current.

3.2 Bump bond connection

In 1960, IBM invented the solder-bumped flip-chip process where conductive bumps provide electrical and mechanical connections instead of wire bonds connections. Flip-chip technology has many advantages like low cost, good performance, and reliability regarding wire bonding [32]. The hybrid pixel detectors use flip-chip process to connect each pixel readout to its associated sensor pixel. High-Z materials such as CdTe and CdZnTe used for their higher X-ray absorption compared to silicon sensors are challenging for bump bonding connections. Indeed, those materials do not withstand the high temperature of soldering. A low-temperature flip-chip bonding process is proposed and tested in [33]. First, the solder bumps are deposited on the semiconductor sensor and the CMOS readout wafer. The bumping process called the electroplating technique is illustrated in Figure 3.7. The process flow is briefly summarized in this section for consistency.

Step 1: The sensor wafer has Al pads and a passivation layer opening to host the bump bonding connection. The wafer is cleaned using oxygen plasma.

Step 2: Sputtering 30 nm TiW, an adhesive layer between the wafer and the Under Bump Metallization (UBM). Then Sputtering of 700 nm of Cu.

Step 3: Deposition of 30 µm of photoresist, then exposition and development to define an opening around 30 µm for the solder bump.

Step 4 & 5: UBM and solder deposition in sequence to limit the oxidation at the interface between the UBM and solder.

Step 6 & 7 & 8: Removal of the photoresist layer, the copper layer, and the TiW layer.

Step 9: Solder bump reflow.

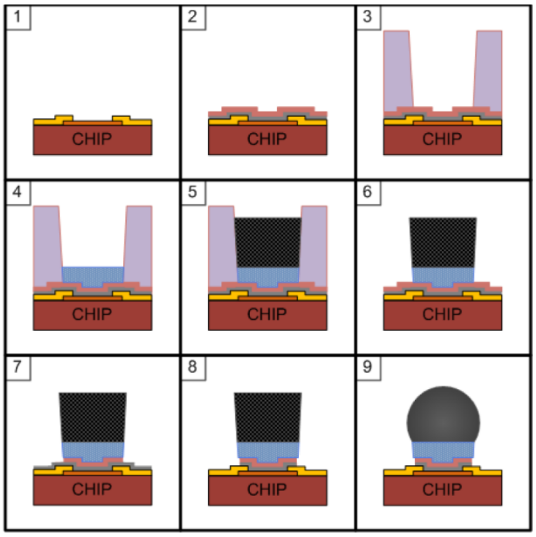


Figure 3.7. The process flow of a solder bumping process using the electroplating technique [33], [34].

The sensor wafer is diced prior to being bonded to a readout die. Prior to bump deposition, the CMOS ASIC wafer is probed and the good dice are identified. Next, the ASIC readout and the semiconductor sensor are aligned using flip-chip bonder equipment. Finally, the leveling of both parts is done using an optical autocollimator. The disadvantage of this electroplating for UBM and solder bump deposition is the high cost for low-volume fabrication. An alternative for a low-cost bump bonding solution is the electroless UBM deposition and solder bumps transfer techniques described in [35]. Figure 3.8 illustrates the placement of 40 µm solder balls on the Timepix chip using the electroless UBM deposition. Solder balls are placed at 110 µm pitch. One advantage of hybrid detectors is to allow different sensor pitch sizes for the same readout ASIC.

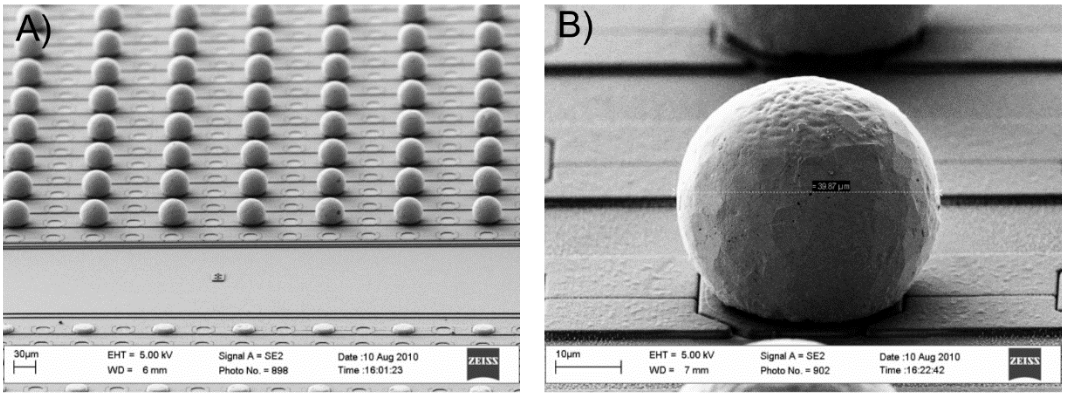


Figure 3.8. Scanning Electron Microscopy (SEM) picture of the deposition of 40 µm solder bumps on a 110 µm pitch Timepix having UBM pads [35].

3.3 Readout electronics for X-ray imaging

3.3.1 Quantum processing in pixels

We have discussed about the interaction of a charged particle or photon in the sensor volume that generates electron-hole pairs that drift towards the collection electrode following the electrical field lines. The signal induced from the movement of carriers in the sensor is small (around a few thousand electrons) and with a short collection time (few ns). The signal generated at the input of the readout pixel can then be represented as a Dirac current impulse, and the processing of this signal by a dedicated readout electronics gives the total deposited charge [11] [26]. Figure 3.9 illustrates the processing of the induced signal by the analog processing electronics within the pixel. A radiation sensor is modeled as a current source, I_{IN}, with a Dirac temporal response. The induced current is connected in parallel with the detector capacitance of the sensor, which is of the order of 100 fF for segmented pixel detectors. In addition, a DC current source models the leakage current coming from the sensor material, which is around 300 pA for silicon sensors and can reach a few nA for high Z-materials like CdTe. A preamplifier called Charge-Sensitive Amplifier (CSA) amplifies the bare small signal. Then, some front-ends require a shaper circuit to optimize the signal-to-noise ratio. The output signal of the shaping circuit is fed to a comparator that converts the analog into a digital signal for further processing by the digital pixel.

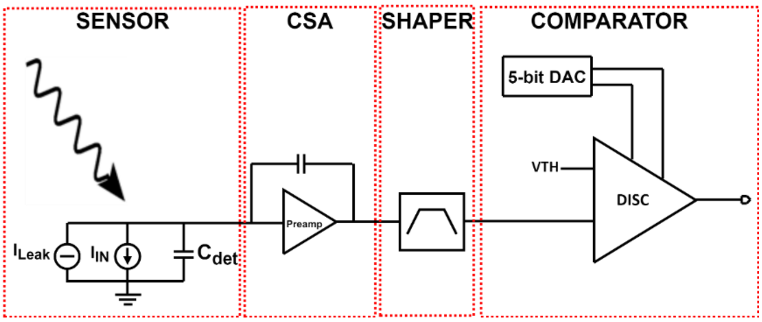


Figure 3.9. Analog pulse processing circuitry in a pixel. The input current generated by the photon is first amplified by a CSA and then processed by a filter circuit. Finally, the signal is fed to a comparator with a threshold higher than the background noise to obtain a "noise-free signal."

3.3.1.1 Charge-Sensitive Amplifier (CSA)

There are various amplification schemes for dealing with the small current induced by the charge carriers. Most pixel architectures use a charge-sensitive topology, so the output voltage depends only on the charge deposited at the input and is insensitive to other system parameters, like temperature or detector capacitance [17]. The topology is shown in Figure 3.10; the CSA contains an inverting operational amplifier with a gain A_V and a feedback capacitance C_f. The small-signal model provides:

$$\begin{cases} V_{OUT} = -A_V * V_{IN} \\ I_{IN} - sC_{DET}V_{IN} + sC_f(V_{OUT} - V_{IN}) = 0 \end{cases} \tag{3-14}$$

The output voltage is then given by:

$$V_{OUT} = -A_V * \frac{I_{IN}}{s(C_{DET}+(1+A_V)C_f)} \tag{3-15}$$

If the inverting amplifier is designed with a significant gain such that $C_{DET} \ll (1+A_V)C_f$ and with $A_V \gg 1$:

$$V_{OUT} = -\frac{I_{IN}}{sC_f} \tag{3-16}$$

This simple relation shows that the response of a CSA is a voltage step with a gain proportional to the inverse of the feedback capacitance. The performance of the CSA is independent of the detector capacitance and other system parameters, as long as the core amplifier provides enough gain to satisfy: $C_{DET} \ll (1+A_V)C_f$.

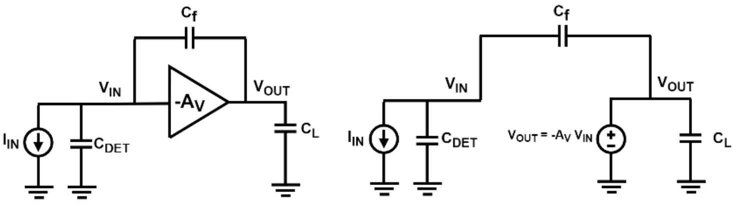


Figure 3.10. Charge-Sensitive Amplifier with a feedback capacitance C_f and an ideal transconductance amplifier on the left and its equivalent ac model on the right.

We have seen that the feedback capacitance provides a step voltage in response to the Delta input signal. A reset feedback element implemented as resistor R_f in Figure 3.11 is required to discharge the signal to the baseline so that the CSA can process subsequent events. The CSA studied previously concerns an ideal transconductance amplifier. The real operational amplifier has a limited gain depending on the characteristics of the input transistor (transconductance g_{m1}), a limited output impedance R_L, and a limited bandwidth. In addition, a buffer follows the inverted operational amplifier to drive the loading capacitance C_{LOAD}. The buffer is modeled as an ideal voltage-controlled voltage source with unity gain. The small-signal model allows expressing the temporal function of the output pulse.

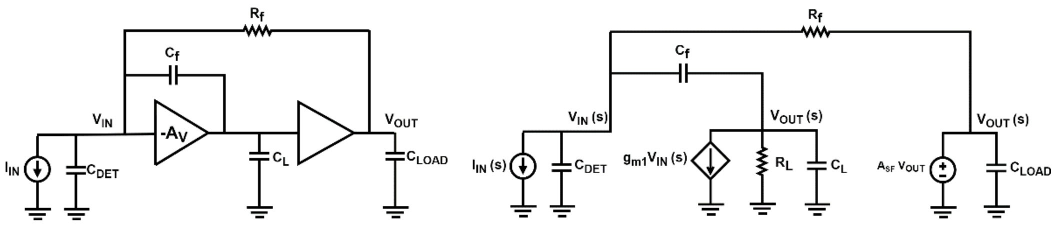


Figure 3.11. CSA with a feedback capacitance and reset element in parallel.

The nodal equations by taking the current flowing in the two branches are [17]:

$$\begin{cases} I_{IN}(s) + s\,C_{DET}\,V_{IN}(s) + s\,C_f\big(V_{IN}(s) - V_{OUT}(s)\big) + \frac{(V_{IN}(s) - V_{OUT}(s))}{R_f} = 0 \\ g_{m1}\,V_{IN}(s) + s\,C_L\,V_{OUT}(s) + \frac{V_{OUT}(s)}{R_L} + s\,C_f\big(V_{OUT}(s) - V_{IN}(s)\big) = 0 \end{cases} \tag{3-17}$$

The transfer function of the CSA is:

$$\frac{V_{out}(s)}{I_{IN}(s)} = \frac{g_{m1}R_fR_L\,(1 - \frac{s\,C_f}{g_{m1}})}{\alpha + \beta\,s + \gamma\,s^2} \quad \text{with} \begin{cases} \alpha = 1 + g_{m1}R_L \\ \beta = C_fR_f + C_{DET}R_f + C_LR_L + g_{m1}R_L\,C_fR_f \\ \gamma = C_L\,C_fR_LR_f + C_T\,C_fR_LR_f + C_L\,C_TR_LR_f \end{cases} \tag{3-18}$$

The gain of the inverting amplifier is very high: $g_{m1}R_L$ >> 1. The zero of the transfer function given by $g_{m1}/\,C_f$ is at very high frequency. Therefore, the transfer function can be simplified as:

$$\frac{V_{out}(s)}{I_n(s)} = \frac{R_f}{1 + s\,C_fR_f + \delta\,s^2} \qquad \text{with} \qquad \delta = \frac{C_L\,C_f + C_T\,C_f + C_L\,C_T}{g_{m1}} * R_f \tag{3-19}$$

The denominator is a second-order polynomial, which could be expressed as (1 + sτ_{rise}) (1 + sτ_{fall}), by assuming that the poles are real and that one time constant is much larger than the other: τ_{fall} >> τ_{rise}. In that case, the time constants are given by:

$$\begin{cases} \tau_{fall} = C_f\,R_f \\ \tau_{rise} = \frac{C_L\,C_f + C_{DET}\,C_f + C_L\,C_{DET}}{g_{m1}C_f} \end{cases} \tag{3-20}$$

By considering a Dirac shaped input current containing a total charge of Q_{in} and taking the inverse Laplace transform, the time response of the CSA is given by:

$$V_{OUT}(t) = Q_{in}\frac{R_f}{\tau_{fall} - \tau_{rise}}\left(e^{-\frac{t}{\tau_{fall}}} - e^{-\frac{t}{\tau_{rise}}}\right) \tag{3-21}$$

Where τ_{fall} is the time constant of the return to the baseline, and τ_{rise} is the time constant of the rising to the peaking value. The temporal expression demonstrates that an extended discharge of the feedback capacitor is required to obtain a CSA response close to the ideal integrator, as seen at the beginning of this section. For the applications requiring high flux processing, both peaking time and discharge time must be decreased at the cost of high power consumption (high value for the transconductance g_{m1}).

3.3.1.2 Pulse shaping circuitry

Implementing a pulse shaping circuitry in a multi-stage analog processing pixel gives more flexibility in front-end design performance. A pulse shaping circuitry or shaper amplifier is an analog chain of filters containing a high pass filter and a low pass filter. The high-pass filter cuts the slow discharge time of the CSA, allowing a faster return to the baseline. The low pass filter smoothes the signal waveform around the peak by filtering the high-frequency components.

Some front-end architectures do not use a pulse shaping circuitry due to the additional area and power consumption required for its implementation. The increase in segmentation decreases the detector input capacitance and permits a lower noise for the same power consumption [36]. Therefore, shaper circuitry is not required for some applications [36]. For instance, Timepix chips [37]–[39] do not contain a pulse shaping circuitry in the front-end pixel because those systems rely on the time duration of the preamplifier's width. Furthermore, adding a pulse shaping circuitry decreases the dynamic range of Time-over-Threshold (ToT) because the shaper output width is no more proportional to the input charge beyond a certain level [40].

3.3.1.3 Comparator

The comparator is the last amplifier in the analog front-end pixel, converting from analog to digital domain. The basic function of this block is to generate a digital signal that decides if the shaper or CSA output pulse is below or above a threshold value, as illustrated in Figure 3.12. The advantage of using this digitizer in a photon counting system is to ignore the electronic noise below the threshold level. Such systems are referred to as "noise-free detectors". The front-end for spectroscopic applications uses multiple discriminators to compare the signal with various thresholds. The output of the comparator is fed to the digital domain to process the data accordingly to the requirements of the application (Photon Counting, Time over Threshold, Time of Arrival, Pile-up correction…).

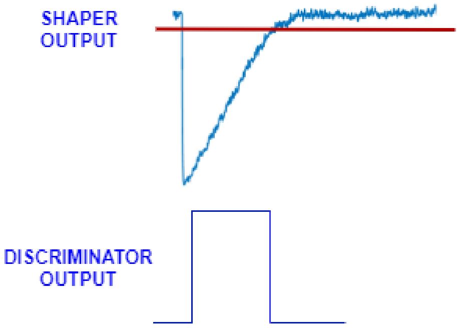


Figure 3.12. Digitization of the shaper output pulse against the threshold value represented in red. The threshold is set above the electronic noise to obtain a "noise-free system".

3.3.2 Limiting factors in electronics for X-ray imaging

3.3.2.1 Electronic Noise

Electronic noise arises from random fluctuations in the transistors and sets a lower limit for the minimum charge that can be correctly processed by the front-end electronics. The front-end noise is referred to as Equivalent Noise Charge (ENC). ENC is the charge at the input of the CSA, which results in a signal with the same magnitude as the noise. For its calculation, the ENC is defined as the ratio between the total r.m.s noise at the output of the analog front-end and the peak amplitude of the front-end having a single electron charge at its input [12]. The signal is amplified in a multi-stage analog processing circuitry; therefore, the contribution of the noise comes mainly from the components in the first stage. In this section, a summary of the noise sources in MOSFET is reviewed, and then the noise calculation in a front-end containing a single CSA without shaping circuitry is covered. The noise analysis of a multi-stages front-end containing pole-zero cancellation and a pulse shaping circuitry will be covered later in this thesis. A more detailed study of the noise of front-end electronics can be found in [17], [41]. There are three primary noise sources in circuit electronics: thermal noise, shot noise, and flicker noise.

3.3.2.1.1 Thermal noise

In resistive devices, the thermal noise comes from the thermal excitation of the resistor's charge carriers, which induces a fluctuation in the device current. The Power Spectral Density (PSD) of the thermal noise is independent of the current flowing across the resistor and is proportional to the resistance R and the temperature T [42]:

$$\frac{\vartheta_R^2}{\Delta f} = 4k_B TR \quad in\ [V^2/Hz] \tag{3-22}$$

Where k_B is the Boltzmann constant equal to 1.38 x 10^{-23} J/K, T is the absolute temperature, R is the device's resistance, and Δf is the system bandwidth.

In the front-end system studied in this thesis, thermal noise is generated from the input MOSFET conductive channel. The PSD depends on the biasing of the transistor and its sizing. The spectral density can be expressed in series with the gate of the MOS transistor as a voltage source:

$$\frac{\vartheta_{n,th}^2}{\Delta f} = 4k_B T\alpha_{th}\gamma_{th}\frac{1}{g_m} \quad in\ [V^2/Hz] \tag{3-23}$$

Where g_m is the transconductance of the MOSFET, α_{th} is the level of inversion of the channel (equal to 1/2 in weak inversion and 2/3 in strong inversion), and γ_{th} is the excess noise factor that represents the noise increase for short channel devices in modern technologies [17], [42].

3.3.2.1.2 Shot noise

The shot noise occurs due to the charge carriers randomly crossing the potential barrier at a diode junction, leading to random fluctuations in the current. In hybrid pixel detectors, the DC leakage current I_{leak} in the sensor produces a shot noise; its PSD is proportional to the DC bias current [43]:

$$\frac{i_n^2}{\Delta f} = 2qI_{leak} \quad in\ [A^2/Hz] \tag{3-24}$$

3.3.2.1.3 Flicker noise

Two mechanisms are proposed for the presence of flicker noise in MOSFET devices. The Hoodge model explains the origin of the noise due to the change of the carrier's mobility with time. This change is due to phonon interaction and interaction with the cristal's lattice, which affects the current flowing in the device [44]. In the McWorther model, the noise originates from the change in the number of carriers. The charge trap centers in the silicon crystal or at the interface between the silicon and the gate oxide are responsible for those carriers' random capture and release [45]. The carrier number fluctuation is the main contribution for flicker noise in NMOS transistors, while the mobility fluctuation is for PMOS devices. Therefore, combining the two models describes flicker noise in MOSFET devices [17]. The PSD of the flicker noise has a 1/f spectral density; the spectral density is expressed as a voltage source in series at the gate of the MOSFET:

$$\frac{\vartheta_{n,f}^2}{\Delta f} = \frac{K_f}{C_{ox}W_1L_1}\frac{1}{f} \qquad in\ [V^2/Hz] \tag{3-25}$$

where K_f is a constant typical to the technology process and device type, C_{ox} is the gate oxide capacitance of the MOSFET, W_1 is the transistor width, L_1 is the transistor length, and f is the frequency.

3.3.2.1.4 Noise calculation in a CSA

There are four main noise contributions in front-end electronics containing a single CSA without further pulse shaping. The input transistor in the inverted operational amplifier generates thermal noise and flicker noise. They are represented as voltage sources at the input transistor's gate illustrated in figure Figure 3.13. The feedback resistor has a thermal noise contribution and is modeled as a current source connected in parallel at the input using the Norton equivalent. The leakage current coming from the sensor produces a shot noise, which is added to the parallel noise of the feedback resistor.

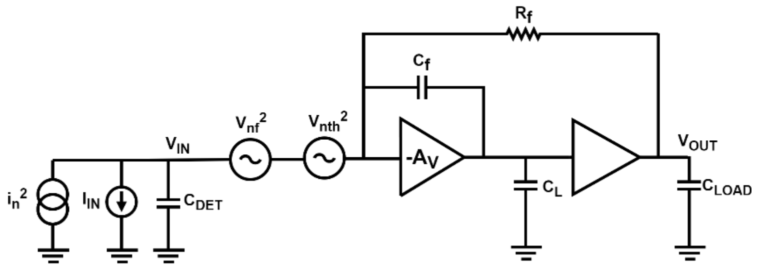


Figure 3.13. Noise contribution in the preamplifier.

The transfer function of the noise at the output of the analog front-end is calculated using the Wiener-Kintchine theorem [42]:

$$< \vartheta_{out}^2 >_n = \int_0^\infty \left|\frac{V_{OUT}(s)}{I_n(s)}\right|^2 \frac{i_n^2}{\Delta f}\ df \tag{3-26}$$

Where $\frac{V_{OUT}(s)}{I_n(s)}$ is the transfer function calculated in section 3.3.1.1. For instance, the output noise voltage of the thermal noise of the feedback resistor is given by:

$$< \vartheta_{out}^2 >_{th,Rf} = \int_0^\infty \left|\frac{R_f}{(1+s\tau_{fall})(1+s\tau_{rise})}\right|^2 \frac{4k_BT}{R_f}\ df = \frac{k_BT}{C_f} \tag{3-27}$$

The noise is usually referred to as the input noise of the front-end. To obtain the ENC, the power of the output noise voltage is divided by the square of the output voltage amplitude of the CSA corresponding to a single electron at its input. The previous chapter shows that the peak amplitude value is q/C_f for an ideal integrator, but a more accurate expression of the peak output voltage, calculated from 3-21, is given by:

$$V_{peak} = \frac{q}{C_f}\left(\frac{\tau_{fall}}{\tau_{rise}}\right)^{\frac{-\tau_{rise}}{\tau_{fall}-\tau_{rise}}} \tag{3-28}$$

Table 3-3 summarizes the ENC from the four main noise contributions. The noise contribution for a front-end having the rising and falling time constants well separated is shown in the last column.

Noise	ENC²	ENC² for $\tau_{fall} \gg \tau_{rise}$
Thermal noise of the feedback resistor	$\frac{k_BTC_f}{q^2}\left(\frac{\tau_{fall}}{\tau_{rise}}\right)^{\frac{2\tau_{rise}}{\tau_{fall}-\tau_{rise}}}$	$\frac{k_BTC_f}{q^2}$
Detector shot noise	$\frac{I_{leak}\tau_{fall}}{2q}\left(\frac{\tau_{fall}}{\tau_{rise}}\right)^{\frac{2\tau_{rise}}{\tau_{fall}-\tau_{rise}}}$	$\frac{I_{leak}\tau_{fall}}{2q}$
Flicker noise input transistor	$\frac{K_{f1}}{C_{ox}W_1L_1}\frac{(C_f+C_{det})^2}{q^2}\ln\left(\frac{C_f\tau_{fall}\,g_{m1}}{C_L\,C_f + C_{DET}\,C_f + C_L\,C_{DET}}\right)\left(\frac{\tau_{fall}}{\tau_{rise}}\right)^{\frac{2\tau_{rise}}{\tau_{fall}-\tau_{rise}}}$	$\frac{K_{f1}}{C_{ox}W_1L_1}\frac{(C_f+C_{det})^2}{q^2}\ln\left(\frac{C_f\tau_{fall}\,g_{m1}}{C_L\,C_f + C_{DET}\,C_f + C_L\,C_{DET}}\right)$
Thermal noise input transistor	$k_BT\alpha_{w1}\gamma_1\frac{C_f(C_f+C_{det})^2}{q^2\,(C_L\,C_f + C_{DET}\,C_f + C_L\,C_{DET})}\left(\frac{\tau_{fall}}{\tau_{rise}}\right)^{\frac{2\tau_{rise}}{\tau_{fall}-\tau_{rise}}}$	$k_BT\alpha_{w1}\gamma_1\frac{C_f(C_f+C_{det})^2}{q^2\,(C_L\,C_f + C_{DET}\,C_f + C_L\,C_{DET})}$

Table 3-3: Summary of the contributions of serial and parallel noises expressed as Equivalent Noise Charge (ENC).

The total noise is obtained by summing in quadrature the contributions of the shot noise, thermal resistance noise (both represented as parallel noise ENC_p), and input transistor flicker and thermal noises (respectively called serial noise ENC_f and ENC_{th}).

$$ENC_{tot} = \sqrt{{ENC_p}^2 + {ENC_{th}}^2 + {ENC_f}^2} \tag{3-29}$$

Front-end electronics having a single-stage preamplifier without pulse shaping circuitry may benefit low power applications. The noise contribution from the preamplifier input transistor thermal noise does not depend on the transconductance value of the input transistor and thus on the current when the two time constants are well separated. Similarly, the thermal noise of the feedback resistor and the detector shot noise do not depend on the current in the front-end. On the other hand, the flicker noise's contribution is generally negligible compared to the thermal noise due to the large bandwidth of the shaper-less readout circuits. Consequently, we can assume that the total noise contribution is practically independent of the overall power consumption of the front-end. In fact, increasing the current in the input MOSFET decreases the PSD of the thermal noise but the bandwidth over which the noise is integrated increases by the same amount. As an example, Timepix3 benefits from this to achieve a low-power consumption mode, which is practical for applications like battery-driven low flux radiation monitoring [46]. Figure 3.14 plots the ENC versus the current in the preamplifier input transistor. For very low current, the peaking time of the front-end increases and gets closer to the discharge time constant. Therefore, the formulas given in the last column are not valid. An abrupt increase of the total noise is seen for low values of the input transistor current, which could be avoided by increasing the discharge time of the preamplifier (to have the rising and falling time constants well separated).

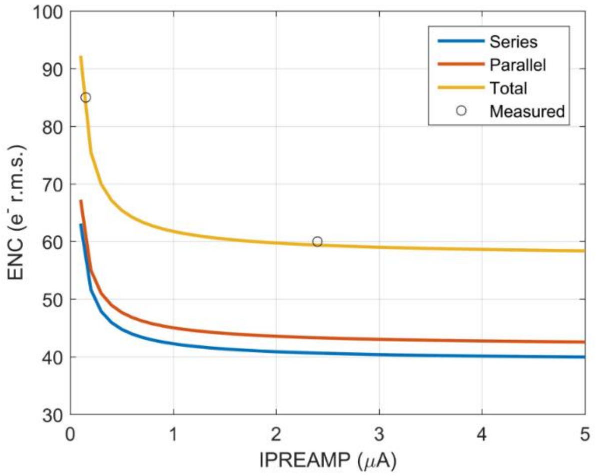


Figure 3.14. Equivalent Noise Charge versus the input transistor current in the front-end pixel of Timepix3 ASIC [46].

3.3.2.2 Offset mismatch

Analog front-end electronics contain circuits like differential pairs or current mirrors that are subject to mismatch. Indeed, equivalent devices may exhibit different behaviors after manufacturing. The mismatches that affect all the transistors of a chip in the same way can be minimized during the layout phase by orienting the transistors in the same direction, using the same metal coverage, finger geometry, etc. Full detail on the engineering of the layout phase is explained in [47]. There are also “random” mismatches due to dopant fluctuations, oxide granularity, and edge roughness. A Study in [48] demonstrated that the variance of the threshold voltage or of the current factor is proportional to the inverse of the transistor area. Random mismatches can therefore be minimized by increasing the area of the critical transistors.

Nevertheless, the transistor mismatch in the front-end and in the comparator generate an undesired offset of the baseline level, which affects the pixel-to-pixel detection threshold mismatch and distorts the energy measurement. The offset in each readout pixel must be equalized in the pixel array to obtain a uniformly distributed effective threshold. Most pixel detectors have a threshold adjustment Digital-to-Analog converter (DAC) in each pixel for correcting the offset spread in the analog front-end circuits. The ASICs have a global DAC in the periphery to set the adjustment range. The distribution of the offset dispersion before local tuning follows a Gaussian shape. The distribution after correction follows a uniform distribution with a width proportional to the tuning DAC step value, given by [11]:

$$\sigma_{eq} = \frac{I_{LSB}}{\sqrt{12}} \tag{3-30}$$

The step value is the Least Significant Bit (LSB) current of the DAC. This is illustrated in Figure 3.15, which shows the simulated mismatch in the front-end of Medipix4. 5-bit trimming DAC is used to cover the mismatch range equal to six times the total mismatch of the analog pixel. The random noise from the electronics and the threshold dispersion after correction determines the pixel detector’s minimum detectable energy. The minimum detectable charge can be approximated to:

$$Q_{min} = 6\sqrt{ENC^2 + {\sigma_{eq}}^2} \tag{3-31}$$

Where ENC is the electronic noise of the analog front-end, and σ_{eq} the standard deviation of the mismatch after equalization. The factor 6 permits 99.99966% noise-free pixels in the matrix.

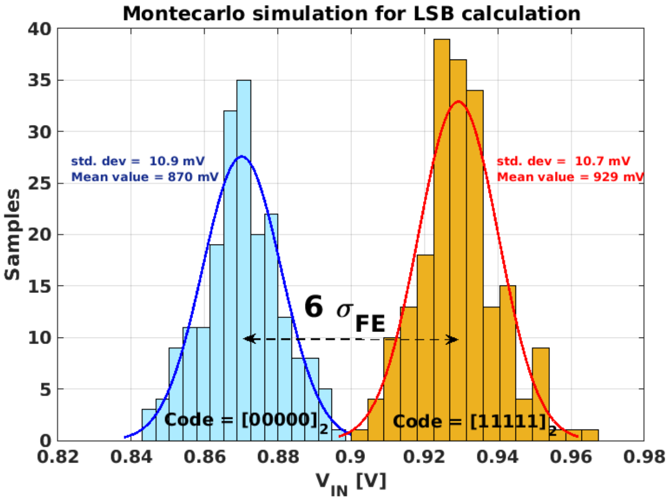


Figure 3.15. Procedure for the choice of I_{LSB} in the threshold adjustment per pixel.

The calibration DACs occupy a large circuit area in the pixel. Indeed, in binary-weighted DACs, the transistors occupy a large area to have a good matching and avoid missing codes. Moreover, adding an extra bit in the DAC increases the area by two. The area constraints may be problematic for small pixel size and front-ends using multiple thresholds. An alternative solution is the sub-binary radix DACs presented in [49]. "Sub-binary" means the weights of the different bits are smaller than two. The transfer function of those DACs is not linear and non-monotonic, as shown in Figure 3.16. Those topologies rely on the redundancy introduced to achieve the same linear dynamic range as a binary-weighted scheme but at a reduced circuit area. Therefore, more bits are required in the sub-binary radix architectures to recover the lost in dynamic range caused by the non-monotonic output characteristic. In the framework of the design of Timepix4, the sub-binary radix DAC was a possible candidate as a correction DAC for the pixel-to-pixel threshold mismatch. The plots in Figure 3.16 show the simulated transfer function of a 7-bit sub-binary DAC (left) and the simulated output response after calibration (right). Two extra bits were needed to achieve the same resolution as a 5-bit binary-weighted DAC, but with a factor two reduction in the circuit area. This alternative solution was not implemented in the end in Timepix4 as the pixel size allowed the implementation of a standard 5-bit binary radix DAC.

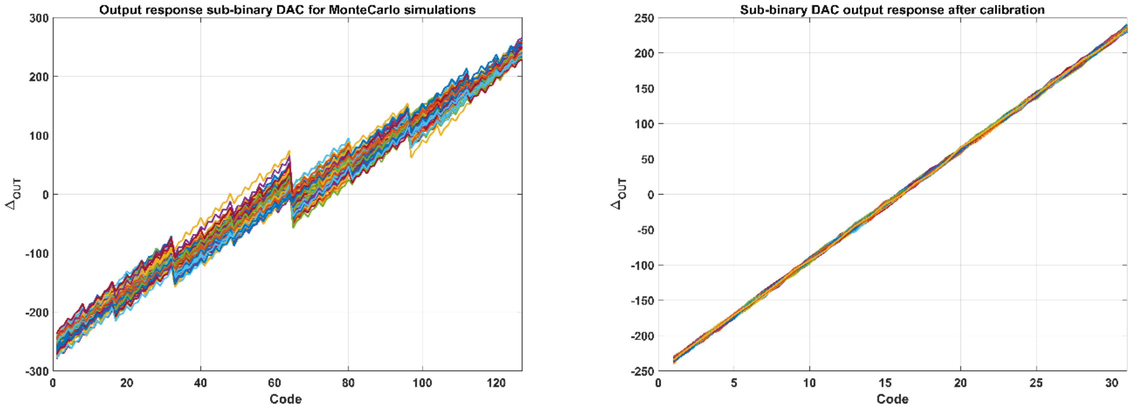


Figure 3.16. Non-linear and non-monotonic transfer function of a 7-bit sub-binary radix DAC on the left. Linear transfer function after calibration on the right (7 bits are necessary to achieve the same dynamic range as a 5-bit binary-weighted DAC).

3.3.2.3 Gain mismatch

In addition to threshold dispersion, there is a gain mismatch between pixels. The gain is the amplitude of the signal given by the analog front-end. The mismatch of the passive or active components in the analog amplifiers from pixel-to-pixel induces a gain mismatch. Some ASICs implement a gain calibration scheme in the pixel front-end for an on-chip correction. For example, the ASIC UFXC32k has a gain trimming circuit using tiny components to correct the gain of the shaper [50], [51]. There are 4 bits for the local tuning of the front-end gain, defined by the ratio between the effective capacitance (overall series capacitance obtained from the 4 bits tuning) and the shaper feedback capacitance C_{sf}. This 4-bit gain calibration allows a factor of three improvement in the gain dispersion between pixels.

3.3.2.4 Ballistic deficit

The time needed for the CSA output to reach the peaking value for a given charge is called peaking time. We have seen that the peak amplitude of the CSA is given by the inverse of the feedback capacitance only when the peaking time and the time for the discharge are well separated in time scales. An amplitude loss is noticed when the discharge time is comparable to the peaking time. This mechanism is referred to as ballistic deficit. The amplitude loss can be avoided by having a longer discharge time at the cost of poor performances at high rates. Another solution is to decrease the time constants, which improves the count-rate capability at the expense of high power consumption. However, the designer must be careful when reducing the peaking time of the front-end because the sensor itself requires a minimum time for inducing the total incoming charge on the collection electrode. Indeed, we have considered for the analysis of the readout electronics that the induced signal pulse is very short. However, the width of the induced charge depends on the mobility of the charge carriers in the semiconductor material, the sensor bias voltage, the dimension of the pixel size compared to the sensor thickness. Larger pixels have a wider induced current pulse response than the small pitch elements due to the lower gradient of the weighting potential, as illustrated in Figure 3.17 [12]. If the signal peaking time is shorter than the sensor-induced signal time, a loss of the peak amplitude happens due to an incomplete integration of the full-deposited charge. This loss degrades the measured energy spectrum.

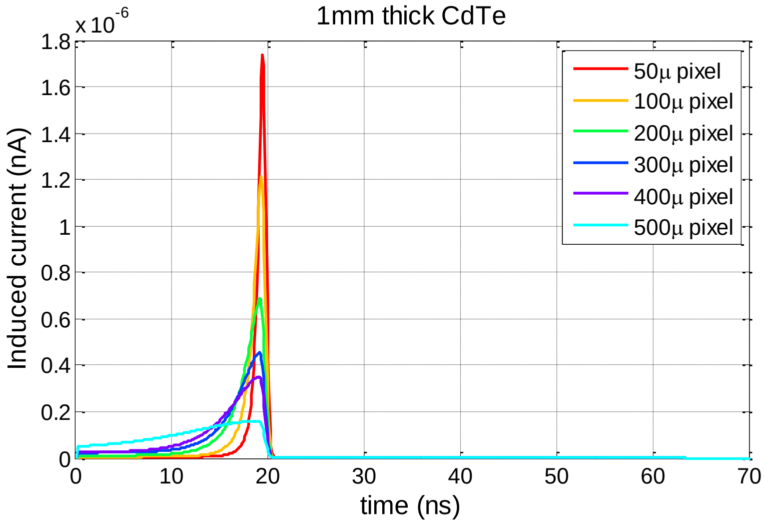


Figure 3.17. Simulated induced signal at the input of the readout pixel for a 1mm thick CdTe sensor as a function of the pixel size dimension. The sensor bias voltage is 600 V, and a 60 keV input photon was taken for the simulation [13].

The choice of the peaking time influences the system's count-rate capability, noise, and energy resolution. A review of the existing hybrid pixel detectors was carried out in [12]. The count-rate capability of those ASICs is plotted as a function of the pixel dimension size in Figure 3.18. More information about the ASICs associated with the numbers on the plots can be found in [12]. The scaling down of the pixel size allows for a higher count-rate capability of the system. However, a drastic reduction of the dead-time and peaking time leads to a ballistic deficit. The dotted red curve indicates the physical limit for a given pixel size to integrate 90%, 95%, and 97.5% of the deposited charge. The induced current signal time was calculated using a 1 mm thick CdTe model at 600 V bias and an input photon of 60 keV. Assuming a front-end with a Gaussian shape response and having a pulse duration equal to twice the induced signal time, the ideal count-rate capability for a given percentage charge integration can be calculated. The ASICs in the plot above the dotted red curve are suffering from a ballistic deficit. Philips developed ChromAIX2 (number 40) using a pixel pitch of 500 µm and a short peaking time of 10 ns [52]. Those design parameters permit a high count-rate capability of 168 x 10^6 counts/mm^2 at the cost of poor energy resolution fidelity. On the contrary, other systems focus on spectral fidelity but with a poor count-rate capability. This is the case for the ASIC HEXITEC, where an energy resolution of 0.8 keV in Full-Width Half Maximal has been reported using an input source of 60 keV [12], [53].

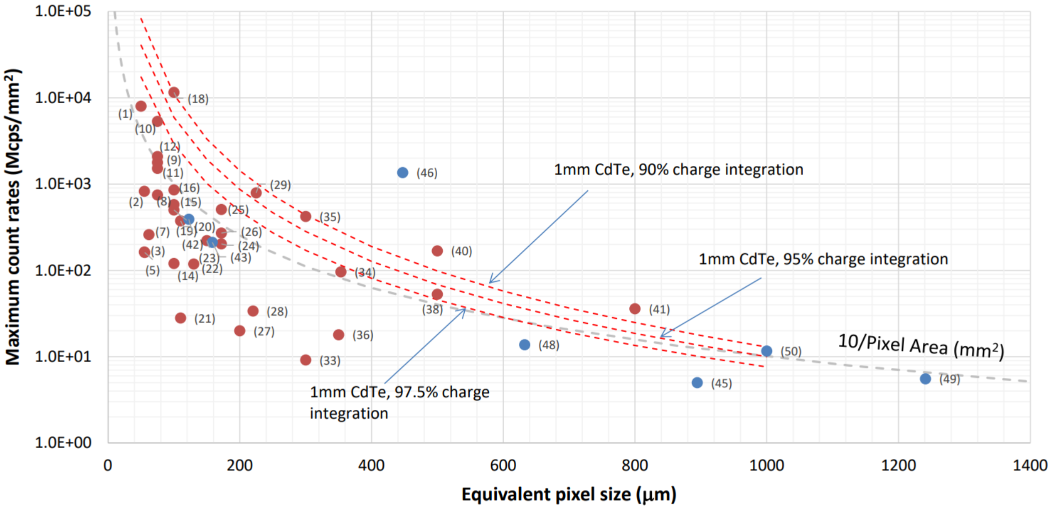


Figure 3.18. Maximum count-rates for different hybrid pixel detectors as a function of the pixel pitch [12].

3.3.2.5 Pulse Pile-up

When measuring the radiation from beam or radioactive sources, the events arriving in the detector follow the Poisson statistics [30]. This means that there is a probability that two photons deposit their energies in the detector very close in time. However, there is an intrinsic limit on the time needed for the front-end pixel to process every single event. The faster the preamplifier's signal returns to the baseline, the faster it will process the next event. Pulse pile-up means that the preamplifier did not return to the baseline between two consecutive events. The counting system's minimum time required to separate two different events is called "dead time" [30]. In chips using multiple thresholds for spectroscopic measurement, pile-up events overestimate the energies of the incoming events. For ASICs with a single threshold, there is an underestimation of the overall counts leading to a degradation of the energy resolution.

This is illustrated in Figure 3.19, where the front-end of Medipix4 has been simulated with an input flux having a mean time between consecutive photons of 1 µs. The events 5 and 6 are very close in time, and the system cannot distinguish those events as separate events.

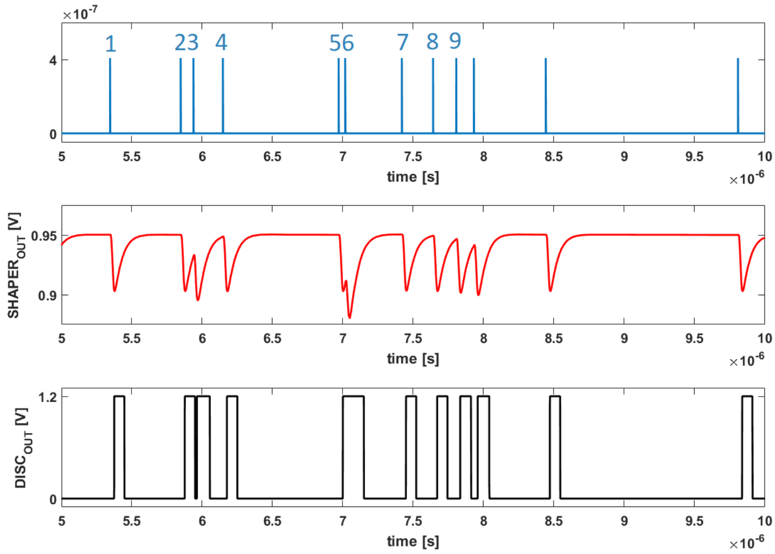


Figure 3.19. Explanation of pile-up events. The blue plot represents the incoming input charges; the red curve is associated with the output of the shaper and the discriminator output in black.

At high flux rates, there are more and more pile-up events, leading to a loss of the measured counts in photon counting systems, referred to as "dead-time loss." Therefore, the system is not reliable from a maximum count-rate value. This is why low flux is used for most applications where spectral fidelity is important. In [13] [12], a review of hybrid pixel detectors is carried out and the count-rate capability of the systems is detailed. There is a trade-off between energy resolution and the count-rate when the chip is used in different applications. The 10% count-rate deviation is a good trade-off for having an accurately measured spectrum [13] [54].

Philips is developing the ChromAIX family of hybrid pixel detector chips using CZT sensors. Figure 3.20 shows the count-rate capability of the ChromAIX2 chip [55]. The maximum count-rate of the chip is 27 million counts per pixel; this corresponds to an observed count-rate of 10 million counts per pixel. Input pulses following the Poisson distribution have more events happening shorter than the mean value of the distribution. This is why the observed count-rate is higher for equidistant pulses. Later in this thesis, a Poisson distribution will be used for simulating the count-rate capability of the Medipix4 chip.

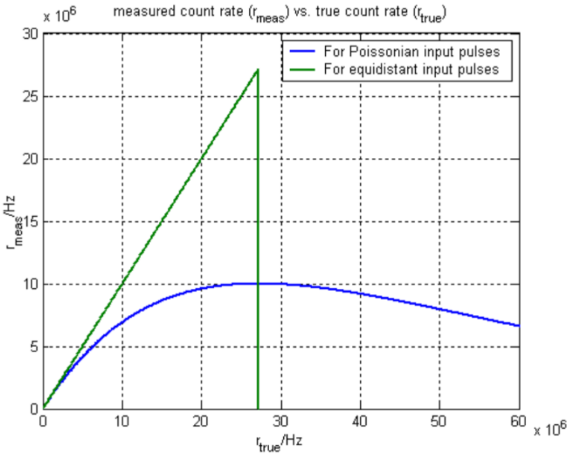


Figure 3.20. Observed count-rate versus incident count-rate for a Poisson distribution in blue and equidistant arrival pulses in green [55].

Some applications like Computerized Tomography (CT) imaging require a very high count-rate capability from the detector. Therefore, some systems implement special features to remove the piled-up events from the processing chain or retrieve the pile-up events, which will be otherwise lost. Such systems are called non-paralyzable systems [30]. On the other hand, paralyzable systems have no additional mechanisms to deal with pile-up events. In the case of paralyzable systems, the observable count-rate f(x) is given as a function of the incident count-rate by the equation [56]:

$$f(x) = xe^{-x\mu} \tag{3-32}$$

Where μ is the dead time of the system.

Some non-paralyzable mechanisms used in the design of ASICs to deal with high flux are presented [13] [12] in the following section.

3.3.2.5.1 Instant retrigger capability of the PILATUS3 ASIC [57]

The first example of a system using a non-paralyzable counting method is the PILATUS3 ASIC. The chip is implemented using a 250 nm CMOS technology with 5 metal layers. The chip is made of an array of 60 x 97 pixels, with a pixel pitch of 172 µm. The principle is to evaluate the state of a pulse after a pre-determined time interval. With pulse pile-up, a longer time is required for the front-end output to return to the baseline. This increases the duration of the Time-Over-Threshold (TOT) of the signal at the output of the comparator. By setting the re-evaluation of the signal after the time interval, subsequent events are retrieved. This is illustrated in Figure 3.21: the first event is counted correctly. The 2nd and 3rd events arrive very short in time, having the re-trigger permits to capture the 3rd event, which will be lost otherwise. It is worth noting that the algorithm is optimized for monochromatic sources.

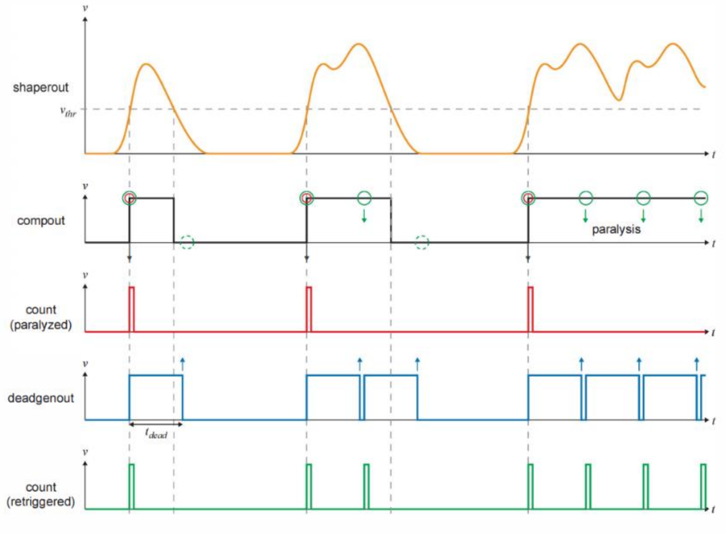


Figure 3.21. Signal waveforms illustrate the operation of the instant retrigger technology. The output of the shaper (in orange) is fed to the comparator (in black). The registered counts for the paralyzed mode are shown in red; the retriggered counts are shown in green. The blue waveform shows the dead-time set for the measurement [57].

Figure 3.22 shows the measured count-rate capability of the PILATUS3 ASIC. A continuous source of 8 keV was used for the measurement with a threshold set at 4 keV. The instant retriggers technology significantly increases the count-rate of the ASIC, but is limited to monochromatic sources [57].

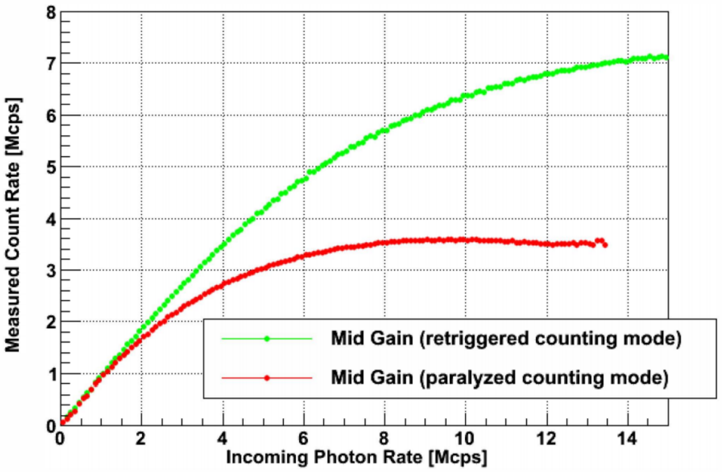


Figure 3.22. The measured count-rate of the PILATUS3 X-ray detector versus the incoming photon rate. The red curve corresponds to the paralyzed counting mode, and the green curve shows the retriggered counting mode. The input source is monochromatic with an energy of 8 keV; the threshold is set at the mid-range for the measurement [57].

3.3.2.5.2 Pile-up trigger method of Siemens photon-counting ASIC [58]

In [58], the implementation of an ASIC to deal with very high flux is explained. The ASIC aims at CT systems, where fast scanning is required. The algorithm relies on setting the two thresholds contained in the front-end. One threshold is set above the maximum energy of the incident X-ray source. Therefore, pile-up events will trigger the counter associated with this threshold. There is a second threshold with an associated counter set at the spectrum's energy under interest. By combining the information from the spectral counter signal with the pile-up counter signal, the overall count-rate of the system is increased. The counting system is a 1.6 mm thick CdTe sensor bonded to a 64 x 64 pixel matrix, with a pixel pitch of 225 µm. The front-end has a high-speed pulse shaping of less than 20 ns and can deal with charges up to 160 keV. Figure 3.23 shows the measurements obtained from the chip. The count-rate capability increases when setting the threshold at higher energies.

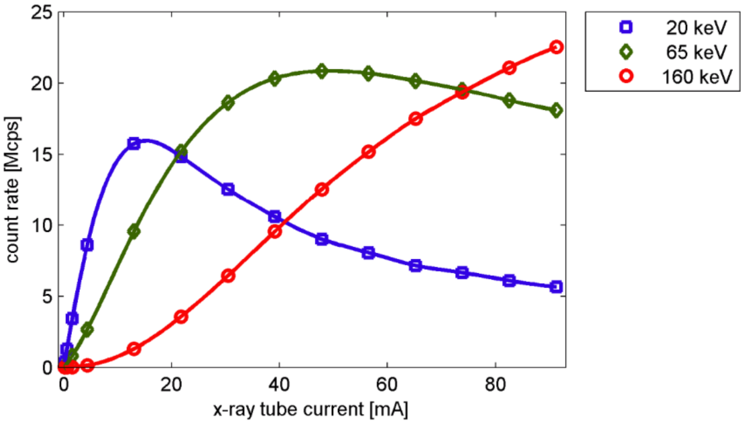


Figure 3.23. The count-rate capability of the ASIC using an unattenuated 140 kVp input spectrum at calibrated energy thresholds, increasing the threshold voltage permits to lower the degree of paralyzation of the chip [58].

3.3.2.5.3 Photon counting and integrating channel in CIX0.2 ASIC [59]

The CIX0.2 chip proposes a front-end allowing simultaneous measurement of the number of absorbed photons and deposited energy. When the photon counting part paralyzes at high flux, the integrating part will extend the dynamic range of the chip. This scheme is interesting for medical X-ray applications where an extensive dynamic range is required and keeping the spectral information in the region where both operating circuitries overlap [59]. The ASIC is manufactured using AMS 0.35 µm technology. The prototype contains 17 pixels, each having a size of 100 µm x 550 µm. The architecture is shown in Figure 3.24. The input node is connected to the photon counting channel and the integrator channel. The pixel can compensate for DC leakage current coming from the sensor. The system's dynamic range goes from 3 pA to 200 nA, extending the detection limits of the respective measurement scheme.

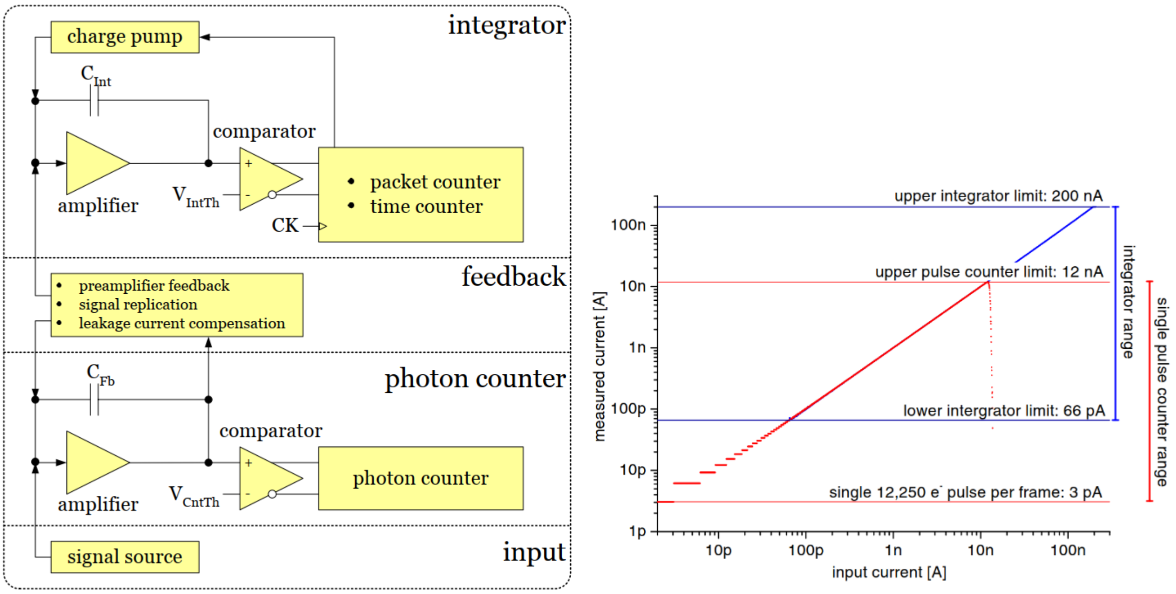


Figure 3.24. The architecture of the CIX0.2 analog pixel (left) and measured dynamic range of the pixel (right) [59].

3.3.2.5.4 Pixel detectors with clocked comparators [60]

Another ASIC developed for CT imaging is presented in [60]. The chip contains 160 pixels, each measuring 500 µm x 400 µm. The readout is implemented using a 180 nm CMOS process with a supply voltage of 1.5 V using a new reset scheme. The system achieves a maximum count-rate of 17 million counts per pixel. Each channel contains 8 thresholds using 8 comparators. Those comparators are clocked at a frequency of 100 MHz or 200 MHz. When an input signal exceeds one of the thresholds, a digital register is set. After a programmable dead-time, the counter associated with the highest detected threshold is incremented. After the counting, the registers are reset, and a new event can be processed after an interval time set by the user. This removes the overestimation of the energy if an event comes very close to its predecessor. The ASIC is also dealing with high count-rates by using the mechanism of digital peak detectors. When a first peak is detected and the pulse peak is passed, the filters in the front-end are reset, bringing the baseline to the original point. This is done by shorting the capacitor in the filter to the reference baseline voltage. A new event can be processed without falling on the tail of the first event.

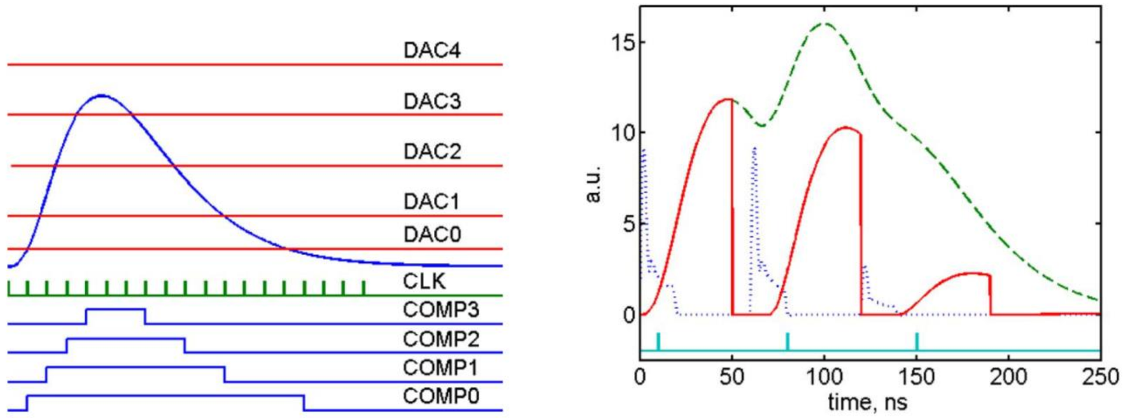


Figure 3.25. Signal waveforms explaining the procedure for detecting a pulse (left) and filter reset mechanism (right) [60].

Figure 3.25 illustrates the working principle. Multiple thresholds are set to detect the incoming event. In this case, only the counter associated comparator 3 is incremented. The scheme to capture pile-up events is presented in the right plot. The blue dashed lines represent the incoming photons very short in time, leading to pulses pile-up as shown in the dotted green line. The reset mechanism permits capturing the events, even a tiny pulse (third event) coming after a strong pulse (second event). However, the mechanism cannot detect peak pile-up events, for which the coincidences of the events happen around the rising edges.

3.4 Summary

This chapter gives an overview of the hybrid pixel detector technology. The electron-hole pairs generated from a photoelectric effect drift towards the collection electrode while the charges also spread out upon diffusion. The motion of the charge carriers induces a small input current in the readout pixel, which is processed by the analog processing circuitry before fedding the digital pixel. Some limitations in the sensor material and the readout electronics must be considered when designing a hybrid detector. The absorption efficiency of the silicon may limit some applications; high-Z materials offer an extended efficiency for capturing high-energy photons. However, high-Z materials create multiple challenges in a hybrid pixel detector. Due to impurities, the charge trapping/recombination in the compound materials leads to a reduction of the signal induced in the collection electrode. The characteristic fluorescence photons generated in the high-Z materials travel away from the initial impact point before depositing their energy. This leads to an incomplete charge integration by a single pixel and the possibility to detect multiple hits for a single photon. The latter can be solved by increasing the collection area of the sensor, but this does not help when dealing with high flux, increases the electronic noise, and are more susceptible to trapping. In addition, larger pixels have a wider induced current pulse response than small pitch pixels and enter in ballistic deficit if the signal peaking time is shorter than the sensor-induced signal time.

On the other hand, an increase in segmentation allows for a better spatial resolution, lower electronic noise, and high count-rate capability at the penalty of degraded energy resolution due to charge diffusion and fluorescence photon effects. In addition, the designer can take advantage of the small pixel effect by minimizing the pixel pitch for the sensor thickness. Indeed, small pixels permit to decrease the time duration of the induced signal at the readout input and minimize the loss by a ballistic deficit. Moreover, the small pixel effect permits minimizing the contribution of the induced current coming from the holes, which are more subject to charge trapping due to lower mobility than electrons. Unfortunately, small pixels are subject to charge sharing due to the charge diffusion and the drift motion. The charge sharing between pixels leads to a distortion of the measured energy spectrum. Chapter 4 and Chapter 5 cover the Medipix and Timepix family of hybrid pixel detectors. Through the different iterations, those ASICs address the limitations highlighted in this chapter.

Chapter 4 Medipix family of chips

Late 1988, using hybrid pixel detectors in other fields of science like medical imaging, synchrotron applications, electron microscopy, or material analysis using X-ray sources was proposed [61]. The idea was to count the number of particles deposited in each pixel during the acquisition time and then read out the number of counts. This idea enabled the first Medipix Collaboration (CERN, INFN of Pisa and Napoli, the University of Freiburg, and the University of Glasgow) to design the Medipix1 chip. The collaborations grew with the development of many Medipix chipsets, and today many groups and institutes are using the chip worldwide [39] [5]. The following section describes the architecture of the Medipix1 (section 4.1), Medipix2 (section 4.2), and Medipix3 (section 4.3) chips. Furthermore, the advantages and limitations of these readout ASICs are highlighted, and the need for a new generation of a readout chip called Medipix4 will be elaborated. The development of the Medipix4 chip is the core of this thesis.

4.1 Medipix1: Photon counting detector for X-ray imaging

4.1.1 Architecture of Medipix1

The chip was designed using the technology SACMOS1 with a minimum feature size of 1 µm, equivalent to a 600 nm standard CMOS process. Using the two metal layers available with that technology, the ASIC was implemented as an array of 64 x 64 square cells with a pitch of 170 µm [62]. The analog front-end consists of a Charge Sensitive Amplifier (CSA) with a feedback capacitance of 3.5 fF, a gain of 30 mV/ke$^-$, and a dynamic range of up to 7 ke$^-$. The 64 columns of pixels are terminated by a dummy cell, which is a reference for the DC leakage compensation for the pixels in those columns. Indeed, in each column of pixels, the current at the dummy cell is subtracted from the preamplifier input. A discriminator and a 3-bit register DAC follow the preamplifier. The threshold variation is improved from 350 e^- r.m.s before tuning to 80 e^- r.m.s after tuning with the 3-bit tuning DAC. In the digital part of the pixel, a 15-bit counter is incremented each time the preamplifier produces a signal exceeding the applied threshold. When the shutter is closed, the 15-bit stored data are shifted pixel-to-pixel towards the end of the column for readout, as is shown in Figure 4.1.

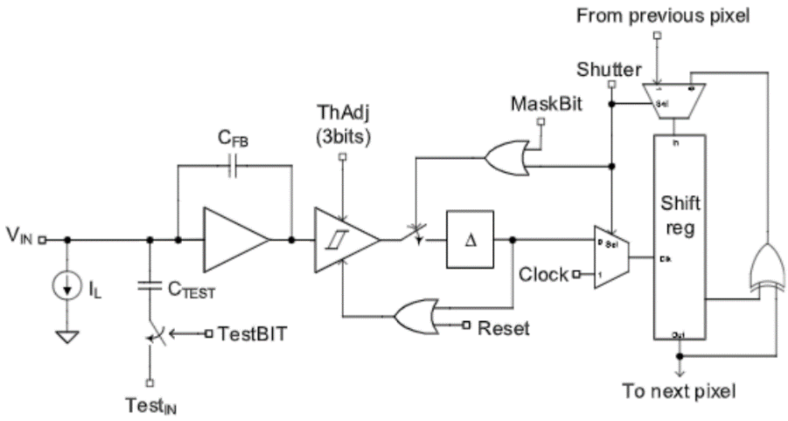


Figure 4.1. Block diagram of the pixel cell in Medipix1 chip [5].

4.1.2 Limitations and motivation for the design of Medipix2

Medipix1 showed promising results with an X-ray imaging quality comparable to those obtained in integrating detector technologies [63]. Those measurements confirmed that photon-counting systems provide a clean image due to the high dynamic range of the system achieved with the 15-bit counter. In addition, different material densities, even in low-contrast objects, are well imaged, benefiting the "noise-free operation" achieved by threshold discrimination [63]. Figure 4.2 shows the X-ray imaging using a ^{109}Cd source obtained with Medipix1 chip of a human tooth having a fine screw inside.

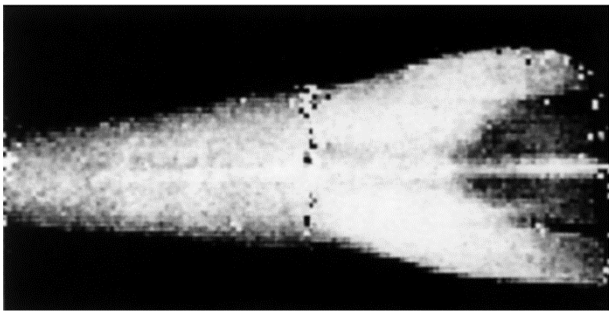


Figure 4.2. Image of a human tooth with a screw inside, X-ray imaging obtained with Medipix1 chip exposed to a ^{109}Cd source. The readout is bonded to a 300 µm silicon sensor [63].

There were few limitations to this chip. For instance, a large guard ring located around the chip makes the tiling difficult, leading to a significant loss in the sensitive area. Also, the DC leakage compensation using the last row of pixels as reference dummies does not work if the sensor pixels have a non-uniform leakage current. In addition, the large pixel size results in a poor spatial resolution [63].

Table 4-1 summarizes the performances of the Medipix1 chip.

Technology	SACMOS1 equivalent to 0.6 µm standard CMOS process 2 metal layers
Pixel size	170 x 170 µm²
Number of pixels	64 x 64
Sensitive area	1.18 cm²
Equivalent Noise Charge	~ 170 e⁻
Dynamic range	Up to 7 ke⁻
Count-rate	Up to 69 x 10^6 photons.mm^{-2}.s^{-1}
Threshold spread before equalization	350 e⁻ r.m.s.
Threshold spread after equalization	80 e⁻ r.m.s.
Number of thresholds	1
Counter-depth	15 bits
Matrix arrangement	Non-buttable
Main functions	Imaging using single-photon counting

Table 4-1: Summary of the performances of the Medipix1 chip.

4.2 Medipix2: dual-threshold X-ray imaging detector

4.2.1 Architecture

The scaling down of the technology and the knowledge learned from the Medipix1 chip permit the Medipix2 Collaboration to develop the first spectroscopic X-ray imaging. The pixel pitch was reduced to 55 µm for a better spatial resolution, and a more complex topology than the first version was implemented using the 250 nm process CMOS technology. The Medipix2 chip contains an array of 256 x 256 pixels [64]. The pixel schematic is shown in Figure 4.3. The analog front-end includes a Charge Sensitive Amplifier (CSA) based on a topology proposed by F. Krummenacher in [36]. This scheme integrates the two feedback loops ((1) the feedback capacitor reset loop and (2) the leakage current compensation loop) in a very compact way. It also has the advantage of being robust against DC leakage current coming from the sensor; this is interesting as a non-uniform leakage current is present in the sensor arrays. The gain of the front-end is around 10.5 mV/ke⁻ giving a dynamic range of linearity up to 100 ke⁻. The output of the preamplifier is connected to two different comparators, both having different thresholds that form an "energy window". "Energy window" means that the digital counter is incremented each time an event falls inside the energy window created by the two thresholds. This idea will be later used in this thesis for the design of the Medipix4 chip. The window discrimination is performed using the Double Discriminator Logic (DLL) in the digital circuitry, and a 13-bit Linear Feedback Shift Register (LFSR) counts the events falling between the two energy bins. The counting is performed when the shutter is low. When the shutter is high, an external clock shifts the counter values from pixel to pixel towards the end of the column. More details about the design and implementation of the chip can be found in [8].

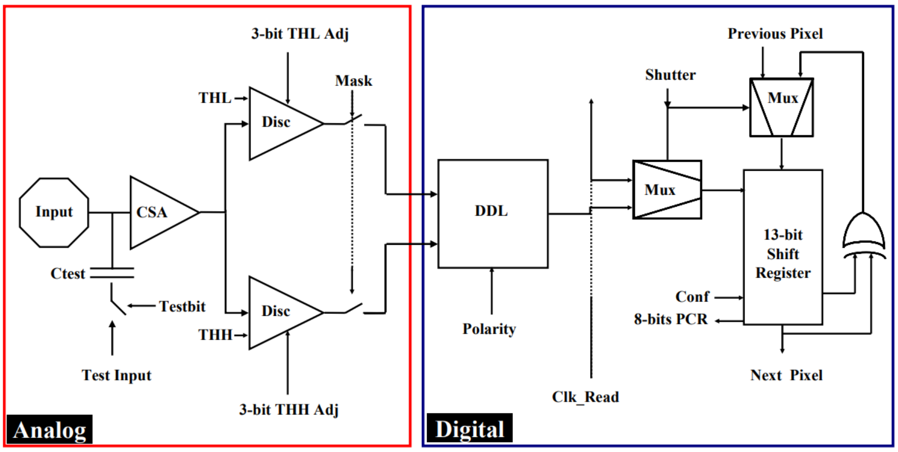


Figure 4.3. Block diagram of the pixel in Medipix2. The left part in red corresponds to the analog processing circuitries, and the blue part to the digital pixel [8].

4.2.2 Applications using Medipix2

Medipix2 ASICs are used in versatile applications with different semiconductor materials. A list of some of the applications using the Medipix2 chip is shown in Table 4-2, and a few more applications were added to the ones already described in [8].

Applications	Medipix2	Detector	Publications
Adaptive optics	1	Micro channel Plate (MCP) [e$^-$]	[65]
X-ray diffraction	1	Si sensor 300 µm [h$^+$] Si sensor 700 µm [h$^+$]	[66] [67]
Micro-radiography	1	Si sensor 300 µm [h$^+$]	[68]
Neutron imaging	1	Si sensor 300 µm [h$^+$] + 6LiF converter [e-] Neutron sensitive MCP [e-]	[69] [70]
Autoradiography	1	Si sensor 300 µm [h$^+$]	[71]
Gamma imaging	1	CdTe sensor 1 mm [e-]	[72] [73]
Electron microscopy	1 2x2	Si sensor 300 µm [h$^+$] Si sensor 300 µm [h$^+$]	[74] [75] [76]
Energy weighting	1	Si sensor 300 µm [h$^+$]	[77]
In vivo optical and radionuclide imaging	1	Si sensor 300 µm [h$^+$] CdTe sensor 1 mm [e-]	[78]
Micro Patterned Gas Detectors	1	Gem and Micromegas [e-]	[79]
Mammography	25x19cm	Si sensor 700 µm [h$^+$] CdTe sensor 800 µm [e-]	[80]
Radiation monitoring	1	Si sensor 300 µm [h$^+$]	[81]
Dental imaging	1	Si sensor 300 µm [h$^+$] Si sensor 300 µm [h$^+$] & CdTe sensor 500 µm [e-]	[82] [83]

Table 4-2: Summary of a few applications using Medipix2 as readout. The size of the detector and the sensor material is indicated.

4.2.3 Limitations and motivation for the design of Medipix3

The pixel size had been reduced to 55 µm for achieving a better spatial resolution with respect to Medipix1. However, when decreasing the size of the pixel with respect to the thickness of the sensor, charge sharing between pixels becomes a limiting factor in the detector's performance [10] [84]. This charge diffusion distorts the energy spectrum seen by the individual pixels. In addition, for high-energy X-rays (more than 20 keV), high-Z materials like CdTe must be used to improve the detection efficiency. The fluorescence photons created within the sensor material have a mean free path similar to the pixel pitch size, which means the fluorescence photons are not deposited on the correct pixel sensor but on one of its neighboring pixels [5].

To evaluate the charge sharing implications of small pixels in photon-counting detectors, simulations were performed on a 300 µm thick silicon and a 300 µm thick GaAs detector bonded to a 55 µm readout pixel [85] [11]. A monochromatic beam of 10 keV was considered as the source beam for the silicon sensor and 20 keV for the GaAs sensor. The front-end's electronic noise is taken into account, taking 100 e^- as it should be for Medipix2. The simulated spectrum is shown in Figure 4.4. The photopeak at 10 keV is detected for the silicon sensor, but the charge sharing between the neighboring pixels creates a low energy tail called 'charge sharing tail' in the simulated spectrum. For the high-Z material sensor GaAs, the main photopeak is still visible at 20 keV. Still, another two peaks are located at 10 keV, which corresponds to the characteristic energy of the fluorescence photons created in GaAs material and the escape peak.

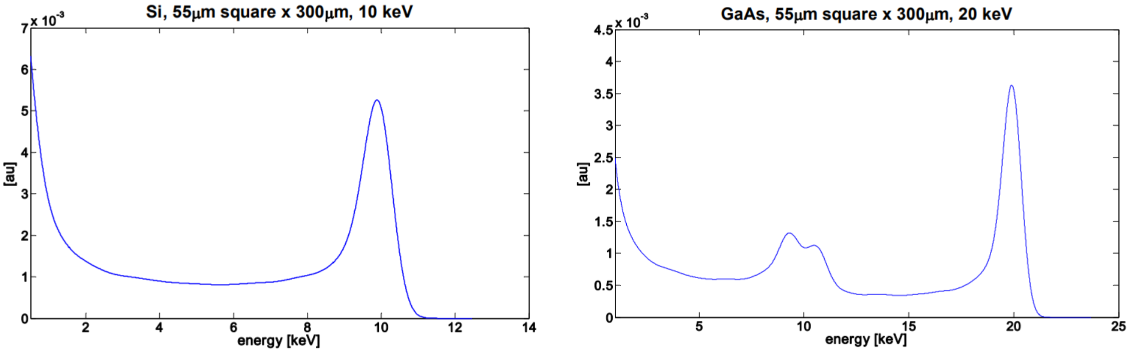


Figure 4.4. Simulation of the energy spectrum seen using a 10 keV monochromatic source on a 300 µm thick Si sensor (left) and 20 keV for the 300 µm thick GaAs sensor connected to a 55 µm pixel pitch [85].

The effect of charge diffusion in the Medipix2 chip is further studied and evaluated in [84]. The chip is connected via indium bump-bond contacts to a CdTe sensor. The charge collection of a 59.5 keV from a ^{241}Am source is measured on a cluster of 2x2 pixels, as shown in Figure 4.5. The charge is split between the four pixels creating a distortion in the measured energy spectrum; this is because a single channel does not collect all the deposit charge. The study in [84] demonstrated that by summing all the contributions of the neighboring pixels, the energy spectrum of the X-ray source could be recovered. Those results agree with the algorithm proposed for the charge sharing correction in the Medipix3 chip.

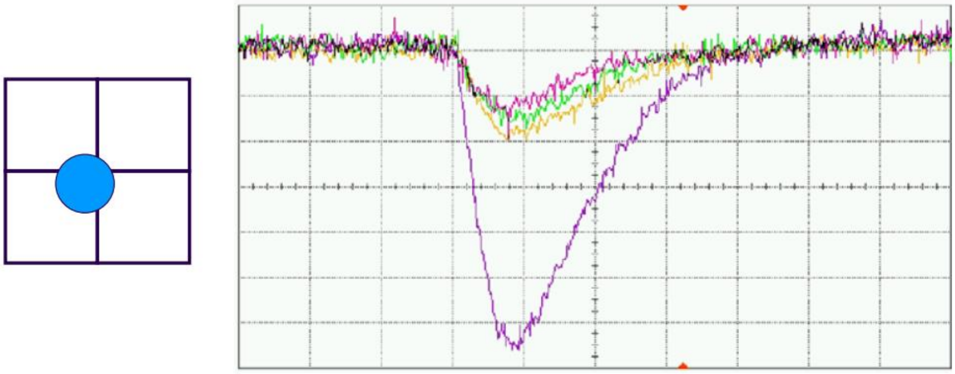


Figure 4.5. Measured responses of 2 x 2 pixels cluster after detecting a 50.5 keV photon from ^{241}Am source. The charge is split between the four pixels generating distortion in the energy spectrum [84].

Table 4-3 summarizes the performances of the Medipix2 chip.

Technology	IBM 0.25 µm CMOS technology
	6 metal layers
Pixel size	55 x 55 µm²
Number of pixels	256 x 256
Sensitive area	1.98 cm²
Equivalent Noise Charge	~ 140 e⁻
Dynamic range	Up to 100 ke⁻
Count-rate	Up to 35 x 10^6 photons.mm^{-2}.s^{-1}
Threshold spread before equalization	500 e⁻ r.m.s.
Threshold spread after equalization	100 e⁻ r.m.s.
Number of thresholds	2
Counter-depth	14 bits
Matrix arrangement	3-side buttable
Main functions	Imaging using single-photon counting

Table 4-3: Summary of the measured performances of Medipix2 chip.

4.3 Medipix3: Spectroscopy imaging with charge sharing correction

4.3.1 Charge sharing correction method

Scaling down the pixel size permits an excellent spatial resolution and high count-rate capability per pixel. However, the charge sharing between the adjacent pixels becomes the limiting factor in the performance of the detector. Indeed, without further correction, the charge diffusion distorts the measured energy spectrum [10] [11].

A method for correcting the charge sharing between pixels is proposed in [86]. The charge is summed in every 2 x 2 cluster of pixels for each incoming event, and the hit is allocated to the pixel having collected the most charge deposit. The architecture must implement those two separate functions in parallel. Figure 4.6 illustrates a charge deposition at the edge of four pixels. The steps for determining the winner among the four pixels are [85], [87]:

Step 1: Local threshold TH_LOCAL is applied to all pixels.

Step 2: An arbitration circuitry determines the pixel having collected the highest charge and suppresses the pixels with a lower signal. This is possible using the Time-over-Threshold information.

Step 3: The sum is reconstructed in a parallel process using an analog summing circuitry. Each pixel sums its own contribution, and the pixel's contribution is on its right, top, and top-right.

Step 4: The winner pixel checks the adjacents summing circuitries if at least one of them exceeds the threshold set for the summing signal: TH_SUM. In this case, the counter associated with TH_SUM is incremented.

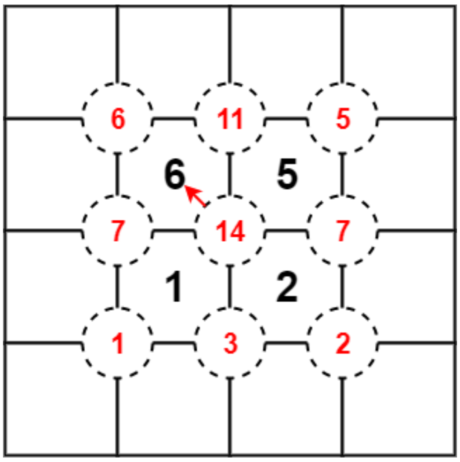


Figure 4.6. Illustration of the implementation of the charge sharing correction by summing the contribution in a cluster of 2 x 2 pixels, and attributing the total reconstructed charge to the pixel having collected the highest charge.

Those steps ensure that the charge deposited in 2 x 2 pixels is fully reconstructed by using an analog scheme, and the digital scheme allocates the reconstructed charge to a single pixel, avoiding mutiple counting for a single hit. Figure 4.7 shows the simulated energy spectrum of a 10 keV and 20 keV input source in a 300 µm thick Si sensor and 300 µm thick GaAs sensor, respectively. The charge sharing tail is suppressed for both cases. In addition, the charge deposited by the fluorescence photons in the GaAs sensor is reconstructed as they fall in the 2 x 2 summing cluster. In this summing mode, the noise from the four pixels is added in quadrature, leading to a factor two increase in the total noise.

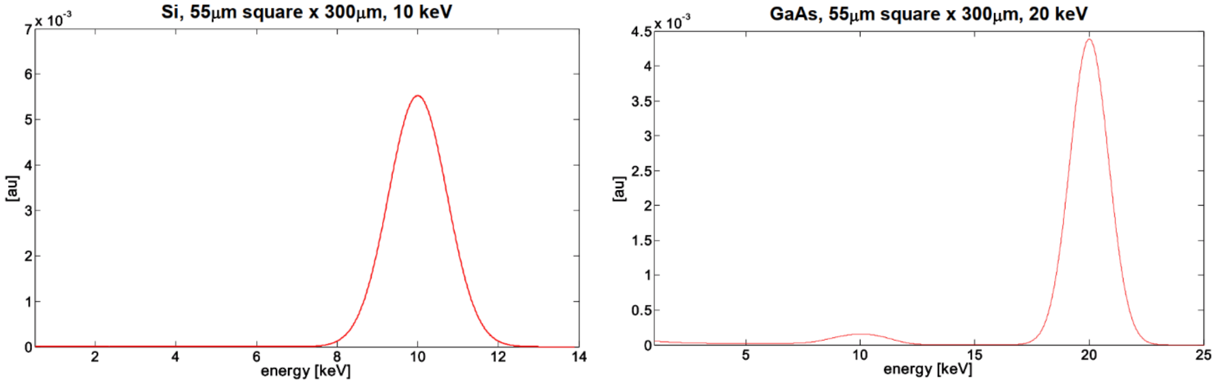


Figure 4.7. Simulation of the energy spectrum of a 10 keV monochromatic source and 20 keV source in a thick 300 µm Si sensor (left) and 300 µm thick GaAs sensor connected to a 55 µm pixel pitch. By applying the charge sharing correction, the charge sharing tail is suppressed. In addition, the energy of the fluorescence photons in the GaAs sensor is included in the charge sum [85].

Medipix3 is the first ASIC to implement the charge sharing correction on an event-by-event basis. The mode is called “Charge Summing Mode”. Similar architectures are implemented on pixels in other ASICs for hybrid pixel detectors. The PIXIEIII has the “Pixel Summing Mode,” where the analog sum is performed on a 62 µm pixel pitch [88]. The “C8P1 algorithm” is built on a 100 µm pixel pitch using 40 nm CMOS process in [89]. The charge sharing has been addressed using digital correction in the readout chip ERICA on a 330 µm pixel pitch [90].

4.3.2 Architecture

A first prototype was implemented using the 130 nm CMOS process. The prototype had an array of 8 x 8 pixels with a pixel size of 55 µm. A full-chip Medipix3 was implemented after the prototype chip. The chip contains 256 x 256 pixels elements, having a size dimension of 55 x 55 µm². In Fine Pitch Mode (FPM), each readout pixel is connected to a 55 µm pitch sensor cell. In Spectroscopic Mode (SM), the readout pixels can be connected to 128 x 128 sensor cells having a pitch of 110 µm. A configurable-depth digital counter architecture is proposed in each pixel: 2 x 1-bit, 2 x 4 bit, 2 x 12 bits or 1 x 24 bit [91]. In SM, the sharing of ressources between the four readout pixels permits eight thresholds per super-pixel. Therefore, each 110 µm pixel can be programmed to have 8 x 1-bit counters, 8 x 2-bit counters, 8 x 12-bit counters, or 4 x 24-bit counters. The counts of the energy bins can be read out in Sequential Read/Write (SRW) or Continuous Read/Write (CRW) modes. In SRW, the number of pulses from the comparator output is stored in a 12-bit depth counter for each threshold. When the signal ‘Shutter’ is low, the data are shifted from pixel to pixel to the end of the column for readout. During this operation, the pixel does not count the incoming photons. A dead-time-free operation is possible when configuring the pixels in CRW. The 24-bit registers available in the digital circuit for counting are split into two 12-bit counters. During the readout of one of the 12-bit registers, the other 12-bit register counts the number of pulses of the comparator. However, only one threshold can be read out at a time in this mode of operation.

The chip is the first large chip implemented for the High Energy Physics community using the 130 nm CMOS process. Some non-desirable effects were found with measurements. Some pixels have their thresholds values varying with time; the effect was similar to Random Telegraph Noise (RTS). The origins of this RTS noise effect are damage in the thin gate oxide (around 2 nm for the 130 nm process) and the large number of target transistors (65000 elements) connected to each global DAC [5].

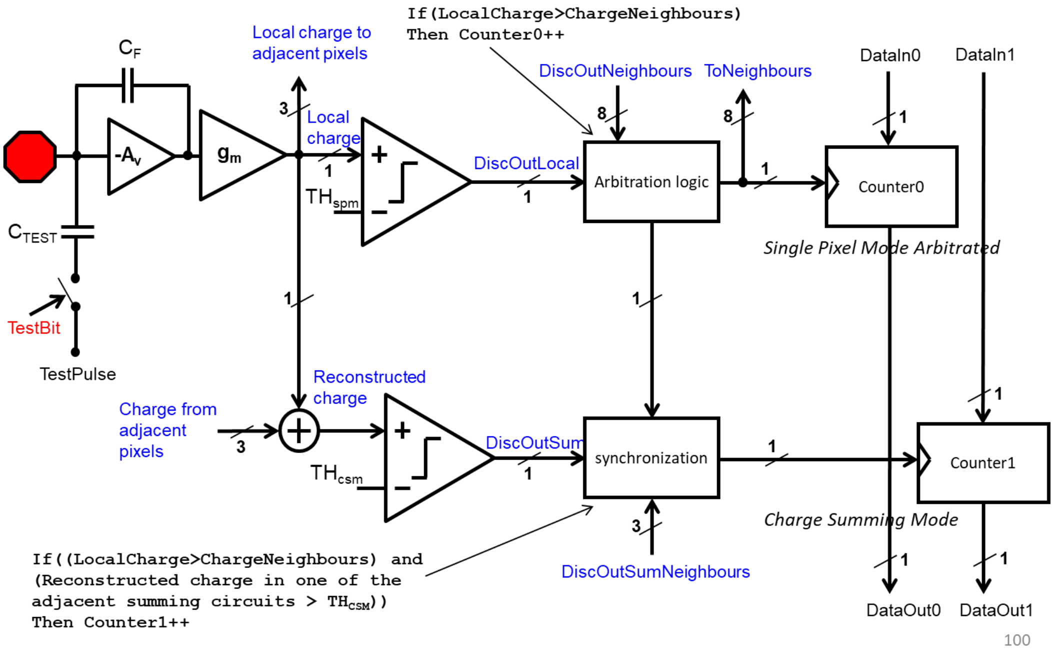


Figure 4.8. Block diagram of the pixel cell in the Medipix3 chip. The analog pixel contains a CSA followed by a first-order semi-gaussian shaper, then a current comparator. The communications between neighboring pixels permit correct the charge sharing between pixels. The digital circuitry contains two 12-bit counters, an arbitration circuitry, and some control logic [85].

A redesign of the chip called Medipix3RX solves the RTS noise effect by implementing a tie-down diode at Metal 1 at the gate of each target transistor [5]. The allocation of the hit for the charge sharing correction algorithm is slightly modified due to the misassignment of hits due to large pixel-to-pixel variation [92]. A new charge summing process and hit allocation are proposed by simulating the charge sharing along the threshold dispersion effects observed in Medipix3 [92]. The pixel having collected the largest local charge deposition is the winner pixel in the new scheme. The block diagram is shown in Figure 4.8. In addition, a new design approach using standard cell library permitted precise simulations of the full readout architecture in Medipix3RX [5].

The performances of the redesigned chip are presented in Table 4-4, and more details about the pixel architecture can be found in [87].

<table>
<tr><td>Technology</td><td></td><td>130 nm CMOS technology</td></tr>
<tr><td></td><td></td><td>8 metal layers</td></tr>
<tr><td>Pixel size</td><td>FPM</td><td>55 x 55 µm^2</td></tr>
<tr><td></td><td>SM</td><td>110 x 110 µm^2</td></tr>
<tr><td>Number of pixels</td><td>FPM</td><td>256 x 256</td></tr>
<tr><td></td><td>SM</td><td>128 x 128</td></tr>
<tr><td>Sensitive area</td><td></td><td>1.98 cm^2</td></tr>
<tr><td>Equivalent Noise Charge
[e$^-$] r.m.s.</td><td>FPM-SPM</td><td>72 | 80 | 93 |100 (4 gain modes)</td></tr>
<tr><td></td><td>FPM-CSM</td><td>148 | 174 | 201 | 233</td></tr>
<tr><td></td><td>SM-SPM</td><td>> 72 | 80 | 93 |100</td></tr>
<tr><td></td><td>SM-CSM</td><td>> 148 | 174 | 201 | 233</td></tr>
<tr><td>Dynamic range [ke$^-$]</td><td></td><td>5 | 9 | 12.5 | 18</td></tr>
<tr><td>Count-rate (10% dead time loss)
[Mphotons.mm^{-2}s^{-1}]
60 keV input / Vth = 30 keV</td><td>SM-CSM</td><td>4.3</td></tr>
<tr><td>Energy resolution with input
60 keV source [keV]</td><td>SM-CSM</td><td>4.4</td></tr>
<tr><td>Number of thresholds</td><td>FPM-SPM</td><td>2</td></tr>
<tr><td></td><td>FPM-CSM</td><td>1 SPMa + 1 CSM</td></tr>
<tr><td></td><td>SM-SPM</td><td>4</td></tr>
<tr><td></td><td>SM-CSM</td><td>1 SPMa + 4 CSM</td></tr>
<tr><td>Matrix arrangement</td><td></td><td>3-side buttable</td></tr>
<tr><td>Pixel counters in SRW</td><td>FPM-SPM</td><td>2 x 1,2,6, 12 or 1 x 24 bit</td></tr>
<tr><td></td><td>FPM-CSM</td><td>2 x 1,2,6, 12 or 1 x 24 bit</td></tr>
<tr><td></td><td>SM-SPM</td><td>8 x 1,2,6, 12 or 4 x 24 bit</td></tr>
<tr><td></td><td>SM-CSM</td><td>8 x 1,2,6, 12 or 4 x 24 bit</td></tr>
<tr><td>Pixel counters in CRW</td><td>FPM-SPM</td><td>1 x 1,2,6 or 12 bit</td></tr>
<tr><td></td><td>FPM-CSM</td><td>1 x 1,2,6 or 12 bit</td></tr>
<tr><td></td><td>SM-SPM</td><td>4 x 1,2,6 or 12 bit</td></tr>
<tr><td></td><td>SM-CSM</td><td>4 x 1,2,6 or 12 bit</td></tr>
</table>

Table 4-4: Performances of the Medipix3RX chip.

4.3.3 Applications using Medipix3

The charge summing correction algorithm, along with the high programmability per pixel, makes Medipix3RX suitable for many applications. For instance, synchrotron applications benefit from the high speed and the readout dead-time free operation of the ASIC. The high count-rate capability and the spectroscopic measurement using four thresholds per pixel benefit spectral CT imaging. MARS Bioimaging (MBI) was founded in 2007 for commercializing the Medipix3RX technology for human clinical imaging [93]. Figure 4.9 shows the color imaging of a wrist of a human subject using the MARS detector [94].

Some other applications using the Medipix3RX as readout systems are listed in Table 4-5. The number of readout chips and the material used for the sensor are indicated.

Applications	**Medipix3**	**Detector**	**Publications**
Electron microscopy	1	Si sensor 300 µm [h$^+$]	[95]
Non-destructive material analysis	1	Si sensor 300 µm [h$^+$]	[96]
Spectroscopic CT imaging	5x1	CZT sensor 2 mm [e$^-$]	[97] [93]
Low dose mammography imaging	1	CdTe sensor 1 mm [e$^-$]	[98]
Synchrotron imaging	6x2	CdTe sensor 1 mm [e$^-$]	[99]
	1	Si sensor 300 µm [h$^+$]	[100]
Study of sensor materials	1	GaAs sensor 500 µm [e$^-$]	[101]
Dosimetry	1	Si sensor 500 µm [h$^+$]	[102]
X-ray diffraction	3 x (2 x 8)	Si sensor 300 µm [h$^+$]	[103]
Radiation monitoring	1	Si sensor 300 µm [h$^+$]	[104]
Particle tracking at the CERN SPS experiment	1	Si sensor 300 µm [h$^+$]	[105]

Table 4-5: Some applications using the Medipix3 readout.

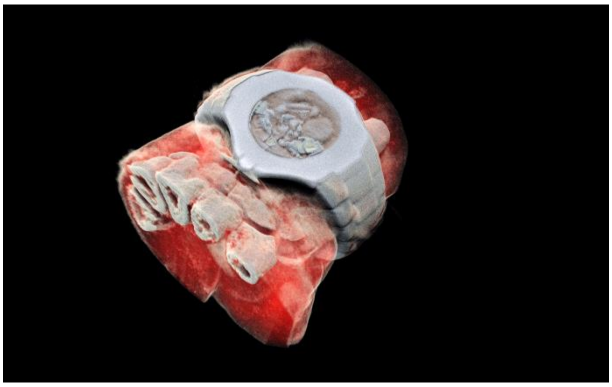


Figure 4.9. Color X-ray imaging of a wrist of a subject was obtained from the MARS detector using Medipix3RX as a readout system [97]. The bone, soft tissues, and metallic watch are identified.

4.3.4 Limitations of Medipix3RX and ideas for the design of Medipix4

In this section, the limitations of the Medipix3RX chip are discussed, and the motivations for the design of Medipix4 are explained. Many ideas were studied during the thesis to improve the limiting performances of Medipix3RX, but not all of them were finally implemented. The implementation of the Medipix4 chip and the design of the front-end pixel will be discussed in the last part of this thesis.

4.3.4.1 3-side buttable chip

Synchrotron and spectroscopic X-ray applications may potentially benefit from the possibility of achieving large sensitive areas with seamless integration. However, the traditional 3-side buttable architecture like in Medipix3RX contains a dead region in one edge where the wire bond pads connections and the peripheral circuit are located. This 3-side buttable configuration allows tiling of Application-Specific Integrated Circuits (ASICs) on three sides but limits their extension in the fourth direction. A new strategy has been adapted for the design of Timepix4 and Medipix4 to suppress the dead region at the edge and thus allowing the tiling of the ASICs seamlessly in both x and y directions. This 4-side buttability has been possible with the development of TSV (Through Silicon Via) technology. This process allows a 3D integration using the vertical axis for component integration [106]. The Input/Output connections can be made using the backside of the ASIC.

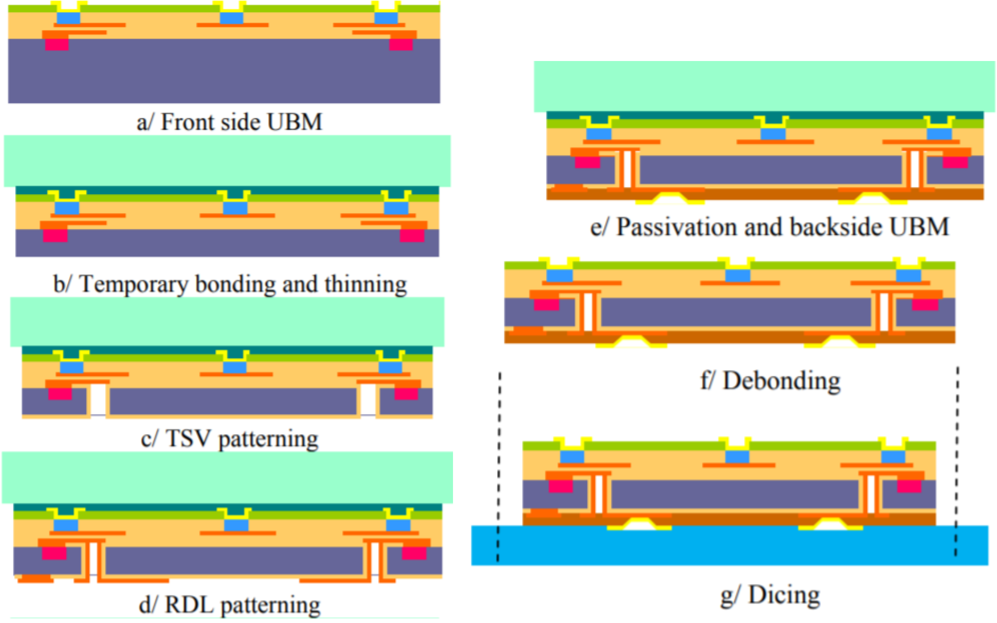


Figure 4.10. Process flow for the TSV last technology [106].

The process flow for the 3D integration using the TSV last technology is summarized here and illustrated in Figure 4.10, and a more detailed description can be found in [106]:

- Step 1: An Under Bump Metallization (UBM) is deposited on the bonding pads of the pixel arrays.
- Step 2: The front side of the wafer is bonded to a dummy wafer using temporary adhesive. The backside of the wafer is thinned by silicon grinding and polishing to obtain a thickness of 120 µm (which corresponds to a ratio of 2:1 with respect to the ~60um TSV).
- Step 3: A Deep Reactive Ion Etch (DRIE) Bosch process is carried out to obtain the 120 µm deep TSV cavities. Then, an insulation oxide layer is deposited to obtain a full insulation of the TSV sidewalls. Finally, a Reactive Ion Etch process removes the oxide layer at the bottom of the cavity and reveals the landing pads. The landing pads must be designed on the ASIC using the Metal 1 of the technology.
- Step 4: Redistribution Layer (RDL) to redistribute all input and output signals of the chip uniformly on the backside of the wafer. Using a sputtering technique (Physical Vapor Deposition), a thin layer of 5 µm is deposited accordingly to the design of RDL.
- Step 5: The backside of the wafer is covered by a polymer layer that passivates the copper lines. Ball Grid Array (BGA) contacts are deposited using the UBM metallization on the backside. The BGA replaces the wire-bonding Input/Output (I/O) pads.
- The dummy wafer is debonded from the main wafer. The latter is ready for further dicing and flip-chip assembly.

The I/O pads in Medipix3RX have been designed to be “TSV ready”, which means landing pads have been placed in Metal 1 for integration of the TSVs [107]. Figure 4.11 shows the lateral view of a Medipix3RX ASIC bonded to a 200 µm thick sensor, with the wire bonds connections at the left. The bottom view shows the chip connected to a 500 µm thick sensor and processed with TSV technology. The wire bond connections are replaced by BGA connections at the backside of the ASIC. The total active area goes from 88.4% to 94.3% of the total chip area [11].

In order to achieve a full sensitive active area and seamless, the periphery circuitry of the chip must be placed beneath the sensor material [108]. This means the readout pixel is slightly smaller than the sensor pixel in one dimension to accommodate the area needed for the periphery. Moreover, another Redistribution Layer (RDL) is required on the top of the ASIC to connect the sensor pixel to the readout pixel.

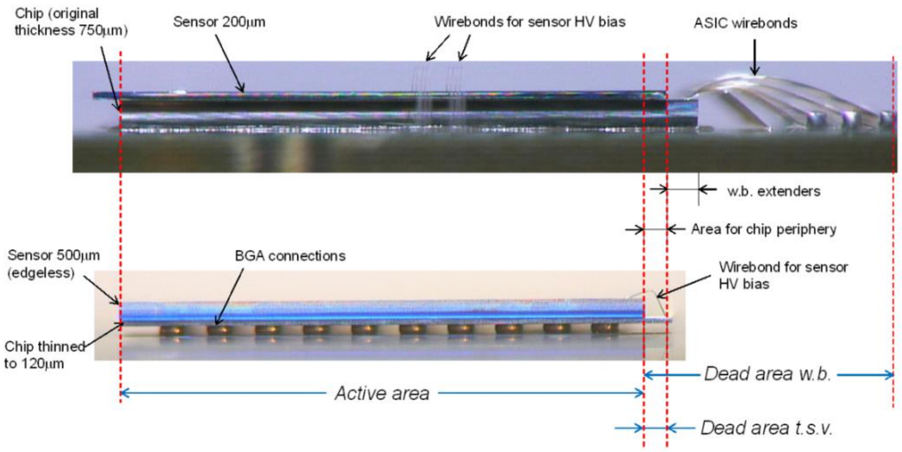


Figure 4.11. Lateral view of the Medipix3RX on chipboard (Top). The bottom view shows the Medipix3RX chip after TSV processing and connecting to the chipboard using BGA [13]**.**

4.3.4.2 Small pixel size

The 110 µm sensor pixel in Medipix3 configured in Charge Summing Mode (CSM) does not register all the fluorescence photons generated in high-Z materials. The fluorescence peaks in the CdTe sensor have a mean free path of around 110 µm, which escapes from the main collection pixel (including the reconstruction area in the case of programming in CSM). Those peaks in the fluorescence are measured in [109] using a 2 mm thick CdTe sensor and photon energy of 60 keV. The measured spectrum is shown in Figure 4.12. The CSM mode permits the suppression of the low-energy tail of the charge sharing between pixels. The Cd and Te characteristics at 23 keV and 27 keV, respectively, are still visible on the measured spectrum. In addition, there is a peak around 35 keV associated to the escape peak, which is the energy that escaped from the main pixel.

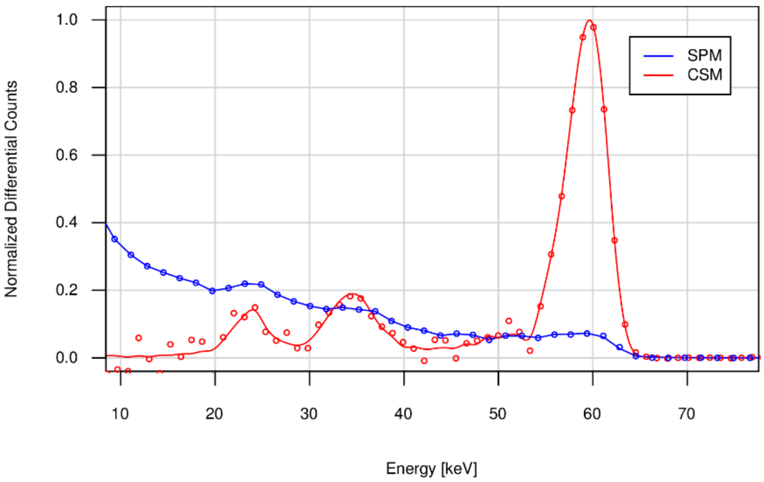


Figure 4.12. the measured spectrum of a 60 keV input source on a 2 mm thick CdTe sensor using Medipix3RX in SPM (blue) and CSM (red) [109].

That is the reason why a pixel pitch of 75 µm is chosen for the readout pixel of Medipix4, allowing a larger collection area of 300 x 300 µm² in SM-CSM.

4.3.4.3 Limited dynamic range

Medipix3RX has a linear dynamic range of up to 100 keV with a CdTe sensor. Some applications like medical X-ray imaging require a good linearity for Medipix4 up to 160 keV.

Using passive components to set the gain of the pixel is the most robust and reliable solution compared to active components. Indeed, the gain of the analog pixel in Medipix3RX is determined by the transconductance value of the input transistor in the semi-gaussian shaper illustrated in Figure 4.13 [11]. The current flowing in the shaper is a critical parameter determining the gain of the pixel. That means a good matching in the current of the shaper is required to minimize the pixel-to-pixel gain variation.

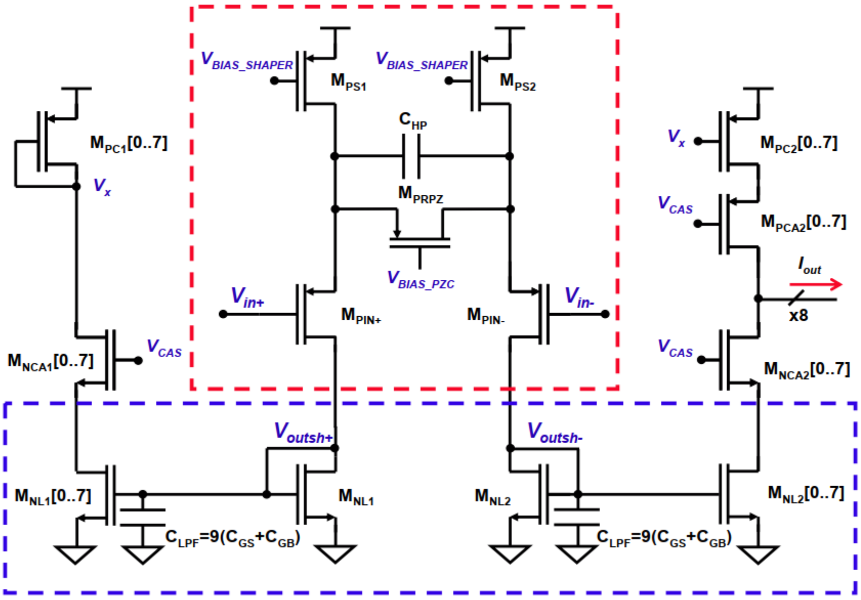


Figure 4.13. Semi-gaussian shaper implemented in the analog pixel of Medipix3RX [11].

4.3.4.4 Limited count-rate capability

Some applications like Computed Tomography (CT) or X-ray applications in synchrotrons require a very high count-rate capability of the pixel detector [110]. The users of Medipix3RX highlighted that a factor four improvement in the count-rate would bring many benefits in the future for clinical imaging. However, the count-rate is inversely proportional to the area of the pixel sensor [12]; the increase of the pixel size from 55 µm to 75 µm does not help to improve the count-rate capability.

However, the increase in the pixel size allows the implementation of more complex circuitry including a pole-zero-cancellation using passive components. The undershoot produced by the differentiation of the slow decay of the CSA in the shaper can be suppressed using an accurate pole-zero cancellation. The semi-gaussian shaper used in the pixel for Medipix3RX shown in Figure 4.13 has the advantage of using only a few transistors to implement the shaping of the signal and to generate copies for the charge-sharing algorithm. Nevertheless, it has the disadvantage of inducing a baseline drift for high flux applications due to AC coupling between the shaper and the CSA. The pole-zero cancellation implemented in the shaper for Medipix3RX must be carefully set to match its zero to the pole in the CSA, which depends on the current I_{krum}.

Moreover, the peaking time of the output signal of the front-end in Medipix3RX is around 110 ns [11]. The transconductance values for the input transistors in the shaper are limited to two values for a given current in the shaper. The implementation of a configurable shaping time for the shaper in Medipix4 will permit the improvement of the count-rate capability per pixel.

4.3.4.5 Energy resolution

The energy resolution measures the ability of a pixel detector to separate two peaks close in energy. The energy resolution for the Medipix3RX has been measured in [109] [54] using a 60 keV input photon with a 110 µm pixel pitch and in Charge Summing Mode. The energy spectrum has an FWHM of 4.4 keV. Material identification and CT imaging applications will benefit from Medipix4 by improving the energy resolution of the system by a factor of two compared to Medipix3RX.

The pixel-to-pixel threshold variation is one of the sources of degradation in the energy resolution. The threshold variability comes from the offset and gain mismatch in the analog processing circuitry. When setting the threshold well above the background noise, the pixel-to-pixel gain mismatch has an important impact on the energy resolution. The gain mismatch affects a charge shared and a non-charge shared hit differently [108]. By simulating the energy spectrum of a 60 keV monochromatic input source added to a readout electronic noise of 100 e^-, an offset dispersion of 100 e^- rms, and a gain mismatch of 3% rms, the energy resolution is estimated to 4.4 keV in FWHM. The simulated spectrum in Figure 4.14 matches the measured performances of Medipix3RX. By decreasing the gain mismatch to 1 % rms, the FWHM of the energy spectrum is reduced to 2.05 keV, as is shown in Figure 4.15.

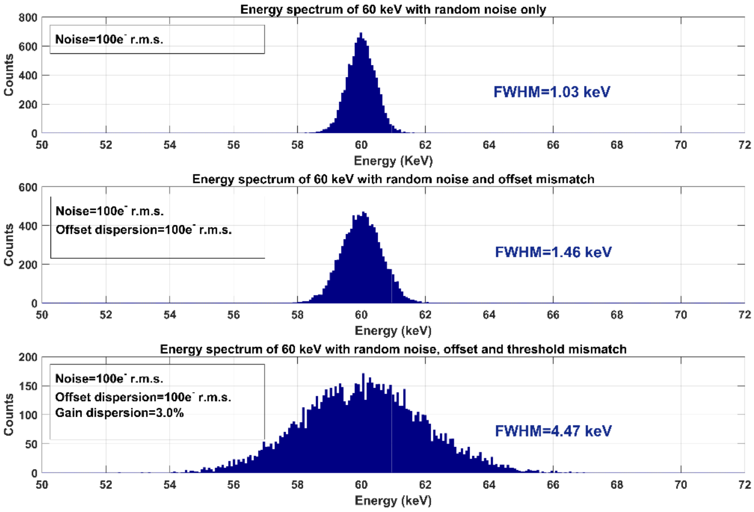


Figure 4.14. The energy spectrum of a 60 keV monochromatic source, adding the readout noise of 100 e^- rms, the offset mismatch of 100 e^- rms and the gain mismatch of 3%. The energy spectrum has a FWHM of 4.47 keV [108].

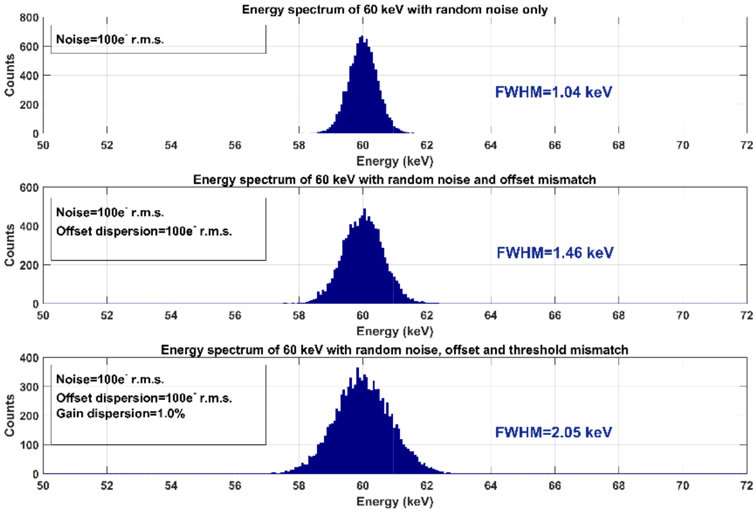


Figure 4.15. The energy spectrum of a 60 keV of a monochromatic source, adding a readout noise of 100 e-, offset mismatch of 100 e- rms, and a gain mismatch of 1% rms. The FWHM is 2.05 keV [108].

The idea of using a gain calibration circuit has been studied in [108]. Using a small trimming capacitance (less than 1 fF) in parallel to the feedback capacitance could reduce the gain mismatch to 1%. However, the limited area in the analog pixel did not allow this implementation. The gain mismatch is still improved with respect to Medipix3RX; this comes from the use of passive components to set the overall gain. The gain mismatch has been simulated at around 1.5 % rms.

4.3.4.6 Number of thresholds in Spectroscopic Mode

Multiple energy thresholds in the same analog processing pixel permit to sample different windows of the energy spectrum simultaneously. Most ASICs used for material analysis or CT imaging implement multiple thresholds with associated counters for readout. A large pixel area is an inevitable consequence to implement those energy bins. For example, the ERICA chip had 6 energy thresholds in a 330 µm pixel pitch [90]. The ChromAIX2 chip, designed by Philips for human CT imaging, has 5 energy bins in a 500 µm pixel pitch [52]. The Dosepix chip designed at CERN contains 16 digital energy thresholds in a pixel pitch of 220 µm [40], [111], [112].

Medipix3RX in Spectroscopic Mode (SM) using 110 µm pitch sensor pixel has 8 thresholds in SPM and only 4 in CSM. The CSM mode in Medipix3RX has four thresholds used for the local charge arbitration, but only one is required to fulfill that process algorithm. We propose in Medipix4, to keep two thresholds per pixel in Fine Pitch Mode (associated to sensor pixels of 75 µm pitch). However, in Spectroscopic Mode (SM) and Charge Summing Mode (CSM), only one threshold is used for the local charge arbitration. The remaining seven are used to sample the energy spectrum reconstructed by the summing circuit. This is possible by configuring the comparators and their associated thresholds in four modes of operations (FPM-SPM, FPM-CSM, SM-SPM and SM-CSM).

4.3.4.7 Readout

The 24-bit registers in Medipix3RX allow the readout of one threshold at a time in CRW. The increase in the pixel area for Medipix4 benefits the readout of all thresholds at the same time in CRW, using 48-bit registers for counting in the digital pixel. Indeed, for each threshold, one 12-bit counter stores the number of pulses while the readout is done through the other 12-bit counter.

In addition, the counting in Medipix3RX is not optimized for low-energy bins. Indeed, a high-energy photon triggering all the comparators in the pixels leads to increasing all the counters associated with those comparators. This means the lower energy bins fill up fast with respect to the higher bins. The 'Window discrimination threshold' implemented in Medipix2 could be the solution to optimize the dynamic range of the lower energy bins.

4.4 Summary and specifications for the design of Medipix4

The chapter summarizes the Medipix family of chips designed over 20 years with successive Medipix Collaborations. The expertise acquired from the design of hybrid pixel detectors for high-energy physics encouraged the formation of the first Medipix Collaboration in view of the design of the Medipix1 chip. This chip demonstrated the possibility of X-ray imaging using single-photon counting systems. The Medipix2 Collaboration was formed in view of exploring the spectroscopic imaging with a small pixel pitch of 55 µm. The Medipix2 proved the possibility of spectroscopic imaging using two thresholds per pixel. However, a degradation of the energy spectrum was measured due to charge sharing between pixels and fluorescence photons in high-Z materials. The Medipix3 Collaboration was formed in 2005, for the design of Medipix3 with the aim of developing a large area chip for spectroscopic measurement and having a charge sharing correction algorithm. The limitations of the latest version of Medipix3 called 'Medipix3RX' were analyzed in this chapter, and solutions were proposed in view of the design of Medipix4. Table 4-6 summarizes the performances required by the Medipix4 Collaboration for the Medipix4 ASIC.

Technology		130 nm CMOS technology
		9 metal layers
Pixel size	FPM	75 x 75 µm^2
	SM	150 x 150 µm^2
Number of pixels	FPM	320 x 320
	SM	160 x 160
Sensitive area		5.76 cm^2
Equivalent Noise Charge	SPM	< 100
[e$^-$] r.m.s.	CSM	< 200
Dynamic range [ke$^-$]		Up to 32
Count-rate (10% dead time loss) [Mphotons.mm-2s-1] 60 keV input / Vth = 30 keV	SM-CSM	17.2
Energy resolution with input 60 keV source [keV]	SM-CSM	2.2
Number of thresholds	FPM-SPM	2
	FPM-CSM	1 SPMa + 1 CSM
	SM-SPM	8
	SM-CSM	1 SPMa + 7 CSM
Matrix arrangement		4 side buttable
Pixel counters in SRW	FPM-SPM	2 x 1,2, 12 or 24 bit
	FPM-CSM	2 x 1,2, 12 or 24 bit
	SM-SPM	8 x 1,2, 12 or 24 bit
	SM-CSM	8 x 1,2, 12 or 24 bit
Pixel counters in CRW	FPM-SPM	2 x 1 or 12 bit
	FPM-CSM	2 x 1 or 12 bit
	SM-SPM	8 x 1 or 12 bit
	SM-CSM	8 x 1 or 12 bit

Table 4-6: Specifications for the design of the Medipix4 ASIC.

Chapter 5 Timepix family of chips

In 2005, the idea of using Medipix2 ASIC for gas detector readout was proposed. The goal was to record the position of individual electrons produced by an ionizing particle in a gas volume [5][79]. The setup is presented in Figure 5.1, showing that when a charged particle crosses a drift gas volume, photo-electrons are generated and drift along the electrical field lines towards a gas gain grid. The latter is implemented as a stack of three Gas Electron Multiplier (GEM), multiplying the charge and sending the cloud of charges to the readout Medipix2. This experiment demonstrated that single particles could be detected from a 3D projection, but the Medipix2 ASIC did not provide the time of arrival or the quantity of charge deposited per pixel. The first idea by J. Visschers, J. Jakubek, and X. Llopart on “Count arrival time by adding a clock in pixel” motivated the design of a new ASIC to track particles in a 3D volume [113]. The modified chip was called Timepix because each pixel provides the Time of Arrival (TOA) information or the Time-over-Threshold (TOT), which allows measuring the total charge deposited. Many chips followed the first Timepix (section 5.1), called Timepix3 (section 5.2), then Timepix2 (section 5.3), and recently Timepix4 (section 5.4). The idea with the Timepix family of chips is to extract the maximum of information about the ionizing particle in the semiconductor material or gas volume. The downscaling of the CMOS processes allowed improved performances in each new generation of the ASIC.

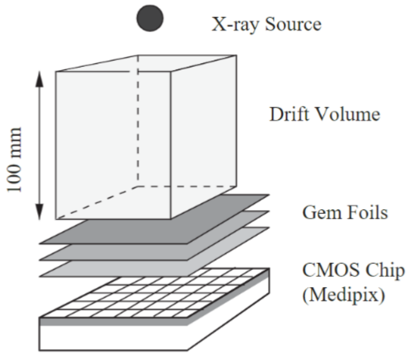


Figure 5.1. The structure of a Time Projection Chamber (TPC) with a 100 mm drift volume and using a stack of three Gas Electron Multiplier (GEM) and a Medipix2 chip for readout [79].

5.1 Timepix

5.1.1 Architecture

Timepix chip has a floorplan directly derived from Medipix2; it contains 256 x 256 pixels having a size dimension of 55 x 55 µm². The pixel cell is slightly different than in Medipix2. The gain in the CSA is improved by adding a cascode stage in the operational amplifier. There is a single threshold with a 4-bit threshold calibration DAC per pixel. Compared to the 3-bit threshold calibration DAC in Medipix2, the extra bit for the threshold calibration and the improvement of the amplifier's gain permits achieving a minimum detectable charge of 600 e^- [37]. The area gained from the suppression of one discriminator and its associated calibration DAC allows the integration of a more complex digital processing in the digital part of the pixel than in Medipix2. The block diagram of the Timepix pixel is shown in Figure 5.2. The pixels can be configured in three different modes of operation through the registers P0 and P1. In Particle Counting (PC) mode, each event above the threshold increments the counter value. The counter is incremented using the counting clock in TOT mode as long as the preamplifier's output voltage is above the threshold. In this mode of operation, the total deposited charge information can be extracted because the TOT (or pulse width of the CSA) is linear with the input charge. In TOA mode, the counter starts counting from the rising edge of the comparator until the closing of the global shutter. Those modes of operation are illustrated in Figure 5.3.

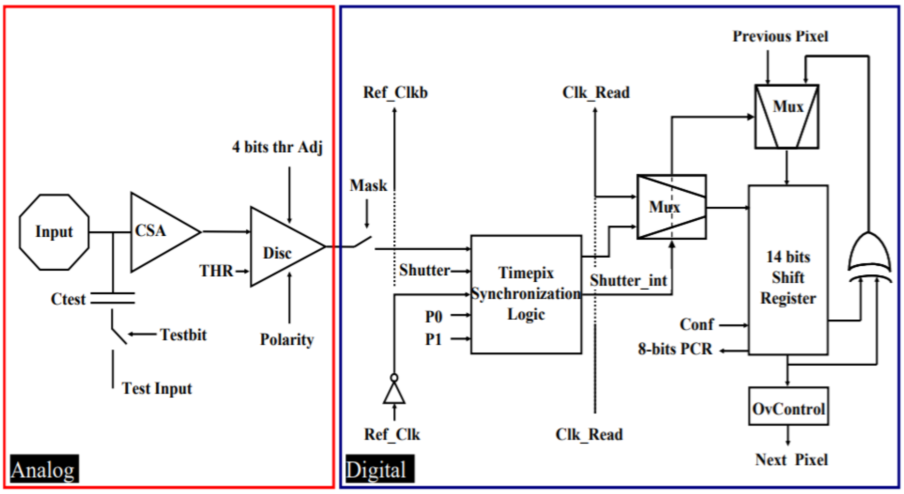


Figure 5.2. Block diagram of the Timepix pixel cell [37].

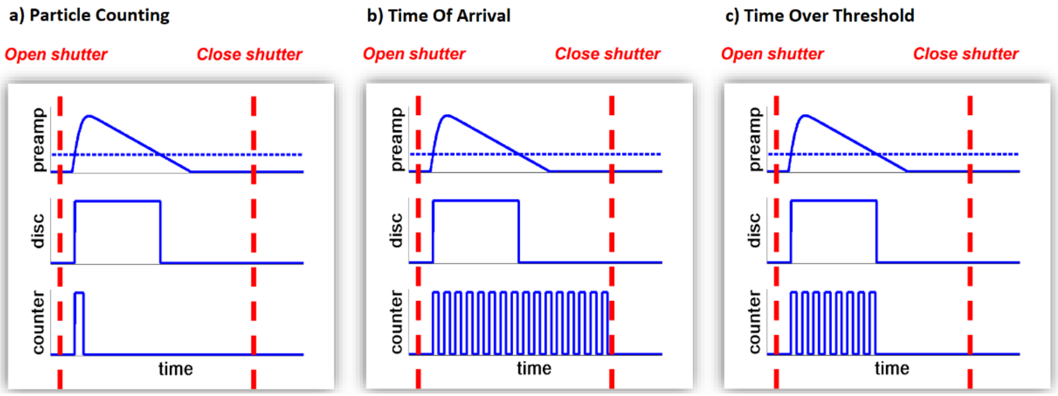


Figure 5.3. Illustration of the working principle of the different modes of operation in Timepix chip. The chip can be configured in (a) Particle Counting mode (PC), (b) Time of Arrival mode (TOA), and (c) Time over Threshold mode (TOT) [113].

5.1.2 Some applications

Detectors with the Timepix readout have become widely used in multiple applications [5]. This is because Timepix chips can read out the signals from semiconductor radiation detectors, and they can read out the signals from detectors like Gas Electron Multipliers (GEMs) or Micro Channel Plates (MCPs). Timepix chips have been assembled with a miniaturized USB readout system, and are designed to be user-friendly, which facilitates the use of Timepix chips in many applications [114]. Some applications are listed in Table 5-1; the semiconductor material and the number of readouts are indicated.

Applications	**Timepix**	**Detector**	**Publications**
Analysis of paint arts	1	Si sensor 300 µm $[h^+]$	[115]
	10 x 10	Si sensor 300 µm $[h^+]$	[116]
Space dosimetry	1	Si sensor 300 µm $[h^+]$	[117] [118]
Education purposes	1	Si sensor 300 µm $[h^+]$	[119] [120] [121]
Radiological safety and homeland security	1	CdTe sensor 1 mm $[e^-]$	[122]
Adaptive optics	2x2	Microchannel Plate(MCP) $[e^-]$	[123]
Time-of-Flight mass spectrometer	2x2	Microchannel Plate(MCP) $[e^-]$	[124]
Real-time radiation monitor by mobile robot	1	Si sensor 300 µm $[h^+]$	[125]
Detection of fast neutrons	1	Si sensor 300 µm $[h^+]$	[126]
	2	Si sensors 300 µm and 500 µm $[h^+]$	[127]
Ion beam therapy	1	Si sensor 300 µm $[h^+]$	[128]
Proton imaging	1	Si sensor 300 µm $[h^+]$	[129]
Positron emission tomography	2x2	Si sensor 300 µm $[h^+]$	[130]
GEMPIX for ^{55}Fe waste management	2x2	Gas Electron Multiplier	[131]
GEMPIX dosimeter for hadron therapy	2x2	Gas Electron Multiplier	[132]
CAST experiment for axions	1	InGrid structure as gas amplification	[133]
Beam monitoring in UA9 experiment at CERN	1	Si sensor 300 µm $[h^+]$	[134]

Table 5-1: Some applications using Timepix readout. The size of the detector and the material used for the sensor are highlighted.

5.1.3 Limitations and motivation for the design of Timepix3

The use of Timepix in many applications highlighted some limitations of the chip. For instance, the use of Timepix with the GEM-TPC shows that the longitudinal resolution is degraded due to a small drift in the gas volume. A better time resolution of less than 10 ns would improve the longitudinal resolution for particle tracking in InGrid applications [135]. One can argue that the charge diffusion in the gas volume still degrades the longitudinal resolution. The frame-based readout in Timepix, where the pixels are insensitive during the readout phase, is a limitation for the applications requiring a dead-time-free operation. Moreover, the TOA information obtained from the number of clock cycles between the firing of the comparator and shutter closing limits the shutter's opening time to the dynamic range of the 14-bit LSFR. In addition, the power consumption increases if many pixels are fired simultaneously, which is a limitation when operating at high rates. One of the main limitations of Timepix is that pixels must be configured in either charge measurement (TOT), time measurement (TOA), or photon counting mode. Some applications may benefit from having both time and charge information simultaneously [117]. The TOT information can be used to correct the time-walk (caused by the different slope of signals with different amplitudes) in TOA measurements [136]. Those limitations encouraged the Medipix3 Collaboration to fund the design of Timepix3. Engineers from the microelectronic group at CERN worked together with Nikhef and the University of Bonn to design the Timepix3 ASIC.

5.2 Timepix3

5.2.1 Architecture

Timepix3 was implemented using a 130 nm CMOS process allowing more complex digital features than its predecessor Timepix does. The chip has the same pixel arrangement as Timepix, as an array of 256 x 256-pixel elements with a size dimension of 55 x 55 µm². The block diagram of the pixel is represented in Figure 5.4. The analog front-end is based on a Krummenacher scheme with a feedback capacitance of ~3 fF. Such a small capacitance value provides a gain of ~50 mV/ke$^-$, which reduces the comparator's impact on the overall mismatch. The amplifier saturates at 12 ke$^-$, which is not an issue for Timepix chips. The information about the events is extracted from the pulse's width rather than its amplitude. This is because the feedback capacitor continues to integrate the charge even beyond the linear range of the preamplifier output amplitude. A detailed description of the analog pixel can be found in [137]. The digital pixel can be configured in three acquisition modes: Charge and time information, photon counting and charge integration, or just the time information. The digital pixel contains a 40 MHz counting clock. A block called "digital superpixel" common to 2 x 4 pixels contains a Voltage-Controlled Oscillator (VCO) running at 640 MHz. This VCO permits a time bin of 1.56 ns, which benefits applications for particles tracking [138]. The VCO is started at the rising edge of the comparator output, oscillates with a frequency of 640 MHz, and stops at the next rising edge of the 40 MHz counter clock. The number of oscillations of the VCO is counted on a 4-bit fine time stamp counter FTOA. There are three different packet formats in the digital pixel of Timepix3 using 28-bit registers, of which 14 bits are used for the time information at 40 MHz and can be improved using the 4 bit of the FTOA. The TOT information is recorded in a 10-bit counter at 40 MHz. A request signal is sent from each pixel having recorded an event to the superpixel to transfer the data later.

The 28-bit data are shifted to the deserializer in the superpixel and are written in a buffer for readout. The buffer can store two data events, which significantly reduces the redout dead-time of the digital pixel front-end [38]. The readout dead-time to send the digital information from the pixel to the superpixel is 475 ns. Each superpixel can access the column bus for readout using a token ring arbitration scheme. In total, 44-bit length information is sent off-chip for each incoming hit. The readout can be configured in frame-based mode as in Timepix, where the data stays in the pixel until the readout request and in data-driven mode. In the latter, the data is sent immediately off-chip when one of the pixels sees an event. More details on the implementation of the Timepix3 can be found in T. Poikela's thesis [139].

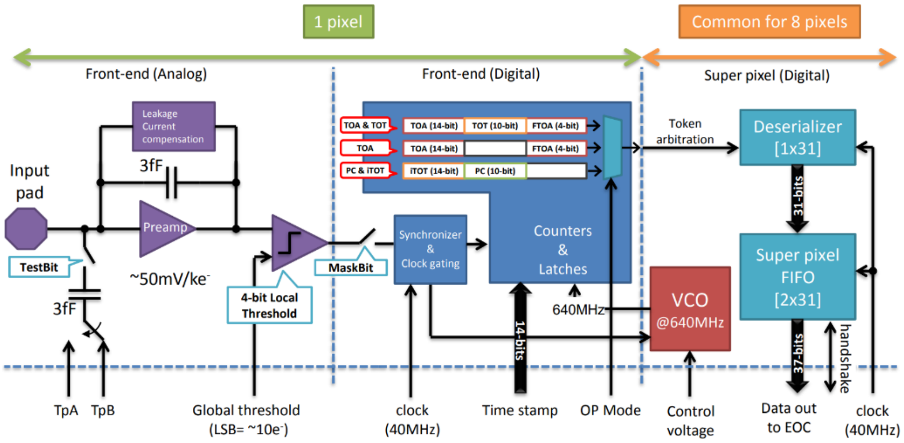


Figure 5.4. Block diagram of the Timepix3 pixel cell [38] [139].

5.2.2 Some applications

Many applications benefit from the use of Timepix3, taking advantage of the time bin of 1.56 ns or the data-driven mode capable of treating up to 80 Mhit per second per chip. Some applications using Timepix3 as a readout system are listed in Table 5-2, along with the sensor's material.

Applications	Timepix3	Detector	Publications
Compton camera	1	CdTe sensor 2 mm [e$^-$]	[140]
Adaptive optics	1	Microchannel Plate(MCP) [e$^-$]	[141]
Beam profile monitor for CERN proton synchrotron	4x1	Si sensor 300 µm [h$^+$]	[142]
Particle tracking	4x1	Si sensor 500 µm [h$^+$]	[143]
Radiation monitor for space application	1	Si sensor 300 µm [h$^+$]	[144]
X-ray phase-contrast imaging	1	CdTe sensor 500 µm [e$^-$]	[145]
Gamma imaging	1	CdTe sensor 1 mm [e$^-$]	[146]
Positron emission tomography	2	CdTe sensor 2 mm [e$^-$]	[147]
Anti-matter research	1	Si sensor 675 µm [h$^+$]	[148]
Transmission electron microscopy	1	Si sensor 500 µm [h$^+$]	[149]

Table 5-2: Some applications using Timepix3 readout. The size of the detector and the material used for the sensor are highlighted.

5.3 Timepix2

5.3.1 Architecture and motivation

Timepix2 was designed after the Timepix3 chip and intended to replace the Timepix chip and is aimed for some particular applications requiring measurement in the mixed radiation field. The chip is funded by the Medipix2 Collaboration and designed at CERN using a 130 nm CMOS process. It contains an array of 256 x 256 pixels on a pitch of 55 µm, like in the Timepix chip. The block diagram of the pixel, illustrated in Figure 5.5, contains an analog processing circuit composed of a CSA based on the Krummenacher topology [36]. The gain of the analog pixel can be configured in two modes: Fixed Gain Mode or Adaptive Gain Mode. In the first mode, the gain is fixed at 25 mV/ke$^-$ using a metal plate capacitance. In Adaptive Gain Mode, the CSA has an additional varying capacitance defined by a MOS capacitor in which the gate is connected to the input of the front-end [150]. In this mode, the gain decreases for the high input charges, allowing an extended TOT up to 950 ke$^-$ [151]. A comparator follows the CSA and a 5-bit trimming DAC for threshold adjustment. The output of the comparator is fed to the digital pixel implementing the new features required for this chip. The chip can operate simultaneously in TOA and TOT like Timepix3 or photon counting mode. There are 8 digital operation modes, where the TOT, TOA, and PC can be configured with different counter depths. The modes are detailed in [151]. A new feature implemented for Timepix2 concerning Timepix/Timepix3 is the “continuous Read/Write” mode allowing the pixels to be sensitive to the incoming hits during the readout phase. The power consumption is optimized in Timepix2, allowing to turn off unused pixels, for instance, when a sensor material with a pixel pitch of 110 µm is bonded to the readout system.

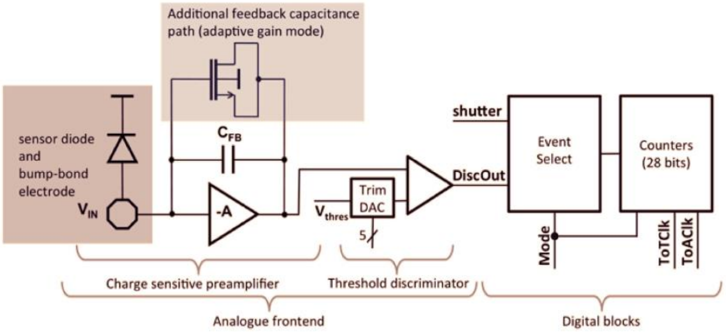


Figure 5.5. Block diagram of the Timepix2 pixel cell [151].

This chapter will explain a Rail-To-Rail (RTR) buffer, which was designed to monitor the output of the CSA and the design of the analog periphery of the Timepix2 chip.

5.3.2 Design of a fast Rail-to-rail buffer for monitoring the front-end of a pixel

Some applications using Timepix detectors operating in hole collection showed a loss of the total measured energy resolution due to the “volcano effect” [152]. In the Timepix2 chip, to better understand this effect, the output of the preamplifiers in the last row of the pixel matrix is buffered and can be monitored on the chipboard [151]. The amplifier needs to achieve total linearity along with the common-mode input voltage. For this reason, a Rail-to-Rail (RtR) buffer is implemented.

5.3.2.1 The architecture of the RtR buffer

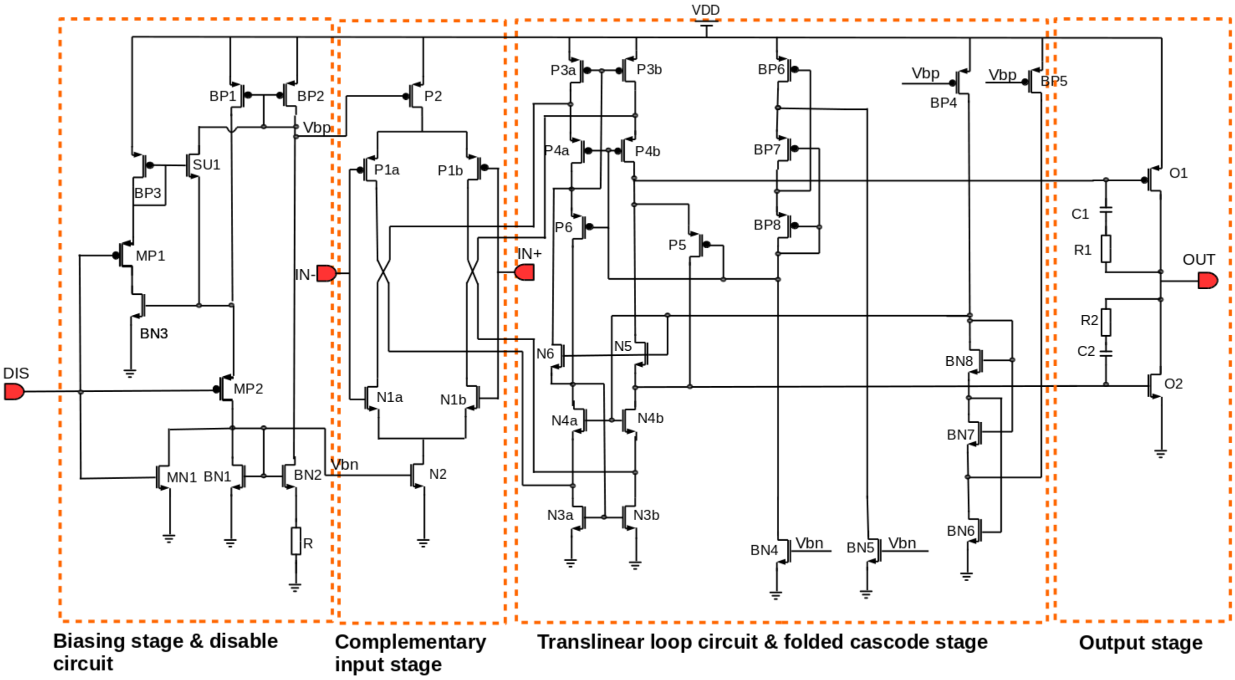


Figure 5.6. Architecture of the RtR buffer achieving full linearity. The circuitry is self-biased using a beta-multiplier topology.

This topology studied in [153], was adapted to this design and optimized for fast monitoring of the front-end’s signal. The overall circuit is shown in Figure 5.6. The operational amplifier comprises four parts: the biasing part, complementary input stage, a folded cascode stage, and a class-AB output stage.

The biasing stage consists of a beta-multiplier voltage reference circuit [154]. There are two stable operating states for this self-biased circuit: the desirable one and the unwanted one, where no current flows in the reference circuit. A start-up circuit composed of the transistors BP3, BN3, and SU1 allows the current to shift to the desired state when the circuit is turned on.

A PMOS and NMOS differential pairs are implemented to obtain a complementary operation. Indeed, the PMOS differential pair will be working for a low common-mode input voltage, and the NMOS transistors are off. In the case of high common-mode voltage, the NMOS pair will be working, and the PMOS is off. This configuration results in a variable transconductance, affecting the stability in the region where both pairs are working [155]. There are some strategies to equalize the buffer's transconductance. The challenges for the compensation due to the variable transconductance were studied in [156]. However, those schemes were not implemented in this design, and the stability of the buffer has been carefully analyzed in the mid-region where both pairs are working.

The folded-stage presented in Figure 5.6 is called folded cascode current summing stage. It adds the currents coming from the complementary stage and then provides a voltage to the output stage. This summing circuit comprises PMOS and NMOS current stage, respectively represented by P3a/P3b and N3a/N3b. There is also a quiescent control circuit in this summing stage, consisting of the transistors N5, N6, P5, and P6. This circuit, also called a "translinear loop," sets a constant voltage between the gates of the output transistors. A constant voltage between their gates permits the output transistors O1 and O2 to operate in class-AB. In addition, this configuration prevents one of the transistors at the output from going off when the other one is carrying a large current.

The output stage operates in AB class, which is a good trade-off between class A and class B and has small distortion and power consumption. The output stage contains miller compensation capacitances in series with a resistor connected between the gate and the drain of each output transistor to ensure the amplifier's stability. This compensation technique called "nulling resistor" permits to push off the zero of the transfer function towards higher frequencies and thus improves the stability of the buffer.

5.3.2.2 Simulated results

The buffer has been designed with relatively high-power consumption (~680 µW) to achieve a fast settling time required to follow the signal generated by the analog pixel for an incoming event. Figure 5.7 shows the simulated response after post-layout extraction of the output of the analog pixel and the signal monitored by the RtR buffer for input energy of 6 ke$^-$. The block has a width dimension of 30.5 µm to fit in the periphery of the matrix at the same pitch as the pixel size of 55 µm. Table 5-3 summarizes the post-layout performances of the RtR buffer. Those buffers can be turned off when monitoring is not required, which optimizes the overall power consumption of the chip. The enable activation time refers to the time required to turn on the buffer to monitor the signal.

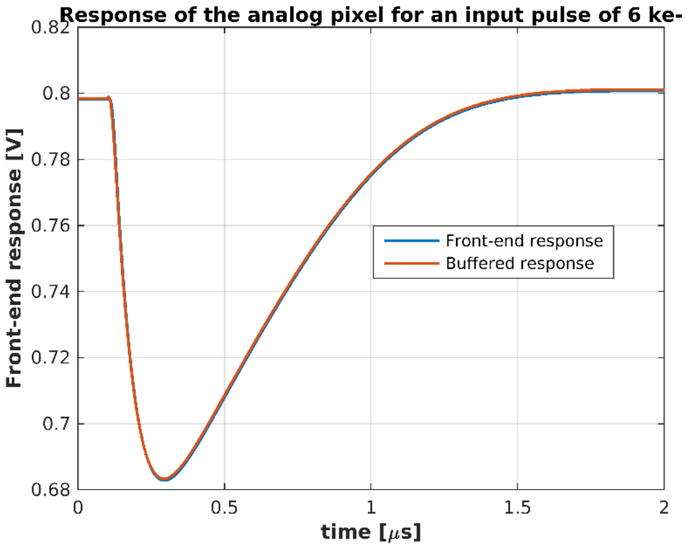


Figure 5.7. Front-end response of the pixel in bleu for an input charge of 6 ke$^-$ and the output signal monitored by the RtR buffer in red.

Parameters	Simulated performances
CMOS technology	TSMC 130 nm
Supply voltage	1.2 V
Linearity range % (< 1 mV)	99 %
Load capacitance	7 pF
Phase margin	Nominal case: 80 Worst case corner: 68
Input referred offset (r.m.s)	< 1.4 mV
Settling time	Nominal case: 14.5 ns Worst case corner: 36.9 ns
Area layout	182 x 30.5 µm²
Power consumption	680 µW
Gain / Unity Gain Frequency	68 dB / 72 MHz
Enable activation time	500 ns

Table 5-3: Simulated performances of the Rail-to-Rail buffer after post-layout extraction.

5.3.3 Voltage and current DACs for the periphery

The analog periphery block contains 7 voltage Digital to Analog Converters (DACs), 8 current DACs, and a bandgap circuitry. Voltage DACs provide a reference voltage to the pixel matrix. The current DACs provide a reference current using a diode-connected configuration at its output. The bandgap circuit provides a reference voltage that is very robust against temperature change and power supply variation. Gate leakage from the 66000 target transistors can induce a fluctuation in the accuracy of the biasing of the DACs. Therefore, an RtR buffer is implemented at the output of each DAC to isolate them from the array of pixels. Any fluctuation in the pixels will not influence the reference voltage due to the compensation of the feedback loop in the buffer. Most of the DACs can be programmed using 8-bit registers, 10 bit for the Vanalog2 used for the test pulse calibration, and 14 bit for the threshold voltage of the pixel. Table 5-4 summarizes the list of DACs in the periphery of Timepix2, along with the nominal value required in the target transistor and the full range of the DAC. The output transistors in the DAC “VBiaskrum” are drawn as ELT (Enclose Layout Transistor) to suppress the drain leakage current and ensure a correct biasing of the target transistor by the small current of 2 nA [11]. The nominal value for the current DACs is set around 30% of the full range, allowing further optimization by the future Timepix2 user for a given application. In addition, 4-bit DACs allow the biasing of the analog pixels that are masked with a small quiescent current that permits to maintain the operation of the DC leakage current compensation network in the CSA while at the same time, minimizing the overall power consumption of the chip. The layout of the analog periphery is shown in Figure 5.8; the size dimension of the block is 3550 x 664 µm².

BLOCK	DAC name	Bits	Type | PMOS	Nominal value	DAC full range
CSA	Vanalog1	8	Voltage		
	Vanalog2	10	Voltage		
	VBiasPreampPMOS	8	Current | PMOS	1.5 µA	4 µA
	VBiasPreampPMOS_stb	4	Current | PMOS	100 nA	1 µA
	VBiasPreampCasc	8	Voltage	370 mV	
	VGND	8	Voltage	750 mV	
	VBiasLevelShifter	8	Current | PMOS	2 µA	6 µA
	VBiasLevelShifter_stb	4	Current | PMOS	50 nA	1 µA
	VFBK	8	Voltage	800 mV	
	VBiaskrum	8	Current | NMOS ELT	2 nA	100 nA
COMPARATOR	VTH	14	Voltage	780 mV	
	VBiasDiscPMOS	8	Current | PMOS	750 nA	3 µA
	VBiasDiscNMOS	8	Current | NMOS	1 µA	4 µA
	VBiasCascDisc	8	Voltage	600 mV	
DAC	VBiasDAC	8	Current | NMOS	15 nA	200 nA

Table 5-4: List of voltage and current DACs in the periphery of Timepix2.

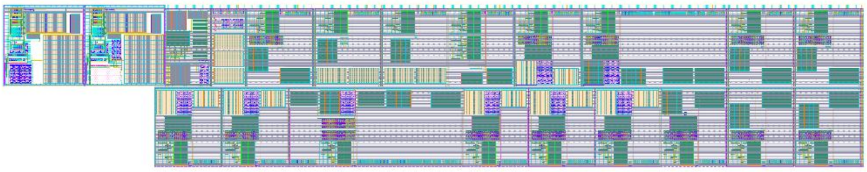


Figure 5.8. Layout of the analog periphery block containing 7 voltage DAC, 8 current DACs, and bandgap circuit. The size dimension of the block is 3550 x 664 μm^2.

5.3.4 Few measurements result from Timepix2

The chip was sent to fabrication in 2019, and the first tests were carried out at CERN. The Timepix2 was connected with bump bonds connections to a 300 µm thick silicon sensor, and the full detector assembly is mounted on custom Timepix2 chipboard shown in Figure 5.9. The entire test system is connected to the AdvaDAQ readout system and controlled by the software Pixet [136]. The results discussed below were already presented in [151] but are briefly described again in this chapter for convenience.

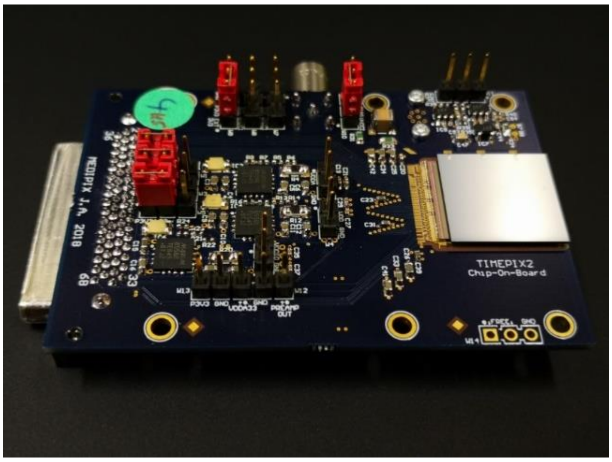
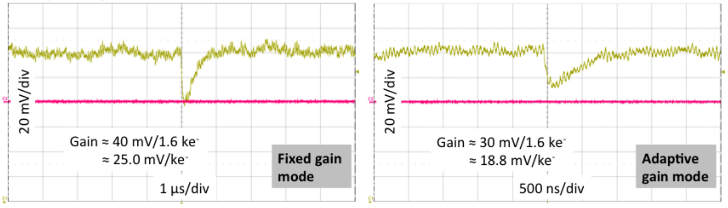


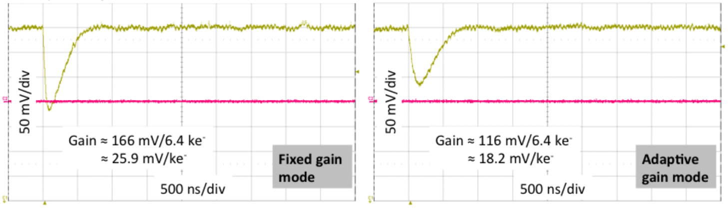
Figure 5.9. Timepix2 readout bonded to a 300 µm thick silicon sensor and connected to a printed circuit board using wire bonds extenders (courtesy J. Alozy).

The output of the analog front-end is monitored through a test point on the chipboard, using an oscilloscope. Input charges of 1.6 ke^-, 6 ke^- and 25.6 ke^- were sent to the input of the readout pixel using the test pulse circuitry. The time waveforms are shown in Figure 5.10 for the fixed gain mode and the Adaptive Gain Mode. In Fixed Gain Mode, the amplitude of the CSA's output pulse is proportional to the input charge until the saturation of the CSA. The MOS capacitor is activated for high input charges in Adaptive Gain Mode, inducing a progressive decrease of the overall gain with the input charge. Those results fit with the simulated gain for the front-end of Timepix2 and confirm the excellent operation of the RtR buffer designed for this purpose.

a) Input charge = ~1.6 ke-



b) Input charge = ~6.4 ke-



c) Input charge = ~25.6 ke-
(note that the saturation of the pulse height is more pronounced in the fixed gain mode)

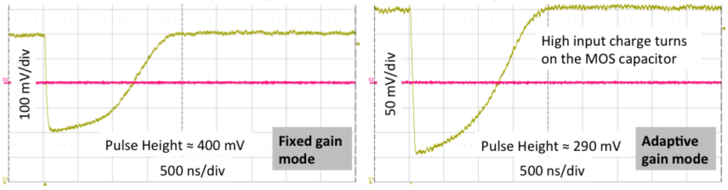


Figure 5.10. Monitoring of the pixel response through the RTR buffer. The Fixed Gain and Adaptive Gain modes are tested by injecting 1.6 ke-, 6.4 ke- and 25.6 ke- [151].

Figure 5.11 shows the response of the voltage and current DACs in the analog periphery by sweeping the input code from 0 to 255. The measured output voltage of the DACs fit with the simulated results.

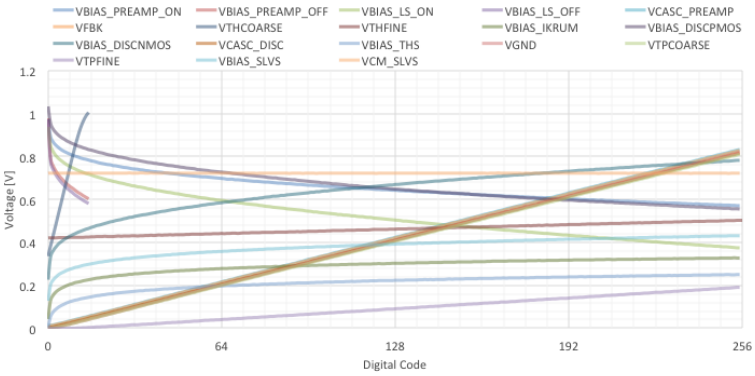


Figure 5.11. DAC scans from 0 to 255. The current and Voltage DACs follow the simulated linearity [151].

Timepix2 detector was used in a readout system called “ethernet embedded readout interface for Timepix2” developed by Czech Technical University in Prague and the University of West Bohemia [157]. The readout system is based on the gigabit ethernet interface. It can operate at a long distance (up to 100 m), which is a practical solution for measurement in places with difficult access. The response of the Timepix2 chip to heavy ions has been measured in [158]. This study aimed to investigate the readout performances in the space environment. Figure 5.12 shows the track created by the Si^{28} ions and detected using the Timepix2 readout bonded to a 500 µm thick silicon sensor. The tracks are measured using the Fixed Gain Mode and the Adaptive Gain Mode; in the latter, the TOT measurement is about 1.9 times larger than the fixed gain.

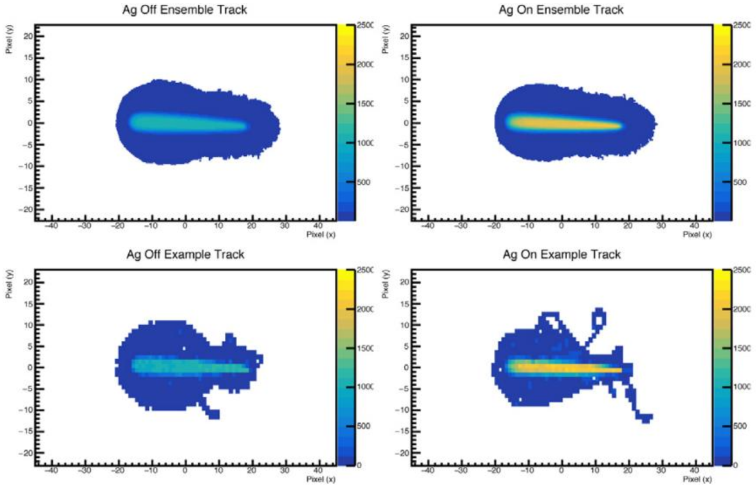


Figure 5.12. Tracks created by Si^{28} ions detected using Timepix2 readout bonded to a 500 µm thick silicon sensor and operated at a bias voltage of 100 V. The tracks are shown with the Fixed Gain Mode on the left, and using the Adaptive Gain Mode on the right [158].

5.4 Timepix4

5.4.1 Motivation and architecture

5.4.1.1 Motivaton

One of the main limitations in Timepix3 is the limited data throughput of 80 Mhit/s per chip, which gives 40 Mhit/s/cm². The rate can be improved by reducing the number of bits per pixel (28 bits for Timepix3), reducing the dynamic range for the TOT and TOA measurement. The other solution is to increase the output bandwidth, which is limited to 5.12 Gbps. In the latter solution, the number of I/O pins must be increased for the readout using parallel links. Another limiting factor is the dead area due to the peripheral control blocks and I/O connections preventing the construction of large-area detectors. Therefore, the Medipix4 Collaboration proposed the design of Timepix4, which is a 4-side tillable large single threshold particle detector chip, with an improved energy and time resolution concerning the Timepix3 chip. The design of Timepix4 is a joint work between the microelectronic group at CERN, Nikhef in the Netherlands, and IFAE in Barcelona.

5.4.1.2 Architecture

The chip is implemented using the 65 nm CMOS process and 10 metal layers. The chip is composed of 448 x 512 readout pixels with a size dimension of 55 µm x 51.4 µm, which can be connected to a sensor composed of an array of 448 x 512 square elements with a pitch of 55 µm. The 4-side buttable feature of this new chip has been possible using the TSV technology to bring the I/O pads connections to the back of the ASIC and make the readout pixel slightly smaller than the sensor pixel to accommodate the peripheral blocks beneath the sensor region. The two top metals of the technology are used to implement the RDL at the top of the ASIC to connect the readout pixel to its associated sensor pixel, adding an extra 60 fF to the input capacitance seen by the front-end electronics [159]. The ASIC has two digital peripheries of 460 µm in height dimension located at the top and bottom of the chip and an analog periphery of 920 µm at the center of the chip. The analog periphery contains the biasing DACs, a bandgap reference circuit, and digital End-Of-Columns circuits to configure the pixels. The digital periphery contains the control logic, I/O, and TSV structures. There are also wire bond connections placed for testing purposes and to probe the ASIC on the wafer without TSV processing. Those wire bond extenders can be diced off after TSV processing.

The analog processing circuitry contains a CSA with a leakage compensation scheme based on the Krummenacher topology like in the other Medipix/Timepix. The gain of the CSA can be configured in three modes of operation, as is shown in Figure 5.13. In High Gain Mode, a fixed gain is defined by a ~3 fF metal-to-metal plate capacitance. In Low Gain Mode, another ~3 fF capacitance in parallel to the main capacitance permits to lower the gain of the amplifier by a factor of 2. The pixel can also be configured in adaptive gain mode, where a MOS capacitor having a gate connected to the input of the front-end electronics provides a varying capacitance value and thus extends the dynamic range of the TOT while processing positive polarity input charges [150], [151]. The output signal of the CSA is fed to a comparator, having a 5-bit threshold tuning circuitry. For electrically characterizing the analog front-end, a test-pulse injection circuitry is implemented at the input of each readout pixel. In this way, voltage pulses can be injected at the input of the CSA through a ~3 fF test capacitance.

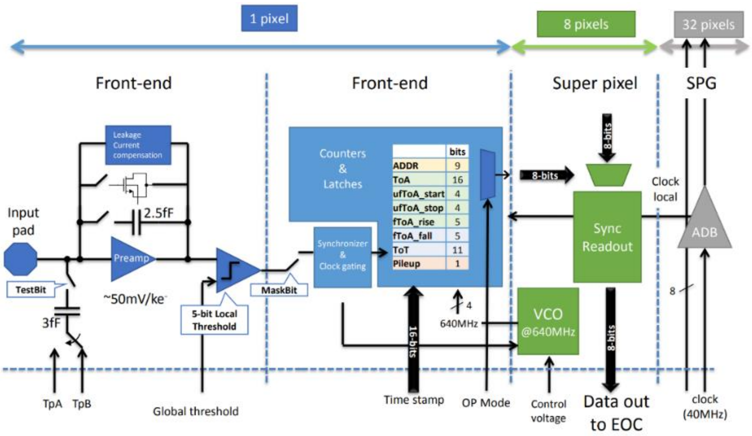


Figure 5.13. Block diagram of the Timepix4 pixel cell [113].

The digital pixel can be configured in photon counting mode or to measure the TOT and TOA information. Each event generating a signal above the threshold will increment the counter in photon counting mode, also called frame-based mode. Each pixel contains two counters with a programmable depth of 8 or 16 bits. The presence of two counters per pixel allows the readout in Continuous Read/Write; one counter is counting while the other one is being read out. In this mode, a counting rate up to 5 Ghits/mm²/s is expected with an input photon energy of 8 keV impinging on a silicon sensor. The measurement of the TOA and TOT information is illustrated in Figure 5.14. There is a master counter-clock of 40 MHz distributed across the chip. The 11-bit TOT counter is incremented with clock cycles from the master clock like in Timepix3. A VCO in the superpixel starts oscillating at 640 MHz when one of the pixel discriminators is fired, and a 5-bit counter counts the number of positive transitions of the VCO until the next rising edge of the master clock. This gives an 11-bit global TOA information, along with a 5-bit fTOA_rise. In addition, the VCO contains four inverter stages with a configurable delay time. The state of the inverter stages is recorded at both the start and the stop of the VCO in a 4-bit register, respectively, named ufTOA_start and ufTOA_stop. At the falling edge of the comparator, the VCO is started again, and a 5-bit fTOA_fall counts the number of positive transitions until the next rising edge of the 40 MHz clocks [46], [159]. This scheme allows allocation of the hits TOA in a 200 ps bin. 9-bit registers record the coordinate of the pixel in the column and 8-bit for the double column address.

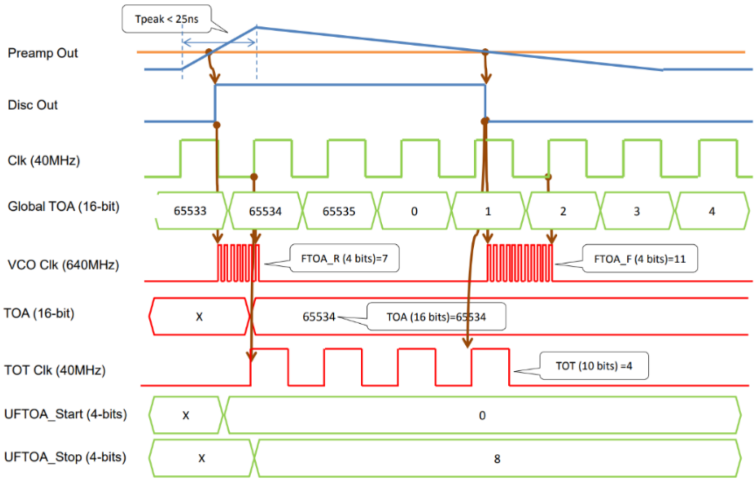


Figure 5.14. Illustration of the TOT and TOA information measurement in Timepix4 pixel cell [113].

5.4.1.3 Delay Locked Loop (DLL)

Another challenge for Timepix4 was setting an accurate reference clock at each superpixel in the matrix. This has been possible by implementing a digital Delay Locked Loop (dDLL) shown in Figure 5.15. This solution was described in [46]. Pixels are regrouped into a superpixel group. The latter contains 4 superpixels, each composed of 2 x 4 pixels. Each superpixel group has two Adjustable Delay

Buffers (ADBs), one for the propagation of the master clock 40 MHz up the column and another one for the downwards propagation of the clock. Each ADB is composed of course and fine delay blocks. A control block located at the bottom of the double column ensures a delay of 25 ns between the input of the master clock and the output. The control block uses an 8-bit bus to tune the ADBs, to ensure that there is precisely 781 ps (25ns / 32) delay per ADB. The 8 bits are decoded into a 29-bit thermometer code, providing the 14 bits for the course elements' tuning and 15 bits for the fine delay tuning.

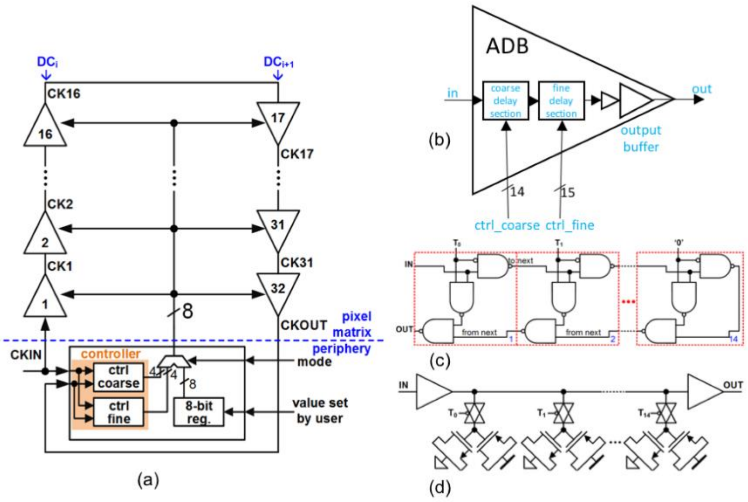


Figure 5.15. Description of the dDLL in Timepix4. (a) The 16 super pixel group blocks of the double-column contain 2 ADBs, one for the propagation upward of the clock, while the other one for the downwards propagation of the 40 MHz clock. (b) shows the structure of the ADB containing coarse and fine delays elements. (c) is the schematic of the coarse delay element, and (d) is the topology of the fine delay element [46].

5.4.2 Design of analog blocks for the periphery of Timepix4

5.4.2.1 *Design of a slow RtR buffer*

The analog periphery of the Timepix4 chip contains DACs that are used to provide a reference voltage to the array of pixels, but there are many pixels connected to a single DAC. Then perturbation on a single-pixel (leakage or dead pixels) would also induce perturbations on the other pixels, ultimately degrading the chip performance. To solve this problem rail-to-rail buffer in voltage follower configuration can be implemented after the DAC to isolate the periphery DAC from the array of pixels. Therefore, the reference voltage provided by the DAC will be kept constant through the feedback loop. The rail-to-rail operation would enable the amplifier to work for any input voltage from VSS to VDD. This operational amplifier has been designed to be linear in the common-mode input voltage range, to be able to carry a large load capacitance of 20 pF, and to have small static power consumption (70 µW) [156]. Figure 5.16 shows the linearity error of the RtR buffer for DC at its output, going up to 1.5 mA; the error remains lower than one mV for 95 % of the common-mode input range, increasing to 3 mV near the rails.

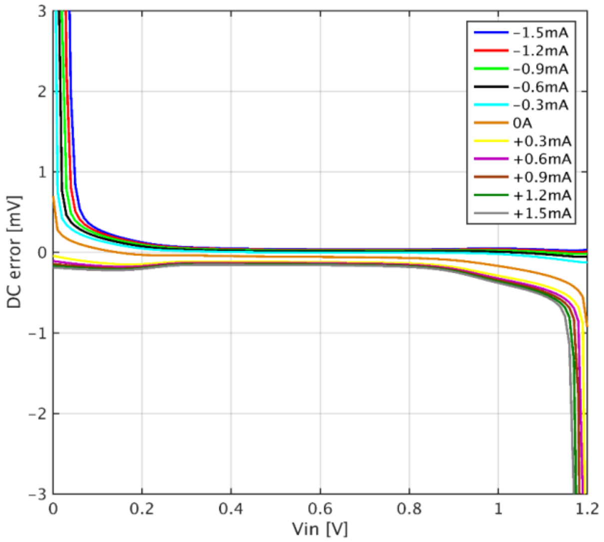


Figure 5.16. Simulated linearity error in the slow RtR buffer from 0 to 1.2 V for an output DC current load varying from -1.5 mA to 1.5 mA. The error increases to 3 mV near the extreme rails values for high DC at the output.

The layout of the slow RtR is shown in Figure 5.17; the size dimension is 39 x 157 µm². The asymmetric and interdigitated layout was drawn for all the critical components like the differential pairs and current mirrors to minimize linear fluctuations like stress, process, and temperature gradient [47]. The performances of the slow RtR after post-layout extraction are detailed in Table 5-5.

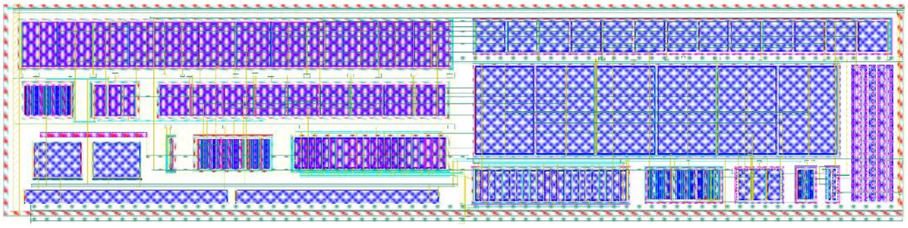


Figure 5.17. Layout of the slow rail-to-rail buffer in Timepix4. The size dimension of the layout is 39 x 157 µm².

5.4.2.2 Design of a fast RtR buffer

Another buffer was implemented for the Timepix4 chip called “fast RtR buffer”. The latter is used to monitor the fast analog signals and the test-pulse circuitry of the pixel. The test-pulse is helpful for testing and calibration purposes of the pixel. Each pixel contains a capacitance of 3 fF, which injects some charge into the CSA. The analysis of the number of counts and the S-curve parameters such as gain, noise, and threshold value can be extracted for the analog front-end. The fast RtR buffer is required to drive the large capacitance and resistance, affecting the testing and providing a full range for the input injection charge. The buffer has been designed with a settling time of 10 ns and to drive a load capacitance up to 5 pF. The high power consumption for the block requires the implementation of a power-down switch to turn on the buffer only when needed. Table 5-5 shows the simulated performances of the fast RtR buffer after post-layout extraction.

Parameters	**Slow RtR**	**Fast RtR**
CMOS technology	TSMC 65 nm	TSMC 65 nm
Supply voltage	1.2 V	1.2 V
Linearity range % (< 1 mV)	100 % for ILOAD= 0 mA	98 %
Load capacitance	20 pF	5 pF
Phase margin	Nominal case: 65 Worst case corner: 56	Nominal case: 83 Worst case corner: 58
Input referred offset (r.m.s)	< 0.6 mV	< 1.8 mV
Settling time	NA	Nominal case: 9.2 ns Worst case corner: 26 ns
Area layout	39 x 157 µm²	35 x 108 µm²
Power consumption	70 µW	970 µW
Gain / Unity Gain Frequency	83 dB / 0.9 MHz	83 dB / 145 MHz
Enable activation time	NA	750 ns

Table 5-5: Simulated performances of the slow and fast RtR buffer after post-layout extraction.

5.4.3 Few measurement results from Timepix4

A first wafer containing Timepix4 ASICs was processed with bump bonds connections by Advacam in Finland. Figure 5.18 shows a Timepix4 ASIC bonded to four 300 µm thick p+ in n silicon sensors. The full assembly is mounted on chipboard designed by Nikhef. The SPIDR system is used as a readout for the testing and characterization of the chip. The details on this readout system can be found in [160]. The RtR buffers perform correctly and agree with the simulated performances. However, two major bugs were found in this first version of the Timepix4 readout. The first major problem was the injection of charges from the digital communication lines located in the analog periphery to the non-shielded Redistribution Layer (RDL) lines. The problem was solved for the next version of Timepix4 by shielding the sensitive RDL lines for the pixels on top of the peripheral circuitry and adding an extra 30 fF to the input capacitance of those pixels [159]. This has been taken into account during the implementation of the RDL for the Medipix4, where all the RDL lines are shielded from the readout electronics (pixels and peripheral blocks), leading to a global constant capacitance distribution across the chip. The second bug was the on-pixel VCO oscillating faster than expected at 920 MHz instead of 640 MHz, which prevents the locking of the VCO to the 40 MHz master clock. The problem came from an inaccurate non-quasi static PMOS model when the source and drain are shorted; this has been redesigned for the second version of Timepix4.

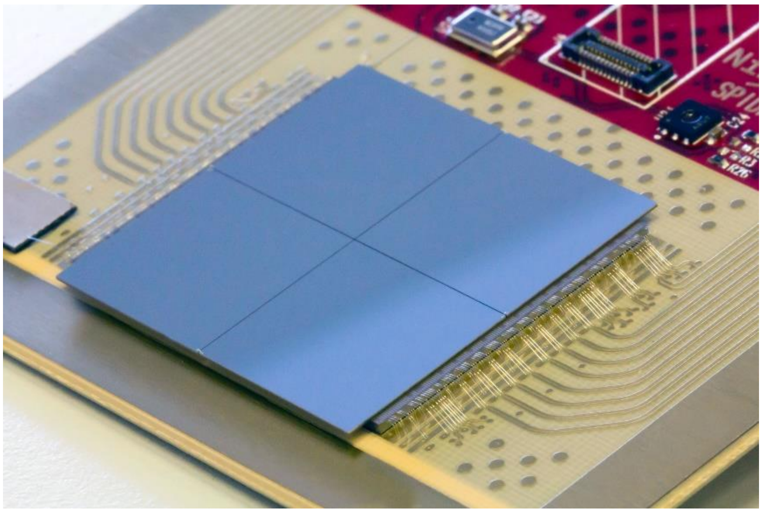


Figure 5.18. Timepix4 is connected to four silicon sensors. The chip is connected to the circuit board using wire bonds for testing purposes. Photo courtesy to M.Fransen (Nikhef).

This first version of Timepix4 was tested in an X-ray imaging setup, using a single large 300 µm thick sensor covering the full readout. Figure 5.19 shows the X-ray images of a dry fish obtained in photon counting mode and frame-based mode for the readout. Only six pixels were masked in this image, illustrating the high quality of the detector. The threshold is set at 650 e-, using an X-ray tube source with Cu target and with a voltage of 30 kV [159].

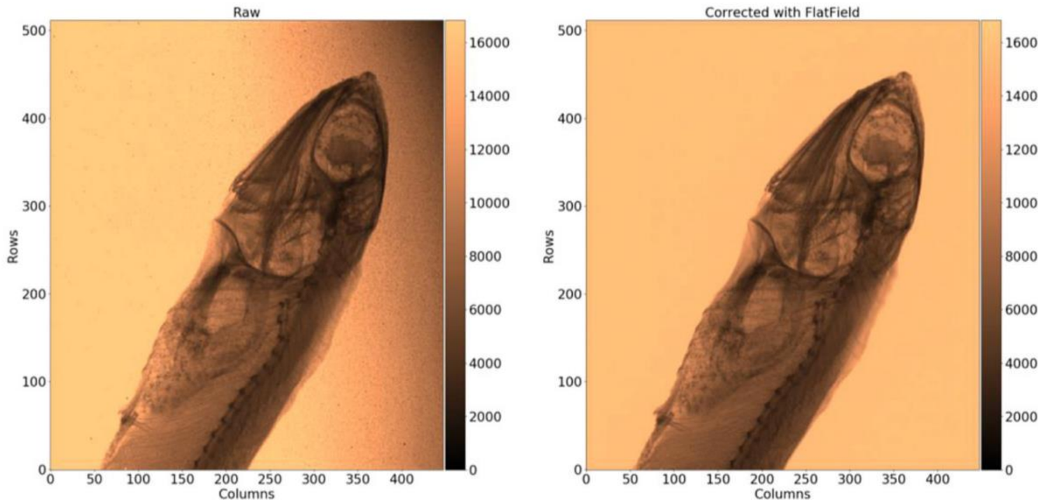


Figure 5.19. X-ray images of a dried fish taken using Timepix4 in frame-based mode; the readout is bonded to a 300 µm thick silicon sensor and mounted on the Nikhef chip carrier board [159].

5.5 Summary

The idea of reconstructing the track of a particle in a Micro Pattern Gas Detector encouraged the Medipix2 Collaboration to design the Timepix chip. The chip detected the energy or the time of arrival of the incoming particles. However, some applications require both information simultaneously and better time resolution. Therefore, the Medipix3 Collaboration proposed implementing Timepix3 readout using the CMOS 130 nm process to overcome those limitations. Recently, the Timepix2 was produced to replace the Timepix readout for some applications requiring measurements in mixed radiation fields. In the framework of the design of Timepix2, a rail-to-rail buffer is incorporated to monitor the output signal of the front-end. Moreover, the chapter explains the implementation of the analog periphery, which contains voltage and current DACs to bias the analog pixel. Timepix4 is the last chip fabricated by the Medipix design team using the CMOS process of 65 nm. The ASIC can be tiled seamlessly on 4 sides and provides a time resolution of 200 ps. The design of a slow RtR buffer for the biasing of the DACs and a fast RtR for monitoring fast signals in the Timepix4 chip is explained. The main features of the Timepix family of chips are summarized in Table 5-6.

Readout chip	**Timepix** [37]	**Timepix2** [151]	**Timepix3** [38]	**Timepix4** [159][161]
Technology	IBM 250 nm 6 metal layers	TSMC 130 nm 7 metal layers	IBM 130 nm 8 metal layers	TSMC 65 nm 10 metal layers
Year of production	2005	2018	2014	2019
Pixel pitch (µm)	55	55	55	55
Number of pixels	256 x 256	256 x 256	256 x 256	448 x 512
Sensitive area (cm^2)	1.98	1.98	1.98	6.94
Number of sides for tiling	3	3	3	4
Acquisition modes	1) Charge (TOT) 2) Time (TOA) 3) Event counting (PC)	1) Charge (TOT) and Time (TOA)	1) Charge (TOT) and Time (TOA) 2) Time (TOA) 3) Event counting (PC) and integral charge (iTOT)	1) Charge (TOT) and Time (TOA) 2) Event counting (PC)
Time bin resolution	10 ns	10 ns	1.6 ns	200 ps
Readout architecture	Frame-based (sequential Read/Write)	Frame-based (sequential or continuous Read/Write)	Frame-based or Data-driven (sequential Read/Write)	Frame-based or Data-driven (sequential or continuous Read/Write)

Table 5-6: Main features of the Timepix family of chips.

Some other ASICs are derived from the Timepix family of chips designed for High Energy Physics. CLICpix2 was designed using 65 CMOS technology. It contains an array of 128 x 128 pixels, with a pitch of 25 µm. The TOT and TOA information can be extracted from the pixel [162], [163]. The Velopix chip has been implemented for the LHCb upgrade. The floorplan is very similar to Timepix3. However, the data throughput is improved by a factor 10 concerning Timepix3 using binary information per pixel [164], [165].

Chapter 6 Implementation and design of Medipix4

This chapter is the core of this thesis and describes the implementation of the new hybrid pixel detector Medipix4. The ASIC targets high-rate applications using high-Z materials. The motivation and the author's main contribution to the Medipix4 development are summarized in section 6.1. The second section describes the floorplan of the entire chip, in which the power distribution scheme and the redistribution layer implementation are carefully analyzed (section 6.2). A detailed circuit implementation of the analog front-end is described in section 6.3. The new analog pixel addresses the limitations of Medipix3RX and other conventional photon-counting detectors. The digital processing circuitries are briefly described in section 6.4; the section focuses on studying a new approach to deal with pile-up events. In general, this chapter provides a guideline to the reader on the challenges encountered in designing and implementing an analog front-end pixel aimed for high-rate applications and the strategies developed to overcome those difficulties. This chapter should not be considered a general guideline for designing ASICs for photon-counting detectors. Indeed, different targeted applications may require other pulse processing circuitries.

6.1 Motivation for the Medipix4 chip

The first motivation for the Medipix4 chip was to remove the dead zone present in most X-ray imaging systems. The wire bond pad connections and the peripheral circuit located on one edge of the traditional 3-side buttable chip are responsible for this dead region in the imaging. To achieve a full sensitive active area and allow the chip's tiling seamlessly in both x and y directions, the peripheral circuit must be placed underneath the sensor pads. This constraint means the readout pixels are slightly smaller than the sensor pixels in one direction to integrate the peripheral circuits. The author studied and implemented the redistribution layer on the readout ASIC to connect the sensor pixel to its associated electronics. The key in the design of a large-area chip is the uniformity of the input capacitance in the pixel array. Also, in large-area ASIC, the power drop along the chip must be minimized. For this reason, the author studied different configurations for the power distribution scheme. This work is carefully described in section 6.2.

Another motivation for the design of Medipix4 was to address the limitations of conventional hybrid pixel detectors for X-ray imaging presented in Chapter 3 and to converge on an ideal X-ray spectroscopic imaging system. Its predecessor, Medipix3RX, covered some of the limitations. For instance, implementing the charge sharing correction algorithm corrects the effect of charge sharing between pixels. Medipix3RX demonstrated the possibility of spectroscopic X-ray imaging at a fine pitch while keeping the spectral fidelity using the inter-pixel architecture. However, the use of Medipix3RX highlighted a few limitations presented in 4.3.4. As a reminder, the main limitations are the dynamic range, the count-rate capability, and the energy resolution. The author's main contribution to this work is the implementation of a new analog front-end to address those limitations while keeping the on-pixel charge sharing correction.

The block diagram of the pixel cell in Medipix4 is shown in Figure 6.1. The pixel contains an analog and a digital part. A Charge Sensitive Amplifier (CSA) with a programmable feedback capacitance in the analog pixel amplifies the input-induced current. A pole-zero cancellation after the CSA permits dynamic cancellation of the non-linear pole of the CSA by a zero in the transfer function. The author implemented two pulse-shaping circuits for the charge sharing correction algorithm in a cluster of 2 x 2 pixels. Section 6.3 provides a detailed circuit implementation of the analog front-end. Two comparators per pixel act as the interface between the analog and digital parts. The digital pixel contains control logic, an arbitration circuit for the charge sharing correction, the counters, and the logic for dealing with pile-up events. The author will discuss in section 6.4 on a new approach he studied to deal with pile-up events.

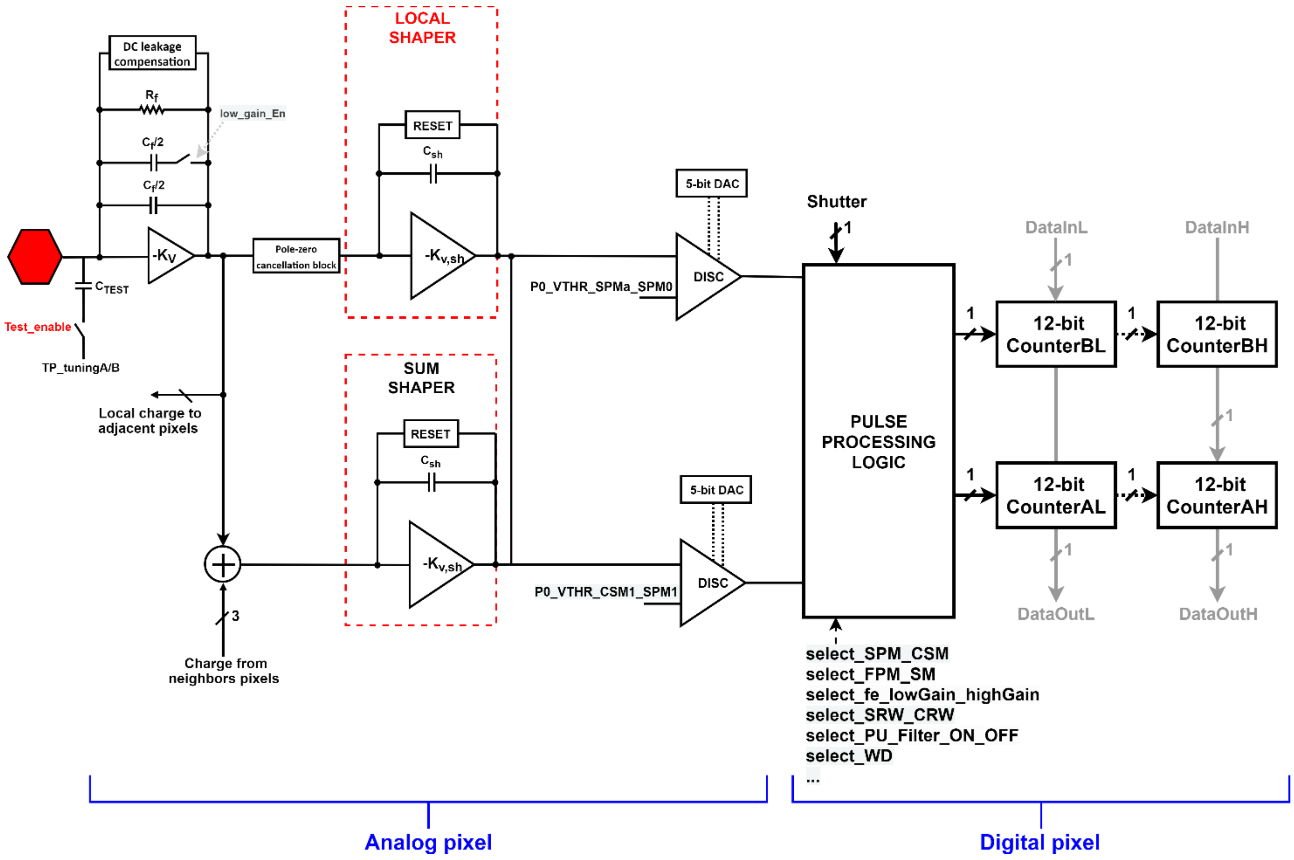


Figure 6.1. Block digram of the pixel cell.

The analog pixel implemented by the author is highly configurable to fulfill the challenging requirements of the Medipix4 collaboration members and address the limitations of conventional hybrid pixel detectors for X-ray imaging. The different modes of operations are already summarized in this section for clarity. Please note the definition of the acronyms for those modes.

The pixel analog front-end can be configured in two acquisition modes: *Single Pixel Mode* (SPM) or *Charge Summing Mode* (CSM). In SPM, the pixel operates like conventional single-photon counting architecture, where each pixel works independently from its neighbors. In CSM, the inter-pixel architecture reconstructs the charge in overlapping clusters of 2 x 2 pixels while an arbitration circuit determines the pixel with the most significant charge deposit. Those two parallel functions correct the spectral distortion produced by charge diffusion through the sensor material.

In addition, the architecture allows pixel size programmability with 75 µm pixel pitch in *Fine Pitch Mode* (FPM) and 150 µm pixel pitch in *Spectroscopic Mode* (SM). FPM is optimal for applications using Si or GaAs as sensor material, whereas SM would be more suitable for spectroscopic imaging using CdTe, CdZnTe, or perovskites. Indeed, the larger charge collection area in SM permits to include the fluorescence photon's energy into the measured energy bin.

Finally, the author proposes three analog modes for the front-end *High Dynamic Range Mode* (HDRM), *Low Noise Mode* (LNM), and *Ultra-Fast Mode* (UFM). In HDRM and UFM, the linear range extends to 154 keV using a CdTe sensor that is beneficial for some applications like medical X-ray imaging. UFM benefits applications like Computed Tomography (CT) or X-ray applications in synchrotrons that require a very high count-rate capability. Finally, the author implemented LNM because of material identification applications and among others that require good energy resolution.

6.2 Towards a 4-side buttable chip

6.2.1 The Medipix4 chip and pixel architecture

The Medipix4 ASIC contains 320 columns by 320 rows of pixels, as shown in Figure 6.2, that process the charge collected from the sensor pixel. The sensor pixel occupies an area of 75 x 75 µm²; the readout electronics is implemented on a pixel area of 70.15 x 75 µm². The readout pixel is slightly smaller than the sensor pixel in height dimension to leave space for the analog and digital peripheries [166]. A redistribution layer (RDL) represented in black arrows connects the readout pixel to the sensor pixel. In order to minimize the RDL pad to pixel distance, the chip contains 3 peripheral regions. The center periphery contains the slow control logic, 320 center digital End-of-Column (EoC), 29 Digital-to-Analog converters (DACs), and 80 analog End-of-Column blocks (AEoC). The height of the analog periphery is 776 µm. The two edge peripheries located at the top and bottom of the ASIC contain 160 edge End-of-Column (EEoC), 32-bit E-fuses for the chip identification, 8 data output serializers, and power & signal wire-bond and TSV pads. The height of the digital peripheries is 388 µm. The chip wire-bonds can be diced off when the TSVs are used.

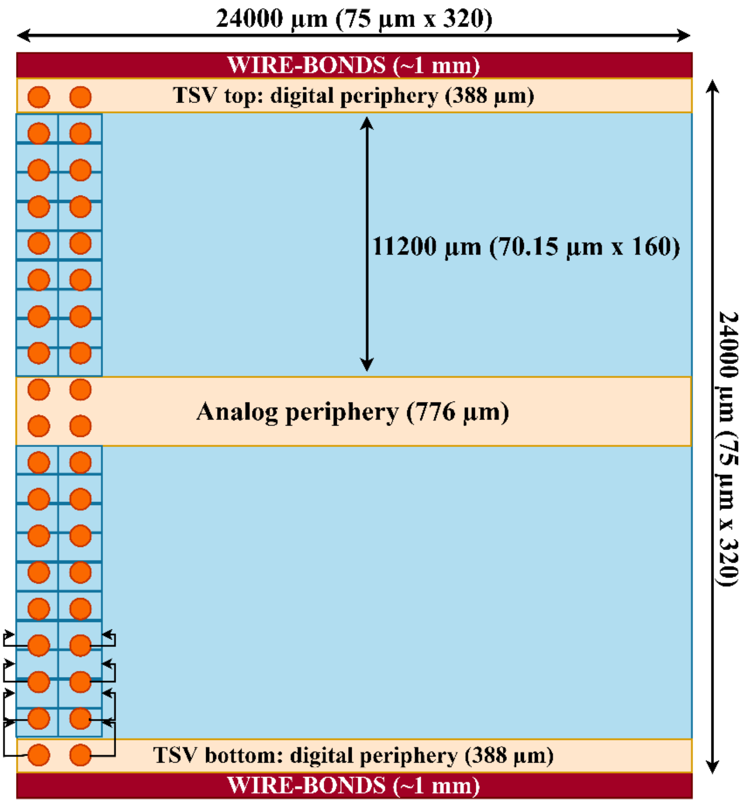


Figure 6.2. Floorplan of the Medipix4 chip. The ASIC contains 320x320 pixels with a pixel pitch of 75 µm. The readout pixels in the blue area are slightly shifted to the sensor pixels. The analog periphery is in the middle. The chip has two digital peripheries at the bottom and top extremities.

The readout pixels are grouped in a 2x2 cluster called "superpixel" and shown in Figure 6.3. The digital circuitries located at the center of the superpixel are common to the four pixels. The common area for the digital pixels allows sharing of resources when implementing the logic for the communication between the neighboring pixels in Charge Summing Mode (CSM). The pad for the bump-bonding connection is centered on the readout pixel. The RDL is drawn on top of the analog pixel to avoid charges injection from the digital signals. When configuring the chip in Spectroscopic Mode (SM), only P0 is connected to the 150 µm sensor pixel. In this case, P0 is called "master pixel" and P1, P2, and P3 are referred to as "slave pixels."

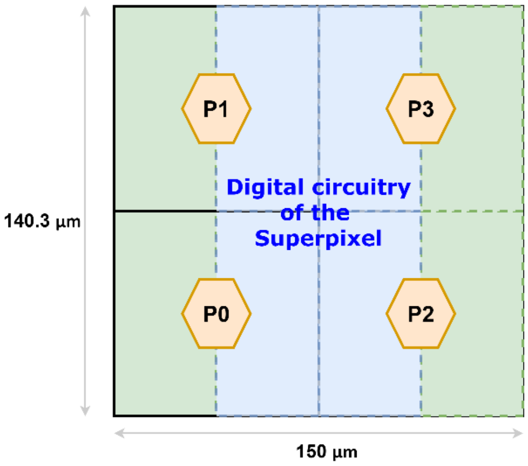


Figure 6.3. The superpixel is composed of 2x2 regular pixels. The digital circuitries are common to the four pixels and located at the center of the superpixel.

6.2.2 Redistribution layer for 4-side buttable chip

Figure 6.4 illustrates the sensor pads covering the periphery and the readout pixels. The blue arrows represent the RDL implemented with the top metals of the ASIC to connect the pads with their readout electronics. The RDL must be drawn such as the pixel matrix has the same input capacitance. In addition, the capacitance must be minimized for lower electronic noise. Finally, the coupling between RDL lines must be suppressed to avoid the injection of charges from neighboring pixels.

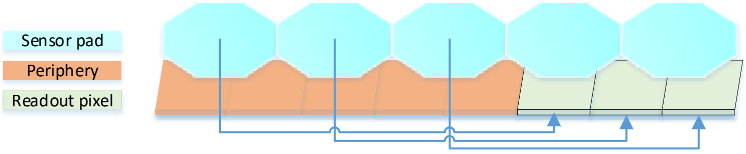


Figure 6.4. Illustration of the sensor pads covering the readout pixels and the periphery. RDL connects the sensor pad to its associated readout pixel.

9 metals are available in the used 130 nm CMOS technology. The orientation of the metals takes into account the constraints of the RDL and the power distribution in the pixel array. The top metals are used for the sensor connection, the power distribution network, and the RDL. M5 is used for biasing lines. The lower metals (M1, 2, 3, and 4) are used for the local routing.

The total input capacitance of a pixel is the sum of the junction capacitance $C_{junction}$, the interpixel capacitance $C_{interpixel}$, the input readout capacitance C_{pad}, and the RDL capacitance C_{RDL} [40]. The capacitances are shown in Figure 6.5, which shows a sensor directly connected to its readout electronics in the case of a 3-sides buttable ASIC. The capacitance C_{RDL} to bring the signals from the sensor input pads to the readout pixels does not appear in the plot.

$$C_{det} = C_{junction} + C_{interpixel} + C_{RDL} + C_{pad} \qquad (6\text{-}1)$$

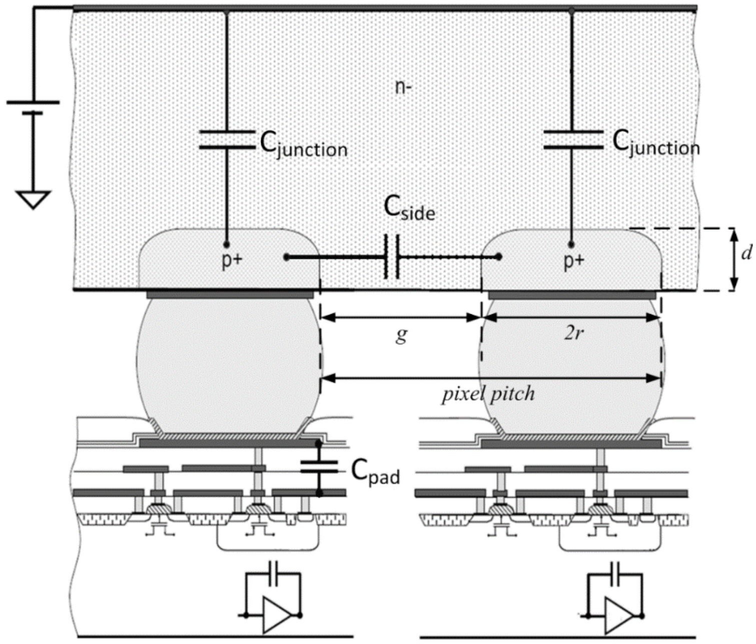


Figure 6.5. Input capacitances for a semiconductor pixel detector [11], [40].

The junction capacitance comes from the pn junction diode having a depletion region between the parallel plates:

$$C_{junction} = A\sqrt{\frac{\varepsilon q N}{2(V_{bias}+V_{bi})}} \tag{6-2}$$

Where A is the area of the plate, N is the dopant concentration, q is the elementary charge, ε is the silicon dielectric constant, V_{bias} is the voltage applied across the diode, and V_b is the built-in voltage of the depletion region.

The interpixel capacitance is the capacitance seen by a central pixel due to its neighbours, is [167], [168]:

$$C_{interpixel} = 4C_{diagonal} + 4C_{side} \tag{6-3}$$

Where $C_{diagonal}$ is the capacitance due to a diagonal neighboring bump bond and C_{side} is the side wall capacitance of the sensor.

Figure 6.6 shows the extracted input capacitances in Medipix4 after RDL implement. The input capacitance in the plot corresponds to the sum of the readout capacitance and the RDL capacitance. The input capacitance uniformity in the pixel array is the key to design a large-area chip.

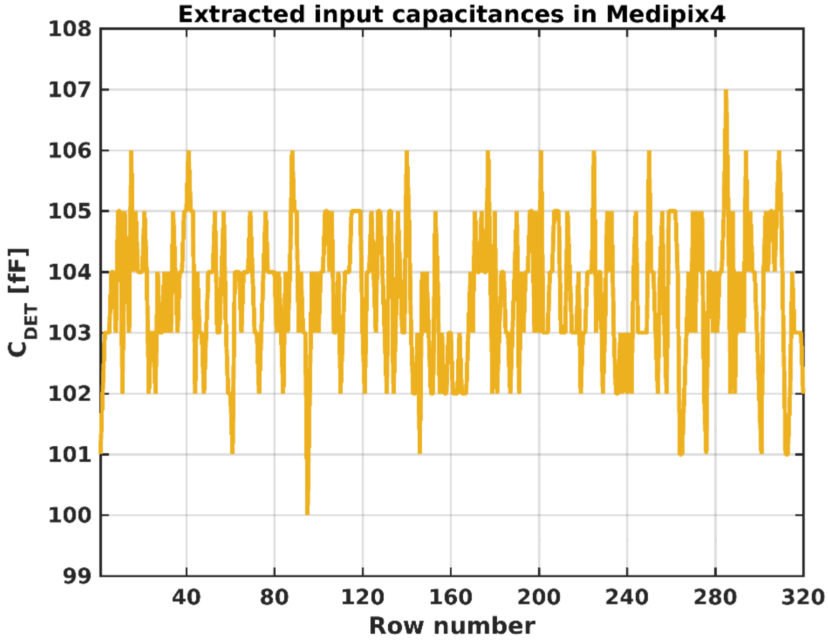


Figure 6.6. Extracted input capacitances in Medipix4 (courtesy X.Llopart).

6.2.3 Power distribution

The power pads in the previous generations before Medipix4 were located on one side of the chip where the periphery was located. This leads to a 3-sides buttable architecture. Medipix4 has three peripheries. The power pads could be placed in those three regions to minimize the power drop along with the chip. A high power drop affects the matching between pixels. Indeed, the pixels close to the power pads will have a different behaviour than those on the chip's other side. This is referred to as the “top-down effect.” The analog periphery contains current Digital-to-Analog Converters (DAC) to bias the target transistors in the analog pixels. Each current source must have a stable reference voltage V_{GS} to ensure the same current flows in the MOSFET devices.

The power consumption is static for the analog supply lines, while the digital blocks have a dynamic power consumption depending on the frequency of the logic. The analog and digital domains have their one power and ground lines, representing four lines to distribute the pixel matrix. The analog and digital power supplies are called VDDA and VDDD, and the analog and digital ground supplies are referred to as VSSA and VSSD. The power distribution is drawn using the lowest resistivity available metal. To ensure a good uniformity between the columns of pixels, each pixel has those four power lines.

Three configurations of the power distribution are studied in this section.

Power scheme 1: One side biasing. Identical power distribution schemes as for Medipix3 and Medipix2.

Power scheme 2: Two sides biasing. Both digital peripheries contain power pads.

Power scheme 3: Top, Center, and Bottom biasing. The analog periphery and the two digital peripheries contain the power pads.

Figure 6.7 is a simplified model of a 3x3 cluster of pixels. Each pixel is represented as a constant current block flowing from VDDA to VSSA and its resistors R_{M8} and R_{AP}, respectively, represent the vertical and horizontal resistors. Only the first column is connected to the power pads in this example. We consider a current of 23.4 µA per pixel for this study, corresponding to a power density of 0.5 W/cm². Below this critical value, we assume the chip can operate without an extra active cooling system [13]. R_{M8} and R_{AP} are given by:

$$\begin{cases} R_{M8} = \frac{70.15\ \mu m/2}{15\ \mu m} * \ \rho(M8)\ with\ \rho(M8)\ the\ sheet\ resistivity\ of\ the\ metal\ 8 \\ R_{M7} = \frac{75\ \mu m/2}{15\ \mu m} * \ \rho(AP)\ with\ \rho(AP)\ the\ sheet\ resistivity\ of\ the\ AP\ layer \end{cases} \quad (6\text{-}4)$$

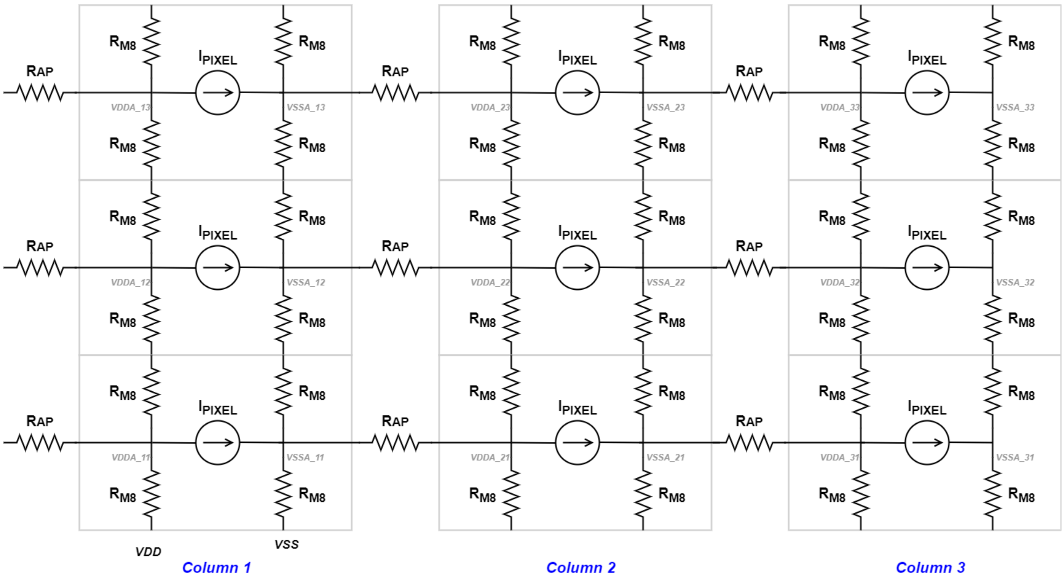


Figure 6.7. Example of power distribution scheme of the critical nets VDDA and VSSA in a 3x3 cluster of pixels. The schematic of the pixel is simplified as a series of resistances for the vertical and horizontal power lines and a constant current flowing in the analog pixel. R_{M8} is the resistance of a 70.15/2 µm long Metal 8, R_{AP} is the resistance of 75/2 µm long metal AP. The current flowing in each pixel is 23.4 µA. The position of the power pads influences the horizontal power drop. In this example, only the first column has the power pads at its end.

6.2.3.1 One side biasing: Bottom periphery

The 320x320 pixel matrix is simulated using the simplified model of the pixel. The power pads are placed at the bottom of the chip and equally spaced to distribute the analog and digital power uniformly.

Figure 6.8 shows the 3-D representation of the simulated power drop Δ(VDDA) – Δ(VSSA) over the whole chip. The power drop, maximal for the pixels at the top edge of the chip, is evaluated at 92 mV in the worst case.

The following equation gives the expected power drop in a single column of pixels:

$$\Delta V_{VDDA} - \Delta V_{VSSA} = 2 * \sum_{k=1}^{320} I_{pixel} * R_{M8} * k = 2 * I_{pixel} * R_{M8} * 160 * 321 = 60.1\, mV \qquad (6\text{-}5)$$

To this sum, add the power drop seen in the periphery where the power pad is delivering all the current for multiple columns of pixels. Each power pad delivers a current of around 92 mA (the total current in the pixel matrix divided by the number of power pads). The periphery is 388 µm in the height dimension. There is an additional 27 mV drop in the periphery using equation 6-4. The total power drop is around 87 mV, which fits the simulated results in Figure 6.8.

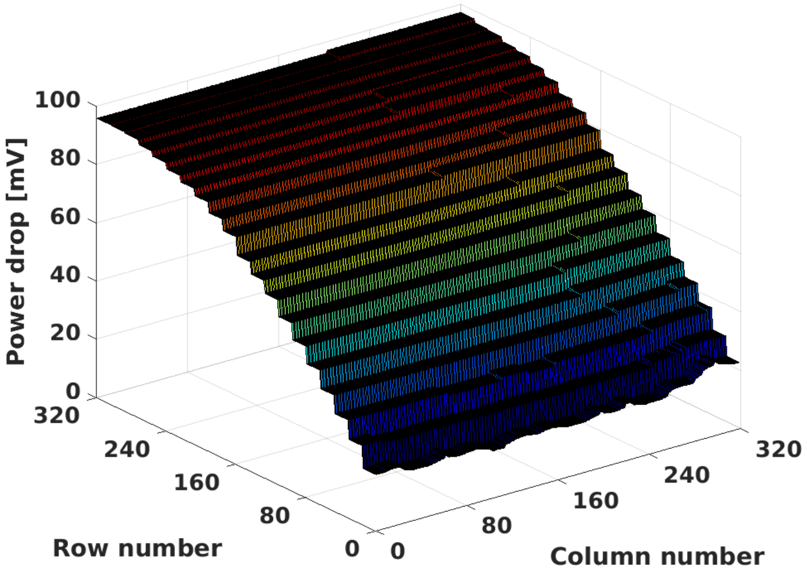


Figure 6.8. 3-D representation of the power drop Δ(VDDA) – Δ (VSSA) in the Medipix4 chip. The power drop increases when moving further from the bottom of the chip where the power pads are located. The horizontal power distribution remains relatively constant thanks to the uniformly spaced power pads. The worst power drop is 92 mV at the top of the matrix. The staircase shape comes from the meshing used in the simulation.

6.2.3.2 Two sides biasing: Top and Bottom peripheries

The power and ground pads are placed symmetrically in the top and bottom digital peripheries. Figure 6.9 shows the 3-D representation of the simulated power drop. The drop is higher for the pixels close to the center of the chip where the analog periphery is located. The worst power drop is simulated at 27 mV.

The following equation gives the expected power drop that is four times smaller than one side biasing:

$$\Delta V_{VDDA} - \Delta V_{VSSA} = 2 * \sum_{k=1}^{160} I_{pixel} * R_{M8} * k = 2 * I_{pixel} * R_{M8} * 80 * 161 \qquad (6\text{-}6)$$

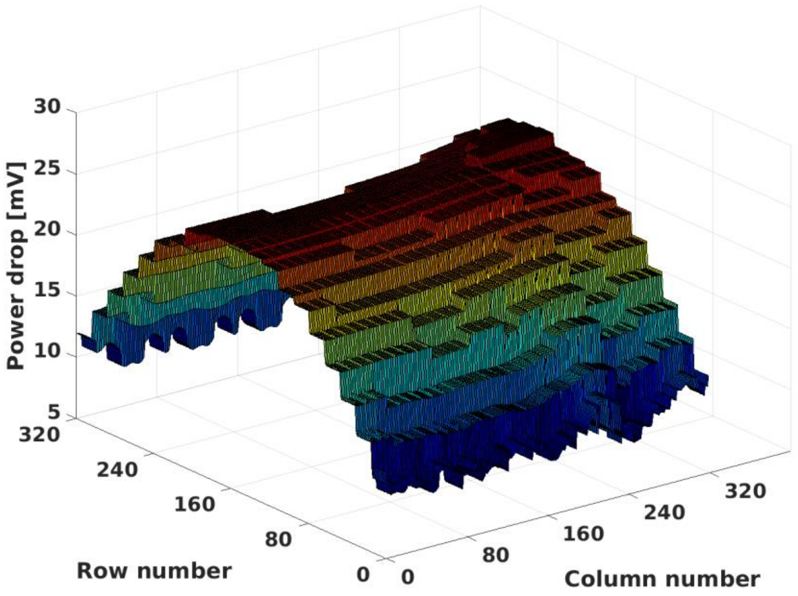


Figure 6.9. 3-D representation of the power drop Δ(VDDA) – Δ (VSSA) in the Medipix4 chip for two sides biasing. The power drop is maximal at the center of the chip, giving the worst power drop of Δ(VDDA) – Δ (VSSA) = 27 mV.

6.2.3.3 Three sides biasing: Top / Center / Bottom peripheries

Figure 6.10 shows the simulated power drop over the whole chip in the case of three sides biasing configuration. In the worst case, the power drop equals 13 mV, which is a factor two improvement regarding the double side biasing. Nevertheless, this configuration has two disadvantages. First, the power drop in the analog periphery is not uniform, leading to a systematic error in the DACs response. Finally, the power pads located at the center periphery deliver 120 mA of current, larger than the limit set by the technology.

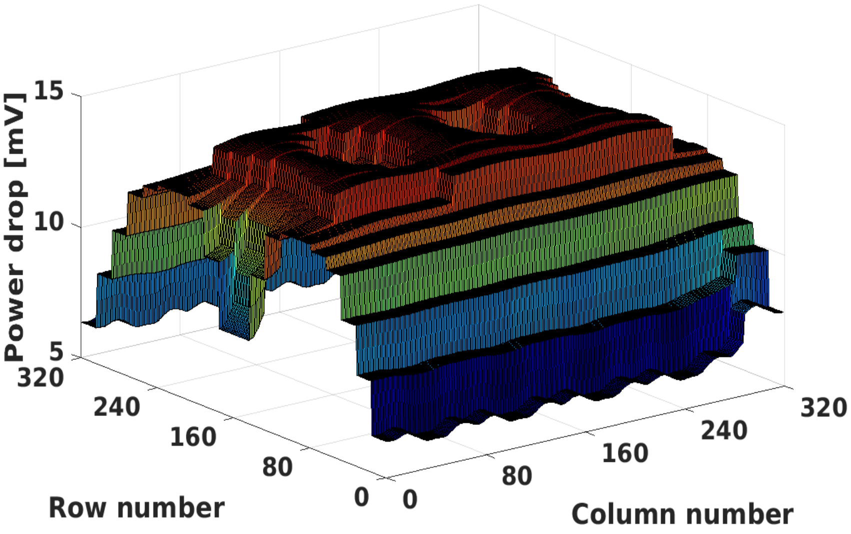


Figure 6.10. 3-D representation of the power drop Δ(VDDA) – Δ (VSSA) in the Medipix4 chip for Bot, Center, and Top biasing. The power drop is still maximal at the center of the chip as the two sides are biasing. This is because only 8 power pads are placed in the central analog periphery leading to a non-uniform power distribution at the center of the chip! In the worst case, the power dop is equal to 13 mV.

6.2.3.4 Summary

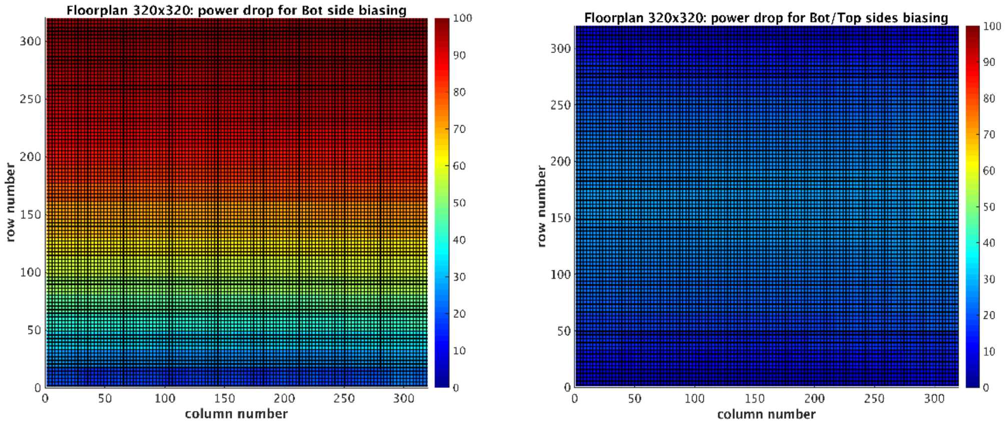


Figure 6.11. 2D representation of the power drop over the chip for the one-side biasing (left plot) and the two-sided biasing (right plot).

Figure 6.11 shows the 2D representation of the 320 x 320 pixels of the power drop. As illustrated, the two-sided biasing provides the the lower power drop and the best uniformity, mainly at the center of the chip where the DACs are located.

6.2.3.5 Power distribution for low power circuits

Some blocks in the analog pixel employ minimal current, in the order of a few nA. A significant mismatch between pixels will be seen by connecting those sensitive blocks to the global power and ground lines. Therefore, a dedicated power distribution is allocated for those blocks using Metal 7. The analog power and ground lines are named "VDDA_LOWPOWER" and "VSSA_LOWPOWER," respectively. In the worst case, the simulated power drop of the low-power lines is equal to 6 mV, which is four times lower than the power drop in the main power lines.

6.3 Details of the analog front-end of the pixel

The analog processing pixel in Medipix4 contains multi-stage amplifiers. The first stage is a CSA amplifying the small signal induced at its input. A baseline holder in the first stage permits to compensate the DC leakage current coming from the sensor pixel. A pole-zero cancellation circuit follows the CSA. Subsequently, the signal is fed to a pulse-shaping amplifier with an adjustable peaking time and discharge time. The new shaper amplifier has a reduced baseline drift at high flux compared to the Krummenacher topology that was implemented in the previous Medipix/Timepix ASICs. The output signal is sampled at different energy windows enabling spectroscopy measurement with polychromatic sources. This is possible using multiple comparators with different threshold levels. 5-bit tuning Digital-to-Analog converters (DAC) compensate the threshold mismatches from pixel to pixel. A dedicated summing amplifier and an arbitration circuit address the charge sharing effect.

6.3.1 First stage amplifier

6.3.1.1 Direct cascode stage

A high-gain voltage amplifier in the CSA makes the front-end response less sensitive to process voltage and temperature variation, and parasitic capacitance of the detector. The single-ended topology called 'telescopic cascode amplifier', shown in Figure 6.12, is particularly suitable for CSA implementation. A single-end architecture provides a lower noise contribution than the differential topology implemented in Medipix3RX. However, the differential architecture provided a better substrate and power supply noise rejection. The input sensor pad is connected at the gate of the NMOS transistor M0. The MOSFET M1 is a cascode transistor biased with an external voltage "$V_{BIAS\_CASC\_NMOS}$" from a global DAC in the analog periphery. Eight branches are providing the current I_{BIAS}=1.25 µA to M0. Two branches connect the output of the amplifier, whereas six connect the drain of the input MOSFET. This configuration provides a higher output resistance than a topology where all branches are connected to the output node. The implementation of switches (not shown in the figure) permits turning off the core amplifier in Spectroscopic Mode (SM). In SM, the slave pixels are not bump-bonded to the sensor pixels. Therefore, they do not require an operating CSA.

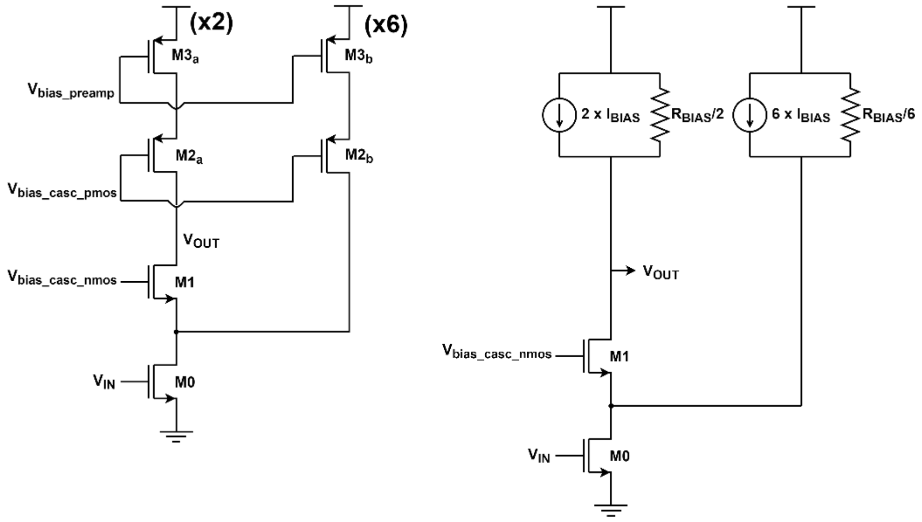


Figure 6.12. CSA core amplifier called telescopic cascode amplifier (left) and its simplified model (right).

The equivalent resistance R_{BIAS} of the current sources formed by M3 and M2 is:

$$R_{BIAS} \approx \left(g_m(M2) + g_{mb}(M2)\right) r_0(M2)\, r_0(M3) \approx 241\ M\Omega \tag{6-7}$$

The output impedance of the core amplifier is defined by:

$$R_{OUT} \approx (R_{BIAS}/2)\ //\ \left(g_m(M1) + g_{mb}(M1)\right) r_0(M1)\ \left(r_0(M0)\ //\frac{R_{BIAS}}{6}\right) \tag{6-8}$$

The DC gain of the core amplifier is given, for nominal conditions, by:

$$K_v = g_m(M0)\, R_{OUT}\ \approx 1100 \tag{6-9}$$

6.3.1.2 Charge Sensitive Amplifier

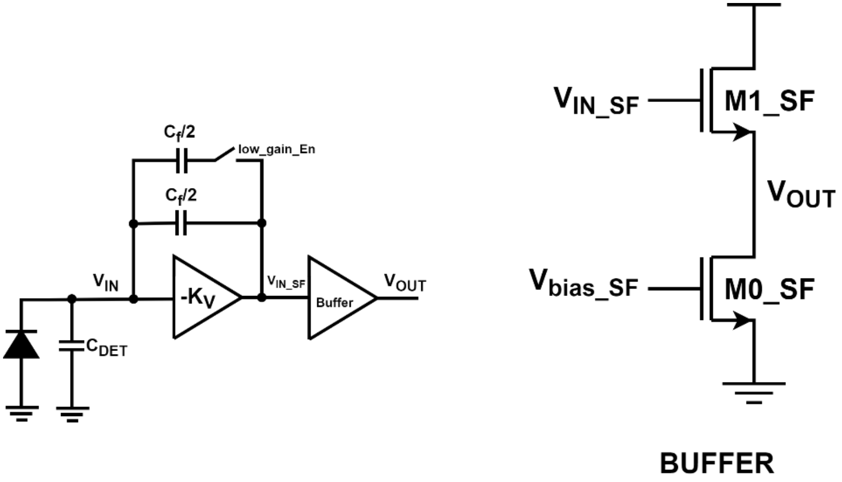


Figure 6.13. Block diagram of the CSA (left) and its buffer (right).

The CSA has a programmable feedback capacitance, as illustrated in Figure 6.13. When the switch "low_gain_En" is off, a 5 fF metal-to-metal capacitance integrates the induced signal at readout pixel input. When the switch is turned on, an additional 5 fF capacitance is added in parallel to the primary capacitance, thereby decreasing the gain of the CSA by a factor of two. A configurable gain permits to optimize the front-end for different applications. A pass-gate structure with NMOS and PMOS transistors in parallel implements the switch. The low gain in High Dynamic Range Mode (HDRM) or Ultra Fast Mode (UFM) extends the linear dynamic range up to 35 ke$^-$, in other words 154 keV for the CdTe sensor. The readout electronics noise is lower using high gain in Low Noise Mode (LNM), at the cost of a reduced dynamic range to around 21 ke$^-$.

The high DC gain of the core amplifier permits integration of the majority of the induced charge on the feedback capacitor C_f. The remaining charge is lost in the parasitic input capacitances (i.e. detector capacitance and test pulse capacitance). The total contribution of the induced signal to the CSA's output pulse is given in percentage by [11]:

$$Integrated\ charge\ [\%] = 100\ \frac{1}{1+\frac{C_{DET}+C_{TEST}}{C_f(1+K_v)}} \qquad (6\text{-}10)$$

The detector capacitance is around 150 fF in FPM, the test pulse capacitance is 5 fF, and the core amplifier DC gain is 1100. From these nominal values, 98.6% of the incoming charge contributes to the output voltage in HDRM and UFM, and 97.3% in LGM (due to lower feedback capacitance).

An NMOS source follower terminates the first stage amplifier and acts as a voltage buffer to drive the resistive and capacitive loads at its output. The analog pixel in Medipix4 is optimized for electron collection using n-type sensors, which justify using an NMOS type source follower to maximize the output swing. Indeed, the signal at the output of the CSA swings upwards; therefore, the DC voltage at its output must be kept at a low voltage level. The NMOS source follower has an asymmetrical driving capability. Consequently, the biasing current must be sufficient to discharge its output capacitance and avoid slew-rate limited operation for the front-end. The output capacitances increase when the front-end is configured in Charge Summing Mode (CSM) or/and in Spectroscopic Mode (SM). Therefore, a global DAC in the analog periphery sets the bias current for the source transistor M0_SF. A large aspect ratio for M1_SF permits driving a high current to the load for large input signals.

This buffer presents two drawbacks. First, the gate-source voltage of the transistor M1_SF reduces the output dynamic range of the CSA. Choosing a low threshold transistor for M1_SF and increasing its aspect ratio attenuate this problem. Finally, the buffer gain is less than one due to the body effect and equals to [17]:

$$\frac{V_{OUT\_SF}}{V_{IN\_SF}} = \frac{g_{m,M0\_SF}}{g_{m,M0\_SF}+g_{mb,M0\_SF}} \approx 0.85 \qquad (6\text{-}11)$$

There are other possible architectures to implement a buffer, but the chosen topology with only two transistors is simple and fulfills the requirements.

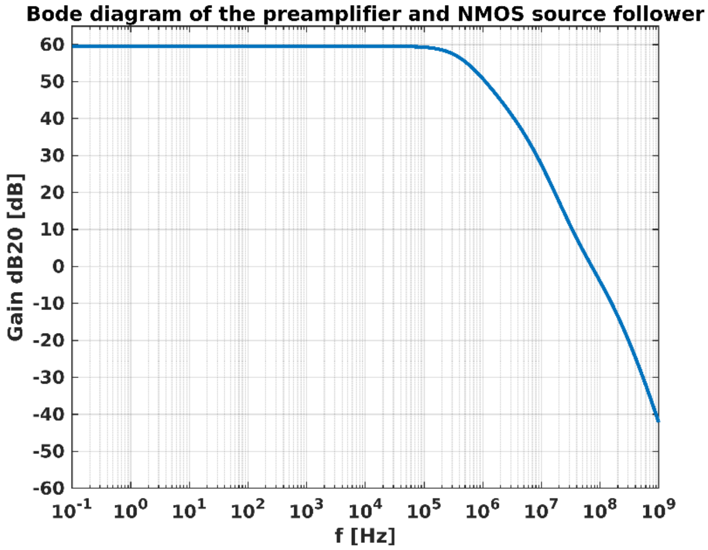


Figure 6.14. Bode diagram of the core amplifier followed by the NMOS type source follower.

The calculated DC gain of the amplifier with its buffer is 1100 x 0.85 = 935. This result is confirmed by the transistor-level simulation shown in Figure 6.14.

6.3.1.3 *Power supply rejection*

The power and ground supply rejection of the CSA are analyzed in this section. The source voltage of the input transistor and the sensor supply line are connected to the ground. The small-signal model in Figure 6.15 represents the CSA without the buffer. Perturbations on the ground supply are seen as a noise source that propagates to the CSA's output.

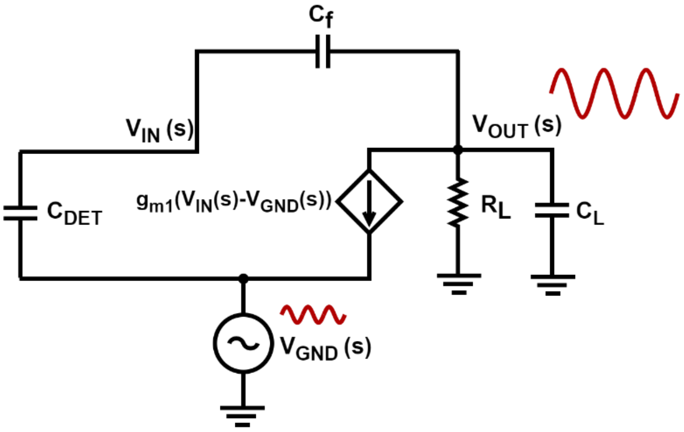


Figure 6.15. Small-signal model for the analysis for the ground supply rejection in the front-end.

The nodal equations of the current flowing in the two branches are:

$$\begin{cases} s\,C_f\big(V_{IN}(s) - V_{OUT}(s)\big) + s\,C_{DET}\big(V_{IN}(s) - V_{GND}(s)\big) = 0 \\ g_{m1}\big(V_{OUT}(s) - V_{IN}(s)\big) + s\,C_L\,V_{OUT}(s) + \frac{V_{OUT}(s)}{R_L} + s\,C_f\big(V_{OUT}(s) - V_{IN}(s)\big) = 0 \end{cases} \tag{6-12}$$

The gain of the transfer function is given by:

$$\frac{V_{OUT}}{V_{GND}}(0) = \frac{1}{1 - \frac{C_{DET} + C_f}{g_{m1}\,C_{DET}\,R_L}} \approx 1 \tag{6-13}$$

Therefore, there is no amplification of the ground noise if the input transistor and the sensor are coupled to the same supply line. However, having the input transistor coupled to the wrong supply line amplifies the noise by about $C_{DET}/\,C_f$ [17]. In addition, if some parasitic capacitances are referenced to the power supply line, this can degrades the power rejection of the amplifier. Figure 6.16 shows the small-signal model in which a parasitic capacitance C_p is referenced to the power supply VDD. This parasitic capacitance provides a path to the noise coming from the V_{DD}.

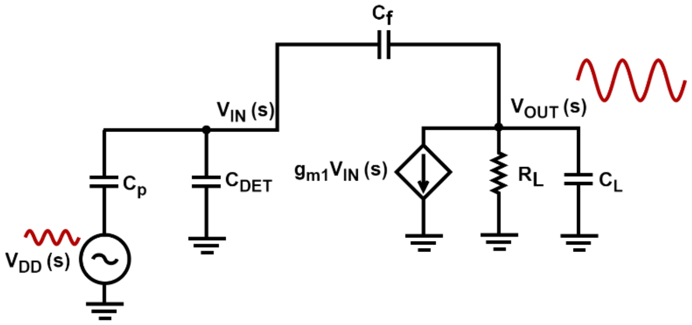


Figure 6.16. Small-signal model for the analysis for the power supply rejection in the front-end in the case of having some parasitic capacitances referenced to the power supply VDD.

The nodal equations by taking the current flowing in the two branches are:

$$\begin{cases} s\,C_{DET}\,V_{IN}(s) + s\,C_f\big(V_{IN}(s) - V_{OUT}(s)\big) + s\,C_p\big(V_{IN}(s) - V_{DD}(s)\big) = 0 \\ g_{m1}\,V_{IN}(s) + s\,C_L\,V_{OUT}(s) + \frac{V_{OUT}(s)}{R_L} + s\,C_f\big(V_{OUT}(s) - V_{IN}(s)\big) = 0 \end{cases} \tag{6-14}$$

The gain of the transfer function of the CSA is:

$$\frac{V_{OUT}}{V_{DD}}(0) = \frac{-C_p}{C_f + \frac{C_{DET} + C_p + C_f}{g_{m1} R_L}} \approx \frac{-C_p}{C_f} \qquad (6\text{-}15)$$

The fluctuations in the power supply are amplified by C_p / C_f. In the case of an NMOS input transistor in the core amplifier, the parasitic capacitances coupled to the power supply V_{DD} must be minimized during the layout phase. That being the case, the RDL lines are shielded to the ground. The extracted coupling capacitance of the input readout pixels to the power supply is around 6 fF. Therefore, the power supply amplification is around 0.6 in HDRM and UFM ($C_f = 10\ fF$), and 1.2 in LNM ($C_f = 5\ fF$).

6.3.1.4 Implementation of the reset circuit

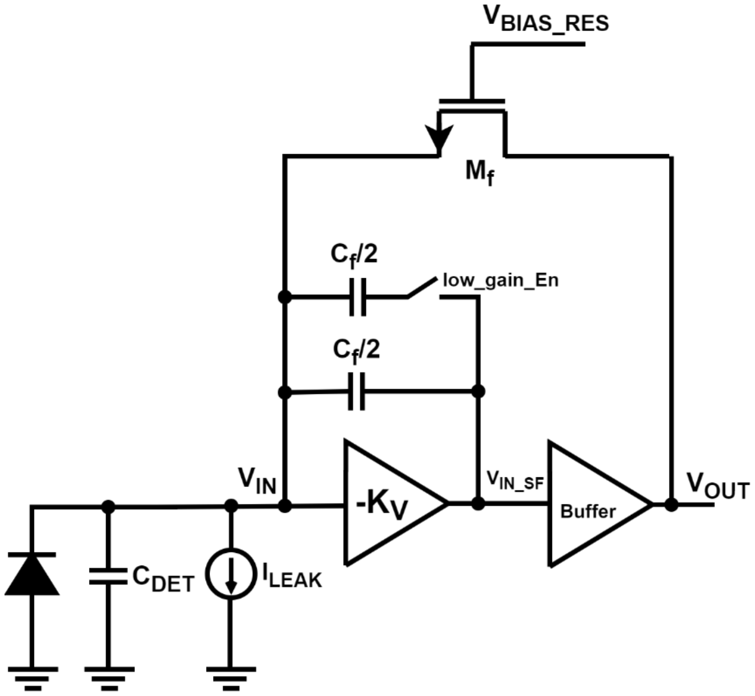


Figure 6.17. Block diagram of the CSA with the feedback reset MOSFET.

The CSA integrates the induced signal on its feedback capacitance and must be reset for further incoming photons. A resistor in the feedback path permits the discharge of the output signal. A large resistor value around a few MΩ is required to minimize the thermal noise introduced by this element. Implementing such a resistor as a passive component consumes a large area. The alternative solution for a compact implementation is to use a transistor working in the linear region, as illustrated in Figure 6.17. The NMOS transistor M_f has its source node connected to the pixel input and its drain node to the CSA's output. In the absence of current flowing across M_f, its sizing and gate-source voltage defines its equivalent resistance. The DC drain-source voltage of M_f is around zero; therefore, the gate-source voltage of the input transistor in the CSA sets the DC output voltage of this first-stage amplifier. This configuration with a NMOS input transistor in the CSA, a NMOS type source follower, and a NMOS feedback transistor optimizes the electrons collection from an n-type sensor. The CSA's output signal goes upwards for such sensors; therefore, the DC output level should be low to maximize the output swing. On that account, the input transistor in the CSA is sized with a large aspect ratio and low threshold voltage flavour available in the 130 nm CMOS technology.

The challenge with this topology is the biasing of active feedback resistances. A replica circuit keeps the equivalent resistance robust against process variations [169], [170]. The circuit is called a replica because the same transistor as the feedback transistor generates the gate voltage for the biasing. Figure 6.18 shows the scheme of the replica circuit. The diode-connected transistor M_{RES} is the replica transistor to bias the analog pixels. This circuitry is located at the center of the analog periphery.

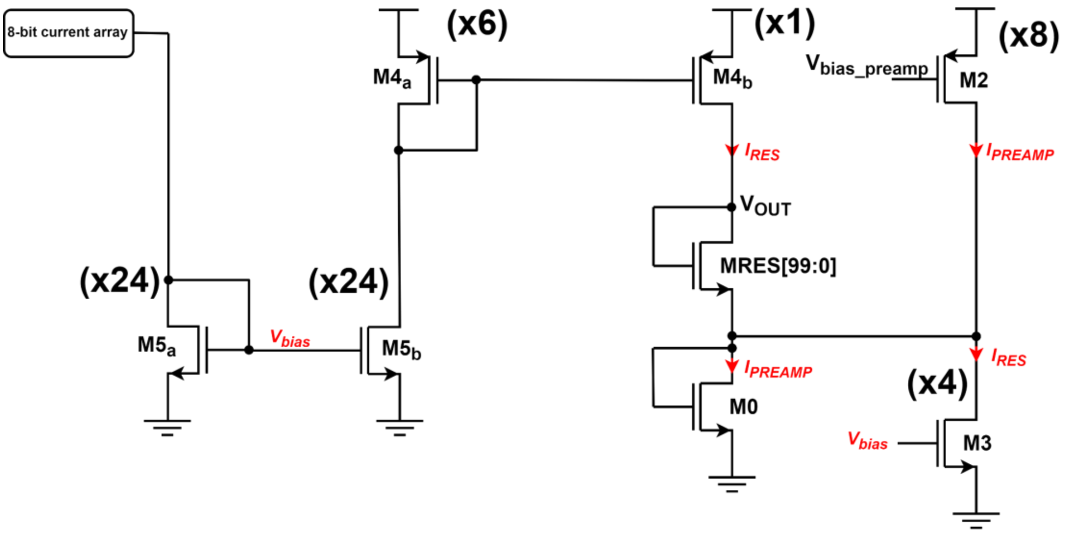


Figure 6.18. Scheme of the replica circuit to bias the reset feedback element in the analog pixels.

The transistor M0 has the same size and current as the input transistor in the CSA's core amplifier and, consequently, the same V_{GS}. Therefore, MRES and M_f of CSA, which already have the same V_G, will also have the same V_S and same V_{GS}.

MRES has the same length as the feedback resistance transistor M_f, but its width is N times larger (N=100). In addition, MRES and M_f both work in weak inversion; however, M_f is in the linear region while MRES in saturation due to the diode-connected configuration. The currents flowing in those transistors are [171]:

$$I_{DS}(Mf) = I_s e^{\frac{V_{GS}-V_{TH}}{nU_T}}\left(1 - e^{\frac{-V_{DS}}{U_T}}\right) \approx I_s e^{\frac{V_{GS}-V_{TH}}{nU_T}} * \frac{V_{DS}}{U_T} \tag{6-16}$$

$$I_{RES} = I_{DS}(MRES) = NI_s e^{\frac{V_{GS}-V_{TH}}{nU_T}} \tag{6-17}$$

With U_T the thermodynamic value and I_S the specific current proportional to the mobility and the ratio W/L of the transistor [171].

By combining both equations, the value of the feedback resistance is [17]:

$$R_{ON}(Mf) = \frac{V_{DS}}{I_{DS}(Mf)} = \frac{N*U_T}{I_{RES}} \; with \; N = 100 \tag{6-18}$$

The equivalent resistance is set by the current I_{RES} flowing in MRES. I_{RES} is programmable using 8 bits as shown in Figure 6.18. The scheme is improved compared to [169], [170] to ensure a stable gate-source voltage for MRES. For that reason, the current I_{PREAMP} in the input transistor M0(CSA) is kept constant. The current I_{RES} provided to MRES is taken out using M3. In HDRM mode, 1 µA flows in the replica source transistor, which sets a feedback resistance value of 2.6 MΩ in the first stage amplifier. For low noise applications, in LNM mode, the resistor is increased to 10.3 MΩ by decreasing I_{RES} to 250 nA. Finally, in UFM mode for fast photon processing, the discharge feedback is decreased to 857 kΩ at the cost of a higher thermal noise contribution.

6.3.1.5 Test pulse circuit

When the readout Medipix4 is mounted on a PCB module, some tests must be carried out before the bump bonding to the semiconductor detector to characterize the pixels. The test-pulse circuitry in Figure 6.19 characterizes the integrated circuit by sending pulses to the front-end input. Indeed, applying a voltage step ΔV through the capacitor C_{TEST}, the square signal is derivated into a Dirac-delta signal triggering the CSA. A configuration bit from the digital End of Column controls the injection: *Sel_inj*. The latter is connected to the input 'Sel' in the Mux of each pixel. A charge is injected in the front-end input during the rising edge of the test pulse and extracted at the falling edge. The amount of injected charge is given by:

$$Q_{test} = C_{TEST} * \left(V_{TP\_ref} - V_{TP\_tuning}\right) \tag{6-19}$$

The capacitance C_{TEST} is carefully chosen to test the full dynamic range of the front-end. Additionally, the capacitor must be small to minimize its impact on the total electronic noise. Since the expected full dynamic range of the front-end is 32 ke^-, and considering a rail-to-rail voltage for the DAC ($V_{TP\_ref} - V_{TP\_tuning}$ = 1.2 V), the required capacitor of C_{TEST} that will be implemented is 5 fF.

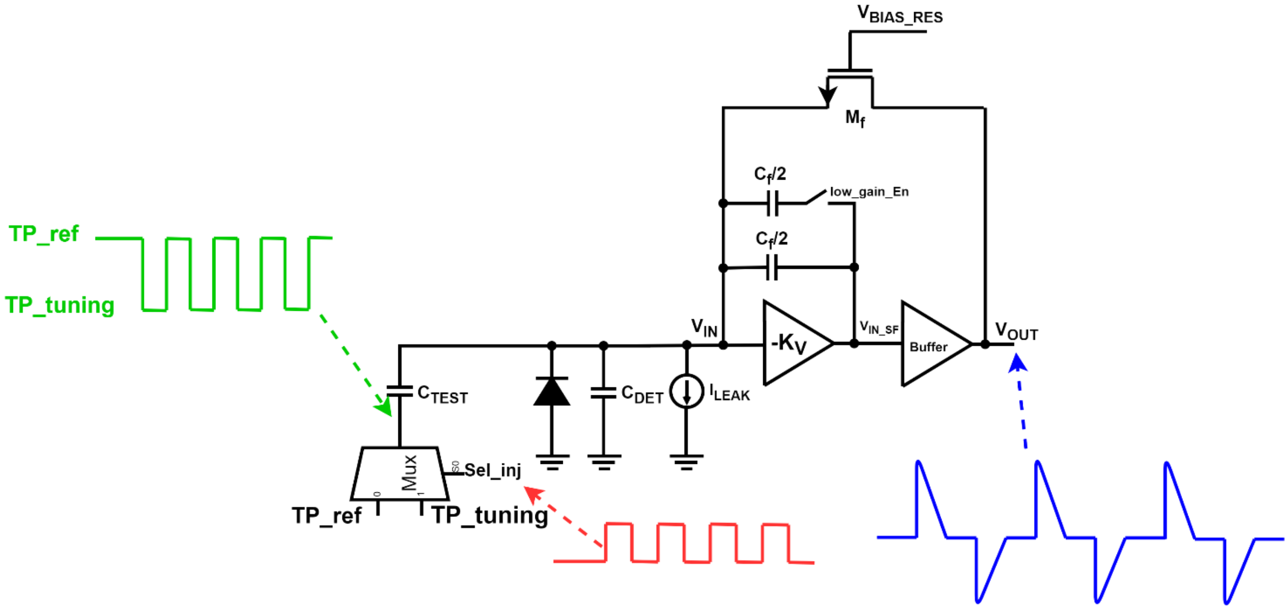


Figure 6.19. Test pulse circuit to test the linearity of the front-end after fabrication.

6.3.1.6 *Pole-zero cancellation circuitry*

The CSA's output signal has a slow discharge time constant compared with the rise time constant. A pulse shaping circuitry containing low-pass and high-pass filters processes the output signal. The differentiation of the slow decay of the CSA response by the high-pass filter produces an undershoot in the output signal. The undershoot translates into a baseline drift and is critical for high-flux applications. The analog pixel in Medipix3RX implements a pole-zero cancellation circuit to cancel the pole corresponding to the slow discharge time. However, the circuit is implemented in the pulse shaping circuitry and requires a manual zero setting to match the discharge pole that depends on the current I_{KRUM} [11]. A dynamic pole-zero cancellation after the CSA facilitates the use of the chip and is implemented in Medipix4.

6.3.1.6.1 Design and sizing of the pole-zero cancellation circuit

Figure 6.20 represents the CSA's block diagram followed by a pole-zero cancellation circuit. In this simplified schematic, the feedback reset MOSFET is represented as a passive resistor R_f, the NMOS source follower has a gain K_{SF}, and the passive components R_{PZC} and C_{PZC} represent the resistor and the capacitor in the pole-zero cancellation circuit.

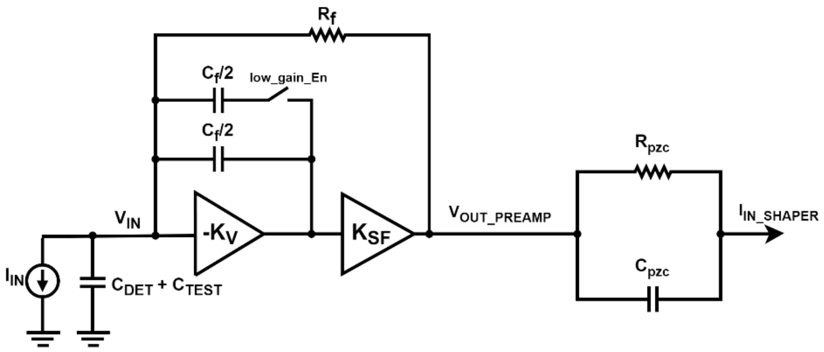


Figure 6.20. Simplified block diagram of the CSA with a pole-zero cancellation network.

Assuming two ideal inverting amplifiers in the CSA and the shaper amplifier with their input nodes considered as virtual grounds and for low_gain_En = active, the nodal equations for the CSA and the pole-zero cancellation block are:

$$\begin{cases} -I_{IN} - \frac{V_{OUT,PREAMP}}{K_{SF}} sC_f - \frac{V_{OUT,PREAMP}}{R_f} = 0 \\ I_{IN\_SHAPER} * \frac{R_{PZC}}{1+s\, R_{PZC}\, C_{PZC}} = V_{OUT,PREAMP} \end{cases} \tag{6-20}$$

The current fed to the second stage amplifier is given by:

$$I_{IN\_SHAPER} = -I_{IN} * \frac{1+s\, R_{PZC}\, C_{PZC}}{K_{SF} * R_{PZC}} * \frac{R_f}{1+\frac{sC_f R_f}{K_{SF}}} \tag{6-21}$$

The zero in the pole-zero cancellation circuit cancels the pole in the CSA if:

$$R_{PZC}\, C_{PZC} = \frac{C_f R_f}{K_{SF}} \tag{6-22}$$

Also written as:

$$K_{SF} \frac{C_{PZC}}{C_f} = \frac{R_f}{R_{PZC}} \tag{6-23}$$

The matching of resistors and capacitors is critical for an accurate cancellation of the CSA's pole. The mismatch from pixel-to-pixel and from one wafer to another also affects the sizing. The rules for the design of matched resistors and capacitors are detailed in [47]. During the layout phase, identical geometries, orientation, and environment must be employed to design resistors and capacitors. In our architecture, the body effect affects the gain of the NMOS source follower (K_{SF} = 0.85) and does not make the design as straightforward as it would have been with an ideal buffer. In addition, the large silicon area in the pixel to implement metal capacitances for C_f and C_{PZC} must be addressed in the design of this stage.

Those considerations lead to regular structures for the resistors and capacitors. A 5 fF metal-to-metal capacitor is taken for the test pulse capacitor and the main feedback capacitor in the CSA. Another 5 fF is added parallel to the main capacitor enabling a larger dynamic range when low_gain_En=1. The 25 fF metal capacitances in the pole-zero cancellation circuit are obtained by connecting five parallel copies of the regular structure. For the resistor R_{PZC}, two copies of R_f are connected in parallel when low_gain_En = active, and four copies when low_gain_En = 0.

6.3.1.6.2 Practical implementation of the pole-zero cancellation circuit

In the simplified model, passive components were taken for the resistors, but the feedback reset element is a MOSFET behaving as a resistor. Figure 6.21 shows the schematic of the CSA and the practical implementation of the pole-zero cancellation with active components. The MOSFETs have the same gate voltage provided by the replica circuit, and their drain nodes are connected to the output of the CSA. All devices provide the same equivalent resistance if the input DC level of the pulse shaping circuit matches the DC input voltage of the CSA. In Figure 6.21, the right-hand side plot details the regular structures used to construct the pole-zero cancellation circuit. When low_gain_En = 1, the equivalent resistance provided by M_{PZC} is twice smaller than with M_f. When low_gain_En = 0, the pass-gates in the pole-zero cancellation circuit are closed, enabling an equivalent resistance four times lower than the reset feedback in the CSA.

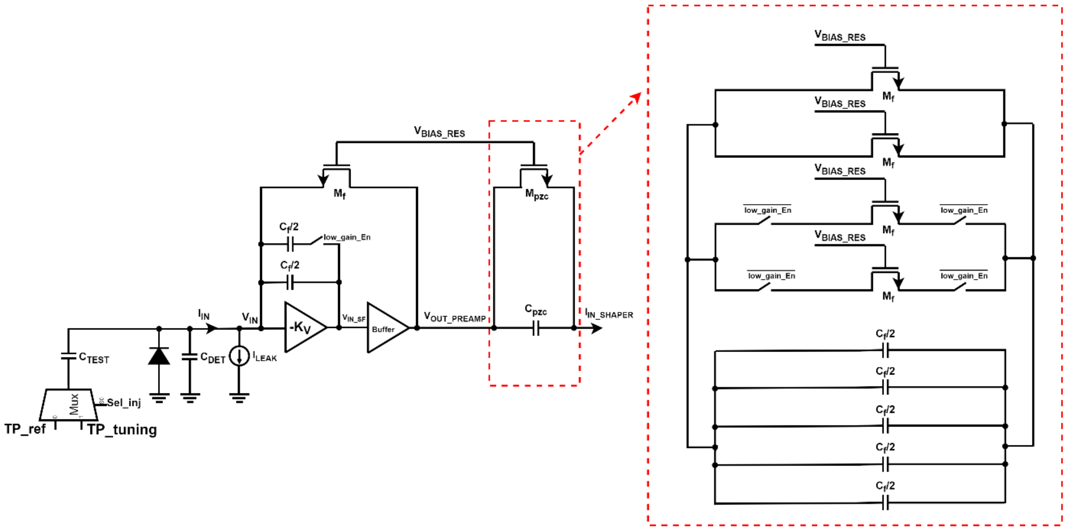


Figure 6.21. Scheme of the CSA followed by a pole-zero cancellation circuit. The equivalent resistance provided by M_{PZC} is twice lower than with M_f when low_gain_En = 1 and four times lower when low_gain_En=0.

By fulfilling the conditions mentioned above, the current fed to the shaping circuitry is given by:

$$I_{IN\_SHAPER} = -I_{IN} * \frac{R_f}{K_{SF}\ R_{PZC}} \tag{6-24}$$

The current provided to the pulse shaping circuit is amplified by 2.35 when the front-end is configured in HDRM or UFM (low_gain_En = 1) and by 4.7 in LNM. In multi-stage front-ends, the first stage amplifier must be designed with high gain to minimize the noise contributions from subsequent amplifiers. For instance, the shaping circuit noise is reduced by 5.5 in HDRM and UFM and by 22 in LNM.

The high leakage current present in high-Z materials perturbates the front-end operation [172]. Moreover, the crystal defects in those materials induce a non-uniform leakage current from pixel to pixel. The leakage is represented as a DC source I_{LEAK} at the input of the front-end in Figure 6.21. Figure 6.22 shows the simulated CSA response for a 60 keV input photon and a varying DC leakage current from 300 pA to 10 nA. A leakage-dependent resistance value leads to a mismatch in the discharge time and noise from pixel to pixel. In addition, the reset MOSFET accommodates only a limited leakage current when pushed into the saturation region. The excess leakage current is integrated into the feedback capacitance and increases the CSA's DC output voltage. Therefore, a DC leakage compensation circuit called baseline holder must be incorporated in the first stage amplifier to avoid reducing the dynamic range.

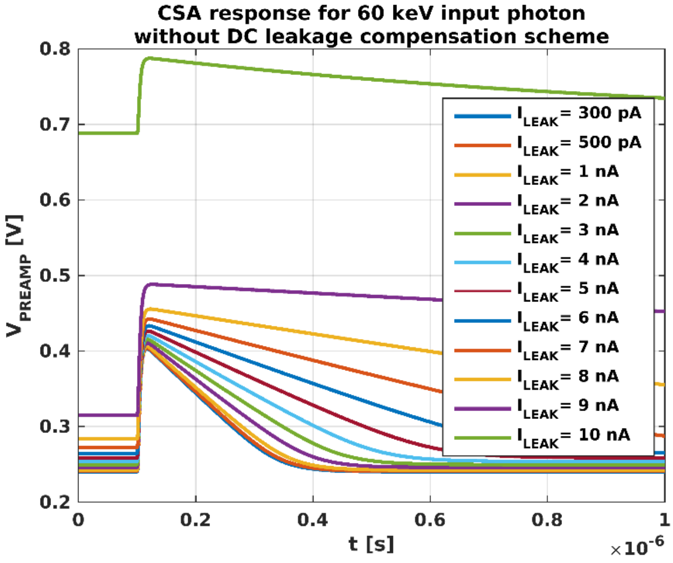


Figure 6.22. CSA response for a 60 keV input photon versus DC leakage current.

6.3.2 Baseline holder

6.3.2.1 Architecture

The scheme in Figure 6.23 is a modified version of the baseline holder proposed in [173]. It contains a differential amplifier that senses the offset between V_{OUT_PREAMP} and V_{IN} and raises the gate voltage in M8 accordingly. The latter sinks the input leakage current, and minimizes the DC current flowing in M_f. In addition, the low-pass RC filter between the differential pair and the MOSFET M8 ensures that only low-frequency signals are processed.

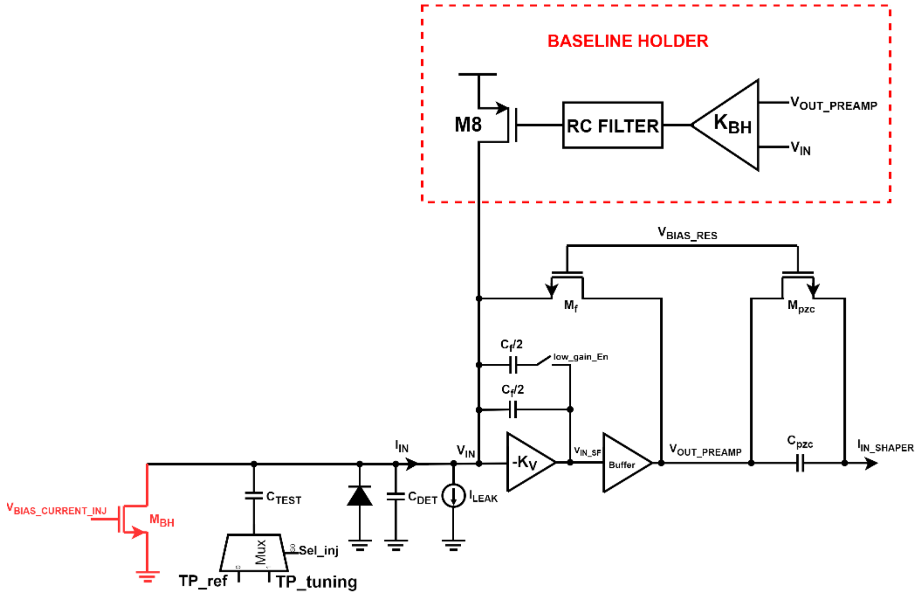


Figure 6.23. Scheme of the baseline holder for compensating the DC leakage current coming to the sensor.

Assuming an ideal inverted amplifier with a virtual ground for the CSA's input and low_gain_En = 1, the nodal equations for the CSA with a baseline holder are:

$$\begin{cases} -I_{IN} - \frac{V_{OUT,PREAMP}}{K_{SF}} sC_f - \frac{V_{OUT,PREAMP}}{R_f} + I(M8) = 0 \\ I(M8) = -\frac{K_{BH}*g_m(M8)}{1+s\,R_{BH}\,C_{BH}} * V_{OUT,PREAMP} \end{cases} \tag{6-25}$$

With $I(M8)$ the current flowing in PMOS transistor M8, $g_m(M8)$ its gate-source transconductance, R_{BH} and C_{BH} are the filtering resistor and capacitor of the low-pass filter, and K_{BH} is the gain of the differential amplifier.

The transfer function of the CSA with the baseline holder in its feedback loop is:

$$\frac{V_{OUT,PREAMP}}{I_{IN}} = -\frac{R_f}{1+R_f\,K_{BH}\,g_m(M8)} * \frac{1+s\,R_{BH}\,C_{BH}}{\left(1+s\frac{R_f\,C_f}{K_{SF}}\right)\left(1+s\frac{R_{BH}\,C_{BH}}{1+R_f\,K_{BH}\,g_m(M8)}\right)} \tag{6-26}$$

The gain of the transfer function is given by:

$$\frac{V_{OUT,PREAMP}}{I_{IN}}(s=0) = -\frac{R_f}{1+R_f\,K_{BH}\,g_m(M8)} \tag{6-27}$$

The zero of the transfer function is:

$$f_{BH,z} = \frac{1}{2\pi\,R_{BH}\,C_{BH}} \tag{6-28}$$

There is the frequency corresponding to the discharge time of the CSA and affected by the non-unity gain of the source follower K_{SF} :

$$f_{CSA,fall} = \frac{K_{SF}}{2\pi\,R_f\,C_f} \tag{6-29}$$

Another pole comes from the baseline holder in the feedback:

$$f_{BH,p} = \frac{1+R_f\,K_{BH}\,g_m(M8)}{2\pi\,R_{BH}\,C_{BH}} \tag{6-30}$$

The low-frequency gain has the term $R_f\ K_{BH}\ g_m(M8)$ in its denominator. By designing a differential amplifier with $R_f\ K_{BH}\ g_m(M8)$ significantly larger than one, the effect of DC input current is attenuated at the CSA's output. For this reason, the circuit is referred to as "baseline holder." The two poles and the zero must fulfill the following condition to obtain a band-pass filter:

$$f_{BH,z} \ll f_{BH,p} \ll f_{CSA,fall} \tag{6-31}$$

The low-frequency gain and pole $f_{BH,p}$ depend on the gate-source transconductance value in M8. The latter is linearly proportional to its drain current in weak inversion and is critical for sensors with a small leakage current. That means the baseline of the CSA varies with the leakage current and temperature. Therefore, a small DC current must continuously flow across M8 to ensure the stability of the baseline. The target transistor M_{BH} is added to provide a small current (~ 1 nA) through a global DAC in the analog periphery ($V_{BIAS\_CURRENT\_INJ}$), as shown in Figure 6.23. Note that this current adds to the DC leakage current and increases the parallel noise contribution.

An Enclosed Layout Transistor (ELT) for the transistor M_{BH} supresses the drain to source leakage current. Furthermore, its source is connected to the low power ground line "VSSA_LOWPOWER" to establish a good uniformity for the biasing. Finally, the inner node of the ELT is connected to the CSA's input taking advantage of its lower capacitance, thus lower readout noise contribution.

6.3.2.2 Practical implementation of the baseline holder

A detailed schematic of the baseline holder is presented in Figure 6.24. The gates of the differential pairs $M1_a$ and $M1_b$ are connected respectively to the output and input of the CSA. The input level can be considered a virtual ground for which the current in the core amplifier sets its DC voltage. The differential folded cascode amplifier is biased at low current using two global DACs in the analog periphery (V_{CASC} and V_{BIAS_BH}). An RC filter follows the differential amplifier and its time constant τ_{BH} must be very large regarding the time constant $\tau_{fall} = R_f C_f$ of the CSA. The large filtering capacitance required to fulfill this condition does not satisfy the limited pixel area. Thanks to their larger capacitance per unit area, gate MOS capacitances seem an attractive solution compared to metal-to-metal implementations. However, in modern technologies, the gate leakage current in MOS capacitors is comparable to the small current flowing in the baseline holder. Those issues encouraged an alternative solution to implement the low-pass filter. The resistive element is obtained using two transistors, M6 and M7, back-to-back connected, in which the source and gate nodes are connected. Large equivalent resistance (in the order of 10 GΩ) is obtained from this configuration [174] [175]. The high resistance value permits the implementation of small metal capacitances around 20 fF. The equivalent resistance from M6 and M7 depends on their threshold voltages; hence, the time constant of the low pass filter must be carefully simulated in Process, Voltage, and Temperature (PVT) corners. The RC filter drives the PMOS transistor M8, which acts as a voltage-controlled current source and injects a DC current equal to the dark current coming into the readout pixel.

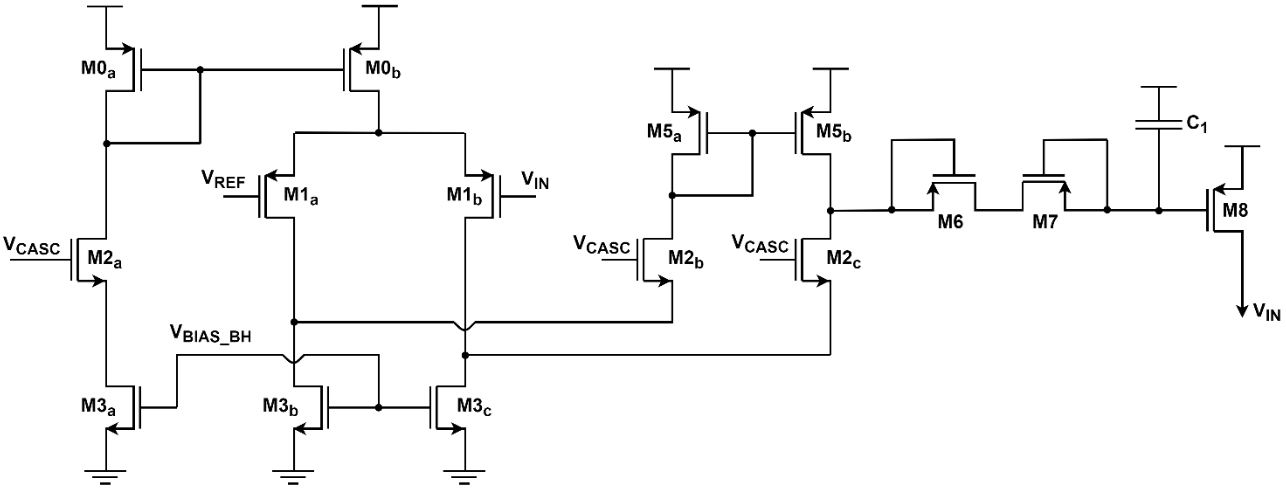


Figure 6.24. Transistor implementation of the baseline holder.

Figure 6.25 shows the simulated bode diagram of the whole chain containing the CSA and the baseline holder circuitry with a DC leakage current varying from 300 pA to 10 nA. The frequency separation permits attenuating the input signal's DC component, while the high-frequency signal is amplified by the resistive feedback element (gain 129.5 dB corresponding to R_f=2.9 MΩ in HDRM). For large DC leakage current, the gate-source transconductance in M8 increases and attenuates the low-frequency gain. The pole $f_{BH,p}$ moves at higher frequencies with the increasing leakage current, whereas the zero and pole of the CSA are unaffected. The zero is located around 3 Hz, corresponding to a filtering capacitance of 20 fF and resistance of 24 TΩ. The pole of the CSA is located at 4 MHz, matching the expected values from a 10 fF feedback capacitance and 2.9 MΩ feedback resistive reset.

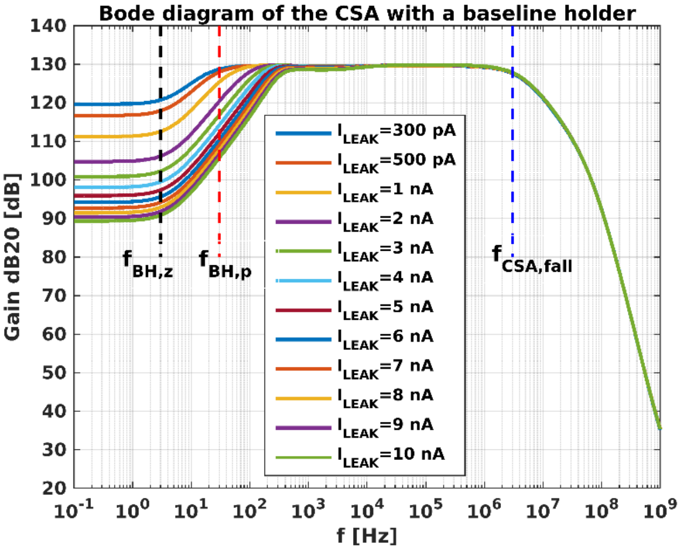


Figure 6.25. Bode diagram of the CSA with the baseline holder circuit for leakage current going from 300 pA to 10 nA.

The CSA response with the baseline holder is simulated for a 60 keV input photon and a varying leakage current from 300 pA to 10 nA in Figure 6.26. The baseline level is locked at 240 mV set by the CSA's input transistor, and the discharge time does not depend on the DC leakage current.

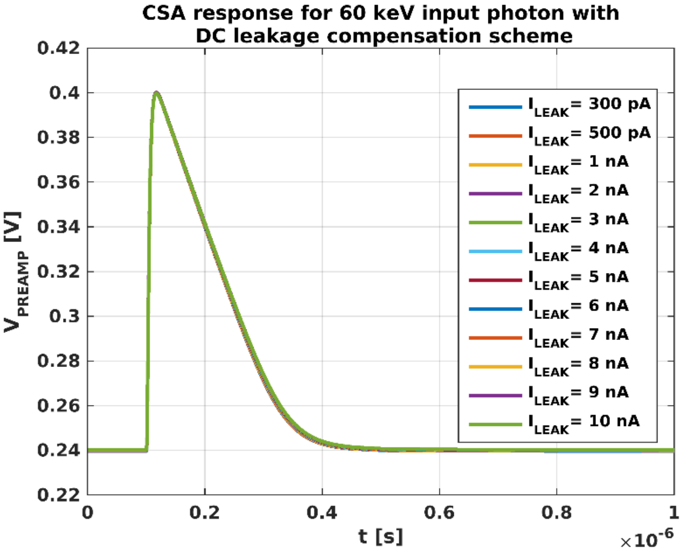


Figure 6.26. The response of a CSA has a DC leakage compensation circuit for a 60 keV input photon and a varying leakage current from 300 pA to 10 nA.

6.3.2.3 Challenges and rules for the layout

The baseline holder uses a tiny current in the order of 10 nA, which means the use of standard transistors with drain leakage current perturbates its operation. Thereby, all transistors are implemented as ELT transistors. In addition, to avoid top-down effects due to the power drop, the circuit is connected to the low-power lines presented at the beginning of the chapter: VDDA_LOWPOWER for the power supply and VSSA_LOWPOWER for the ground.

In addition, zero current must flow in the net connected at the gate of M8. Indeed, the equivalent resistance provided by M6 and M7 amplifies any parasitic current and keeps the transistor M8 off, which is not practical for the DC leakage compensation. Therefore, M6, M7, and M8 are implemented as thick oxide transistors with no gate leakage. The capacitance C_1 is drawn as metal capacitances with the stacks of Metal 1, 2, and 3. The sensitive node is drawn using Metal 1 and is shielded to VDDA_LOWPOWER using Metal 3, which minimizes all possible leakage sources to this node. The layout view of the low-pass filter and the MOSFET M8 is illustrated in Figure 6.27.

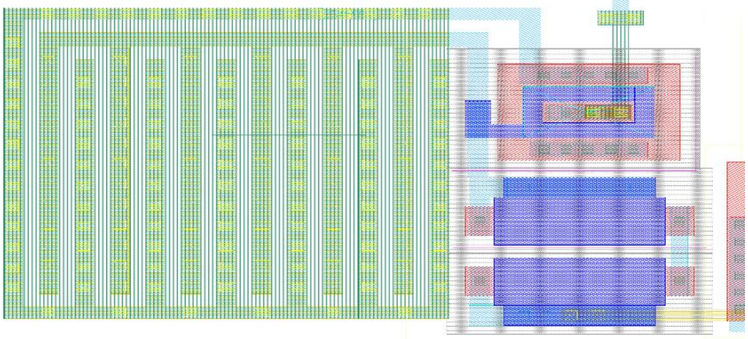


Figure 6.27. Layout view of the sensitive components in the baseline holder. M6, M7, and M8 are drawn as thick oxide MOSFETs to suppress the gate leakage current. M8 is implemented as ELT to minimizing its drain leakage. The green block is drawn in a 'comb shaped' providing 20 fF capacitances.

6.3.3 Pulse shaping circuit

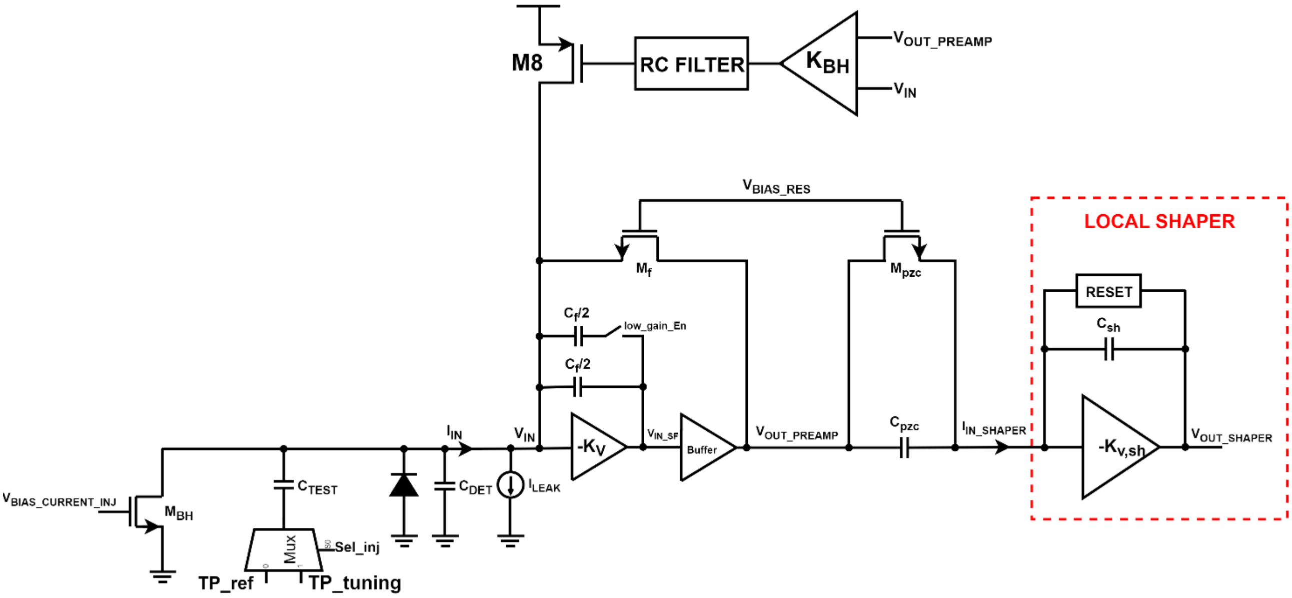


Figure 6.28. Block diagram of the CSA followed by a pole-zero cancellation circuit then fed to a pulse-shaping amplifier.

A pulse-shaping circuit called "local shaper" follows the pole-zero cancellation circuit as shown in Figure 6.28. The shaper is referred to as "local" to distinguish it from the "summing shaper" later implemented for the CSM mode. The block acts as a band-pass filter to optimize the signal-to-noise ratio.

6.3.3.1 Design of the core amplifier and source follower

The gate-source voltage of the MOSFET S0 in the shaper's core amplifier shown in Figure 6.29 must be equal to the gate-source voltage of M0 in the CSA for an accurate pole-zero cancellation. M0 and S0 operate in weak inversion and work in saturation, the gate-source voltage is:

$$\begin{cases} V_{GS}(M0) = nU_T \ln\left(\dfrac{8\,I_{BIAS}}{2n\mu_n C_{ox} U_T^2 \frac{W(M1)}{L(M1)}}\right) \\ V_{GS}(S0) = nU_T \ln\left(\dfrac{I_{DS}(S0)}{2n\mu_n C_{ox} U_T^2 \frac{W(S1)}{L(S1)}}\right) \end{cases} \quad (6\text{-}32)$$

A trivial solution to fulfill the condition is using the same core amplifier as the CSA in the shaper. However, this solution involves a significant power consumption without significant noise or speed benefits. Indeed, the gain factor introduced by the pole-zero cancellation (2.35 in HDRM/UFM and 4.7 in LNM) allows the design of a low-power shaper without degradation in the noise figure. Therefore, the shaper's core amplifier is implemented using the same telescopic topology of CSA and the same global DACs for biasing. Only the transistors' sizes are halved to decrease power consumption by two while keeping its input DC voltage at the same level as the CSA. The circuit is shown in Figure 6.29.

Since the front-end is optimized for n-type sensors and the signal goes upwards at CSA's output, the output DC level at the CSA was brought close to the ground (V_{GS}= 240 mV). At the output of the shaper, however, the signal goes downwards, and the DC output level must be brought close to the power supply VDD=1.2 V to maximize the dynamic range. For this reason, a PMOS source follower is required. A global DAC (V_{BIAS_SF}) provides the current biasing for this buffer. The schematic of the buffer is presented on the right-hand side in Figure 6.29.

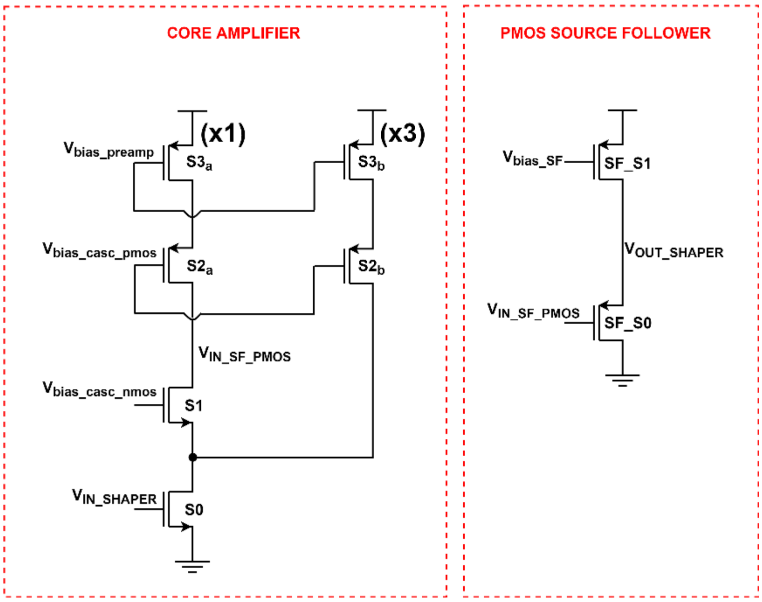


Figure 6.29. Transistor implementation of the core amplifier for the shaper in the left plot and the PMOS type source follower in the right plot.

6.3.3.2 *Krummenacher topology and limitations*

The input DC level of the shaper is close to the ground while its output is closer to the power supply. The reset system in the pulse-shaping circuit requires a feedback mechanism to set the DC output level at the reference voltage 'V_{REF}'. In addition, some residual DC current flowing in the second stage must be compensated. As a first iteration, the amplifier proposed by F. Krummenacher in [36] was considered for the discharge current generation and the compensation of the current from the previous stage. The transistor implementation of this amplifier is presented in Figure 6.30. The current I_{KRUM} determines the discharge time for the amplifier. The transistors $M1_a$ and $M1_b$ have the same drain current and gate-source voltage thanks to the feedback action of the loop. Therefore, the baseline level is locked at the desired value, which can be preset using a global DAC in the analog periphery.

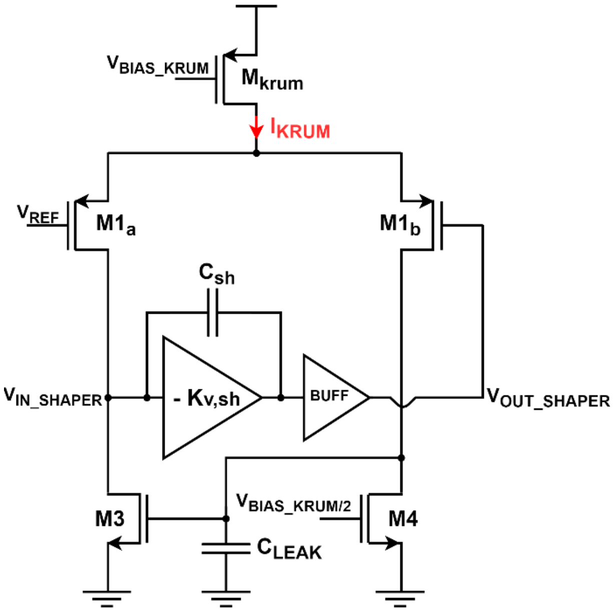


Figure 6.30. Krummenacher amplifier topology used in Medipix/Timepix front-end pixels.

A detailed small-signal analysis of this architecture is found in [11], [17], and poles and zero are extracted.

The zero at the lowest frequency is:

$$f_{z1} = \frac{g_{m3}}{2\pi\, C_{LEAK}} \tag{6-33}$$

Where g_{m3} is the gate-source transconductance of M3.

The pole associated with the discharge of the feedback capacitor C_{sh} by the equivalent feedback resistance $1/g_{m1}$ is:

$$f_{p2} = \frac{g_{m1}/2}{2\pi\, C_{sh}} \tag{6-34}$$

The parasitic capacitance C_p at the source nodes of M1$_a$ and M1$_b$ yields a pole located at:

$$f_{p3} = \frac{g_{m1}}{2\pi\, C_p} \tag{6-35}$$

The pole due to the bandwidth limitation of the core amplifier in the shaper is:

$$f_{p4} = \frac{C_{sh}\, g_m(S0)}{2\pi\,(C_{IN\_SH}\, C_L + C_{IN\_SH}\, C_{sh} + C_{sh}\, C_L)} \tag{6-36}$$

Where $g_m(S0)$ is the gate-source transconductance of the transistor S0 in the core amplifier, C_L the load capacitance at the output of the shaper and C_{IN_SH} its input capacitance.

To ensure the stability of the pulse-shaping amplifier, those four poles must be well separated in frequencies [17]:

$$f_{z1} \ll f_{p2} \ll f_{p3} \ll f_{p4} \tag{6-37}$$

The design challenges for this amplifier are:

- A large C_{LEAK} and a small value for the transconductance g_{m3} are required to push f_{z1} at low frequencies. If f_{z1} moves towards high frequencies, an overshoot in the output pulse is observed due to the differentiation of the signal, which limits the systems' rate. A large filtering capacitance requires a significant silicon area in the pixel cell. In addition, a summing shaper is required to implement the CSM architecture, which requires the same amount of filtering capacitance. Moreover, the design of a fast front-end means a high value of I_{KRUM}, increasing the transconductance value g_{m3}. The filtering capacitance should be sized for the maximum expected value I_{KRUM} = 200 nA, leading to a significant silicon area.

- The mismatch between $M1_a$ and $M1_b$ in the differential pairs affects the frequency pole f_{p3} and the spread in the DC output voltage of the shaper. Indeed, a large transistor area means less spread in the baseline level from pixel to pixel but at the same time pushes the third pole towards lower frequencies.

- Good uniformity of the discharge time is desired from channel to channel to implement the arbitration circuit for the CSM mode. Indeed, in CSM, the pulse's width information from a cluster of 2x2 pixels is compared to determine the pixel having the highest charge. In other words, the discharge time of the current I_{KRUM} must be uniform in the pixel matrix. The mismatch between $M1_a$ and $M1_b$ must be optimized, and the channel length modulation effect in M_{KRUM} must be minimized.

- A high value for the feedback capacitance C_{sh} and gate-source transconductance $g_m(S0)$ permit to push f_{p4} at higher frequencies and separate f_{p2} far from f_{p3}.

6.3.3.3 New pulse-shaping circuit

The challenges above motivated the exploration of a new pulse-shaping circuit. The schematic is presented in Figure 6.31. The transistors $M1_a$ and $M1_b$ provide the discharge current and lock the baseline level at V_{REF}. The feedback system contains two 10 fF metal capacitances. One capacitor is connected between the input and output of the shaper, while the second is connected between the input and output of its core amplifier. The pole splitting acts between the input and the high impedance-node of the core amplifier but also between the input pole and the output pole of the buffer. This configuration provides better stability by splitting the poles between the input and output [17]. Using the same unit of 5 fF in the shaper, the test-pulse circuitry, the CSA, and the pole-zero cancellation circuit, allows for better matching. The same baseline holder as in the first stage enables the DC compensation network. The block diagram of the baseline holder is represented on the right-hand side in Figure 6.31. The large equivalent resistance provided by the back-to-back diode-connected transistor M6 and M7, along with a 15 fF metal capacitance, pushes the dominant pole towards very low frequencies. A small current is necessary through M8 to activate the DC compensation feedback loop.

For this reason, the biasing circuit presented on the left-hand side sets a current equal to I_{RATE} through $M3_a$. In this configuration, the current in M8 is $I_{RATE}/2$ when no DC residual current enters the shaper, and $I_{RATE}/2 - I_{RESIDUAL}$ for an input DC current equal to $I_{RESIDUAL}$. The transistors $M1_a$ and $M1_b$ are drawn as ELT transistors during the layout phase. The inner nodes of the ELT are connected, minimizing the parasitic capacitance seen at their source nodes. The mismatch in the baseline spread is optimized using wide transistors in the differential pairs while maintaining minimal parasitic contribution. The mismatch in the discharge time is further optimized using the self-cascode structure for the biasing [176]. In self-cascode topology, the transistors MH_a and ML_a are connected in series and have their gates connected. MH_a is implemented with a high-threshold voltage transistor flavour, whereas ML_a is implemented with a low-threshold voltage. This combination permits to have both transistors in saturation and mitigates the decrease in output resistance due to the channel-length modulation effect. In other words, the bias current I_{RATE} is less sensitive to its drain-source voltage. Finally, the gain factor introduced with the pole-zero cancellation enables a large value feedback capacitor and pushes f_{p4} far from f_{p2} and f_{p3}.

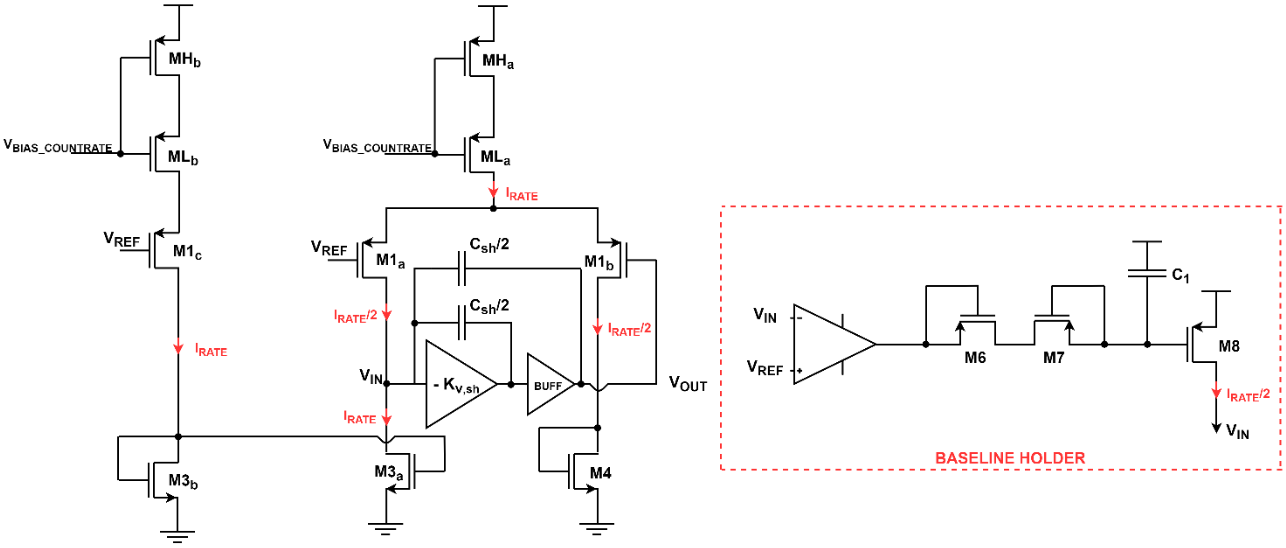


Figure 6.31. Schematic of the new shaper. A baseline holder compensates for all residue DC leakage current at the shaper's input.

Assuming the capacitance C_p negligible in the modified amplifier and taking an ideal unity gain buffer, the transfer function of the core amplifier with the reset feedback system and without the baseline holder is [11]:

$$\frac{V_{SHAPER\_OUT}}{I_{SH\_IN}} = H_0 * \frac{(1-s\tau_{sh,z1})}{(1+s\tau_{sh,p1})(1+s\tau_{sh,p2})} \tag{6-38}$$

The DC gain of the transfer function is:

$$H_0 = -\frac{2}{g_m(M1_a)} \tag{6-39}$$

The zero is located at the frequency:

$$f_{sh,z1} = \frac{g_m(S0)}{2\pi\, C_{sh}} \tag{6-40}$$

Where C_{sh} is the feedback capacitance in the shaper and g_m(S0) the gate-source transconductance value of the input transistor in its core amplifier.

The poles are the same as in the Krummenacher amplifier, corresponding to the discharge of the feedback system and the bandwidth limitation of its core amplifier:

$$f_{sh,p1} = f_{p2} = \frac{g_{m1}/2}{2\pi\, C_{sh}} \tag{6-41}$$

$$f_{sh,p2} = f_{p4} = \frac{C_{sh}\, g_m(S0)}{2\pi\left(C_{IN\_SH}\, C_L + C_{IN\_SH}\, C_{sh} + C_{sh}\, C_L\right)} \tag{6-42}$$

Where g_{m1} is the gate-source transconductance of the differential pair $M1_a$ and $M1_b$, C_{IN_SH} and C_L the input and output capacitances of the pulse-shaping amplifier.

The transfer function of the baseline holder in the feedback is:

$$I(M8) = -\frac{K_{SH\_BH} * g_m(M8)}{1+s\, R_{SH\_BH}\, C_{SH\_BH}} * V_{SHAPER\_OUT} \tag{6-43}$$

Where K_{SH_BH} is the gain of the differential amplifier in the baseline holder, R_{SH_BH} is the equivalent resistance obtained from the back-to-back connected transistors M6 and M7, C_{SH_BH} the filtering capacitance, and $g_m(M8)$ the gate-source transconductance of M8.

The transfer function of the closed-loop system is:

$$\frac{V_{SHAPER\_OUT}}{I_{SH\_IN}} = -\frac{H_0}{1+H_0 * K_{SH\_BH} * g_m(M8)} * \frac{(1-s\tau_{sh,z1})(1+s\tau_{sh,z2})}{(1+s\tau_{sh,p1})(1+s\tau_{sh,p2})(1+s\tau_{sh,p3})} \tag{6-44}$$

There is a zero coming from the DC compensation network:

$$f_{sh,z2} = \frac{1}{2\pi\, R_{SH\_BH}\, C_{SH\_BH}} \tag{6-45}$$

The function has a new pole located at:

$$f_{sh,p3} = \frac{1+H_0\, K_{SH\_BH}\, g_m(M8)}{2\pi\, R_{SH\_BH}\, C_{SH\_BH}} \tag{6-46}$$

The modified shaper provides reset feedback and DC leakage compensation networks. The gain factor $H_0\ K_{SH\_BH}\ g_m(M8)$ attenuates the effect of DC current at the input. The small current across M8 keeps the attenuation factor larger than one.

In Fine Pitch Mode (FPM) and Single Pixel Mode (SPM), each 75 µm pitch pixel works independently from its neighbors. Three analog configurations are possible: High Dynamic Range Mode (HDRM) using I_{RATE}= 80 nA, Low Noise Mode (LNM) with I_{RATE}= 60 nA, and Ultra Fast Mode (UFM) by having I_{RATE}= 200 nA.

The simulated front-end response after parasitic extraction is presented in Figure 6.32 when configured in FPM-SPM-HDRM. The analog pixel processes input charges from 1 ke$^-$ to 41 ke$^-$ without significant overshoot in the output pulse. The dead time is around 130 ns for an input charge of 13.7 ke$^-$, equivalent to 60 keV energy photon using CdTe sensor.

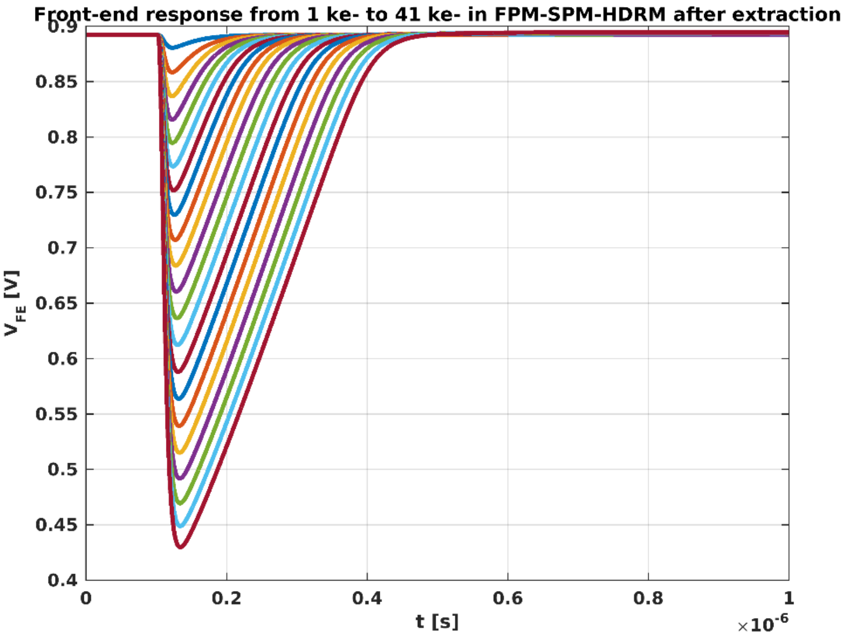


Figure 6.32. Front-end response from 1 ke$^-$ to 41 ke$^-$ in FPM-SPM-HDRM after parasitic extraction.

The front-end is limited to 21 ke$^-$ input charges in FPM-SPM-LNM, as shown in Figure 6.33. The dead-time is around 250 ns for a 60 keV input photon.

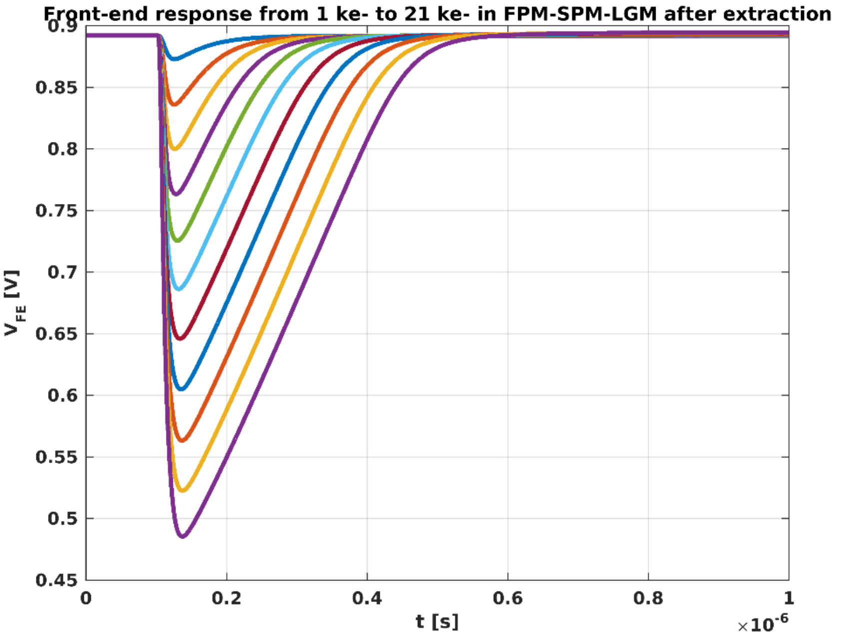


Figure 6.33. Front-end response from 1 ke$^-$ to 21 ke$^-$ in FPM-SPM-LGM after parasitic extraction.

In FPM-SPM-UFM a very fast discharge to the baseline permits high-rate input photons processing. Figure 6.34 shows the front-end response for input charges from 1 ke$^-$ to 41 ke$^-$. The dead-time is around 55 ns for a 60 keV input photon.

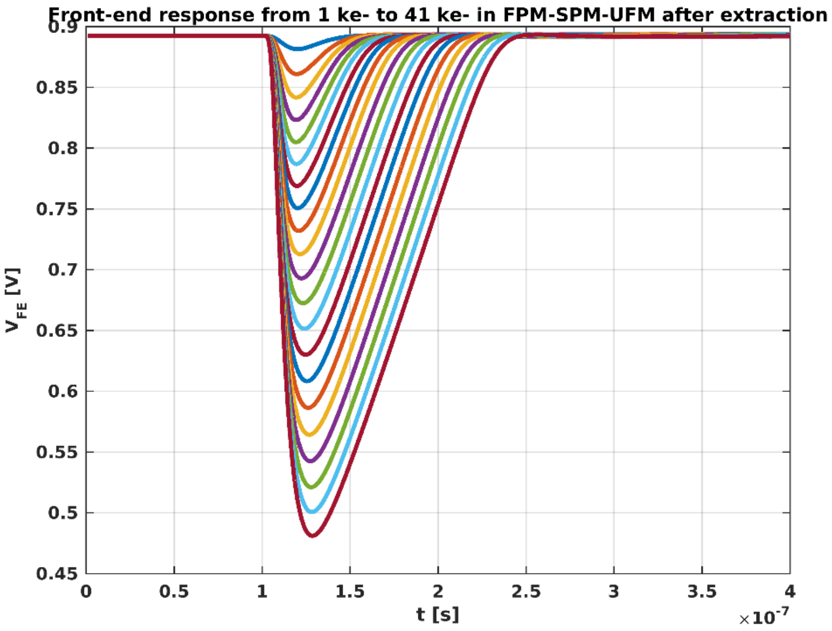


Figure 6.34. Front-end response from 1 ke$^-$ to 41 ke$^-$ in FPM-SPM-UFM after parasitic extraction.

6.3.3.4 *Electronic noise and design trade-off*

The noise analysis of the analog front-end can be found in the Appendix at the end of this manuscript. The total noise is [108]:

$$ENC_{tot}{}^2 = \frac{I_{LEAK}+\boldsymbol{I_{BH}}}{q} * \frac{C_{sh}}{\boldsymbol{g_m(M1_a)}} + \frac{2k_B T C_{sh}}{q^2} * \frac{1}{\boldsymbol{g_m(M1_a) * R_f}} + k_B T \alpha_{w1} \gamma_1 * \frac{\boldsymbol{C_{det}}^2}{q^2} * \frac{1}{\frac{\varepsilon_{CSA}}{C_f} + \frac{\varepsilon_{SH}}{C_{sh}}} \tag{6-47}$$

The noise figure optimization depends on the parameters represented in red in the previous equation. The thermal noise contribution increases with the detector capacitance. Therefore, the extra capacitance coming from the RDL must be minimized in the layout phase. Thermal noise from the feedback resistance in the first stage and the shot noise contribution are reduced by short shaping time. However, a drastic reduction of the discharge time leads to a ballistic deficit.

On the other hand, a large feedback resistance value results in pile-up events in the first stage amplifier. The overall rate capability affects the readout noise and indirectly the power consumption. Indeed, for the peak amplitude calculation, we assumed that the rise and discharge time constants are well separated. However, for high-rate applications, the reduction of the discharge time must be accompanied by a reduction of the rise time constant to avoid loss of charge by a ballistic deficit. The power density per pixel is limited to 1 W/cm^2. Otherwise, active cooling must be implemented on-chip. A trade-off between power, count-rate capability, and noise is inevitable in this design. This encouraged the implementation of three analog modes of operations:

- High Dynamic Range Mode (HDRM): input charges up to 35 ke$^-$ can be detected in this mode. The dead time is 130 ns for a 60 keV input photon and the readout noise is equal to 165 e$^-$ for C_{DET}= 150 fF, as illustrated in Figure 6.35.
- Ultra-Fast Mode (UFM): Input charges up to 35 ke- and a dead time around 55 ns for a 60 keV input photon. This mode provides a very high rate capability for the chip at the cost of a poor noise figure equal to 190 e$^-$ for C_{DET}= 150 fF.
- Low Noise Mode (LNM): By removing 5 fF in the feedback loop of the CSA, a larger feedback resistance can be used to lower the noise figure while keeping a short discharge time. In addition, the high gain factor introduced in the pole-zero cancellation circuit desensitizes the noise contribution from the second stage amplifier. The readout noise is reduced to 115 e- for C_{DET}= 150 fF in this mode. The dynamic range of the front-end is up to 21 ke$^-$, and the dead time is 250 ns for 60 keV input photon.

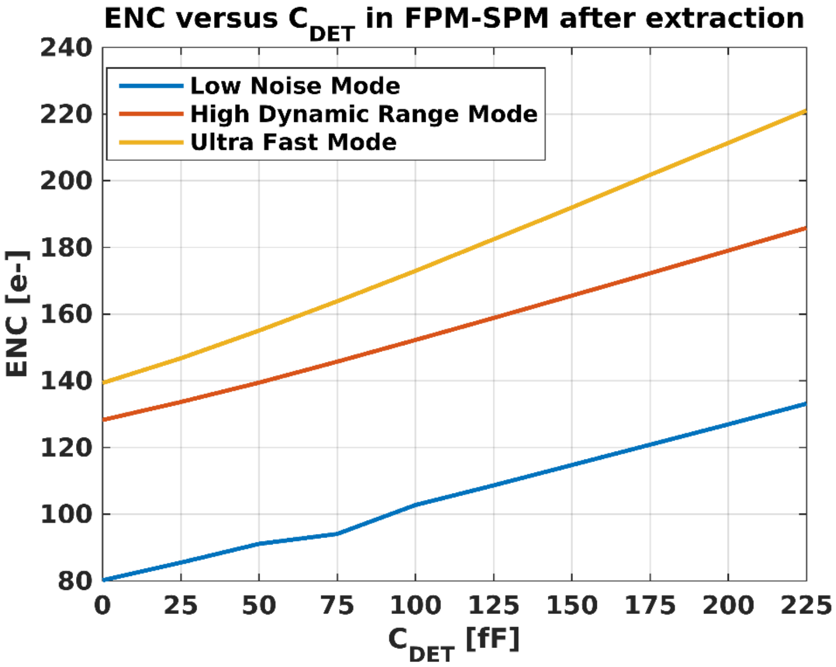


Figure 6.35. Equivalent Noise Charge versus detector capacitance for the three analog configuration modes.

6.3.4 Comparator

The output pulse generated from the pulse-shaping amplifier is fed to a comparator, illustrated in Figure 6.36. The task of a comparator or discriminator is to distinguish if the signal is below or above the threshold V_{THR}. The output data is then processed by the digital pixel, which operates with two possible states: '0' and '1.'

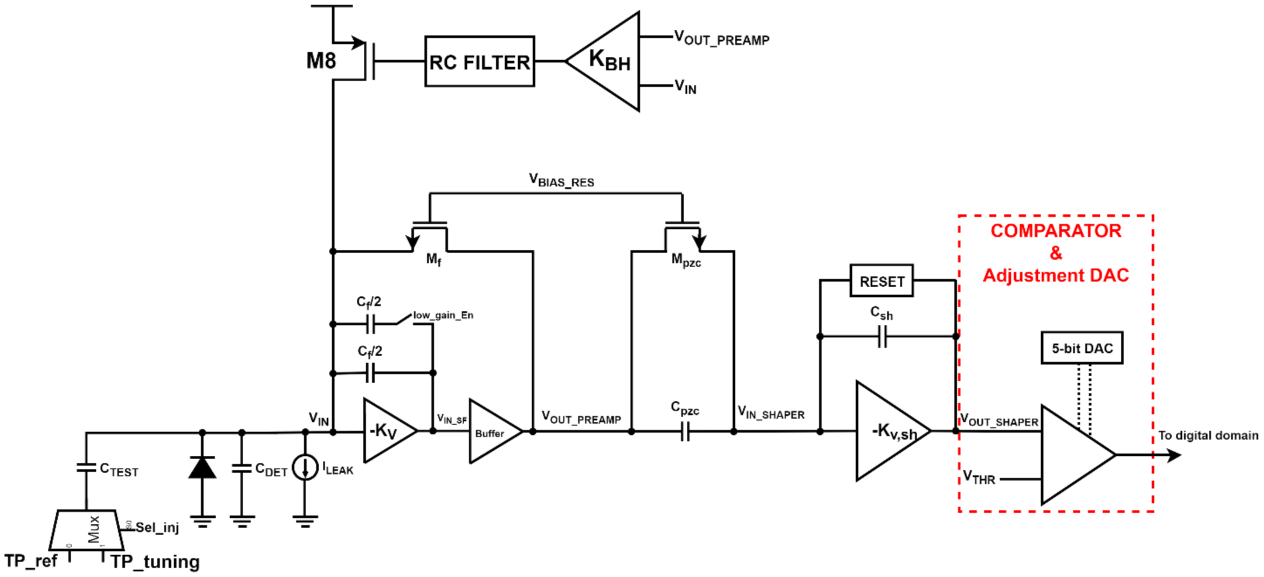


Figure 6.36. Block diagram of the two stages amplifiers fed to a comparator. A 5-bit local tuning DAC enables threshold adjustment.

The comparator consists of two-stage amplifiers. The first stage is an operational amplifier with a folded-cacode input stage to compare the shaper's output versus the reference voltage V_{THR}. The current-mode discriminator in the second stage converts the current signal of the folded-cascode amplifier into a digital signal. This current comparator requires only few extra transistors for its implementation. The comparator is presented in Figure 6.37. The gates of the NMOS pair $M1_a$ and $M1_b$ are connected respectively to the output of the shaper and the reference threshold level. A 14-bit DAC in the analog periphery sets the threshold voltage. A 8-bit DAC provides the current I_{DISC}= 550 nA to the target transistor M0. The load branches are biased at I_{LOAD}= 600 nA through the target transistors $M2_a$ and $M2_b$. A 8-bit DAC provides the reference voltage for the cascode transistors $M3_a$ and $M3_b$. At equilibrium for V_{IN} = V_{THR}, the current in $M5_a$ and $M5_b$ is $I_{LOAD} - I_{DISC}/2$= 325 nA. The arrival of an X-ray photon higher than the threshold energy creates a pulse going downwards at the gate of M1$_a$. When the gate voltage of M1$_a$ is lower than M1$_b$, the latter drives more current. Therefore, the current in M3$_a$, M4$_a$, and M5$_a$ decrease to $I_{LOAD} - I(M1_b)$ and is mirrored to the transistors M4$_b$ and M5$_b$, whereas the current in M3$_b$ increases to $I_{LOAD} - I_{DISC} + I(M1_b)$. Consequently, the excess current $2 \times I(M1_b) - I_{DISC}$ is injected in the second stage, from which the topology is derived from [177]. This current flows through the PMOS M8, while M9 goes into the linear region. The comparator output level decreases to $V_1 - V_{sg}(M8)$. In the opposite case, if the photon's energy is lower than the threshold, M1$_a$ drives more current while M3$_b$ decreases. The first stage pulls the missing current from the NMOS transistor M9, increasing the comparator output DC level to $V_1 + V_{gs}(M9)$. The comparator switches from $V_1 - V_{sg}(M8)$ to $V_1 + V_{gs}(M9)$. CMOS digital inverters follow the output of the comparator to define a digital-friendly logic signal. The negative feedback amplifier in the second stage sets the DC level V_1.

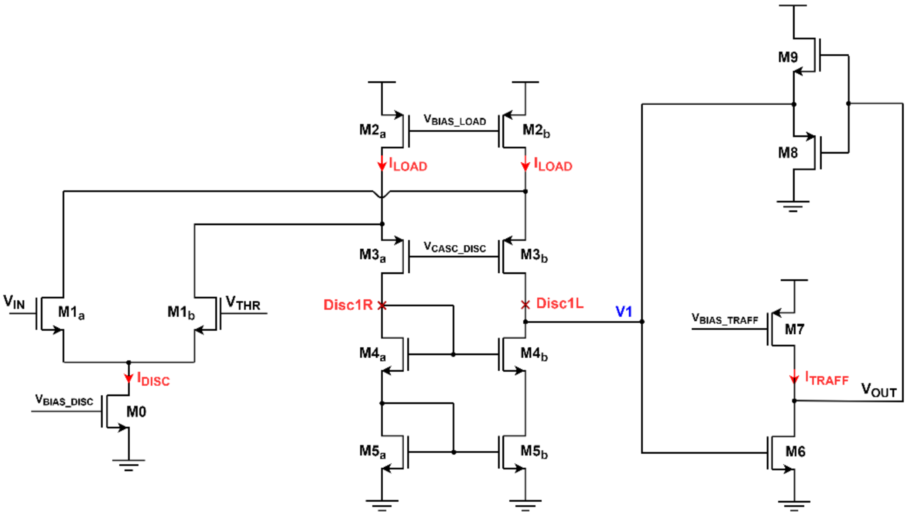


Figure 6.37. Scheme of the comparator.

6.3.5 Digital-to-Analog Converter

The transistor mismatch in the front-end and in the comparator and the power drop along the pixel matrix generate an undesired offset of the baseline. An uncorrected comparator offset results in a systematic error added to the signal. The offset in each electronic pixel must be equalized in the pixel array to obtain a uniformly distributed effective threshold. Otherwise, the threshold dispersion affects the energy resolution and increases the fixed pattern noise in the image. Our threshold equalization method relies on the principle that if the comparator's threshold is set at the DC level of the front-end baseline, the discriminator starts firing a series of pulses due to the electronic noise [37]. The global DAC in the analog periphery fixes a desired global threshold for all pixels, while a fine-tuning DAC in each pixel compensates for the pixel-to-pixel threshold variation. Figure 6.38 presents the topology of a constant current 5-bit DAC to inject current in the two nodes 'Disc1L,' and 'Disc1R' of the comparator presented in Figure 6.37. The injected current unbalances the comparator and modifies its effective threshold. For instance, if the baseline level is lower than the threshold, the transistor M1$_b$ in Figure 6.37 drives more current than M1$_a$, leading to an increase of the current in M3$_b$. The current mismatch between the load branches of the folded cascode amplifier is solved by injecting a small current in the node Disc1R and, at the same time, pulling out the same amount from the node Disc1L.

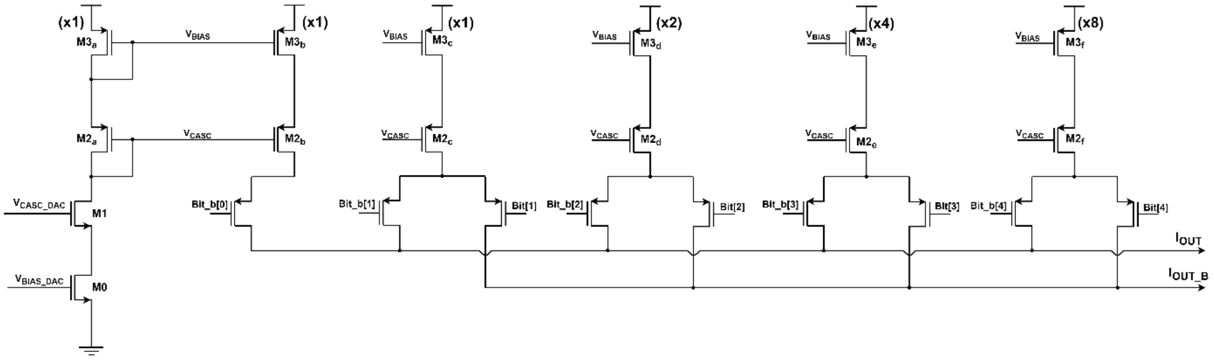


Figure 6.38. Schematic of the 5-bit DAC used for the threshold calibration.

On the left-hand side of the topology, the diode-connected configuration provides the adjustment step I_{LSB} to the current branches in the DAC. The current array is not a regular 5-bit binary structure, as the Most Significant Bit (MSB) branch contains twice fewer components, therefore, occupies twice less area in the pixel. In addition, the same current factor scales the two first branches. The PMOS switches connected to the branches are configured by the digital pixel through a 5-bit digital code. This topology provides two complementary output currents, I_{OUT} and I_{OUT_B}, respectively connected to the nodes 'Disc1L' and 'Disc1R' in the comparator. The output current difference ranges from – 15 I_{LSB} to 16 I_{LSB}, with a step of I_{LSB} given in Table 6-1.

Code: Bit_b[4:0]	I_{OUT}	I_{OUT_B}	$\Delta I_{OUT} = I_{OUT} - I_{OUT\_B}$
00000	16 I_{LSB}	0	16 I_{LSB}
00001	15 I_{LSB}	0	15 I_{LSB}
00010	15 I_{LSB}	I_{LSB}	14 I_{LSB}
00011	14 I_{LSB}	I_{LSB}	13 I_{LSB}
00100	14 I_{LSB}	2 I_{LSB}	12 I_{LSB}
00101	13 I_{LSB}	2 I_{LSB}	11 I_{LSB}
00110	13 I_{LSB}	3 I_{LSB}	10 I_{LSB}
00111	12 I_{LSB}	3 I_{LSB}	9 I_{LSB}
…	…	…	…
…	…	…	…
11100	2I_{LSB}	14 I_{LSB}	-12 I_{LSB}
11101	I_{LSB}	14 I_{LSB}	-13 I_{LSB}
11110	I_{LSB}	15 I_{LSB}	-14 I_{LSB}
11111	0	15 I_{LSB}	-15 I_{LSB}

Table 6-1: DAC response value versus the digital code of threshold adjustment DAC.

The front-end electronic noise can be used to compensate for the effective threshold spread between pixels [37]. By setting the threshold of the comparator at the desired baseline level, the comparator starts firing pulses due to electronic noise. For a given input offset at the comparator, an optimal DAC setting code is found to unbalance the comparator, resulting in a series of pulses at its output.

The upper plot in Figure 6.39 shows the threshold dispersion effect in the comparator without threshold adjustment. The spread in time follows a Gaussian distribution shape with a standard deviation equal to 7.91 µs, as shown in the bottom plot. This fluctuation in time translates into an offset mismatch of 1582 e^- in HDRM and 879 e^- in LNM. This threshold fluctuation adds quadratically to the electronic noise and worsens the minimum detectable charge given by equation (3-31). The front-end response after threshold equalization is shown in Figure 6.40. The spread is reduced with a standard deviation equal to 460 ns. The offset mismatch after threshold calibration is 92 e^- in HDRM and 51 e^- in LNM. The minimum detectable charge is dominated by the intrinsic electronic noise of the front-end.

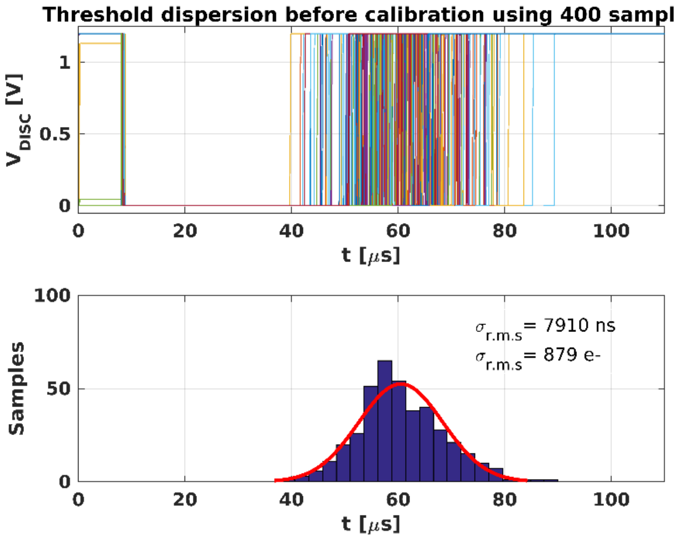


Figure 6.39. Simulated threshold dispersion of the front-end without threshold tuning. The offset mismatch is 879 e$^-$ r.m.s. in LNM.

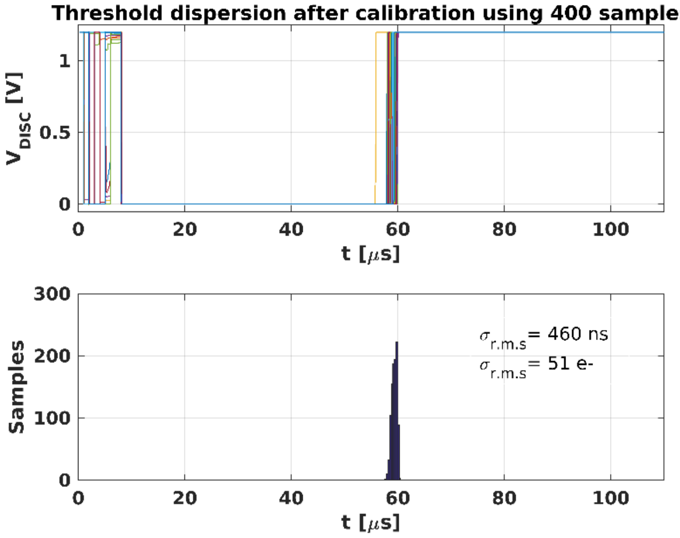


Figure 6.40. Simulated threshold dispersion of the front-end after threshold calibration using 5-bit tuning DAC. The offset mismatch is 51 e$^-$ r.m.s. in LNM.

The analog chain processes each X-ray photon depositing its total energy within the sensor pixel's 75 x 75 µm² collection area. This mode is referred to as "Single Pixel Mode." However, the diffusion effect in thick sensor materials and the fluorescence photons in high-Z materials lead to charge sharing between neighboring pixels. A charge sharing correction architecture reconstructs the total charge in a cluster of 2x2 pixels and reduces the spectral distortion produced by charge diffusion. This mode is called "Charge Summing Mode" (CSM).

6.3.6 Implementation of the charge sharing correction

The analog and digital pixels perform two processes in parallel to mitigate the effect of charge sharing described in 4.3.1. First, the pixel with the largest charge deposit from its neighbors is determined through a network of arbitration circuits in the digital pixel. In parallel to this step, the total charge must be reconstructed in a cluster of 2 x 2 pixels to obtain a 150 x 150 µm² equivalent collection area. The two functions could be executed in offline post-processing, but that would not be compatible with high-rate applications due to the large amount of data required off-chip. An alternative way for on-chip correction would be to make digital sum in each electronic pixel. Full digital processing benefits from the scaling down of CMOS technologies but is limited by the loss of sub-threshold charge [178]. The charge reconstruction in the analog pixel overcomes those limitations [87].

The front-end pixel configured in Charge Summing Mode is represented in Figure 6.41. There are two pulse-shaping circuits called “Local shaper” and “Sum shaper”, followed by their associated comparators. The local shaper provides the energy information about the local charge. In addition, an arbitration circuit in the digital pixel compares the local signal with its neighbors to determine the largest charge deposit. The arbitration circuit relies on the TOT information. The sum shaper fulfills two functions that are filtering and summing. Indeed, the output currents from adjacent pixels are fed to the summing amplifier for the charge reconstruction. Implementing four additional pole-zero cancellation blocks per pixel permit minimizing the input capacitance of the summing shaper. The pixel E sends its local charge to the summing node of the pixels D, G, and H and receives the charge contribution from the pixels B, F, and C. The reconstructed charge is compared to a threshold (V_{THR_SUM}) using a discriminator.

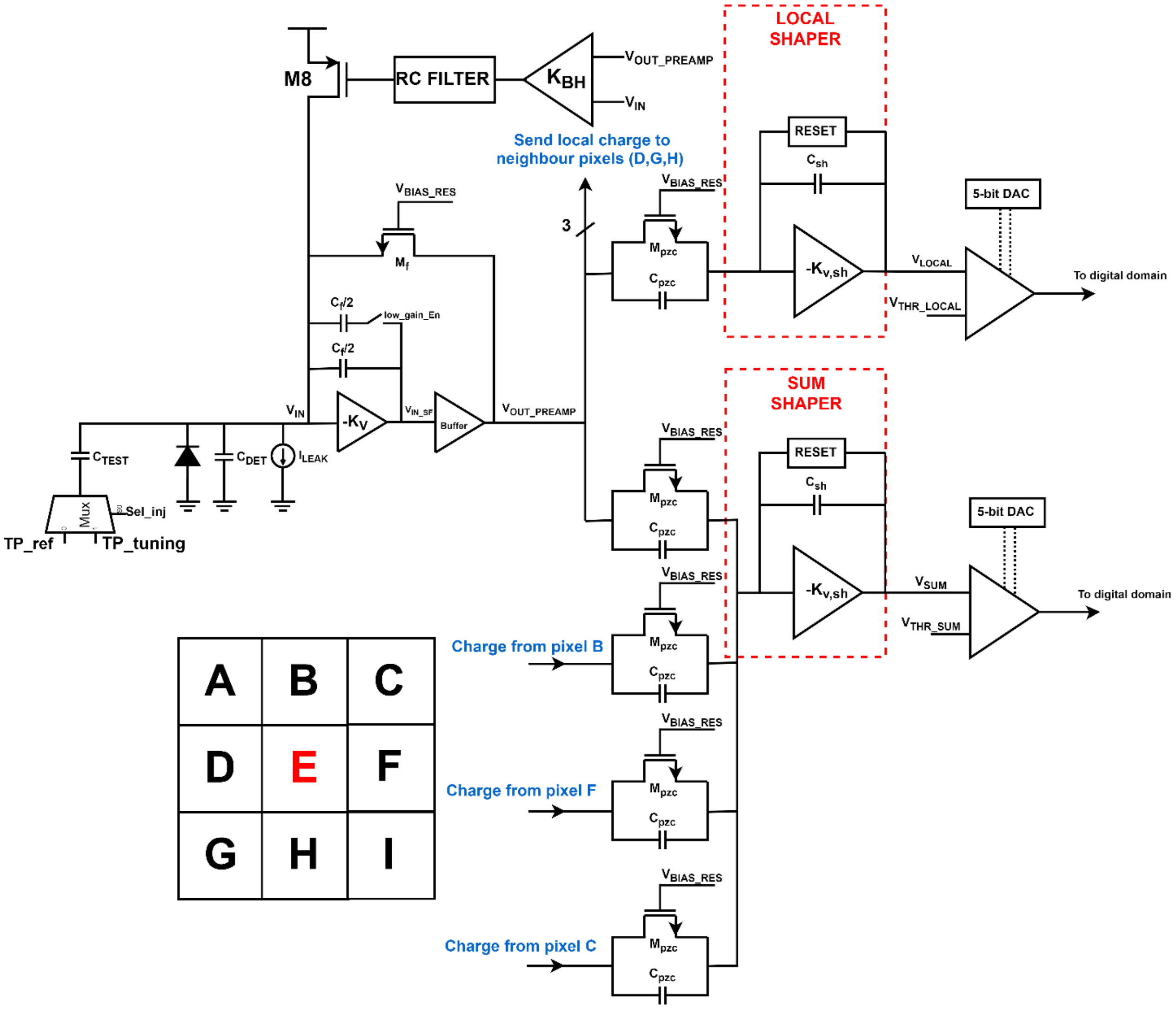


Figure 6.41. The architecture of the analog front-end configured in Charge Summing Mode.

The noise is also added when combining the signals from adjacent pixels. Figure 6.42 plots the electronic noise when the front-end is configured in CSM for the three analog modes of operations. The noise is approximately twice larger in CSM than in SPM. For instance, for C_{DET}= 150 fF in CSM, the electronic noise equals 265 e^- in HDRM. The lower thermal noise contribution in LNM decreases the overall noise at 210 e^-, whereas the fast discharge to the baseline in UFM leads to an electronic noise of 320 e^-. The wider spread of the baseline requires a larger adjustment step for the threshold adjustment. Therefore, independent global DACs in the analog periphery define the step I_{LSB} for the two tunings DACs.

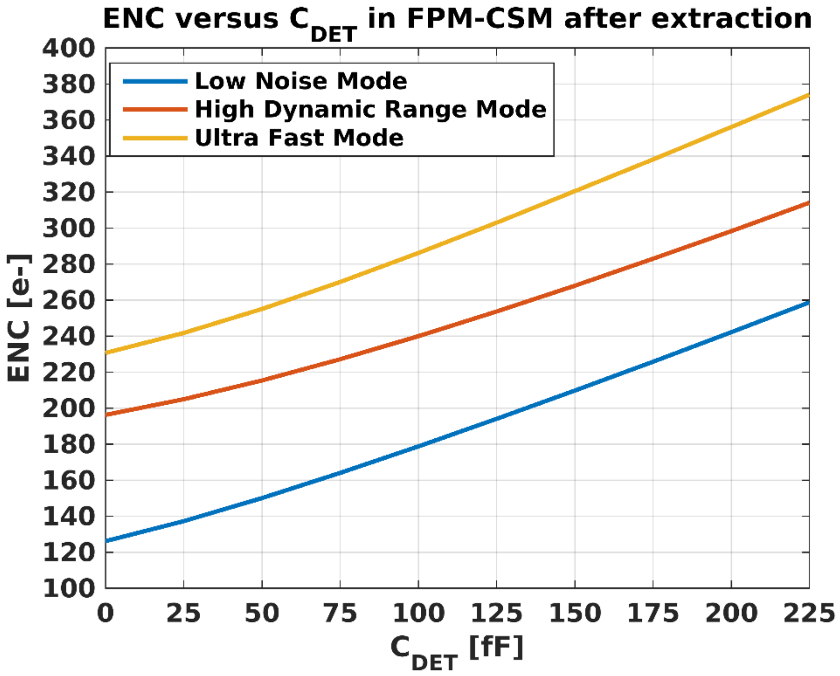


Figure 6.42. Equivalent Noise Charge versus detector capacitance when configured in FPM-CSM.

The fluorescence photons studied in 3.1.2.4 deposit their energies far from their initial impact point. Multiple hits are detected for a single incoming photon if the mean free path is larger than the pixel size. Medipix4 proposes the pixel size programmability with 75 µm pixel pitch in Fine Pitch Mode (FPM) and 150 µm pixel pitch in Spectroscopic Mode (SM) to deal with this limitation.

6.3.7 A configurable pixel for spectroscopic imaging

FPM is optimal for applications using Si or GaAs as sensor material, while SM is more suitable with CdTe, CdZnTe or perovskites [108]. The front-end can be configured in SPM or CSM for both pixel pitches, providing four modes of operations with different charge collection areas: FPM-SPM, FPM-CSM, SM-SPM, and SM-CSM. In FPM-CSM, the spatial resolution is 75 µm, but the spectra correspond to what would be achieved with four times larger pixels. Similarly, in SM-CSM the spatial resolution is 150 µm while having 300 µm x 300 µm charge collection area.

6.3.7.1 Fine Pitch Mode / Single Pixel Mode

In Fine Pitch Mode (FPM) and Single Pixel Mode (SPM), all single pixels work independently from their adjacent pixels. The readout pixels are bump bonded to 75 µm pitch sensor pixels. This mode fulfills the demands of a high count-rate and a fine spatial resolution. The summing shaper is turned off, as shown in Figure 6.43. The non-active blocks are not shown in the figure for clarity. The two comparators are connected to the local shaper providing two thresholds independently set by two global 14-bit DACs in the analog periphery.

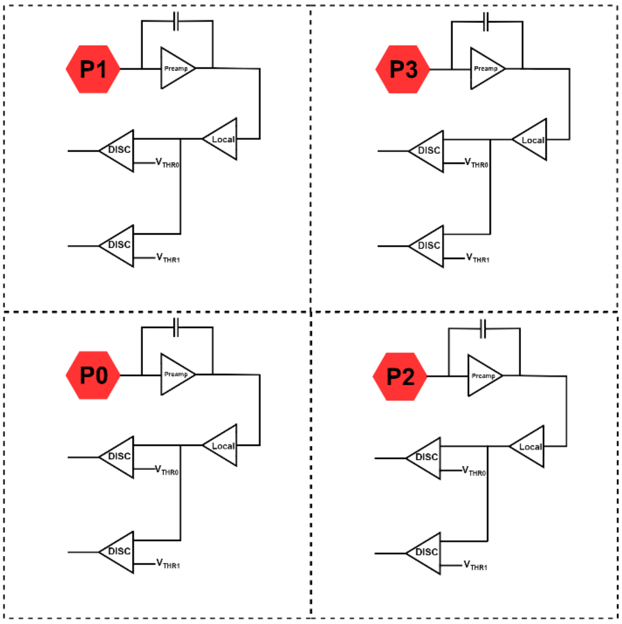


Figure 6.43. Configuration of the analog pixel in FPM-SPM.

6.3.7.2 *Fine Pitch Mode / Charge Summing Mode*

The charge is summed in every cluster of 2x2 pixels, and the hit is assigned to the pixel with the largest energy deposit. Figure 6.44 shows the configuration of the front-end in FPM-CSM. The summing shaper in every pixel takes its own local energy contribution summed to the energy of the adjacent pixels located on its left, upper, and upper-left sides. For instance, P0 takes its own contribution combined with the one coming from P1, P2, and P3. One threshold is used for the charge arbitration and one for the reconstructed charge.

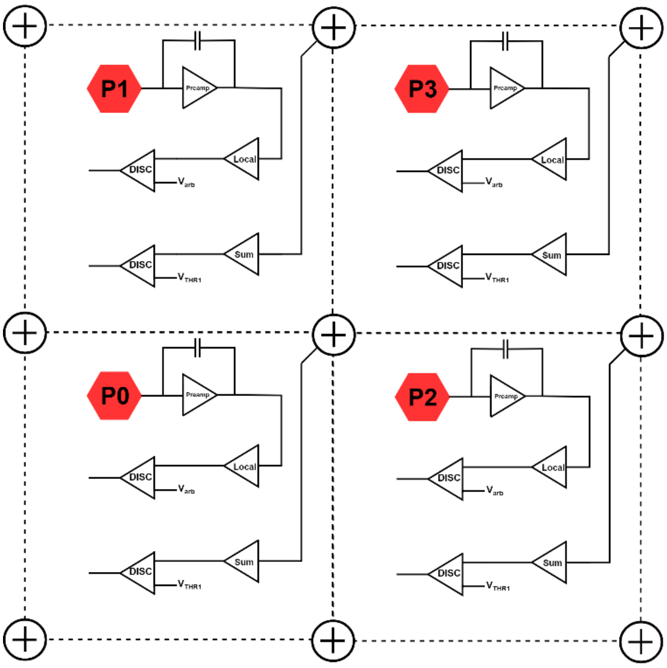


Figure 6.44. Configuration of the analog pixel in FPM-CSM.

6.3.7.3 Spectroscopic Mode / Single Pixel Mode

In Spectroscopic Mode, one pixel in a cluster of 2x2 pixels is connected to a 150 µm pitch sensor pixel. In Figure 6.45, P0 is the readout pixel connected to the semiconductor material, and its summing shaper is turned off in SPM. In the case of pixels P1, P2, and P3, the CSA and both pulse-shaping circuits are powered-down. However, their comparators and associated turning DACs are connected to the output of the local shaper in P0, proving eight independent thresholds. The thresholds can be individually set using 14-bit DACs in the analog periphery. P0 is called the "master pixel," whereas P1, P2, and P3 are called the "Slave Pixels." The cluster containing the master pixel and its slave pixels is called "superpixel."

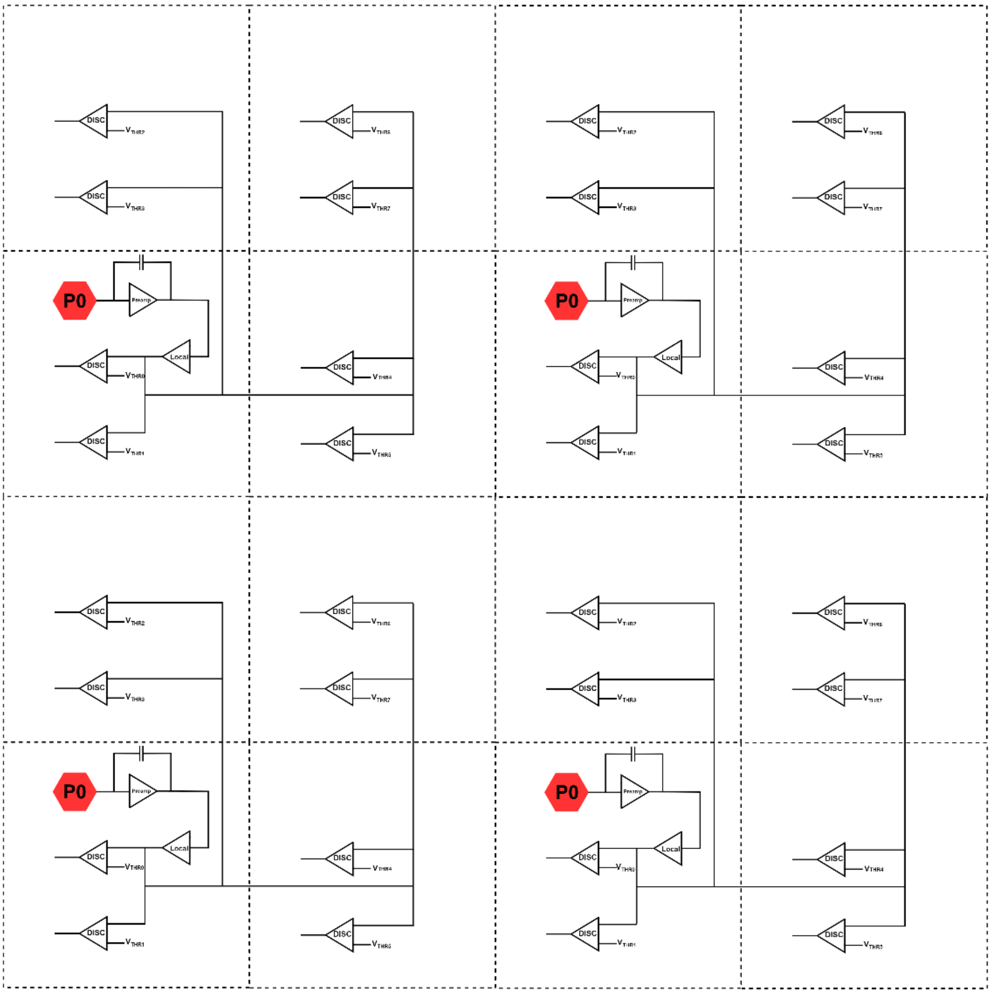


Figure 6.45. Configuration of the analog pixel in SM-SPM.

6.3.7.4 Spectroscopic Mode / Charge Summing Mode

A charge collection area equal to 300x300 µm² is possible in SM-CSM. Only the master pixel P0 has all its circuits operating, while the slave pixels provide the thresholds for the spectroscopy measurement. The local threshold in P0 corresponds to the arbitration threshold, and seven thresholds are associated with the discrimination of the reconstructed charge. The block diagram is illustrated in Figure 6.46.

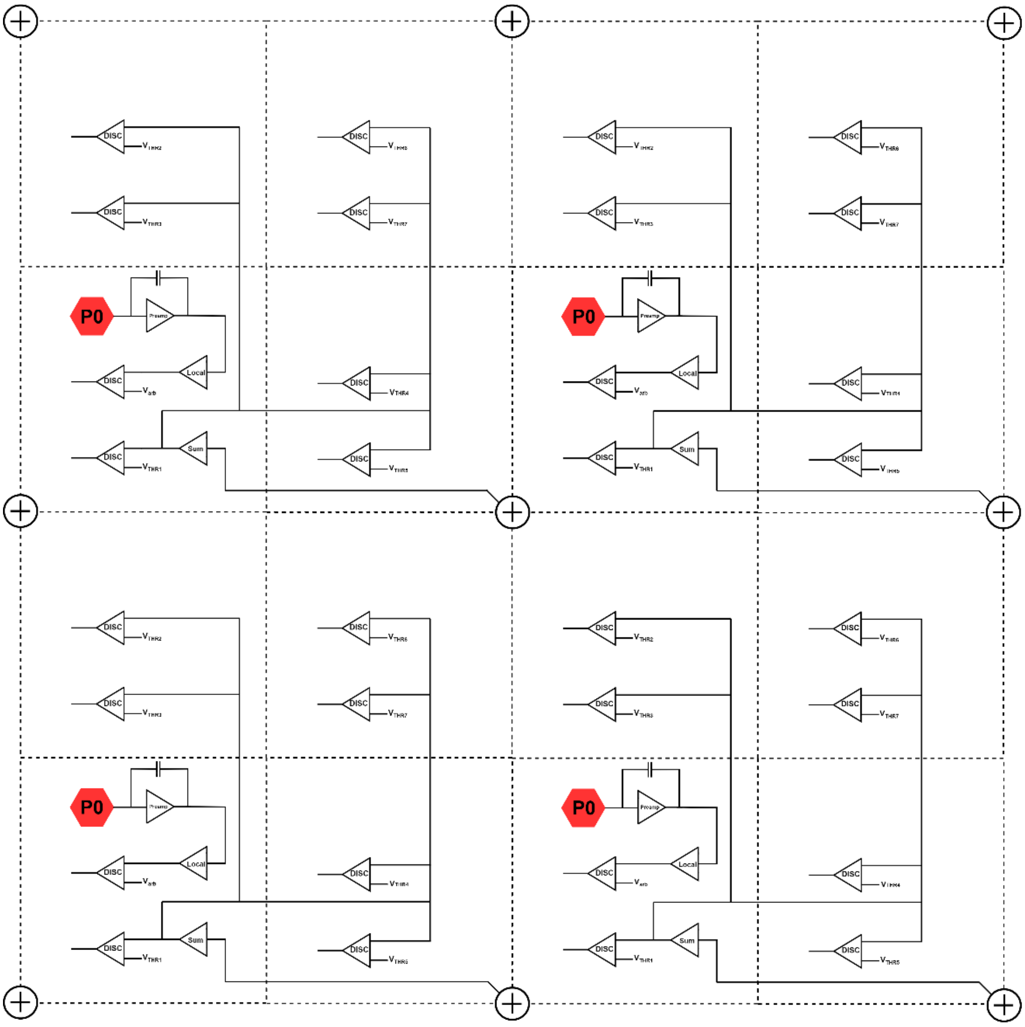


Figure 6.46. Configuration of the analog pixel in SM-CSM.

6.3.7.5 Summary

Table 6-2 summarizes the number of thresholds available in the different modes of operations. Moreover, each mode can be configured in HDRM, LNM, or UFM, providing 12 configurations for the front-end.

Operation modes	Pixel size (μm^2)	Area of charge collection (μm^2)	Thresholds
Fine Pitch Mode – Single Pixel Mode	75 x 75	75 x 75	2
Fine Pitch Mode – Charge Summing Mode	75 x 75	150 x 150	1
Spectroscopic Mode – Single Pixel Mode	150 x 150	150 x 150	8
Spectroscopic Mode – Charge Summing Mode	150 x 150	300 x 300	7

Table 6-2: Mode of operations in Medipix4. The charge collection area can be increased when the readout is used with high-Z materials. The number of thresholds is indicated in the last column.

Independent global DACs in the analog periphery to bias the analog pixel benefit the optimization of the front-end for each configuration. Figure 6.47 and Figure 6.48 plot the ENC versus the detector capacitance in SM-SPM and SM-CSM, respectively.

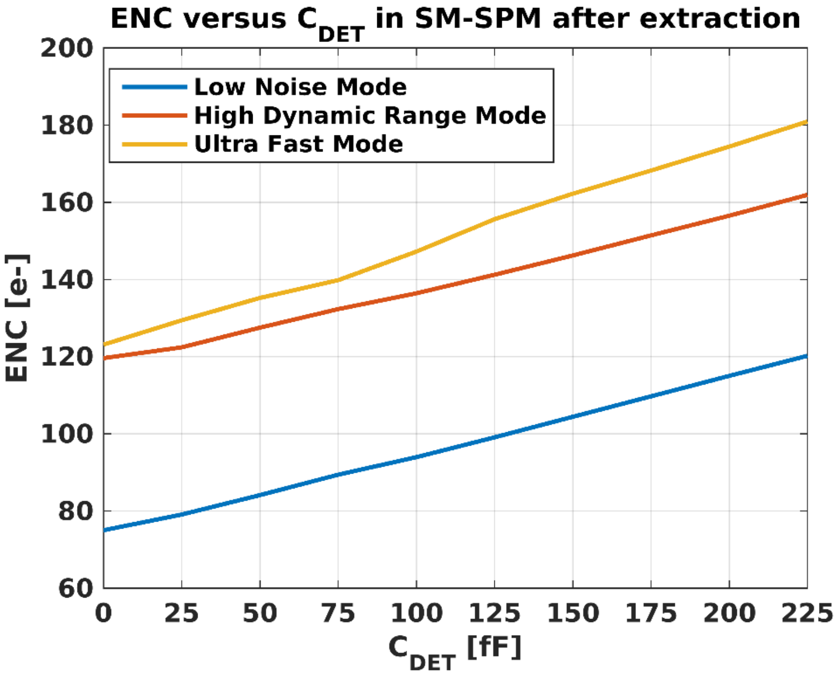


Figure 6.47. ENC versus detector capacitance in SM-SPM for the three analog configuration modes.

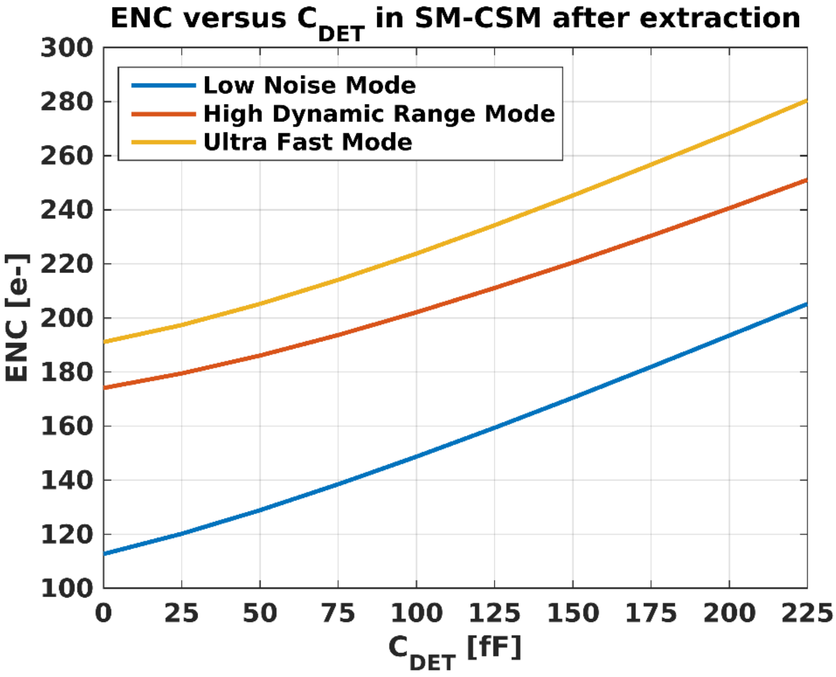


Figure 6.48. ENC versus detector capacitance in SM-CSM for the three analog configuration modes.

6.4 The pixel digital circuitry

The digital pixel processes the comparator output pulse and decides how the binary counters are incremented. It contains pulse-processing logic to attribute the hit to the correct pixel. The communication between the digital pixel and the digital EoC permits loading the pixel configuration data and reading. The first part focuses on methods to deal with pile-up events. The digital pixel architecture is briefly discussed in the second part.

6.4.1 Techniques to improve the spectroscopic performances at high-rates

In [110], the authors offer their vision for the future of photon-counting detectors in medical X-ray Computed Tomography (CT) and X-ray imaging. One of the main limitations is the pulse pile-up due to the intrinsic dead time of the counting systems. The unattenuated X-ray flux reaching the CT systems with no additional filters is in the order of 10^9 counts/mm^2. Considering a pixel with a size dimension of 1 mm x 1mm, a dead time smaller than 50 ps is required to have a count-rate loss of less than 5% [110]. Such fast systems are challenging to implement due to ballistic deficit and charge sharing between pixels degrading the energy spectrum. The future of photon-counting detectors for medical applications should focus on the filters to optimize the intensity and spectrum of X-rays and the calibration and compensation methods to deal with pile-up events [110]. New ideas are studied, and some are implemented for dealing with pile-up events in Medipix4 ASIC.

6.4.1.1 Motivation and new ideas for dealing with pile-up events

The pile-up events can be divided into two categories. First, the tail pile-up comes from the long discharge time constant in the analog pixel. In the case of unipolar shaping pulse, the event falling on the tail of its predecessor has its energy overestimated. For bipolar shaping pulse, its energy is underestimated due to the undershoot in the output signal [179]. The second category is the peak pile-up, in which the coincidences of the events happen around the rising edges [179]. A new solution is studied to process pile-up events using polychromatic sources in the framework of this thesis. By assigning the tail pile-up events into the correct energy bins, the weight of low-energy photons is not overestimated in the spectral information. The proposed algorithm uses a large number of thresholds available per pixel (up to 8 in SM). By equally spacing the thresholds, the pulses are processed by analyzing the states of the corresponding comparators. Each time the rising edge of a comparator's output detects an event, a circuit counts the total number of rising edges, and attributes the photon to the Nth counter.

Figure 6.49 illustrates events that are processed by a unipolar-shaped front-end with three equally spaced thresholds. In this example, the first event is correctly processed, but the second is attributed to a higher energy bin (counter associated with "DISC_H") due to tail pile-up. The 5th event is also misallocated to the counter corresponding to "DISC_M." Applying the algorithm, the 5th event is correctly attributed to the first energy bin, which is the counter associated with "DISC_L." However, the second event is still misallocated to a higher energy bin, as its energy is very close to the energy threshold Vth_H. This algorithm is referred to in this thesis as "pile-up correction."

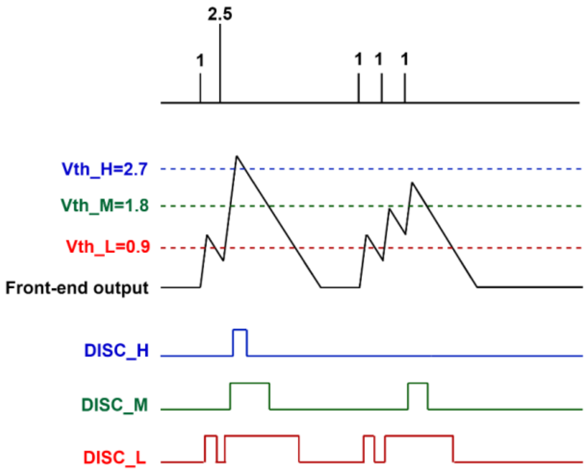


Figure 6.49. Illustration of pile-up pulses in the front-end with multi-thresholds.

6.4.1.2 Matlab model and results

A simplified model of the front-end using the mathematical tools Matlab permits to simulate the algorithm for high-rates. The convolute function between the time response and the random time arrival provides an accurate approximation. The time response of the front-end is:

$$V_{FE}(t) = \frac{Q_{IN}R_f}{\tau_{p1}-\tau_{r1}} * \left(e^{-\frac{t}{\tau_{p1}}} - e^{-\frac{t}{\tau_{p2}}}\right) \text{ with } \begin{cases} \tau_{p1} = R_f * C_f \\ \tau_{p2} = \frac{C_fC_L+C_{DET}C_L+C_fC_{DET}}{g_{m1}C_f} \end{cases} \qquad (6\text{-}48)$$

Q_{IN} is the input charge, R_f and C_f are respectively the feedback reset element and capacitance in the CSA, C_{DET} is the detector capacitance, C_L the load capacitance, and g_{m1} is the transconductance value of the input transistor.

The arrival time of the events fits the Poisson distribution statistics. The probability of observing n events in an interval with mean value µ is:

$$P(n) = \mu^n \frac{e^{-\mu}}{n!} \qquad (6\text{-}49)$$

Figure 6.50 illustrates the front-end response using this model. The input energy follows the Gaussian distribution with a mean value of 13 ke$^-$ and a standard deviation of 4 ke$^-$, whereas the arrival time follows the Poisson statistics with 1 µs mean time between consecutive photons.

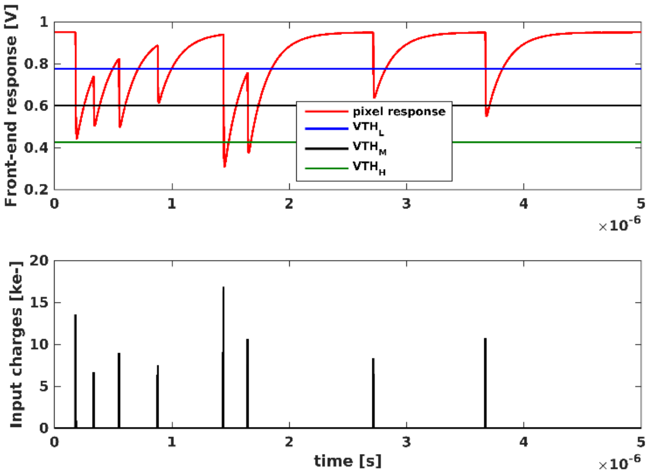


Figure 6.50. Model of the front-end response for a polychromatic input source having a Poisson distribution for the time arrival.

To quantify the pixel count-rate capability with the new algorithm, random 10 keV input pulses are used with the lower threshold set at 7 keV. The front-end is configured in FPM-SPM-HDRM. The results are shown in Figure 6.51. The red points corresponds to the simulated count-rate without pile-up correction, the simulated 10% dead-time loss is 444 Mcps/s/mm². The count-rate is extended by a two factor with the pile-up correction at 1 Gcps/s/mm².

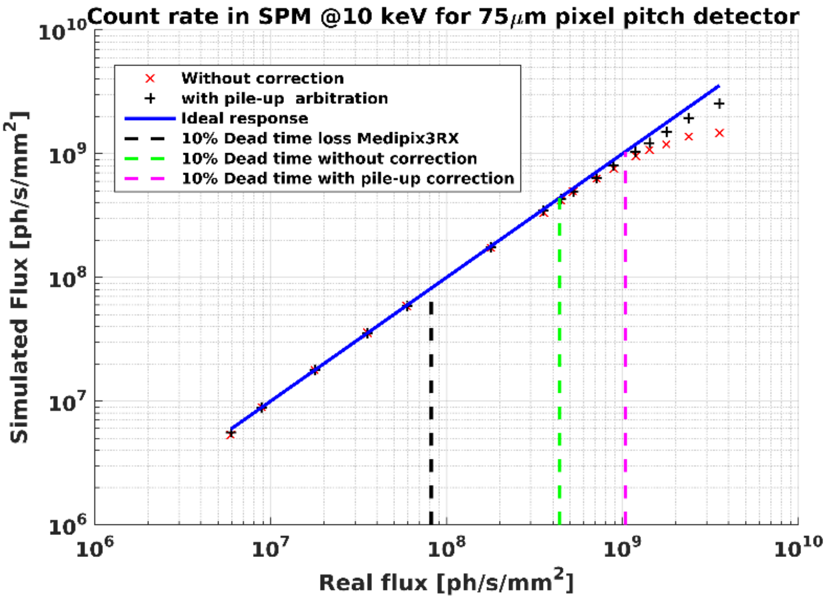


Figure 6.51. Simulated count-rate capability of the Medipix4 with and without pile-up correction for 10 keV input monochromatic source and threshold at 7 keV. The 10% dead-time loss is improved by a factor 2 when activating the pile-up correction.

6.4.1.3 RTL simulation framework and spectroscopic performances of Medipix4

The results presented above concern the front-end operating in Single Pixel Mode. In addition, the fluorescence photons and charge-sharing effects are not taken into account. The RTL simulation framework developed for functional verification is adapted to simulate the spectroscopic performance of Medipix4 at different count-rates and for the different modes of operations (by A. Pulli and X. Llopart). The RTL simulation framework is particularly advantageous to test the performances in CSM in which the analog and digital pixels perform two processes in parallel to mitigate the effect of charge sharing. Furthermore, realistic hits injection is generated for a 2 mm thick CdTe sensor with 60 keV monochromatic source and with fluorescence photons. The pile-up correction algorithm is tested using this new RTL simulation framework. The results were not fully satisfying to implement the pile-up correction in the digital pixel. Indeed, implementing this mode requires extra logic without a significant increase in the spectroscopic performance. This encouraged the implementation of the Ultra-Fast Mode (UFM) by configuring the global DACs in the analog periphery. The simulated count-rate performances of the chip configured with a 150 µm pitch sensor (SM) and with charge sharing correction (CSM) for the different analog modes of operations (HDRM, LNM, and UFM) are presented in Figure 6.52. The black curve represents the simulated count-rate capability of Medipix3RX configured in SM-CSM; the 10% dead-time loss is 4.3 Mcps/s/mm². This value matches with the measured count-rate capability in [109]. The orange, blue, and yellow curves plot the simulated performances in LNM, HDRM, and UFM, respectively. The 10% dead-time loss is 5.5 Mcps/s/mm² in SM-CSM-LNM, 9 Mcps/s/mm² in SM-CSM-HDRM, and 19 Mcps/s/mm² in SM-CSM-UFM showing factor 5 improvement compared to its predecessor.

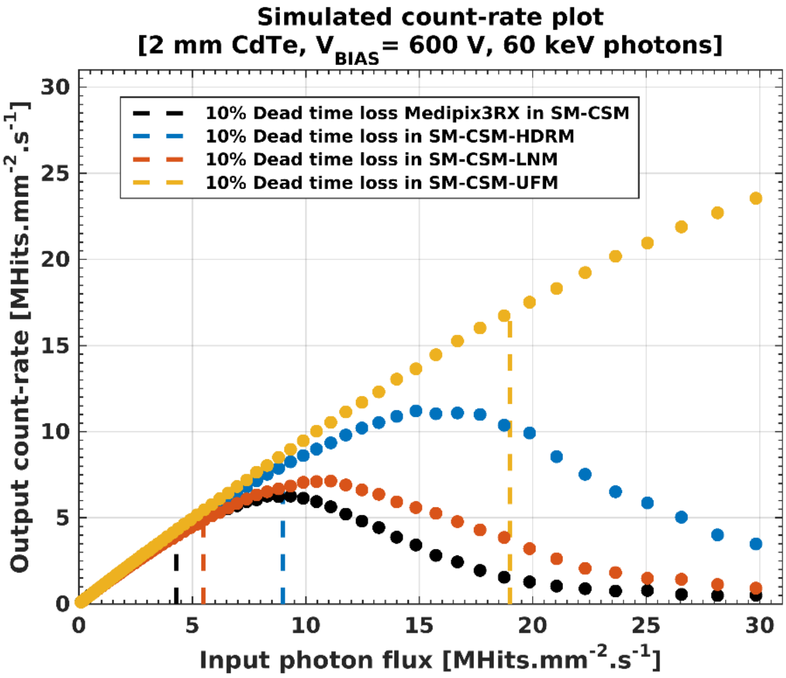


Figure 6.52. The count-rate capability of the chip in SM-CSM for a 60 keV input source and a 2 mm think CdTe sensor (courtesy to A. Pulli).

6.4.1.4 Digital mode of operations

The digital pixel can be configured in:

- Window Discrimination threshold mode: only events falling within the energy window defined by the thresholds are taken into account. This mode enables optimal use of the counter depth by attributing each event to a single counter bin.
- Pile-up filtering mode: tail pile-up events are not considered during imaging to reduce spectral distortion at higher count rates.

6.4.1.4.1 SPM with Pile-up Filtering mode OFF and Window Discrimination mode OFF

The working principle of the digital pixel configured in SPM with Pile-up Filtering OFF and Window Discrimination OFF is shown in Figure 6.53. The impulses in the top plot illustrate the time of arrival of seven events to the detector; the amplitude of the events is proportional to their energies. Photons 3, 5, and 6 suffer from the tail pile-up. The example illustrates the processing of those events by the Medipix4 front-end with three energy thresholds set at 1 ke$^-$, 5 ke$^-$, and 9 ke$^-$. The response of the three comparators and their associated counters are shown in the bottom plot. The 6th event is wrongly associated to the higher energy bin 'counter_H' due to tail pile-up. In addition, the counting is not optimized for the lower counter bins. Indeed, the lower energy bins fill up fast compared to the higher bins.

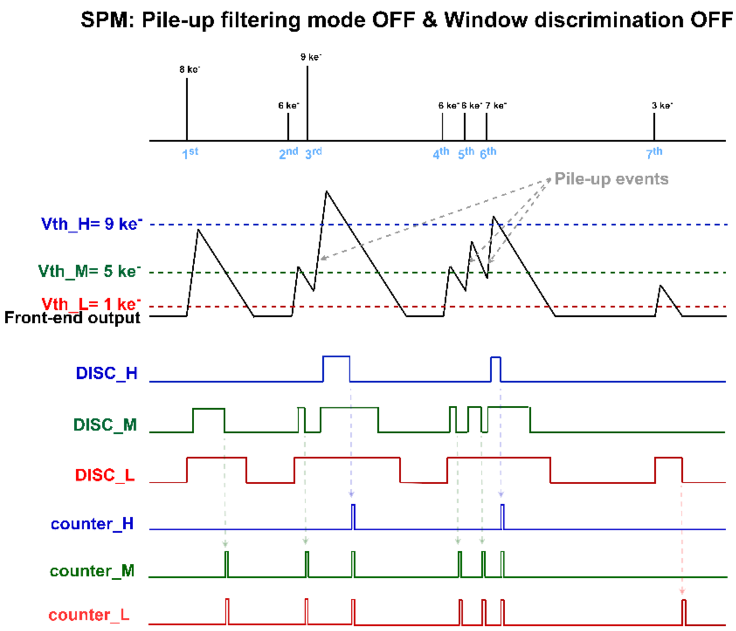


Figure 6.53. Working principle of the digital pixel configured in SPM with Pile-up Filtering mode OFF and Window Discrimination mode OFF.

6.4.1.4.2 SPM with Pile-up Filtering mode OFF and Window Discrimination mode ON

The working principle of the digital pixel configured in SPM with Pile-up Filtering OFF and Window Discrimination ON is shown in Figure 6.54. The counting is optimized for the lower counter bins. Indeed, only the counter associated to the highest detected energy threshold is incremented. The photons 1, 2, 4, and 5 are attributed to counter_M. However, the 6th event is still wrongly associated to the higher energy bin 'counter_H' due to tail pile-up.

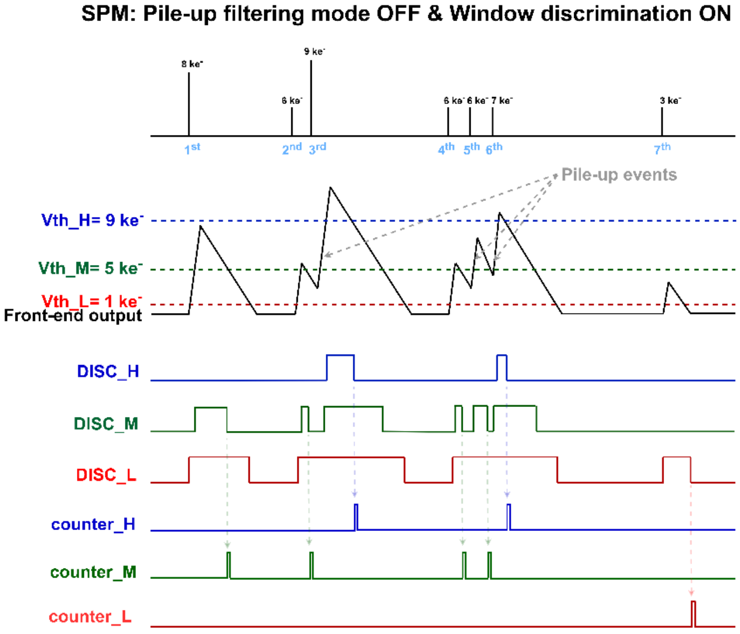


Figure 6.54. Working principle of the digital pixel configured in SPM with Pile-up Filtering mode OFF and Window Discrimination mode ON.

6.4.1.4.3 SPM with Pile-up Filtering mode ON and Window Discrimination mode ON

The working principle of the digital pixel configured in SPM with Pile-up Filtering ON and Window Discrimination ON is shown in Figure 6.55. The counting is optimized for the lower counter bins with the window discrimination threshold mode. Tail pile-up events are not taken into account during imaging to reduce spectral distortion at higher count-rates. The placement of the lowest threshold close to the baseline permits detecting events that are falling on the tail of its predecessor. The 3rd, 5th, and 6th events correspond to tail pile-up and are discarded.

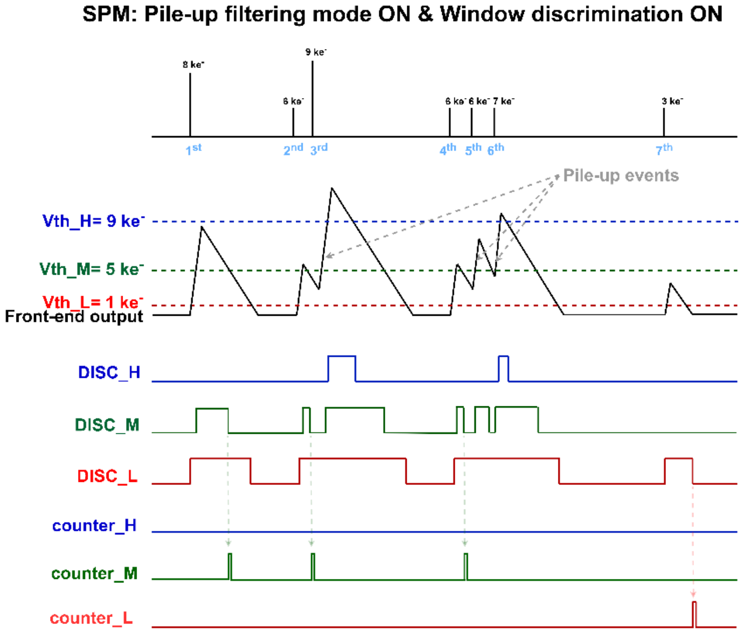


Figure 6.55. Working principle of the digital pixel configured in SPM with Pile-up Filtering mode ON and Window Discrimination mode ON.

6.4.1.4.4 CSM with Pile-up Filtering mode ON and Window Discrimination mode ON

The working principle of the digital pixel configured in CSM with Pile-up Filtering ON and Window Discrimination ON is shown in Figure 6.56. The counting is optimized for the lower counter bins with the window discrimination threshold mode. Like SPM, tail pile-up events are not taken into account during imaging to reduce spectral distortion at higher count-rates. The 3rd, 5th, and 6th events are discarded in this mode. If a pile-up event is detected, its predecessor is also removed in the measurement, as the correct allocation of the hit is not guaranteed. For this reason, the 2nd and 4th events are also discarded.

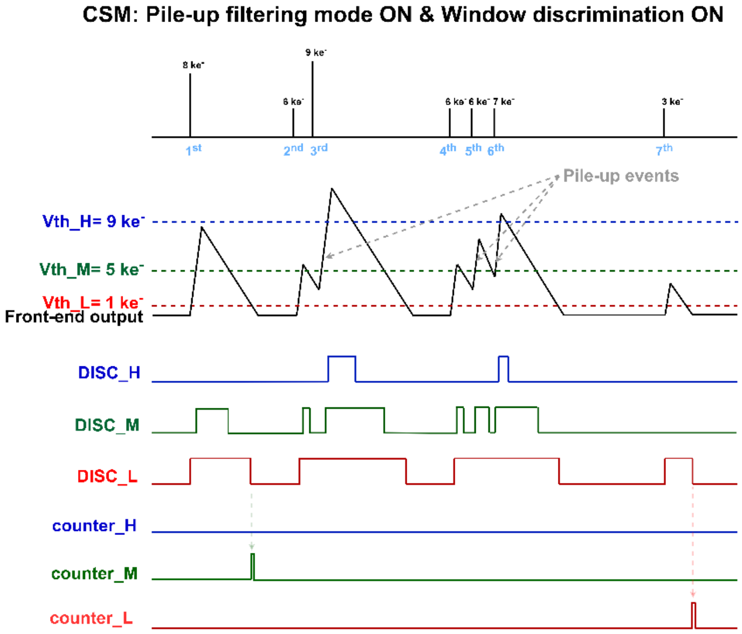


Figure 6.56. Working principle of the digital pixel configured in CSM with Pile-up Filtering mode ON and Window Discrimination mode ON.

6.4.2 Architecture

The digital pixel block diagram is shown in Figure 6.57. It contains the arbitration circuit for the hit allocation in CSM, the configurable counters, control logic for the communication to the digital EoC, and the register latches for pixel configuration. The arbitration circuit uses the falling edge of the comparator's output pulse (DISC_A) to compare the charge collected by the local pixel to its neighbors. If the local pixel has the largest charge deposit, only its associated CounterAL (+CounterAH) is incremented to avoid multiple counting for the same photon. In parallel to the hit allocation, the charge is reconstructed in a cluster of 2x2 pixels in the summing shaper. The synchronization block increments CounterBL (+CounterBH) if the winner pixel has one of its adjacent summing circuits above the threshold.

Each pixel contains four 12-bit counters named: CounterBL, CounterBH, CounterAL, and Counter AH. The counts of the energy bins can be read out in Sequential Read/Write (SRW) or Continuous Read/Write (CRW) modes. In SRW, the number of detected events is stored in a 1-bit, 2-bits, 12-bits, or 24-bits depth counter for each threshold. In the case of 24-bit SRW mode, CounterBL and CounterBH are associated to Disc_B, while CounterAL and CounterAH to DISC_A. When the signal "Shutter" is low, the number of counts is shifted from pixel to pixel towards the end of the column for readout. To achieve dead-time-free operation, the ASIC is programmed in CRW. In this mode of operation, the number of pulses is stored in a 1-bit or 12-bit depth counter while the readout is done through the other 1-bit, 12-bit depth counter. For this reason, the pixel cannot be configured in 24-bit mode in CRW to readout both thresholds simultaneously.

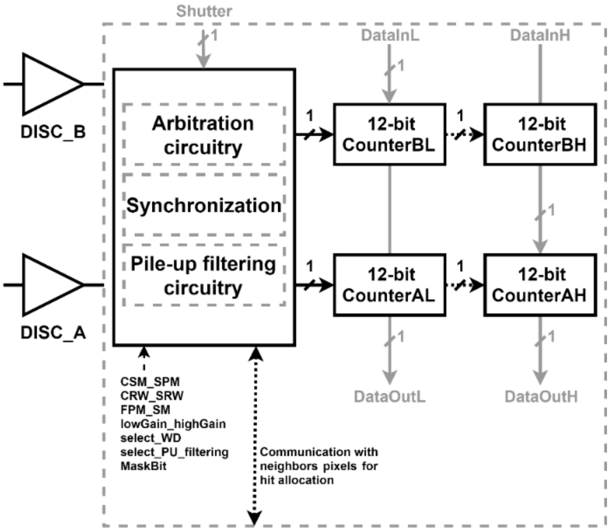


Figure 6.57. Simplified block diagram of the digital pixel.

6.4.3 Full pixel layout

Figure 6.58 shows the superpixel layout containing the master pixel on the bottom-left part and the slave pixels on the three other corners. The target transistors in the analog pixel have the same orientation and current direction as the biasing transistors in the Analog End-of-Column (EoC) for matching purposes [48] [47]. The low-power analog blocks are drawn with ELT transistors to suppress the drain leakage current. The PMOS transistors are decoupled to the power supply to maximize the ground supply fluctuation, while the NMOS transistors are decoupled to the ground supply line. The analog pixel local routing is drawn using the four lowest metals layers in the technology. Metal 5 biases the target transistors from the analog periphery, and Metal 6 shields the RDL lines to avoid the injection of charges from neighboring pixels. The high density of components at the center of the superpixel represents the digital circuitries. There are around 10000 transistors to implement the digital logic circuit. The layout of the analog blocks is drawn using deep N-well transistors to minimize the substrate noise generated from the digital switching logic. This protection suppresses the substrate noise injection into the bulk of standard NMOS transistors [180]. In addition, the analog inter-pixel communication lines are shielded to avoid the injection of charges from the digital logic.

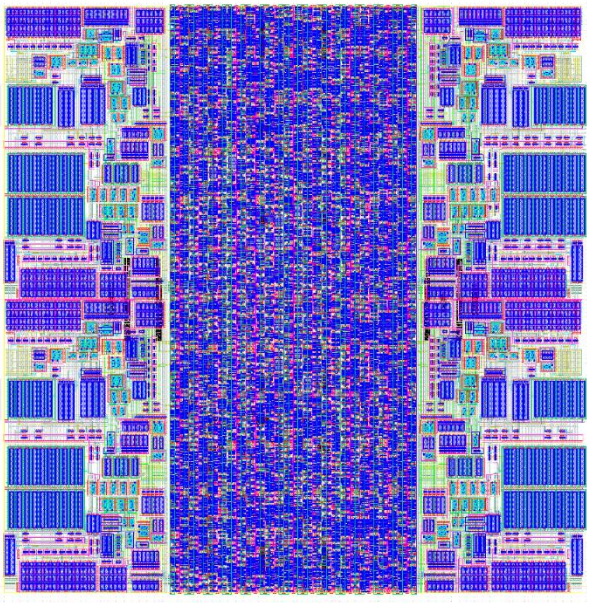


Figure 6.58. Layout view of the superpixel. The superpixel size dimension is 140.3 µm x 150 µm.

6.5 Full chip implementation

The Medipix4 design was integrated using the digital-on-top approach. The analog blocks are “islands” inside the digital design flow; they require careful physical and functional characterization before integration. Moreover, someone other than the designer verifies the analog blocks to maximize the chances of first time working silicon. The chip is thoroughly verified before being submitted. The verification was first performed using the behavioral models of the different blocks with RTL netlist. In a second phase, the design was synthesized, and the verification was carried out using the post-layout netlist [181]. The chip was submitted to the foundry for fabrication in March 2022. Figure 6.59 shows the layout of the entire Medipix4 ASIC. It contains 320 x 320 pixels designed in a CMOS 130 nm technology process with a power supply of 1.2 V. The chip size is 25530 µm x 24031 µm. The extra 1.5 mm in the vertical direction permits the bond extenders in the top and bottom parts of the ASIC. The extender pads enable the probing of the ASIC on a wafer and to wire-bond single ASIC without TSV processing. They can be diced off when the I/O interconnections are done through TSV processing. The extra 31 µm in the horizontal direction enables the communication between peripheries and accommodates the termination blocks for the analog pixels. Termination blocks at the extremities of the chip ensure uniformity of the pixels’ response in CSM. The chip size is 24 mm x 24 mm and covers 99.37% active area when using TSV connections only.

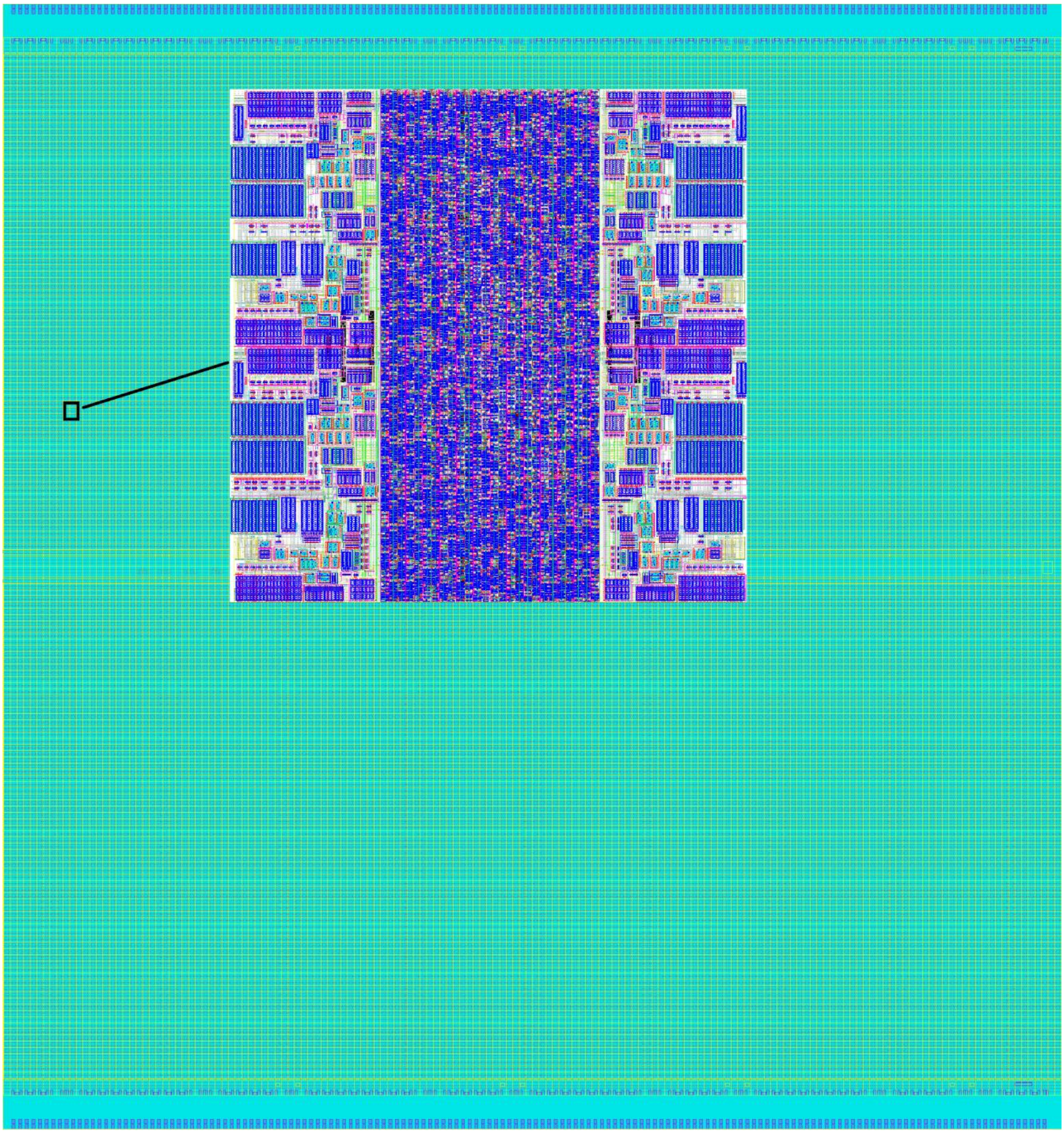


Figure 6.59. Medipix4 chip layout.

6.6 Summary

The Medipix4 ASIC is manufactured using a commercial 130 nm technology process having 8-metal layers and a power supply voltage of 1.2 V. The methodology “digital on top” is used for the chip integration due to the complexity of the digital circuitries and the high density of components. The chip contains 320 x 320 sensitive pixels with a size dimension of 75 x 75 µm². The chip is 4-sides buttable allowing construction of large-area detectors without dead-area; this is possible using the TSV last technology. For this reason, I/O M1 pads are designed with landing pads to connect to the printed circuit board. The readout pixels are slightly smaller than the sensor pixels in one direction allowing the integration of the peripheral circuitries underneath the sensor pads. A Redistribution layer connects the readout pixel to the sensor pad with an equalized input capacitance. The limiting factors in Medipix3RX and other photon-counting detectors motivate implementing a new architecture for the analog front-end. The analog pixel contains a Charge Sensitive Amplifier with a leakage current compensation scheme. A pole-zero cancellation after the CSA minimizes the overshoot in its output pulse. After the pole-zero cancellation block, two pulse shaping circuits implement the charge sharing correction algorithm.

The analog pixel contains two comparators and two associated threshold equalization DACs. The architecture enables pixel size programmability with 75 µm pixel pitch in FPM and 150 µm in SM. The SPM and CSM modes are available for both pixel pitches providing four different charge collection areas. In addition, the analog front-end can be configured in LNM, HDRM, and UFM. LNM provides a low noise figure at the cost of a reduced dynamic range up to 92 keV. In HDRM, the dynamic range is extended up to 154 keV. In UFM, a swift return to the baseline helps deal with high input flux at the cost of higher electronic noise. Table 6-3 provides a detailed summary of the simulated results for the twelve configurations of the front-end. The measured performances with Medipix3RX are shown in the first column as reference. The counts of the energy bins can be read out in SRW or CRW. The 48-bit registers in the digital pixel allow the readout of all thresholds simultaneously in CRW. In addition, the counting is optimized for low-energy bins with the window discrimination threshold mode. Finally, the digital pixel can be configured in "filtering mode." The pile-up events are discarded in the measurements. The analog periphery contains 29 DACs to configure the analog pixels, 320 Digital EoCs to configure the digital pixels, and 80 analog EoCs. The digital peripheries are located at the bottom and top of the ASIC. They contain the control logic, I/O, and TSV structures. The whole chip size is 25530 µm x 24031 µm. Medipix4 has been submitted for fabrication in silicon in March 2022.

		Medipix3RX	Medipix4 (HDRM)	Medipix4 (LNM)	Medipix4 (UFM)
Technology		130 nm CMOS technology	130 nm CMOS technology		
		8 metal layers	9 metal layers		
Pixel size	FPM	55 x 55 µm^2	75 x 75 µm^2		
	SM	110 x 110 µm^2	150 x 150 µm^2		
Number of pixels	FPM	256 x 256	320 x 320		
	SM	128 x 128	160 x 160		
Matrix arrangement		3 side buttable	4 side buttable		
Sensitive area		1.98 cm^2	5.76 cm^2		
Acquisition mode		Single Pixel Mode Charge Summing Mode	Single Pixel Mode Charge Summing Mode		
Polarity		Electron / hole	Electron		
Equivalent Noise Charge [e$^-$]	FPM-SPM	72 | 80 | 93 |100	165	117	193
	FPM-CSM	148 | 174 | 201 | 233	270	210	320
	SM-SPM	> 72 | 80 | 93 |100	155	112	170
	SM-CSM	> 148 | 174 | 201 | 233	235	190	265
Dynamic range [ke$^-$]		5 | 9| 12.5 | 18	35	21	35
Count-rate (10% dead time loss) [Mphotons.mm^{-2}s^{-1}] 60 keV input / Vth = 30 keV	SM-CSM	4.3	9	5.5	19
Number of thresholds	FPM-SPM	2	2		
	FPM-CSM	1 SPMa + 1 CSM	1 SPMa + 1 CSM		
	SM-SPM	4	8		
	SM-CSM	1 SPMa + 4 CSM	1 SPMa + 7 CSM		
Energy resolution with input 60 keV source [keV]		4.4	3	2.5	3
Power density in W/cm^2	FPM-SPM	0.27	0.5		
	FPM-CSM	0.51	0.5		
	SM-SPM	0.27	0.32		
	SM-CSM	0.51	0.37		
Pixel counters in SRW	FPM-SPM	2 x 1,2,6, 12 or 1 x24 bit	2 x 1,2, 12 or 24 bit		
	FPM-CSM	2 x 1,2,6, 12 or 1 x 24 bit	2 x 1,2, 12 or 24 bit		
	SM-SPM	8 x 1,2,6, 12 or 4 x 24 bit	8 x 1,2, 12 or 24 bit		
	SM-CSM	8 x 1,2,6, 12 or 4 x 24 bit	8 x 1,2, 12 or 24 bit		
Pixel counters in CRW	FPM-SPM	1 x 1,2,6 or 12 bit	2 x 1 or 12 bit		
	FPM-CSM	1 x 1,2,6 or 12 bit	2 x 1 or 12 bit		
	SM-SPM	4 x 1,2,6 or 12 bit	8 x 1 or 12 bit		
	SM-CSM	4 x 1,2,6 or 12 bit	8 x 1 or 12 bit		
Other features			Window Discrimination Pile-up filtering Mode		

Table 6-3: Summary of simulated performances of Medipix4 for the different modes of operations. The measured performances of the Medipix3RX are shown in the first column as reference.

Chapter 7 Conclusion

Hybrid pixel detectors consist of a 2-dimensional array of microscopic radiation-sensitive elements connected to their readout electronics. The two are connected using flip-chip technology. This hybrid pixel technology relies on direct detection for better energy and spatial resolution than indirect conversion. Moreover, the single pulse processing architecture in the readout electronics enables the detection of individual X-ray photons on an event-by-event basis. The implementation of complex processing circuits required for each application benefits from the modern deep sub-micron technologies. Single-photon processing enables noise rejection during imaging using the energy threshold per pixel. In addition, pixel segmentation helps to improve the spatial resolution, to lower the electronic noise, and achieve high count-rate capability. Those numerous features present hybrid pixel detectors as excellent candidates for particle tracking systems in High Energy Physics experiments. However, there are limiting factors in sensor material and the readout electronics that must be examined in the design of photon-counting detectors. Indeed, the high-Z materials offer an extended efficiency for detecting high-energy photons but suffer from charge trapping/recombination due to impurities. In addition, X-ray photons in high-Z materials produce characteristic fluorescence that travels away from its initial impact point before depositing its energy. On the other hand, small pixels are subject to charge sharing that distorts the measured energy spectrum.

Medipix and Timepix families of chips implement hybrid pixel detectors and address some limiting factors through different iterations. Indeed, the single pulse processing architecture in the Medipix1 chip demonstrated the possibility of X-ray imaging with total noise rejection. Medipix2 proved the feasibility of spectroscopic imaging at a small pixel pitch of 55 µm using two thresholds per pixel. However, the small pixel size manifested the effects of charge sharing between pixels and fluorescence photons in high-Z materials. A novel architecture eliminated the energy spectral distortion produced by charge diffusion in Medipix3RX. Many applications have used the Medipix3RX chip with different detector types. This demonstrated that hybrid pixel detectors are excellent candidates for high-rate spectroscopic imaging at a fine pitch. However, detectors using Medipix3RX and other X-ray imaging systems introduce a dead area in the imaging that prevents the construction of a seamless large-area detector.

Medipix devices demonstrated the possibility of spectroscopic X-ray imaging at high rates while preserving the spectral fidelity using inter-pixel architecture to correct the effect of charge sharing. Whereas, Timepix chips aim to extract the maximum information about the events and send their data off-chip for processing.

The design of a rail-to-rail buffer and the analog periphery for Timepix2 highlighted some key blocks in a large configurable ASIC. Timepix4 demonstrated the feasibility of a 4-side buttable chip with minimal dead area between the adjacent sensitive devices.

The main topic of this doctoral work concerns the architectural design of the Medipix4 ASIC development aimed for high-rate applications using high-Z materials. The Medipix4 chip is designed to read out a sensor of 320 x 320 pixels with dimensions of 75 µm x 75 µm or 160 x 160 pixels with dimensions of 150 µm x 150 µm. It is manufactured using a commercial 130 nm technology process with 8-metal layers and a power supply voltage of 1.2 V. The chip is 4-side buttable allowing the construction of large-area detectors with minimal dead-area. This is possible using the TSV last technology to access I/O landing pads implemented on the first layer of metal. The readout pixels are slightly smaller than the sensor pixels in one direction, allowing the integration of the peripheral circuitries underneath the sensor pads at the chip's top, middle, and bottom. A redistribution layer on the top metal connects the readout pixels to the sensor pads with an equalized input capacitance. The chip is terminated in both directions by wire-bonding extenders used during wafer probing, which can be diced off after TSV processing. The chip size is 24 mm x 24 mm and covers 99.37% active area when using TSV connections only.

Each analog pixel contains a Charge Sensitive Amplifier (CSA) with a DC leakage compensation network up to 50 nA. The latter is a baseline holder with a modified filter circuit with back-to-back connected transistors that provide a considerable large equivalent resistance. This solution permits the implementation of a relatively small metal capacitance requiring less area. A pole-zero cancellation circuit improves the rate capability for high input flux. Moreover, a new pulse shaping circuitry reduces the overshoot in the output pulse, minimizing the baseline drift at a high rate. Two threshold bins are available in each pixel, and each incoming X-ray photon is associated with one threshold bin for spectroscopy measurement. The analog chain configured in Charge Summing Mode (CSM) corrects the charge sharing effect in overlapping clusters of 2 x 2 pixels. Additionally, the pixel size can be programmed at 75 µm in Fine pitch Mode (FPM) and 150 µm in Spectroscopic Mode (SM). In SM-CSM, seven threshold bins are available compared with four in Medipix3RX. The front-end can be configured in three analog modes: High Dynamic Range Mode (HDRM), Low Noise Mode (LNM), and Ultra-Fast Mode (UFM). In HDRM and UFM, the linear range extends to 154 keV using a CdTe sensor, showing 40% improvement regarding Medipix3RX. In UFM, the count-rate capability of the front-end is 19 x 10^6 photons.mm^{-2}.s^{-1} at 10 % hit loss for a 150 µm pixel pitch and not affected by charge sharing effect, implying a factor 5 gain compared with Medipix3RX. Fast discharge to the baseline in UFM results in slightly higher electronic noise, increasing the minimum detectable charge. In LNM, the contribution of thermal noise is reduced, and its expected energy resolution is 2.5 keV for 60 keV input photon, implying a 55 % improvement compared with its predecessor.

The counts of the energy bins can be read out in Sequential Read/Write (SRW) or Continuous Read/Write (CRW). The 48-bit registers in the digital pixel allow the readout of all thresholds simultaneously in CRW. In addition, the counting is optimized for low-energy bins with the Window Discrimination threshold mode. Finally, the digital pixel can be configured in “Pile-up Filtering mode.” The pile-up events are discarded in the measurements.

The full Medipix4 chip functionality has been verified by simulation and meets the specifications. In March 2022, the chip was submitted to the foundry for fabrication. The first tests will be performed in June-2022.

Appendix: Noise calculation

The relevant noise contribution in the analog front-end comes from the white noise of the input transistor in the CSA, the parallel noise in the reset feedback element in the CSA, and the shot noise produced by the DC leakage current at the input. The noise generated in the pulse-shaping amplifier is neglected thanks to the gain factor introduced with the pole-zero cancellation circuit. The whole transfer function of the analog chain composed of the CSA, pole-zero cancellation circuit and local shaper is cumbersome for the noise calculation. The DC compensation feedback loops in the CSA and the pulse-shaping circuit are removed in the noise calculation as a first approximation. The simplified transfer function is:

$$\frac{V_{SHAPER\_OUT}}{I_{IN}} = K_{DC} * \frac{(1-s\tau_{sh,z1})}{(1+s\tau_{sh,p1})(1+s\tau_{CSA,p2})(1+s\tau_{sh,p2})} \tag{7-1}$$

Where K_{DC} is the DC gain of the transfer function given by:

$$K_{DC} = \frac{R_f}{K_{SF}\ R_{PZC}} * \frac{2}{g_m(M1_a)} \tag{7-2}$$

Where the time constants are:

$$\tau_{sh,z1} = \frac{C_{sh}}{g_m(S0)} \tag{7-3}$$

$$\tau_{sh,p1} = \frac{2C_{sh}}{g_m(M1_a)} \tag{7-4}$$

$$\tau_{CSA,p2} = \frac{(C_{DET}\, C_{L\_CSA}+C_{DET}\, C_f+C_f\, C_{L\_CSA})}{C_f\, g_m(M0)} = \frac{\varepsilon_{CSA}}{C_f\, g_m(M0)} \tag{7-5}$$

$$\tau_{sh,p2} = \frac{(C_{IN\_SH}\, C_{L\_SH}+C_{IN\_SH}\, C_{sh}+C_{sh}\, C_{L\_SH})}{C_{sh}\, g_m(S0)} = \frac{2\varepsilon_{SH}}{C_{sh}\, g_m(M0)} \tag{7-6}$$

<u>Parallel noise contribution from the reset element in the CSA</u>

The output noise contribution of the equivalent resistor R_f in the CSA is:

$$< \vartheta_{out}^2 >_{th,Rf} = \int_0^\infty \left| K_{DC} * \frac{(1-s\tau_{sh,z1})}{(1+s\tau_{sh,p1})(1+s\tau_{CSA,p2})(1+s\tau_{sh,p2})} \right|^2 \frac{4k_BT}{R_f}\ df \tag{7-7}$$

The time constants are defined as:

$$\tau_{sh,z1} < \tau_{sh,p2} < \tau_{CSA,p2} < \tau_{sh,p1} \tag{7-8}$$

Therefore, the integral is simplified as:

$$< \vartheta_{out}^2 >_{th,Rf} \approx \frac{4k_BT}{R_f} * {K_{DC}}^2 * \frac{1}{4\,\tau_{sh,p1}} = \frac{4k_BT}{R_f} * {K_{DC}}^2 * \frac{g_m(M1_a)}{8\, C_{sh}} \tag{7-9}$$

To obtain the ENC, the power of the output noise voltage is divided by the square of the peak amplitude for a single electron at the front-end's input. If the rise and discharge time constants in the two stages are well separated, the peak amplitude of the front-end is:

$$V_{FE\_peak} = K_{DC} * \frac{q}{\tau_{sh,p1}} \tag{7-10}$$

Therefore, the ENC of the parallel noise in the reset element is:

$${ENC_{Rf}}^2 = \frac{2k_BTC_{sh}}{q^2} * \frac{1}{g_m(M1_a)*R_f} \tag{7-11}$$

<u>Shot-noise contribution</u>

The shot noise is generated from the leakage current I_{LEAK} and the small current I_{BH} in the CSA to bias the baseline holder. Its output noise contribution is:

$$< \vartheta_{out}^2 >_{leak} = \int_0^{\infty} \left| K_{DC} * \frac{(1-s\tau_{sh,z1})}{(1+s\tau_{sh,p1})(1+s\tau_{CSA,p2})(1+s\tau_{sh,p2})} \right|^2 2q(I_{LEAK}+I_{BH})\, df \tag{7-12}$$

The ENC of the shot noise is:

$$ENC_{leak}{}^2 = \frac{I_{LEAK}+I_{BH}}{q} * \frac{C_{sh}}{g_m(M1_a)} \tag{7-13}$$

Thermal noise input transistor in the CSA

The input transistor in the inverted operational amplifier within the CSA generates thermal noise, represented as ϑ_{nw}^2. Its output contribution is equal to:

$$< \vartheta_{out}^2 >_{nw} = \vartheta_{nw}^2\, C_{det}{}^2 \int_0^{\infty} \left| K_{DC} * \frac{(1-s\tau_{sh,z1})}{(1+s\tau_{sh,p1})(1+s\tau_{CSA,p2})(1+s\tau_{sh,p2})} \right|^2 * |j2\pi f|^2\, df \tag{7-14}$$

We have:

$$\int_0^{\infty} \left| K_{DC} * \frac{(1-s\tau_{sh,z1})}{(1+s\tau_{sh,p1})(1+s\tau_{CSA,p2})(1+s\tau_{sh,p2})} \right|^2 * |j2\pi f|^2\, df \approx \frac{1}{4\tau_{sh,p1}{}^2(\tau_{CSA,p2}+\tau_{sh,p2})} \tag{7-15}$$

The gate-source transconductance of the input transistor in the shaper is twice lower than in the CSA. Therefore, the ENC of the thermal noise is:

$$ENC_{nw}{}^2 = k_B T \alpha_{w1} \gamma_1 * \frac{C_{det}{}^2}{q^2} * \frac{1}{\frac{\varepsilon_{CSA}}{C_f}+\frac{\varepsilon_{SH}}{C_{sh}}} \tag{7-16}$$

The total noise is obtained by summing in quadrature the shot noise, thermal resistance noise, and input transistor thermal noise contributions:

$$ENC_{tot}{}^2 = ENC_{leak}{}^2 + ENC_{Rf}{}^2 + ENC_{nw}{}^2 \tag{7-17}$$

We, therefore, have [108]:

$$ENC_{tot}{}^2 = \frac{I_{LEAK}+\boldsymbol{I_{BH}}}{q} * \frac{C_{sh}}{\boldsymbol{g_m(M1_a)}} + \frac{2k_B T C_{sh}}{q^2} * \frac{1}{\boldsymbol{g_m(M1_a)*R_f}} + k_B T \alpha_{w1} \gamma_1 * \frac{\boldsymbol{C_{det}}{}^2}{q^2} * \frac{1}{\frac{\varepsilon_{CSA}}{C_f}+\frac{\varepsilon_{SH}}{C_{sh}}} \tag{7-18}$$

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Curriculum Vitae

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Education

Feb 2017 - present	Doctor of Philosophy (Ph.D.) in Microsystems and Microelectronics at Ecole Polytechnique Fédérale de Lausanne, Lausanne, Switzerland.
2014 - 2016	Master of Science (M.Sc.) in Micro and Nanotechnologies for Integrated Systems. Common master between three universities: Politecnico di Torino (Torino, Italy), Grenoble INP (Grenoble, France) and Ecole Polytechnique Fédérale de Lausanne (Lausanne, Switzerland).
2013 - 2014	Bachelor's degree (B.Sc.) in engineering science, specialization in physics, electronics, and telecommunication at Grenoble INP: Phelma, France.
2011 - 2013	Preparatory class, specialization in physics, mathematics and engineering science at Lycée Jacques Decours, Paris 09, France.
2011	French Baccalaureate, specialization in Mathematics at Lycée Général et Technologique de la Tourelle, Val d'Oise, France.

Research

Sept 2016 - present	Doctoral student at CERN, Switzerland. Project: Medipix4 chip for high-rate spectroscopic X-ray imaging Tasks: Main designer of the novel analog pixel front-end architecture. Analyze and implementation of new features to address actual limitations in Medipix3 chip, to improve the dynamic range, the energy resolution and the count-rate capability using CMOS 130nm technology.
March - September 2016	Master thesis in the Microelectronics group at CERN, Switzerland. Project: Timepix4 Tasks: Design of rail-to-rail unity gain buffers for Timepix4 chip using CMOS 65nm technology. Project: Timepix2 Tasks: Design of rail-to-rail unity gain buffers and analog blocks for the periphery of Timepix2 chip using CMOS 130nm technology.
June - August 2015	Internship in the laboratory CEA at Paris Saclay, France. Tasks: Characterization and simulation of the detector MINOS for the spectroscopy of the most exotic nuclei using COMSOL Multiphysics.
June - August 2014	Internship in STMicroelectronics at Crolles, France. Tasks: Operator in the field CMP (Chemical Mechanical Polishing) in a cleanroom environment.

Skills

- Design and simulation of full-custom analogue and mixed signal microelectronic circuits using CADENCE Virtuoso Platform.
- Experienced in the design of radiation tolerant, low-power low-noise charge sensitive amplifiers for hybrid pixel detectors.

- IC physical Verification (Calibre and Assura tools).
- Knowledge of the digital design flow and verilog hardware description language.
- Schematic and PCB layout on Altium.
- Modeling and data analysis with Matlab.

Languages

- Tamil and French: native proficiency.
- English: professional proficiency.

List of Publications

- V. Sriskaran, J. Alozy, R. Ballabriga, M. Campbell, N. Egidos, J.M. Fernandez Tenllado, E. Heijne, I. Kremastiotis, A. Koukab, X. Llopart, J.M. Sallese and L. Tlustos, “New architecture for the analog front-end of Medipix4,” *Nucl. Instruments Methods Phys. Res. Sect. A Accel. Spectrometers*, Detect. Assoc. Equip., vol. 978, no. July, p. 164412, 2020, doi: 10.1016/j.nima.2020.164412.

- R. Ballabriga, J. Alozy, F.N Bandi, M. Campbell, N. Egidos, J.M. Fernandez Tenllado, E. Heijne, I. Kremastiotis, X. Llopart, B. J. Madsen, D. Pennicard, V. Sriskaran and L. Tlustos, “Photon Counting Detectors for X-Ray Imaging With Emphasis on CT,” *IEEE Trans. Radiat. Plasma Med. Sci.,* vol. 5, no. 4, pp. 422–440, 2020, doi: 10.1109/trpms.2020.3002949.

- W. S. Wong, J. Alozy, R. Ballabriga, M. Campbell, I. Kremastiotis, X. Llopart, T. Poikela, V. Sriskaran, L. Tlustos and D. Turecek, “Introducing Timepix2, a frame-based pixel detector readout ASIC measuring energy deposition and arrival time,” *Radiat. Meas.*, vol. 131, no. January 2019, p. 106230, 2020, doi: 10.1016/j.radmeas.2019.106230.

- X. Llopart, J. Alozy, R. Ballabriga, M. Campbell, N. Egidos, J.M. Fernandez, E. Heijne, I. Kremastiotis, E. Santin, L. Tlustos, V. Sriskaran and T. Poikela, “Study of low power front-ends for hybrid pixel detectors with sub-ns time tagging,” *J. Instrum.*, vol. 14, no. 1, 2019, doi: 10.1088/1748-0221/14/01/C01024.

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