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New ultrahigh-speed device concepts: from THz nanoplasma devices to glass-like electronics for neuromorphic computation

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Mohammad Samizadeh Nikoo

Abstract

There is a never-ending push for electronic systems to provide faster operation speeds, higher energy efficiencies, and higher power capabilities at smaller scales. These requirements are apparent in different areas of electronics, from radiofrequency (RF) to logic and power electronic systems. For instance, a faster operation would result in communication links with higher capacities, logic circuits with higher processing speeds, and more compact power converters.

Metal-oxide-semiconductor (MOS), as the main platform for electronics so far, has enabled a variety of functional devices with applications in our everyday lives. The speed, power delivery, energy consumption, and size of MOS-based devices, however, are constrained by fundamental properties of semiconductor materials. For example, the trade-off between electron density and mobility limits the current density of semiconducting channels, resulting in a power-frequency trade-off in active devices, and the thermionic subthreshold-slope limit imposed by Boltzmann–Tyranny constrains their minimum supply voltage and ultimately their power consumption. Besides the intrinsic properties of materials, the interfaces (*e.g.* metal-semiconductor junctions) in classic devices also limit the performance of electronics. For example, the contact resistance of metal-semiconductor tunneling junctions severely constrain the high-frequency performance of diodes and transistors in the millimeter and sub-millimeter bands, and short-channel effects in MOS-based devices restrict downscaling of transistors, which hinders the extreme integration in logic circuits.

This thesis tackles some of the most fundamental challenges in different areas of electronics, with a focus on high-speed devices. The first part of the thesis is dedicated to high-speed radiofrequency electronics, where two new device concepts are proposed: electronic metadevices and nanoplasma switches. Electronic metadevices operate based on collective and controllable electromagnetic interactions in deep-subwavelength scales, as an alternative to controlling the flow of electrons. The proposed devices overcome some the theoretical limits in classical electronic devices such as diodes and transistors. Electronic switches realized based on this new concept enable achieving very high cutoff frequency figure-of-merit (FOM) exceeding 10 THz, very low losses with ultra-small contact resistances below 20 Ω μm, and large breakdown voltages over 30 V, extending state-of-the-art by two orders of magnitude. Based on this new device concept, two-port and three-port ultrahigh-speed modulators operating in the THz band are demonstrated.

In the second chapter, the common drawback of power-frequency trade-off in semiconductor devices which ultimately leads to the terahertz gap, is tackled by proposing ultrafast nanoplasma devices – new electronic switches operating based on plasma formation in nano-gaps. Nanoplasma switches offer current densities over 300 A mm^{-1} and switching speeds over 10 V ps^{-1}. A compact nanoplasma-based

terahertz source capable of generating peak powers above 1 W at 300 GHz is demonstrated. This new concept sets the stage for the future ultrafast electronics with applications in terahertz sources and modulators, relying only on a single metal layer. Nanoplasma devices are compatible with any kind of electronic platforms, from CMOS and III-V to flexible electronics.

High-speed logic electronics is concerned in the second part of this thesis, where we focus on a new observation in Vanadium Dioxide (VO_2). Classically, VO_2 is known to exhibit short memories due to metastability. Our results challenge this view and indicate that the incubation time of insulator-to-metal switching reveals the history of the previous phase transitions up to 10,000 seconds. We demonstrate this effect as a new electronic functionality where the state of a two-terminal device can be arbitrarily manipulated and tracked. This effect is relevant to high-speed information storage and processing schemes which are compatible with post von Neumann architectures. The results show that the states carrying information are structural and exhibit similar features of glasses, which are beyond the classic metastability in Mott systems. Glass-like electronics can potentially overcome some of the most fundamental limitations in conventional metal-oxide-semiconductor electronics, such as the thermionic subthreshold slope and miniaturization limits, and open avenues for neuromorphic computation and multi-level memories.

The final part of the thesis is dedicated to high-speed power electronics, and in particular to adopt some of the techniques used to characterize RF devices to study output capacitance losses in power transistors. The development of fast-switching wide-band-gap transistors, such as those based on Gallium Nitride (GaN), has enabled more compact power converters. However, the anomalous losses in their output capacitance has hindered their full potential at high frequencies. This thesis provides new measurement techniques based on large-signal and small signal approaches to quantify these high-frequency losses. The provided methods enable selecting packaged devices with lowest unwanted losses. Finally, a radiofrequency wafer-level measurement technique is proposed to evaluate losses in the epitaxial level, prior to the device fabrication.

Keywords: Electronic devices, ultrafast electronics, millimeter waves, terahertz, neuromorphic computation, memory devices, plasma, nanoplasma, electronic metadevices, Vanadium Dioxide, glass-like electronics.

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1 Introduction

1.1 Electronics in a glance: from semiconductor materials to system-level functionalities

Today's electronics largely owes to the development of semiconductor materials [1]. By definition, semiconductor is a material whose electrical conductivity falls between conductors and insulators. This behavior exists in certain pure element crystals such as Silicon (Si) and Germanium (Ge), as well as several compounds such as Gallium Nitride (GaN), Silicon Carbide (SiC), and Indium Aluminum Nitride (InAlN). Electrical properties of semiconductor materials can be modified by doping and by the application of electrical fields or light, which has led to a variety of functional devices such as amplifiers [2], logic gates [3], and sensors [4].

Semiconductor materials offer platforms to control the flow of electrons by electrostatic potentials [5] or injection of currents [6]. The most notable and widely used example of such control is in metal–insulator–semiconductor field-effect transistors (MISFETs), in which the number of electric charge carriers—and thus the electrical conductivity—is precisely controlled by an external voltage, providing electrical switching capability [7]. This simple but powerful feature is essential for lots of our everyday-life applications such as information processing [8], energy conversion [9], and telecommunications [10]. The performance of these electronic systems heavily relies on the characteristics of their building block electronic elements.

Fig. 1.1a show three major categories of electronics: Radiofrequency (RF) electronics, logic electronics, and power electronics. Such electronic systems operate in very different range of voltages (powers) and frequencies (Fig. 1.1b), however, they are all strictly constrained by fundamental material- or device-level limitations (dashed lines in Fig. 1.1b). For instance, the operation voltage of logic devices is constrained by the thermionic subthreshold-slope limit, imposed by Boltzmann–tyranny [11], which defines the minimum supply voltage of the chip and thus the power consumption of processors [12], and the (trans)conductance of field-effect transistors is limited by the close-to-surface conduction

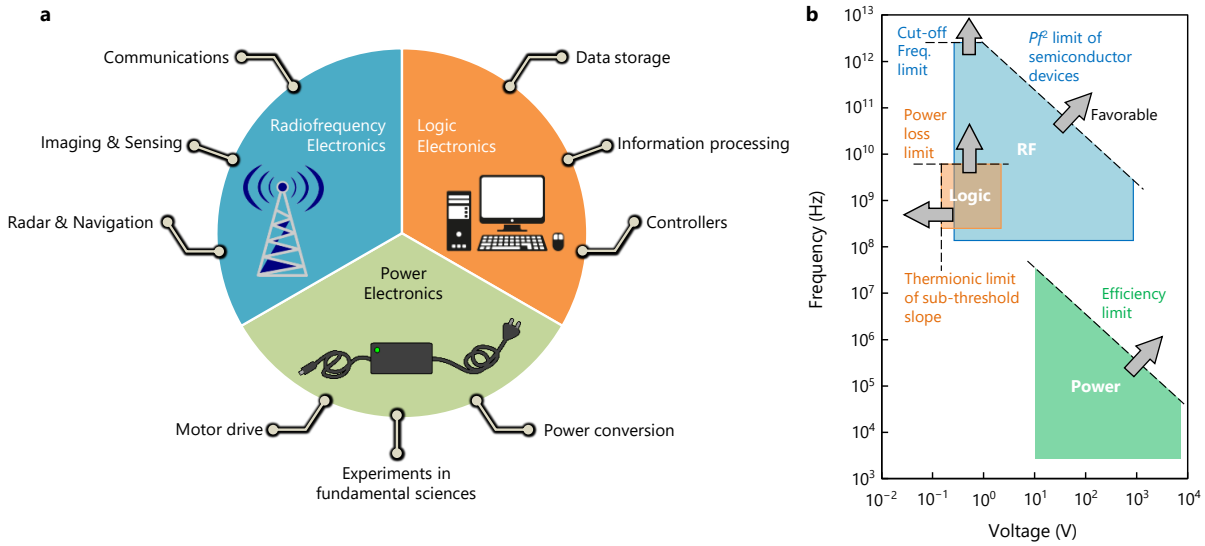

Figure 1.1 | Electronics in a glance. a, Categorization of electronics into three major branches: RF electronics with applications in communications, imaging, sensing, and radars, logic electronics with applications in data storage and processing, and power electronics for energy conversion and motor drives. **b,** RF, logic, and power electronics on the frequency-voltage plane. The arrows indicate favorable directions and dashed lines show fundamental limits.

Table 1.1 | Consequences of device properties on the performance of different electronic systems

Device properties	RF electronics	Logic electronics	Power electronics
Higher operation frequency	Higher data rates Higher imaging resolutions	Faster processing	Reducing the size of power converter
Higher current density / higher conductance	Pushing the limits towards the THz band	Higher miniaturization Increasing the computational capacity	Higher efficiencies
Larger breakdown voltage	Larger covering range in telecommunications and radars	Ruggedness against strong electromagnetic interfaces	Larger power conversion
Steep transfer characteristic	Larger gains for amplifiers	Lower power consumption	Smaller soft-switching[1] losses

imposed by Thomas–Fermi screening [13], which limits the cutoff frequency of RF electronics [14] and the energy-efficiency of power electronics [15]. Table 1.1 summarizes the consequences of device properties on the performance of different electronic systems.

This chapter discusses some of the major challenges of electronic systems in all three domains RF, logic, and power electronic, with a particular focus on their high-speed operation. The thesis proposes new device concepts and measurement techniques to tackle some of these challenges.

[1]In the context of power electronics, soft-switching is a condition where there is no time overlap between the non-zero output (drain-to-source) voltage and drain current waveforms, meaning a lossless switching transient [16].

1.2 Radiofrequency systems: Towards Terahertz Electronics

Since 1980s, when the 1G analog wireless cellular network enabled mobile communications of voice, there has been a continuous progress towards increasing the operation frequency of communication systems to achieve higher speeds and provide new services [17]. The 5G, which operates in the bottom of millimeter-wave (mm-wave) band with data rates up to 10 Gbps, is now available in growing number of cities in the world [18]. The visioning and planning of 6G communications—which is expected to provide much higher data rates up to 100 Gbps—has begun, with an aim to provide communication services for the future demands of the 2030s [19]-[21] (Table 1.2). The 6G will operate in the THz band (0.1 to 10 THz) which is a region of electromagnetic spectrum that lies between microwaves and infrared (IR). Generation and control of terahertz signals, however, is challenging for traditional electronic devices [22].

The classic approach to speed-up electronic devices to operate in the THz band has been by shrinking their dimensions [23]. Reducing the gate and channel length of transistors, thanks to the increasing lithography precisions over the past decades, resulted in devices with higher cutoff frequencies. This general trend, however, faces fundamental constrains for ultra-scaled devices [24] (Fig. 1.2a). Let us consider the case of planar transistors, which are major candidates for high-speed integrated electronics. In simple form, the cutoff frequency of the device can be expressed as

$$f_T = \frac{g_m}{2\pi C_g} \tag{1.1}$$

where g_{m} and C_{g} represents the transconductance and the gate capacitance of the devices. Reducing the gate length decreases the gate capacitance, however, for very short gates (< 20 nm) short channel effects disrupts the gate control[2] [25] and also extrinsic capacitances dominate the intrinsic ones. In addition, the carrier injection through (semi)metal-semiconductor tunneling junctions dominates the active region of the device [26] which limits the ON-state current and the transconductance of the devices. Such limitations have severely limited the cutoff frequency (f_{T}) and the maximum oscillation

Table 1.2 | Progress of telecommunications from 1G to 6G (supposed) [18]-[21]

Features	1G	2G	3G	4G	5G	6G (supposed)
Period	1980-1990	1990-2000	2000-2010	2010-2020	2020-2030	2030-2040
Maximum rate	14.4 kb/s	144 kb/s	2 Mb/s	1 Gb/s	10 Gb/s	100 Gb/s
Maximum frequency	894 MHz	1.9 GHz	2.1 GHz	6 GHz	47 GHz	10 THz
Service	Voice	Text	Picture	Video	3D VR/AR	Tactile

[2]Two-dimensional transistors have shown promise to mitigate short-channel effects [28]-[29].

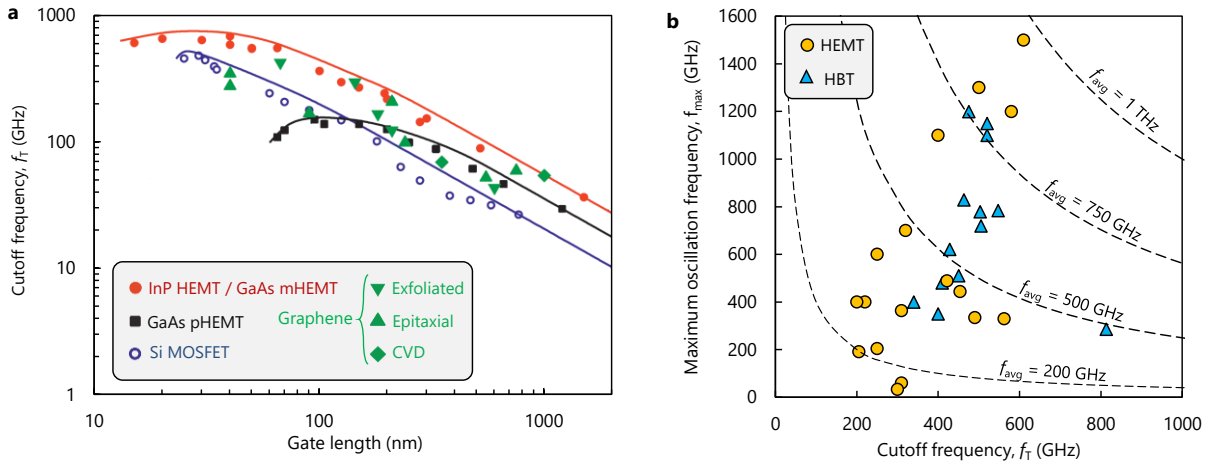

Figure 1.2 | State-of-the-art performance of radiofrequency transistors. a, Cutoff frequency (f_T) of different types of transistors versus gate length. The cutoff frequency initially increases by reducing the gate length, and it reaches a saturation for ~20 nm gate length for the state-of-the-art transistors. The data is presented based on information given in [24]. **b,** Maximum oscillation frequency (f_{max}) versus f_T for ultrahigh-speed transistors from two major families HEMT (▲) and HBT (●) [30]-[54]. The dashed lines illustrate the average frequency ($f_{avg} = \sqrt{f_T f_{max}}$) lines.

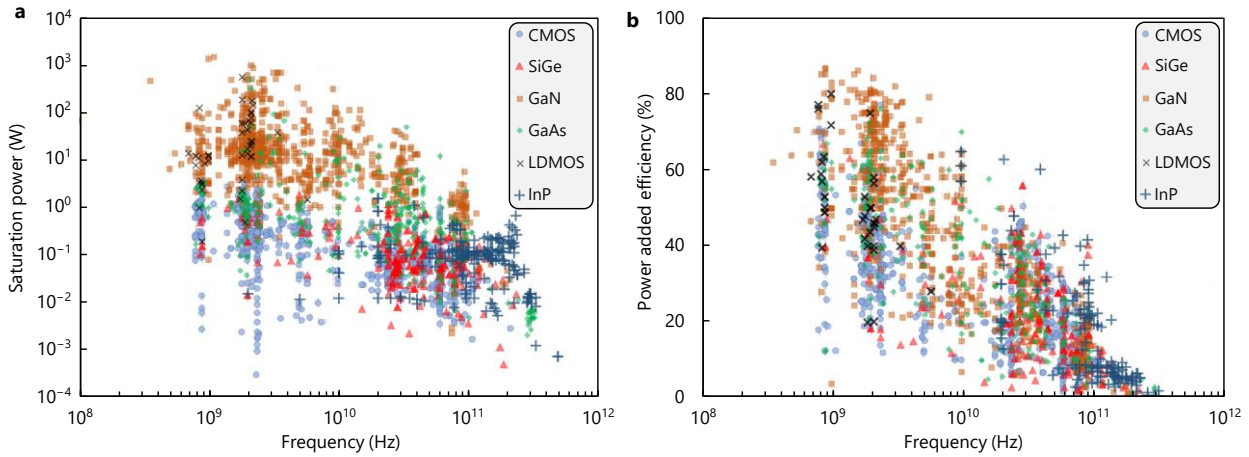

Figure 1.3 | State-of-the-art performance of radiofrequency power amplifiers. a, Saturated power and **b,** power added efficiency of power amplifiers based on CMOS (●), SiGe (▲), GaN (■), GaAs (◆), LDMOS (×), and InP (+), versus frequency. Based on information given in [59].

frequency (f_{max}) of transistors, as they strongly depend on the transconductance and the input capacitance of the devices [27]. The cutoff frequency and the average frequency ($f_{avg} = \sqrt{f_T f_{max}}$) of state-of-the-art transistors are still below 1 THz (Fig. 1.2b).

The large-signal operation of semiconductor devices is yet another fundamental challenge which has imposed a power-frequency trade-off known as Pf^2-limit in solid-state radiofrequency sources. The trade-off between the operation speed and the breakdown voltage of semiconductor devices (imposed

by the saturation velocity of electrons and the critical electric field of semiconductor materials, described by Johnson's Figure of Merit [55]) as well as their output capacitance with respect to the ON state current, limit the maximum power delivery of ~10 mW THz^2 (see section 3.1). In addition, several phenomena happening at high frequencies and small spatial scales—such as radiofrequency g_m collapse [56], short-channel effects [57] and surface traps [58]—result in considerably lower-than-expected powers at terahertz frequencies. Such limitations results in solid state amplifiers and oscillators with low output powers (Fig. 1.3a) and low efficiencies (Fig. 1.3b), which have challenged the development of terahertz electronics that is critical for future technologies including the 6G mobile communications [19].

Controlling terahertz signals using electronic switches, essential for high-speed data modulation, is also a major challenge in high-frequency electronics. The limited ON state conductance ($1/R_{ON}$) of conventional electronic switches, such as diodes and transistors, with respect to their considerable OFF state susceptance ($2\pi fC_{OFF}$)—corresponding to parasitic capacitances—hinders the terahertz switching capability of these devices. The cutoff frequency figure-of-merit (FOM) of a radiofrequency switch is defined as $f_{CO} = (2\pi R_{ON} C_{OFF})^{-1}$, at which the on-state resistance and the off-state reactance are equal. Shrinking semiconductor devices has extended their operation frequency to the mm-wave and low-terahertz bands, however, achieving f_{CO} values well-beyond 1 THz remains a challenge [60] (Fig. 1.4). Alternative platforms such as micro-electro-mechanical systems (MEMS) [61], phase-change materials [62], and memristors offer higher cutoff frequencies compering to their semiconductor counterparts, however, they exhibit either slow switching time, or cycle-to-cycle variability and limited durability [63].

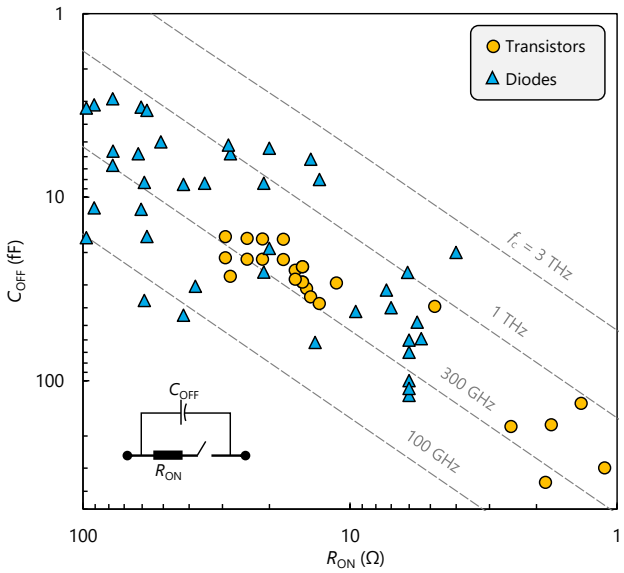

Figure 1.4 | Cutoff frequency FOM of state-of-the-art charge-based THz switches. Benchmark of transistors (▲) and diodes (●) in the R_{ON}-C_{OFF} plan showing their cutoff frequency FOM $f_{CO} = (2\pi R_{ON} C_{OFF})^{-1}$ [64]-[79]. The inset shows a simplified circuit model of an RF switch, where R_{ON} and C_{OFF} are the ON resistance and OFF capacitance of the device, respectively.

1.3 Logic systems: Crossing the memory wall

The progress in the performance improvement of computers is significantly slowed down over the last years (Fig. 1.5), owing to the fundamental hardware limits [81], while the generation of data and demand for computing are increasing sharply with time. The clock frequency of conventional computers has been almost flat for over a decade, due to the intrinsic response of ultra-scaled transistors and exponentially increasing losses at higher clock frequencies. The forecasted 10-GHz Intel processor [82] finally did not reached out, and the maximum clock frequency of current processors is stalled at a few gigahertz [83]. The increase in the operation speed of computers has been heavily relied on the integration capability, either by shrinking the node size [84] or three-dimensional integration schemes [85]. Whether the computation power of CMOS processors can still be improved in the future decades by further extending the Moore's law is an open question, at least for now [86], [87].

While there are giant investments on increasing the integration capability in CMOS electronics [88], widespread research is being carried out on hybrid or even alternative platforms [89]-[91]. For example, manipulation of lattice properties, instead of charges, can overcome fundamental limits of conventional semiconductor devices, such as operation at voltages below those dictated by the room temperature thermionic subthreshold-slope limit in charge-based devices [11]. Memristors based on transition metal-oxides [93], [94] are among the most explored examples of post-CMOS functional devices so far [91]. They have shown promise to realize ultra-dense memories [95], as well as proving compatibility with post von Neumann architectures [96], although their cycle-to-cycle variability and limited conductance states are still major challenges that have to addressed in the hardware level [97].

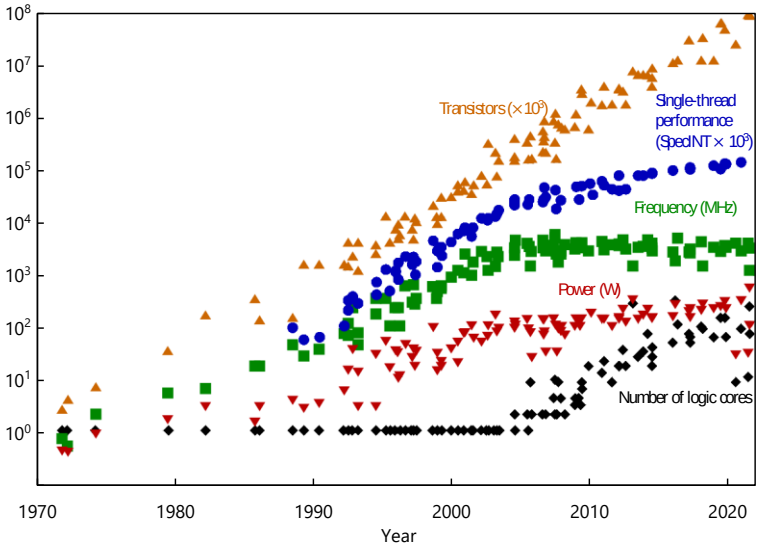

Figure 1.5 | The progress in conventional processors over time. Total number of transistors in processors (▲), the SpecINT[3] benchmark (●), clock frequency (■), typical power consumption (▼), and the number of logic cores (◆) [80].

[3]SPECint is a computer benchmark specification for CPU integer processing power. It is maintained by the Standard Performance Evaluation Corporation (SPEC).

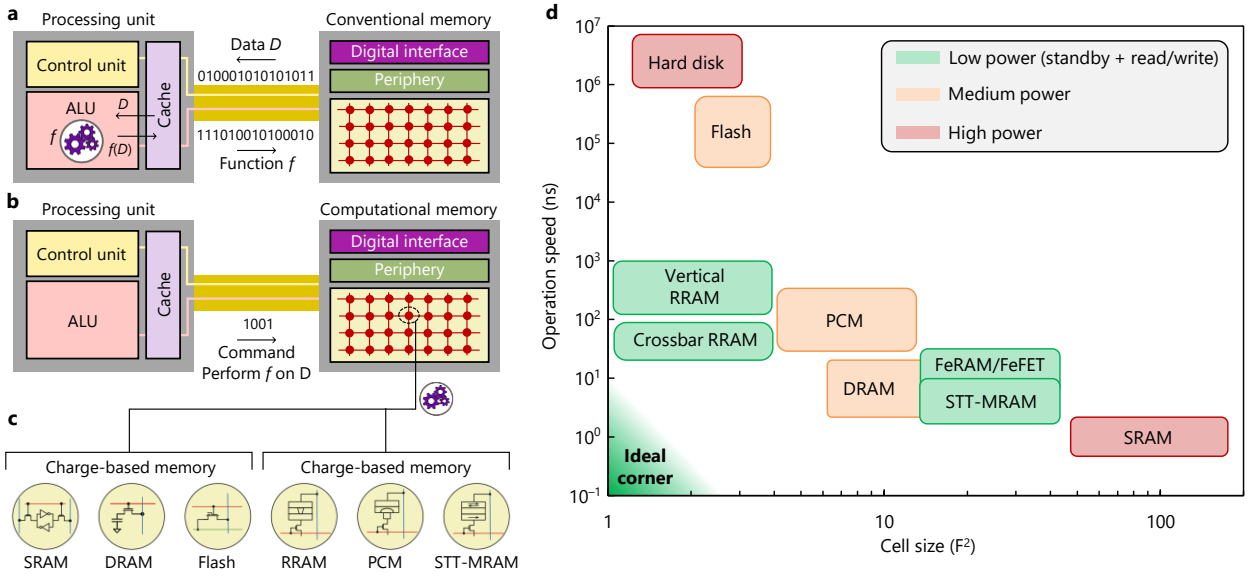

Figure 1.6 | A perspective of different memory technologies. a, Schematic of a traditional computation system where processing happens outside the memory unit. When an operation *f* is performed on data *D*, *D* has to be moved into a processing unit, leading to significant costs in latency and energy. **b,** Schematic of an in-memory computation scheme. *f*(*D*) is performed within a computational memory unit by exploiting the physical attributes of the memory devices, thus obviating the need to move *D* to the processing unit. **c,** Both charge-based memory technologies, such as Static Random Access Memory (SRAM), Dynamic RAM (DRAM) and flash memory, and resistance-based memory technologies, such as Phase-change memory (PCM) and Spin Transfer Torque Magnetoresistive RAM (STT-MRAM), can serve as elements of such a computational memory unit. Parts a-c are replotted from [98]. **d,** Benchmark of charge-based and emerging memory technologies concerning operation speed, cell size, and power consumption (including standby and transient power in read/write processes) [103].

Memory devices play a critical role in the speed of processors [98]. In traditional von Neumann computing systems, which consist of separate processing and memory units [99], when an operation *f* is performed on data *D*, *D* has to be moved from the memory into an arithmetic-logic unit, and the result should come back to the memory unit (Fig. 1.6a). In this case, the read/write speed from the memory and its energy consumption directly affect the performance of the processor. In fact, there is an increasing disparity between the speed of the memory and processing units, typically referred to as the memory wall [100], which slows down the classic processors. Now considering the case of modern in-memory computation scheme, where the computational tasks are performed within the confines of the memory array and its peripheral circuitry [98], the importance of fast functional memory devices with a high scalability capability is noticeable more than ever (Fig. 1.6b). Several types of memory devices, either charge-based [101] or resistance-based memories [102], can potentially exhibit in-memory computation schemes (Fig. 1.6c).

Fig. 1.6d presents a benchmark for memory technologies concerning their speed, cell size, and energy consumption. Static random access memory (SRAM) and hard disk are the extreme sides of the plot showing a trade-off between speed and cell size for the conventional charge-based memories. Emerging memory technologies based on resistive switches and ferroelectricity have showed promise

to achieve further down-scaling with decent energy consumption [103], [104]. The cross-bar configuration, compatible with two-terminal resistive memories, in which an N^2 array is accessed through $2N$ terminals are particularly promising for ultra-dense high-performance memories for data storage [95] and computation [105].

The development in the emerging computational memory devices was also quite beneficial for hardware implementation of neuromorphic computing schemes [106], [107]. Inspired by the co-location of logic and memory, robustness against local failures, and parallel processing in the human brain, neuromorphic computing architectures showed promise and become a strong alternative to traditional processors [108]. Early hardware realizations of neuromorphic computing was based on conventional electronics, particularly complementary metal–oxide–semiconductor (CMOS) spiking neural networks, however the energy efficiency of synaptic operations based on volatile random access memories was low [109]. Significant efforts have been devoted to non-volatile memory as a foundation for neuromorphic computing, and several memory technologies have emerged [110]-[112], among them, memristors have the advantage of smaller footprints and lower power consumption without compromising other metrics [113]-[119], while their inherit stochasticity challenges large-scale implementations [97].

As a summary of this sub-section, developing ultrafast energy-efficient computational memory devices with a high consistency and durability is crucially important to overcome the memory-wall and speed-up both traditional and modern processors [100]. More specifically in case of brain-inspired computation, the impact of new electronic device concepts that can better mimic the operation of synapses can be significant for the future neuromorphic chips [97].

1.4 Power electronic systems: Miniaturization-efficiency trade-off

A considerable part of the cost and volume of modern electronic equipment is due to the energy-conversion systems that they require, and the need for power electronics having greater compactness, better manufacturability, and higher transient performance motivates pursuit of dramatic increases in switching frequencies [120]. Such increase in the switching frequency thanks to the development of post-Si semiconductor devices [121] has enabled pushing the power densities[4] towards 100 kW/L (Fig. 1.7). The development of GaN semiconductor power devices with low ON resistances [123] and fast switching capabilities [124] was an important step to realize such compact energy-efficient power converters [125], [126]. At the same breakdown voltage, GaN transistors can potentially exhibit three orders of magnitude lower conduction losses comparing to their traditional Si counterparts [127], and have shown large-signal switching times below 1 ns [128]. In addition, the planar configuration of GaN transistors has enabled power integrated circuits, which sets the stage for extreme miniaturization in power converters [129].

[4]Energy storage passive devices (inductors and capacitors) occupy a large portion of the entire volume of power converters. At a fixed power level, by increasing the switching frequency of active devices, less energy is needed to be stored in the passive components which enables shrinking the size of these elements.

Despite these great potentials, higher-than-expected losses were observed in GaN-based power circuits, especially those operating at frequencies well above 1 MHz. Researchers explored commercial GaN devices operating up to 27 MHz and observed unexpected losses up to three times larger than the predicted values [130]. Over a decade of study, two major sources of excessive losses have been found in GaN HEMTs: the degradation in the dynamic ON resistance [131] and the output capacitance losses under soft-switching conditions [132]. The former takes place when the ON resistance of the device, right after holding a voltage stress in OFF state, is significantly higher than the ON resistance of a fully relaxed device, and the latter corresponds to unexpected losses in resonantly charging and discharging of the output capacitance [133]. Both types of losses have a more severe impact at higher frequencies, which has challenged engineers to implement compact power converters with high efficiencies [134]. Interestingly, the two types of losses have shown correlations suggesting that both might have identical microscopic origin [135].

The first step to resolve such high-frequency soft-switching losses in power transistors is to be able to measure and accurately quantize them at high frequencies. The first studies on the evaluations of C_{OSS} losses were based on the Sawyer-Tower (ST) circuit[5] which captures the charge stored in a DUT with respect to a known capacitor [132]. The method properly works at rather low frequencies, at which the impedance of the parasitic inductances is notable less than the impedance of C_{OSS}. High-frequency characterization of C_{OSS} losses is particularly important in GaN devices as their switching harmonics can

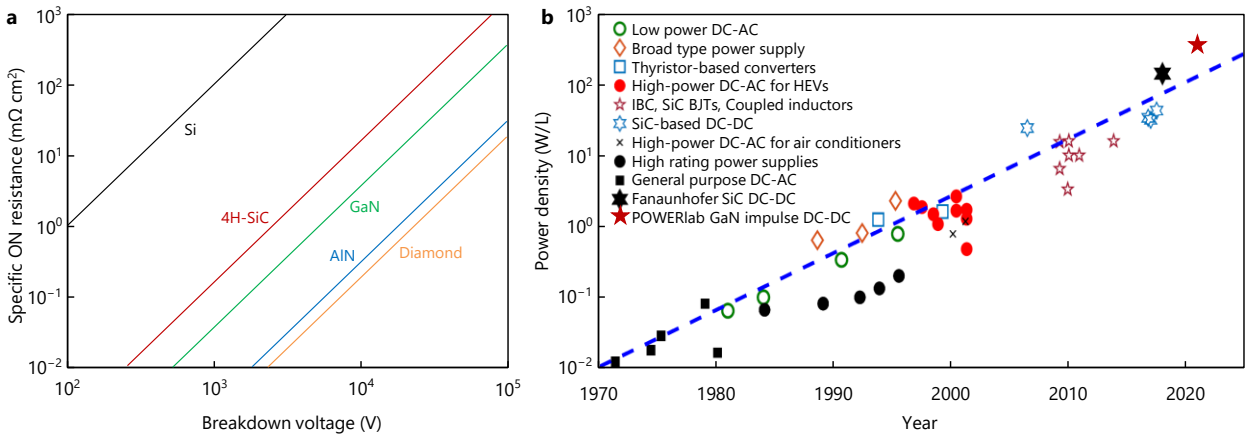

Figure 1.7 | Post-Si semiconductor materials for energy-efficient power electronics and projected growth of power densities in power converters. a, Contours of constant Baliga figure-of-merit (BFOM) for various conventional, WBG and UWBG semiconductors, drawn on a log-log specific on-resistance versus breakdown voltage plot [127]. **b,** The trend of power densities of the state-of-the-art power converters shows a continuous increase towards 100 kW/L. Increasing the switching frequency plays a key role to realize ultrahigh power density converters. Combination of MHz switching GaN HEMTs with the proposed impulse rectification boost converter concept resulted in the power density of 52 kW/L which is one of the highest power densities have been demonstrated so far [122]. The measurement techniques presented in thesis enable selecting the active device with the lowest losses to achieve such high energy efficiency.

[5]The Sawyer-Tower circuit was initially used to study hysteresis losses in ferroelectrics [136].

well exceed 100 MHz [127], while the maximum reported operation frequency of the ST circuit was about 30 MHz [134]. In addition to that, the method is applicable to packaged devices so it is less relevant for optimization purposes. High-frequency characterization of soft-switching losses in the epitaxial level, prior to the device fabrication and packaging, would be a major step which can set the stage for optimization and understanding the microscopic origin of such losses.

1.5 Thesis outlines

This thesis aims to tackle the challenges outlined in subsections 1-2, 1-3, and 1-4 by developing new device concepts and proposing new ultrafast measurement techniques. The next chapters of this thesis are organized as follows:

Part I includes two chapters and address some of the fundamental challenges in radiofrequency electronics. Chapter 2 presents the concept of electronic metadevices in which microscopic manipulation of radiofrequency fields leads to extraordinary electronic properties. This new device concept controls electrical signals by manipulation of collective electromagnetic interactions in deep-subwavelength scales, as an alternative to controlling the flow of electrons in classic devices. High-performance switches with cutoff frequency FOM of 18 THz, breakdown voltage of 30 V, and contact resistances below the state-of-the-art achieved by tunneling junctions are demonstrated. Electronic metadevices have relevance to ultrahigh-speed wireless communications. This chapter is based on the published results presented in [137] and [138].

Chapter 3 demonstrates nanoplasma devices for generation and modulation of high-power terahertz signals. The device operates based on formation of plasma in a nano-gap which leads to picosecond switching speeds at large signal levels, from 10 V to 1,000 V. Extremely fast switching transients with dv/dt values exceeding 10 V ps^{-1} are demonstrated. By integration of nanoplasma devices with THz resonators, a 2-W source at 300 GHz is presented. In addition, millimeter-wave digital modulators which only rely on a single metal layer are demonstrated which shows the potential of nanoplasma switches for high-performance system-level applications. This chapter is based on the published results presented in [139]-[142].

Part II of this thesis includes one chapter which presents a new concept for data storage and processing. Electrically accessible glass-like states are demonstrated in Vanadium Dioxide (VO_2). The state of a two- or multi-terminal VO_2 device can be arbitrarily manipulated in short time scales and tracked beyond 10,000 seconds after excitation. In two-terminal devices with channel lengths down to 50 nm, sub-nanosecond electrical excitation can take place with energy consumption down to 100 femto joules. In addition, the state of the device is determined by a nonlinear superposition of multiple excitations, which enables processing of a sequence of data bits. Advanced experimental results will be presented, showing that this observation is beyond the classic metastability in Mott systems, while showing features similar to glasses. These glass-like functional devices can outperform conventional metal-oxide-semiconductor electronics in terms of speed, energy consumption, and miniaturization, and open avenues for neuromorphic computation and multi-level memories. This chapter is based on the published results presented in [143].

Part III includes two chapters which apply some of the measurement techniques in radiofrequency electronics to characterize power devices to address the efficiency-miniaturization trade-off in high-speed power electronics. Chapter 5 presents new measurement methods to quantify soft-switching losses in power transistors at very high frequencies, even beyond 100 MHz, which is essential for high-speed power devices such as those based on GaN HEMTs. These new methods significantly extend the measurement range of the traditional Sawyer-Tower circuit. A small signal model is presented which predicts large-signal frequency dependent output capacitance losses in power transistors. Using these new methodologies, low loss devices are selected and being used to realize dc-dc converters with voltage gains up to 200 and record high efficiencies. This chapter is based on the published results presented in [144]-[149].

Chapter 6 presents a new paradigm to evaluate soft-switching losses in the epitaxial level, prior to the device fabrication. A new on-wafer measurement technique is presented which can precisely extract losses in power epitaxies up to very high frequencies, well above 100 MHz. Applying this new measurement technique on GaN-on-Si epitaxies reveals unexpected resonances which significantly contribute to the soft-switching losses in fast switching transients. The frequency of these resonances is higher than the frequency limitation of traditional techniques. The method operates based on scattering parameter evaluation of power epitaxies which leads to circuit models that can be used in circuit-level simulations. This chapter is based on the published results presented in [150].

2 Electronic metadevices: A new paradigm to exploit the full potential of semiconductors

The evolution of electronics has largely relied on down scaling to meet the continuous needs for faster and highly integrated devices [23]. As the channel length is reduced, however, classic electronic devices face fundamental issues that hinder exploiting materials to their full potential and ultimately, further miniaturization [151]. For example, the carrier injection through tunneling junctions dominates the channel resistance [26], while the high parasitic capacitances drastically limit its maximum operating frequency [152]. In addition, these ultra-scaled devices with highly nonuniform electric-field distributions can only hold a few volts, which limits their maximum delivered power [60], [139]. For example, a 100-nm-long channel with a sheet resistance of 300 Ω/▪ can potentially exhibit an ON resistance of R_{ON} = 30 Ω µm, which together with an approximate coplanar capacitance of 200 fF mm^{-1} in the OFF state (C_{OFF}) would result in a cutoff frequency FOM ($f_{CO} = \frac{1}{2\pi R_{ON} C_{OFF}}$) of over 20 THz. In addition, considering the high critical electric field of wide-band-gap semiconductors (> 2 MV cm^{-1}), such a device should be able to hold up to 20 V in the OFF state. These values are by far higher than those achieved by conventional high performance electronic devices up to date [60].

This chapter challenges such traditional limitations and proposes the concept of electronic metadevices, in which the microscopic manipulation of radiofrequency fields results in extraordinary electronic properties beyond the fundamental limitations of traditional electronics. The devices operate based on electrostatic control of collective electromagnetic interactions in deep sub-wavelength scales, as an alternative to controlling the flow of electrons in traditional devices such as diodes and transistors. This enables a new class of electronic devices which can operate well above 10 THz, exhibiting record high conductances among semiconductor devices close to the quantum limit, extremely high breakdown voltages and picosecond switching speeds.

Metastructures have revolutionized optics by enabling the realization of exotic media presenting functionalities beyond the material properties [153]-[156]. The principle is based on the subwavelength manipulation of electromagnetic fields which results in distinct macroscopic optical properties. In this work we show a new concept in which the microscopic manipulation of radiofrequency fields leads to extraordinary macroscopic electronic device characteristics. This concept, named electronic metadevices, can be generally applied to any semiconductors platform, such as III-V compounds, complementary metal-oxide-semiconductor (CMOS), wide-band-gap and 2D semiconductors, to explore the full capability of these materials. Using the electronic metadevice idea, we realize high performance terahertz switches on a high-electron-mobility InAlN/GaN platform, which outperform the state-of-the-art among classic semiconductor devices in multiple aspects, such as cutoff frequency FOM, conductance and breakdown voltage. Finally, we demonstrate the application of two-terminal and three-terminal electronic metadevices in high-speed THz modulators and mixers for ultrahigh-capacity telecommunications.

2.1 Concept of electronic metadevices

The metal-semiconductor interface to inject (extract) electrons to (from) the semiconductor channel in classic devices is a major bottleneck in nano-electronics. The state-of-the-art contact resistance values reported in the literature are still notably larger than the channel resistance of ultra-scaled devices, dominating the active region of nano-devices, which ultimately limit their (trans)conductance. Using displacement-field coupling instead of electron injection through ohmic contacts, is an alternative approach to realize functional electronic devices [137].

Fig. 2.1 shows a schematic of a displacement-field radiofrequency switch. The device is normally ON, transmitting the signal applied to port 1 to port 2 through the displacement-field coupling between the terminals and the 2DEG. Depleting the 2DEG under one of the terminals eliminates the

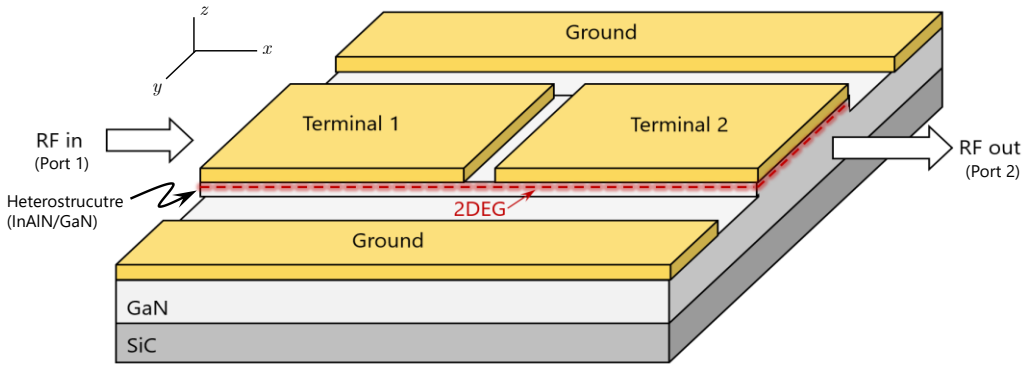

Fig. 2.1 | Displacement-field radiofrequency switch. Three dimensional schematic of a two-terminal displacement-field radiofrequency switch based on InAlN/GaN heterojunction, integrated on a coplanar transmission line. A radiofrequency signal is applied to the first port. The signal couples from metal (terminal 1) to the 2DEG through displacement fields, induces current at the 2DEG close to the gap, and couples from 2DEG to terminal 2 through displacement fields. In this case, the device transmits the radiofrequency signal from port 1 to port 2. Applying a negative voltage to one of the terminals depletes the 2DEG under the terminal and eliminates the displacement field coupling between the metal and 2DEG, thus turning off the switch.

displacement-field coupling and turns OFF the switch. In this chapter, it will be shown that the metal-2DEG displacement coupling is enabled by a sub-wavelength mode, with field patterns radically different from the displacement-fields in a normal capacitor. It will be argued that this subwavelength mode can interact with patterned terminals, which leads to microscopic manipulation of radiofrequency fields at the metal-2DEG barrier, resulting in exceptional electrical properties.

Fig. 2.2a shows a metal-insulator-semiconductor (MIS) structure, where an insulating barrier with thickness d is sandwiched between a top metal and a semiconductor layer with thickness d_0 and resistivity ρ. Assuming a symmetry along the y direction, and writing the Maxwell's equations at the insulating barrier (with permittivity ε and permeability μ_0) results in

$$\frac{\partial^2}{\partial x^2}E_z - \frac{\rho}{d}\frac{\partial}{\partial x}J_x + \xi^2 E_z = 0, \quad \xi^2 = \mu\varepsilon\omega^2 \tag{2.1}$$

where E_z represents the vertical component of electric field at the barrier, J_x is the current density at the semiconductor channel, and ω represents the angular frequency. For the case of $\rho \to 0$, equation (2.1) simplifies to an ordinary Helmoltz equation with a transverse electromagnetic mode (TEM) solution. For a non-zero ρ and small values of d, however, the second term of Eq. (2.1) can dominate the third term. In this case, considering the current continuity in the semiconductor layer results in:

$$\frac{\partial^2}{\partial x^2}E_z = j\frac{\omega\varepsilon R_{\mathrm{sh}}}{d}E_z, \tag{2.2}$$

where ω is the angular frequency and $R_{\mathrm{sh}} = \rho/d_0$ is the sheet resistance of the semiconductor layer. Eq. (2.2) corresponds to a dissipative transverse magnetic (TM) mode with a subwavelength oscillatory nature with wavelength λ_{sub} (Fig. 2.2b)

$$\lambda_{sub} = 2\pi\sqrt{\frac{d}{2\omega\varepsilon R_{\mathrm{sh}}}} \tag{2.3}$$

As illustrated in Fig. 2.2c, by forming a discontinuity on the top metal, exciting the structure from one side and terminating the other side by a resistive matched load, the excited TM mode constrains the electric fields close to the gap (g). In this case, a microwave or a terahertz wave can be confined in micro- and nano-scales, which are much shorter than their wavelength (Fig. 2.2d).

Now let us look at a case in which the simple straight gap between two sides of the PEC is replaced by an array of narrow stripes with a length comparable to λ_{sub} (Fig. 2.2e). This metallic texture can strongly interact with the TM mode and change the electric field pattern over the device layout, which results in exceptional electronic properties in a device form factor, which we call an electronic metadevice. Fig. 2.2f presents the simulated E_z at the 8-nm-thin barrier of a metadevice with stripe width of 0.4 μm and stripe length of 3.4 μm, showing a very different pattern compared to the straight-gap device. This sub-wavelength manipulation of the electric field pattern can significantly change the electronic properties of the device, and in this case, results in an outstanding signal transmission from port 1 to port 2.

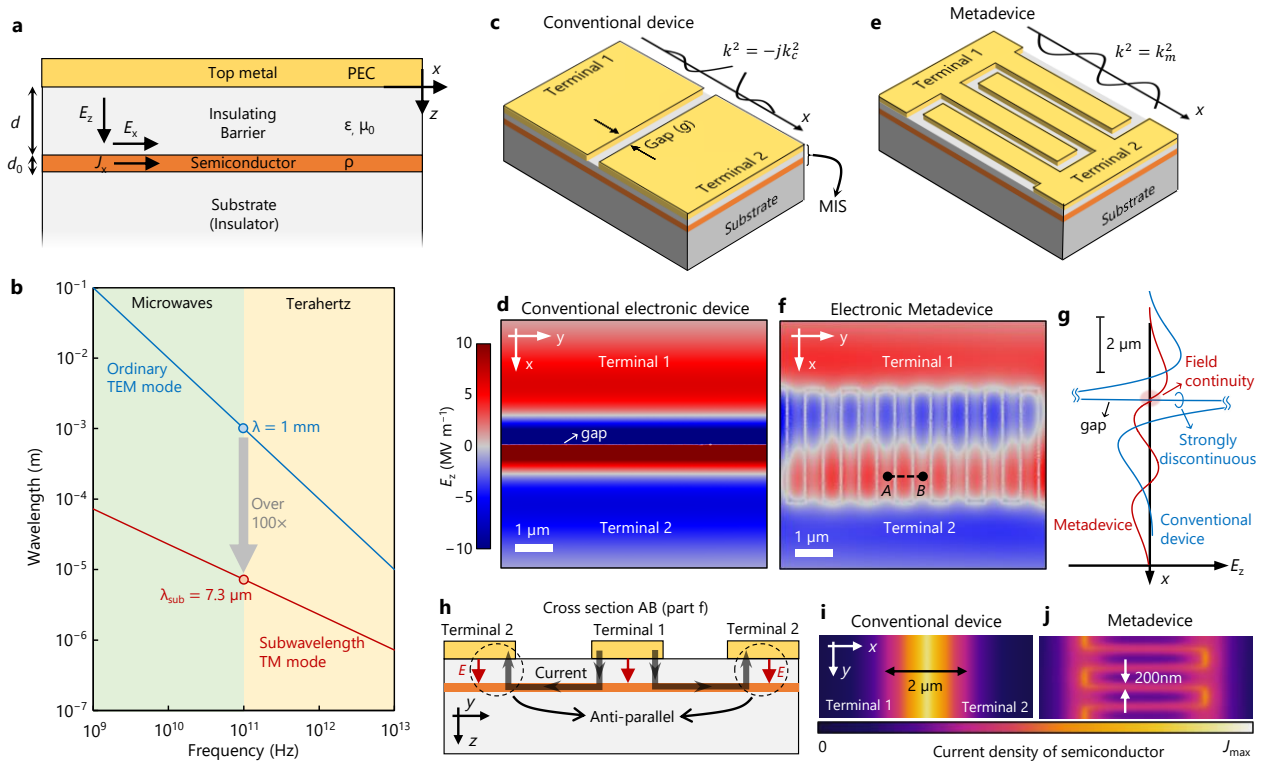

Fig. 2.2 | Concept of electronic metadevices based on the microscopic manipulation of radiofrequency fields leading to extraordinary electrical properties. a, Schematic of a thin metal-insulator-semiconductor (MIS) structure. **b,** Wavelength versus frequency of an ordinary TEM mode as well as the subwavelength TM mode (d = 10 nm). **c,** Illustration of a MIS structure with a discontinuity on the top metal. The excited TM mode results in oscillatory fields close to the gap. k_c^2 represents the square of the effective wavenumber of the mode (Eq. 2.2). **d,** Simulated E_z at the barrier of an 8-nm-thin MIS structure with 100-nm-long gaps at 120 GHz. **e,** Metadevice geometry on the same MIS structure, in which instead of a straight gap, stripes with a subwavelength length are patterned to form metastructures. The gap length (g) is identical to the straight-gap device. E_z satisfies the equation $\partial^2 E_z/\partial x^2 + k_m^2 E_z = 0$, with k_m being the effective wavenumber of the oscillatory subwavelength mode. **f,** Simulated E_z at the barrier of a metadevice with 100-nm-long gaps at 120 GHz. **g,** Simulated E_z at the barrier along the propagation axis (x) for straight-gap (conventional) device (blue) and metadevice (red). **h,** Illustration of the electric field at the barrier for a metadevice (part f). The vectorial integration of electric field for the metadevice just depends on the potential drop on the gap, resulting in an extraordinary transmission. **i, j,** Simulated semiconductor current density for the straight-gap device and the metadevice, showing the concentration of the current density on the gap.

As presented in Fig. 2.2g, E_z for the straight-gap device has a strong discontinuity close to the gap, which results in a large potential drop across the terminals, hindering an efficient signal transmission. The metadevice, however, exhibits an E_z that becomes almost zero at the end of the stripes, resulting an ideal metal-semiconductor coupling. The subwavelength electric field manipulation also provides an excellent property of signal transmission between the two sides of the stripes, as both electric fields have the same direction, while one stripe injects current to the other (Fig. 2.2h). In this case, the effective potential differences at the barrier, at the two sides of the gap cancel each other out and result in a perfect metal-semiconductor coupling. In addition, electronic metadevice exhibit a lower magnitude of E_z at the same current density, which results in a lower ON-state resistance and higher transmission.

The outcome of this effect can be clearly seen in the current density of the semiconductor layer. As shown in Fig. 2.2i and 2.2j, for the straight-gap device, the current is only confined in $\sim\lambda_{sub}$ in both sides of the gap. The metadevice (Fig. 2.2k) exhibits ten times more confinement of the current density leading to significantly lower losses, which predicts an extraordinarily high transmission for the metadevice. By applying an electrostatic voltage to one of the terminals, the semiconductor under one terminal is depleted, which completely eliminates the transmissive mode (Fig. 2.3), thus turning off the device. Alternatively, the sub-wavelength mode can be also controlled by a gate electrode (Section 2.5).

Number of stripes significantly affects the field pattern in the electronic metadevices. The oscillatory field pattern in the propagation direction do not shape up for devices with only two stripes. By increasing the number of stripes (Fig. 2.4a) this transmssive mode form more homogeneously over the device layout, expect for the very first and very last stripes which do not show the same field pattern as other stripes. Fig. 2.4b-g show the simulated electric field patter (E_z at the barrier) and current density at the 2DEG, for devices with two different number of stripes. The device with 8 stripes clearly show a greater current confinement compared to the device with 2 stripes. This leads to a superlinear increase of conductance with respect to the number of stripes (Fig. 2.4h).

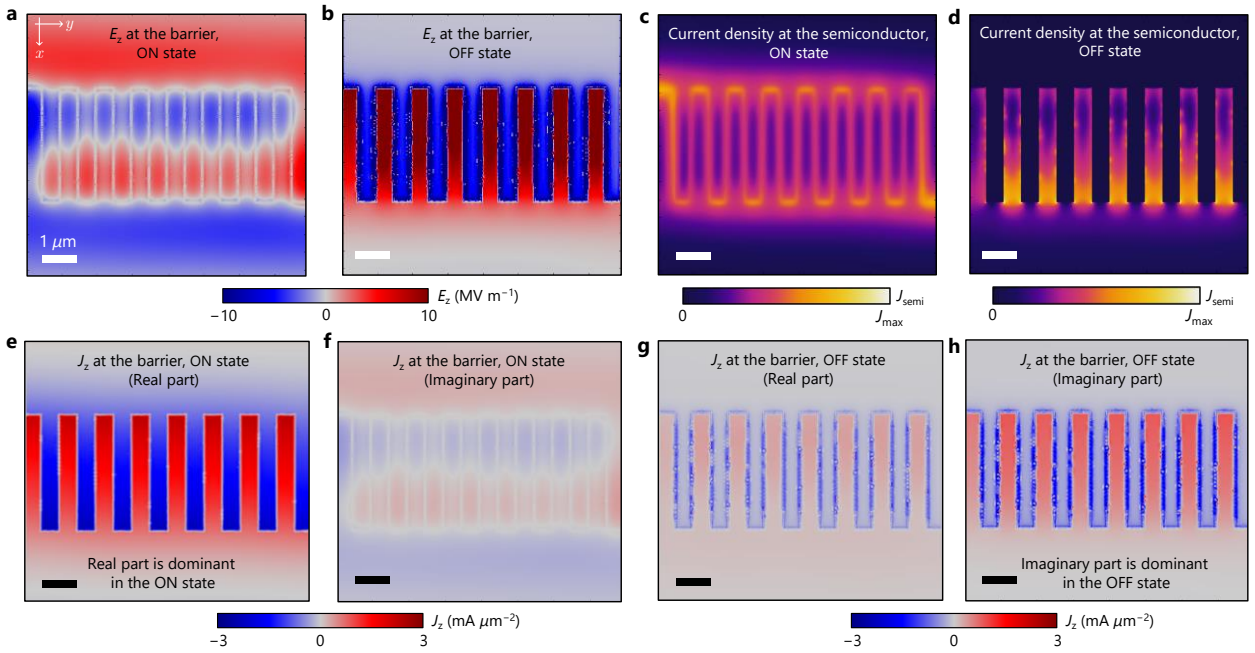

Fig. 2.3 | ON-state and OFF-state electric field patterns and current densities in metadevices. Simulated vertical electric field at the barrier in the **a,** ON state and **b,** OFF state. The lateral depletion length due to fringing fields [157] in the OFF state was considered to be 20 nm. The field pattern in the OFF state does not exhibit the oscillatory shape corresponding to the highly transmissive mode. Therefore, it can be seen that an electrostatic voltage can control electromagnetic interactions in the devices, which is the basis for the switching mechanism in electronic metadevices. Simulated current deinsity at the semiconductor channel in the **c,** ON state, and **d,** OFF state. The current density in the OFF state do not show any confinement. **e,** Real and **f,** imaginary parts of the current density at the barrier (J_z) in the ON state. The real part of the input current is totally dominant in the ON state, which makes the device impedance to be resistive. **g,** Real and **h,** imaginary parts of the current density at the barrier (J_z) in the OFF state. The imaginary part of the input current is dominant in the OFF state, which makes the device impedance mostly reactive.

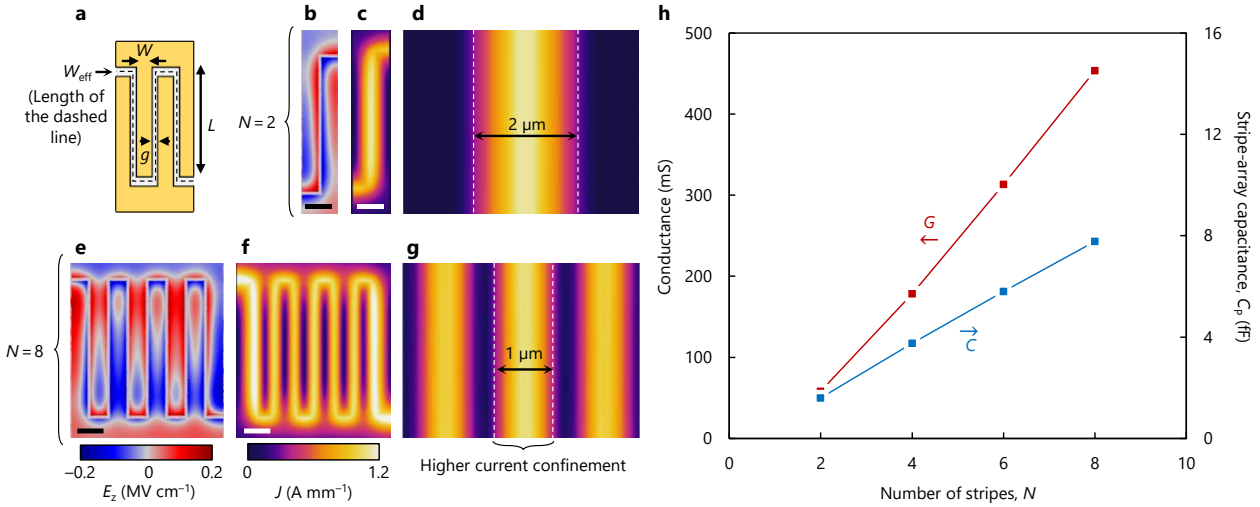

Fig. 2.4 | Effect of number of stripes on the collective interaction, and the superlinear scaling. a, Schematic (top view) of an electronic metadevice with an effective width of $W_{\text{eff}} \cong (N-1)L + N(W+g)$. Microwave metadevices (Table 2.1) were simulated at 70 GHz by COMSOL, where the first port was excited by a current source $I = W_{\text{eff}} \times (1\ \text{A mm}^{-1})$ to scale the total current of electronic metadevices with respect to their effective width. The second port was short circuited. **b,** Vertical electric field at the barrier E_z (real part; in-phase with input current) simulated for a device with two stripes. Similarly to the straight gap device (Fig. 2.2d), the adjacent stripes do not share the same polarity of E_z. **c,** Current density at the 2DEG. **d,** Zoomed in current density at the 2DEG, showing confinement in about 2 μm. **e,** Vertical electric field at the barrier E_z (real part; in-phase with input current) simulated for an electronic metadevice with 8 stripes. The electric field flips within a single stripe and adjacent stripes share the same E_z polarity. **f,** Current density at the 2DEG. **g,** Zoomed in current density at the 2DEG, showing confinement in about 1 μm. The device shows two times more confinement compared to the device with two stripes. The results also indicates the capability of the devices in high-power operation, since at very high current densities of ~1 A mm^{-1}, the devices exhibit E_z much below the critical electric field of wide-band-gap materials. **g,** Simulated conductance and stripe array capacitance (entire gap depleted) of devices with different number of stripes. By increasing the number of stripes from 2 to 4, the capacitance is increased by 2.3-fold, while the device gains 3.1-times in conductance. The increase in the conductance is more than the 2.8-time increase in W_{eff}. Such superlinear increase in the conductance, enhances the cutoff frequency FOM of the devices.

2.2 Electronic metadevices for THz switching: towards infrared electronics

Different metadevices designed for operation in microwave, millimeter-wave (mm-wave), and terahertz bands (Table 2.1) were realized on a high-electron-mobility InAlN (5.3 nm) / GaN epitaxy with a 1.1-nm-thin AlN interlayer and 1.1-nm-thin GaN cap layer grown on a Silicon Carbide (SiC – 6H) substrate.

Table 2.1 | Geometries of metadevices for microwave, mm-wave, and THz operation

Metadevice type	*L* (μm)	*W* (μm)	*g* (nm)	Number of stripes
Microwave metadevices	10.8	1.2	320	2, 4, 6, 8, 12, 16, 20
mm-wave metadevices	3.4	0.78	220	2, 4, 6, 8
Terahertz metadevices	1.7	0.33	120	2, 4, 8

The devices were fabricated in two steps. The first step was an e-beam lithography with with a double layer PMMA 495K A8 / PMMA 495K A4 resist followed by a metal deposition (80 nm Ni / 40 nm Au) to form the pads by lift-off. The second step was to define the mesa region by photolithography and inductively coupled plasma (ICP) etching.

As shown in Fig. 2.5a, the devices were characterized based on two-port complex scattering parameter measurements at microwave, mm-wave, and terahertz frequencies (Fig. 2.5b). For a terahertz electronic metadevice with 8 stripes (inset of Fig. 2.5c), the ON-state resistance (R_{ON}) and OFF-state capacitance (C_{OFF}) extracted from scattering parameter measurements up to 1 THz show extremely high cut-off frequency of 18 THz, which agrees well with simulations (Fig. 2.5c). Fig. 2.5d benchmarks microwave, mm-wave, and terahertz metadevices with different number of stripes on a C_{OFF}-R_{ON} plane, which indicates cut-off frequencies much higher than those achieved by traditional devices.

The benchmark presented in Fig. 2.5d also reveals two major features of metadevices. First, the device performance becomes better at higher frequencies, as terahertz metadevices significantly outperform microwave devices: the cut-off frequency of terahertz devices evaluated at 1.1 THz is notably higher than that of microwave switches evaluated at 50 GHz. This is due to the fact that the subwavelength λ_{sub} becomes shorter at higher frequencies which enables a higher confinement of current in the semiconductor channel, and therefore results in a higher conductance. Second, increasing the number of stripes enhances the device performance. This originates from the collective interaction between the TM mode and the stripe array that becomes more pronounced with larger number of stripes (Fig. 2.4),

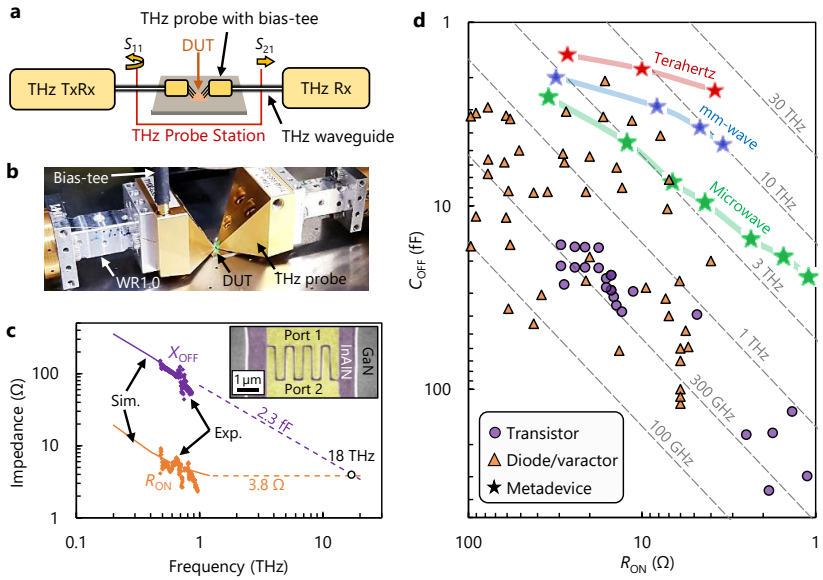

Fig. 2.5 | High-frequency characterization of electronic metadevices. a, Schematic of the experimental setup to characterize electronic metadevices based on complex scattering parameters. **b,** Photograph of the setup corresponding to 0.75-1.1 THz band. **c,** Measured ON-state resistance (R_{ON}) and OFF-state reactance (X_{OFF}) of a terahertz metadevices with 8 stripes (1.7 μm x 330 nm) and channel length of 120 nm (inset) versus frequency. **d,** Benchmark of metadevices with mainstream electron devices on a C_{OFF}-R_{ON} plane showing outstandingly high cut-off frequencies for electronic metadevices. Microwave, mm-wave, and terahertz devices were characterized at 50 GHz, 260 GHz, and 1 THz, respectively.

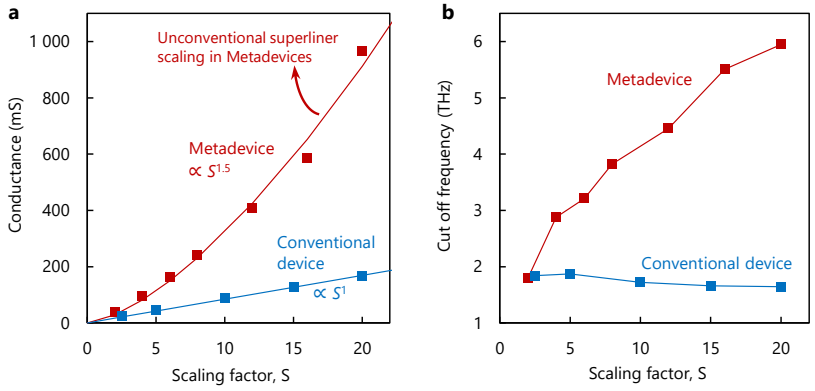

Fig. 2.6 | Superlinear scaling in electronic metadevices. a, ON-state (zero bias) conductance of electronic metadevices (measured at 50 GHz) with different number of stripes (scaling factor, S) indicates a superlinear scaling. This relation is linear for straight-gap devices ($S = W/W_0$ where W is the device width and $W_0 = 4\ \mu$m). **b,** Cutoff frequency of straight-gap devices and metadevice versus scaling factor.

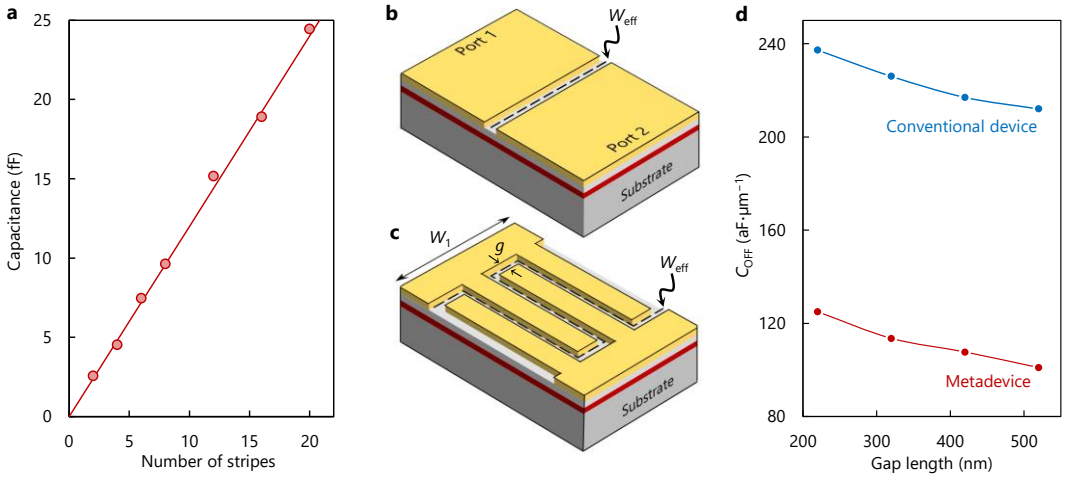

Fig. 2.7 | OFF state capacitance evaluation in metadevices and comparison to straight-gap devices. a, Although the ON-state of the metadevices exhibit a superlinear increase in the conductance with respect to the number of stripes, the OFF capacitance scales just linearly, because the highly transmissive mode is no longer supported by depleting the 2DEG. The measurement results correspond to microwave metadevices. **b,** Schematic of the stripe array structure showing the effective active width of the device (W_{eff}), which is considerably greater than the width W_1. **c,** Schematic of a straight gap structure in which the effective active width of the device is equal to the width of the metallic pad. **d,** Normalized capacitance with respect to the effective active width of the devices in a stripe-array structure (microwave metadevices in Table 2.1) and a straight gap structure for different gap distances (g). The stripe array structure has a notably lower normalized capacitance. This indicates that the metadevices are not only beneficial with regards to the low R_{ON}, but also favorable as they offer a lower OFF state capacitance.

and therefore the conductance of metadevices grows super-linearly with respect to the number of stripes (Fig. 2.6a). Scaling conventional devices reduces R_{ON} and increases C_{OFF} at the same rate, so that the cutoff frequency remains constant (Fig. 2.6b). The metadevice breaks this trade off by significantly reducing the resistance which outbalances the linear increase in C_{OFF} (Fig. 2.7) and results in notably higher cut-off frequencies.

2.3 Contact resistance and quantum resistance

A limitation for conventional ultrascaled semiconductor devices is their large resistance of ohmic contacts. The state-of-the-art tunneling junctions, which are widely used in transistors and diodes, exhibit contact resistance (R_C) values larger than ~30 Ω μm [26], which by itself is equal to the resistance of a 100-nm long channel on a semiconductor with a sheet resistance of 300 Ω/▪. So in the case of ultra-scaled devices, contact resistances totally dominate the semiconducting channel [45]. Fig. 2.8a shows the contact resistance of electronic metadevices (measurement and simulation) versus frequency. Fig. 2.8b presents the obtained contact resistance values versus the total ON-state resistances of metadevices (based on scattering parameter measurements at higher frequencies) comparing to those reported for traditional devices. Thanks to the current confinement (Fig. 2.9), electronic metadevices operate notably better than straight-gap devices and can also outperform tunneling junctions. In case of metadevices operating at terahertz frequencies, a very low contact resistance below 20 Ω μm has been achieved.

The devices also show very low total ON-state resistance (R_{ON}) values approaching the quantum limit of resistance in 2D channel semiconductor devices: The minimum resistance of a two-dimensional semiconductor channel can be represented as $R_q = \pi h/(4q^2 k_F)$, where h is Planck's constant and q is the elementary charge, k_F is the Fermi wavevector. The expression can be simplified to $R_q = 0.072\left(\frac{n_S}{10^{13}\ \mathrm{cm}^{-2}}\right)^{-1/2}\ \mathrm{k\Omega}\ \mu m$, where n_S is the carrier density per unit area. Since R_q is independent from the channel length, it is sometimes referred to as the quantum limit of contact resistance ($R_q = 2R_C$). Considering $n_S = 1.8 \times 10^{13}\ cm^{-2}$, the minimum resistance of device based on a 2DEG channel would be ~54 Ω μm. The results in presented in Fig. 2.8 shows that the R_{ON} value obtained for the terahertz devices is close to this theoretical limit. Such a low resistance can play a key role to enable not only high-performance terahertz switches, but also terahertz amplifiers with very large transconductances in a three-terminal device form factor.

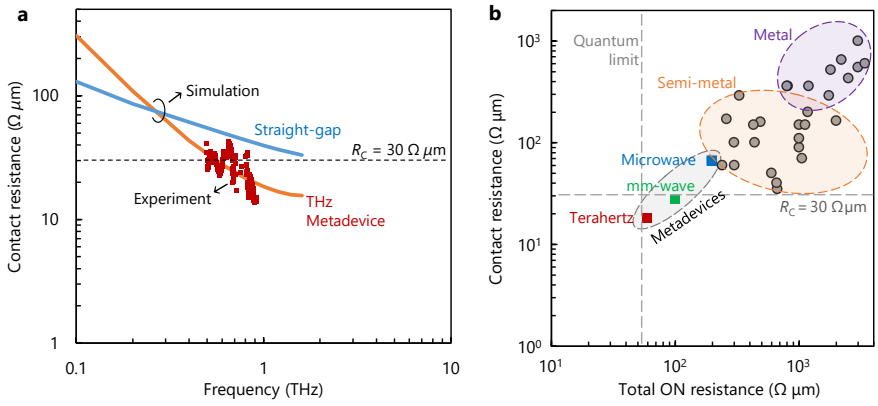

Fig. 2.8 | Electronic metadevices enabling ultralow on-state resistances. a, Simulated contact resistance of conventional (straight-gap) and metadevices showing the superior performance of metadevices showing below 30 Ω μm contact resistances which agrees well with the measurements. **b,** Normalized contact resistance and total ON-state resistance of metadevices and classic devices with tunneling junctions based on metal and highly-doped semiconductor (semi-metal) contacts. Electronic metadevices show record low contact resistance and total resistance values. The RON achieved for electronic metadevices approach the quantum limit of resistance.

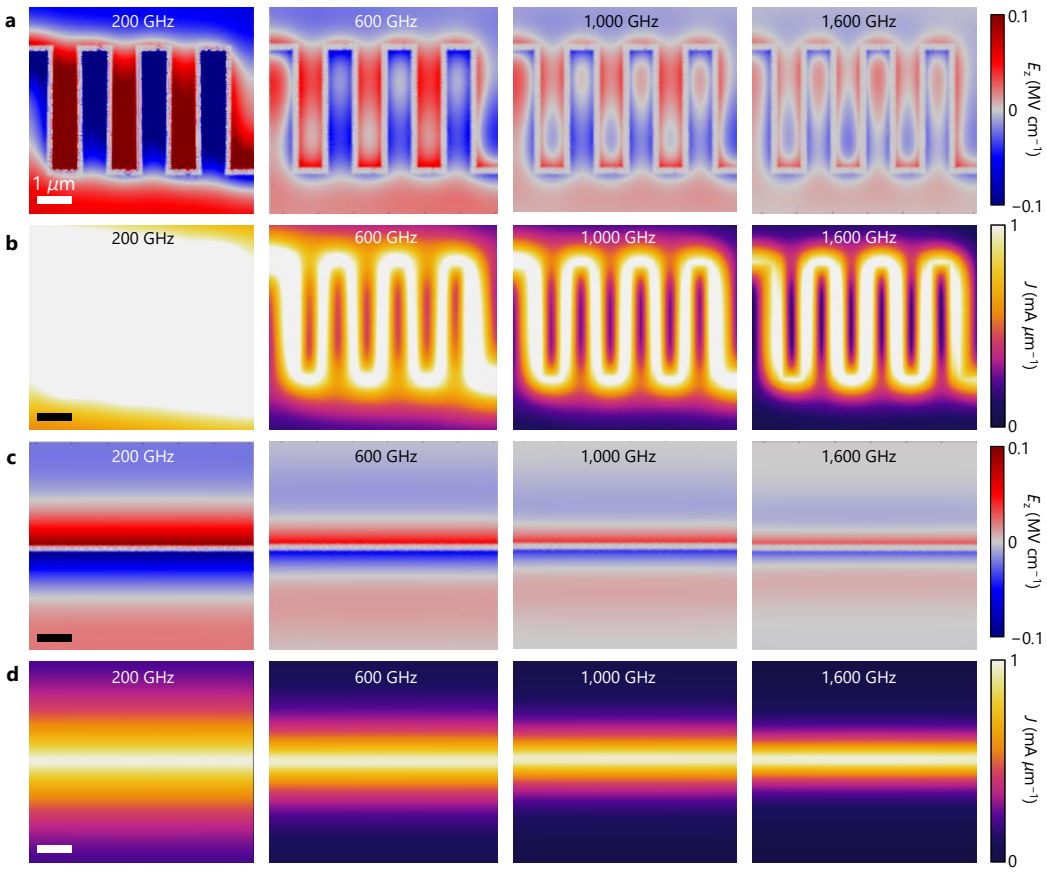

Fig. 2.9 | Simulation of electronic metadevices operating at terahertz frequencies. a, Simulated vertical electric field pattern (real part) at the barrier of the terahertz metadevice at different frequencies from 200 GHz to 1.6 THz. The input port of the devices was excited by a current source (15 mA with zero phase), and the real part of E_z is plotted. The absolute value of the current density was selected to have a current density of ~1 A mm^{-1} in the 2DEG. **b,** Simulated current density at the semiconductor channel at different frequencies from 200 GHz to 1.6 THz. At 200 GHz, there is almost no interaction between the TM mode and the stripe array, and therefore, current density is not confined. The current density has the most confinement at the highest frequency, 1.6 THz. **c,** Simulated electric field pattern (real part) at the barrier of a straight-gap device at different frequencies from 200 GHz to 1.6 THz. The input port of the devices were excited by a current source (3.2 mA with zero phase), and the real part of E_z is plotted. The absolute value of the current density was selected to have a current density of ~1 A mm^{-1} in the 2DEG. **d,** Simulated current density at the semiconductor channel at different frequencies from 200 GHz to 1.6 THz. The straight-gap device clearly does not show the level of current confinement seen in the Metadevices at high frequencies.

2.4 High breakdown voltage and high-power operation of electronic metadevices

The proposed metadevices not only exhibit extremely high performance at high frequencies, but also provide a very high breakdown voltage, which enables a robust performance and an excellent prospect to operate at large powers. Conventional terahertz switches break at only a few volts [159], while metadevices with very high cut-off frequency show large breakdown voltages over 30 V. Figure 2.10a presents the breakdown test of metadevices with different gap distances, showing a low leakage current below 200 nA mm^{-1}, and a very high breakdown voltage, from 50 V for 220-nm-long gaps up to 125 V for 520 nm-long gaps, corresponding to a high average critical electric field of 2.4 MV cm^{-1}.

Fig. 2.10b presents the breakdown voltage versus cut-off frequency of electronic metadevices, which shows almost two orders of magnitude increase in $V_{BR} \times f_c$ with respect to traditional devices. This resolves a key challenge in terahertz electronics, as traditional terahertz devices can only handle very low voltages of only a few volts [159], while electronic metadevices with cut-off frequency of 18 THz can withstand 30 V.

Carrier density and electron mobility together with the critical electric field impose a fundamental trade-off between conductance and breakdown voltage in semiconductor devices. In a lateral device, this trade-off is determined by the sheet resistance, contact resistance, and the critical electric field. The ideal device line in Fig. 2.10c assumes a zero contact resistance, while the other dashed line indicate the maximum conduction considering the state-the-art contact resistance of R_C = 30 Ω μm. The proposed metadevices outperform the best traditional devices in the literature due to their outstanding conductance, enabling the device performance to approach the ideal device limit determined by the semiconductor material.

Another important aspect of a radiofrequency device is the ON-state linearity at high-power regime, which is typically evaluated by the third-order intercept point, so called IP3, which is the linearly extrapolated input power at which fundamental and third-order harmonics intersect [160]. Fig. 2.11a shows the linearity of a 220-nm-long-channel switch in the ON state, where the input signal was supplied at 10 GHz and both the fundamental frequency and the third harmonic of the input (P_{in}) and output (P_{out}) were obtained. In addition to the very low loss, the switch exhibited a remarkable linearity,

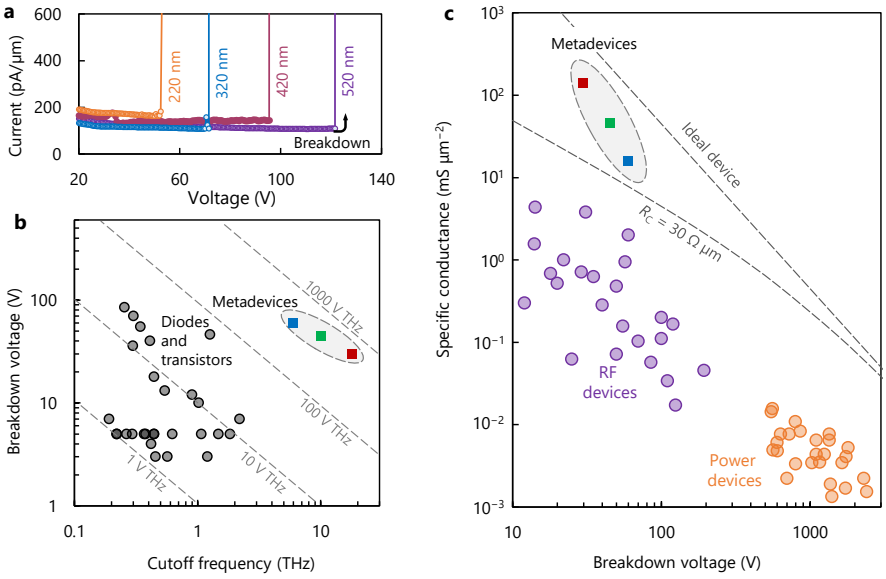

Fig. 2.10 | Conductance-versus-breakdown trade-off in metadevices. a, Breakdown test on metadevices with different gap distances, 220 nm, 320 nm, 420 nm, and 520 nm. **b,** Breakdown voltage versus cutoff frequency FOM in diodes and transistors, as well as metadevices (red: THz, green: mm-wave, and blue: microwave). The results show that the proposed metadevice concept outperforms the state-of-the-art in mainstream electron devices. **c,** Specific conductance versus breakdown voltage for metadevices and classic radiofrequency and power devices. The performance of metadevices is very close to the ideal limit corresponding to the critical field of GaN (3 MV cm^{-1}) and a sheet resistance of 200 Ω/▪. **c,** Breakdown voltage versus f_{CO} for transistors and diodes, as well as electronic metadevices.

along with a high power capability of ~0.5 W mm^{-1}, corresponding to a ~20 dBm input power (limited by the radiofrequency signal source used). The device did not show any notable non-linearity, as the levels of the third harmonic at the input and output of the device are almost equal. In this case, it is not possible to determine the IP3 frequency, as the switch behaves highly linearly. Another sign of high linearity is the lack of signal deformation between the input and output voltage waveforms (Fig. 2.11b), for fairly large amplitudes.

The P_{out} was calculated based on the measured voltage waveform at the oscilloscope port (v_{osc})

$$P_{out} = \frac{1}{NZ_0}\sum_{n=1}^{N} v_{osc}^2(nt_S). \tag{2.4}$$

Here Z_0 = 50 Ω is the oscilloscope termination impedance, t_S = 10 ps is the sampling time, and N = 2,000,000 is the captured sample length which includes 200,000 cycles. To measure the input radiofrequency power, the same integration was used on the measured waveform corresponding to a through feature. The losses in the radiofrequency probe (Fig. 2.11c) and the coaxial cable (Fig. 2.11d), were de-embedded to obtain the input radiofrequency power P_{in}. These losses were also de-embedded to achieve the Pout.

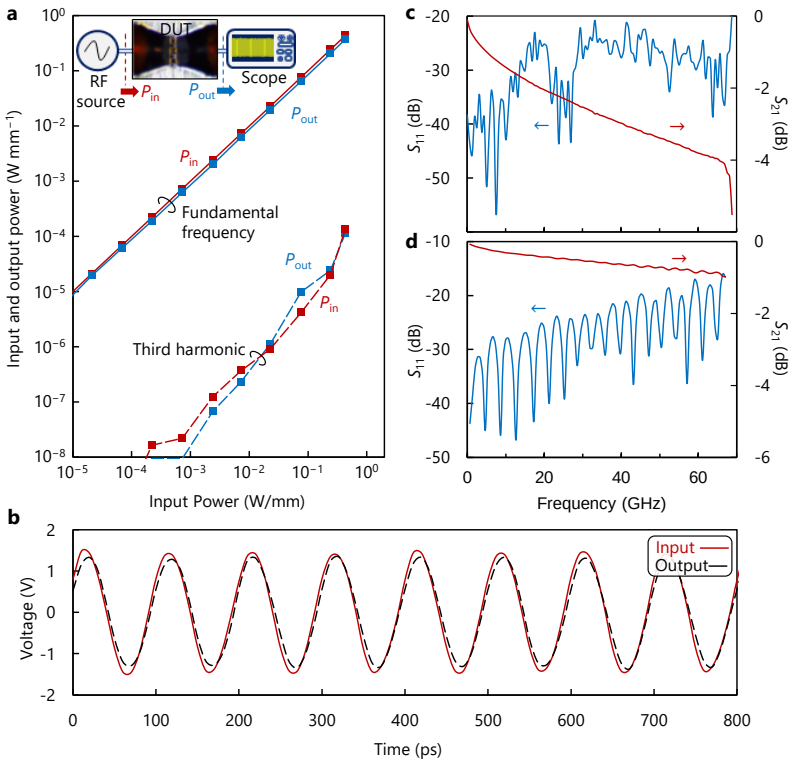

Fig. 2.11 | Evaluation of the linearity of displacement-field switches. a, Input and output radiofrequency powers at 10 GHz, for the fundamental frequency as well as the third harmonic, showing a high-power highly-linear performance. The inset shows a schematic of the experimental set-up. **b,** Sample input and output voltage waveforms showing a deformation-less high-amplitude operation. Scattering parameters of **c,** the radiofrequency probe (port 2), and **d,** the cable connecting port 2 to oscilloscope port.

2.5 Compact Circuit Model of Electronic Metadevices

Based on the discussions and physical insights given by the results shown in Fig. 2.3 and the transient performance described in Fig. 2.12, we presents a compact circuit model for the electronic metadevices in Fig. 2.13. The model consists of the following elements (Figs. 2.3a-c):

1. The channel resistance R_{ch}: This part can be considered to be constant with respect to frequency and voltage. It represents the pure resistive impedance corresponding to the semiconductor channel. For a metadevice with effective width W_{eff} and gap g (see Fig. 2.7), we have $R_{\mathrm{ch}} = gW_{\mathrm{eff}}^{-1}R_{\mathrm{sh}}$, where R_{sh} is the sheet resistance of the semiconductor layer.

2. The series resistance R_S: This part models the losses due to the presence of current in the semiconductor outside the gap (equivalent to the summation of contact resistances from the two sides of the channel). The contact resistance drops with increasing the frequency and ultimately becomes insignificant compared to R_{ch} (as shown in Fig. 2.8b, R_C is only ~10% of the total R_{ON}). R_S is a function of voltage, and becomes larger while switching OFF the device (Fig. 2.12). This happens due to the depletion of the semiconductor layer under one terminal.

3. The series reactance $X_S = L_S\omega - (C_S\omega)^{-1}$: This part models the reactive impedance due to the metal-semiconductor coupling. The electric field distribution in the transmissive mode forces X_S to be zero (Fig. 2.3f). This can be modeled by a series inductor-capacitor resonator. We can re-write X_S as

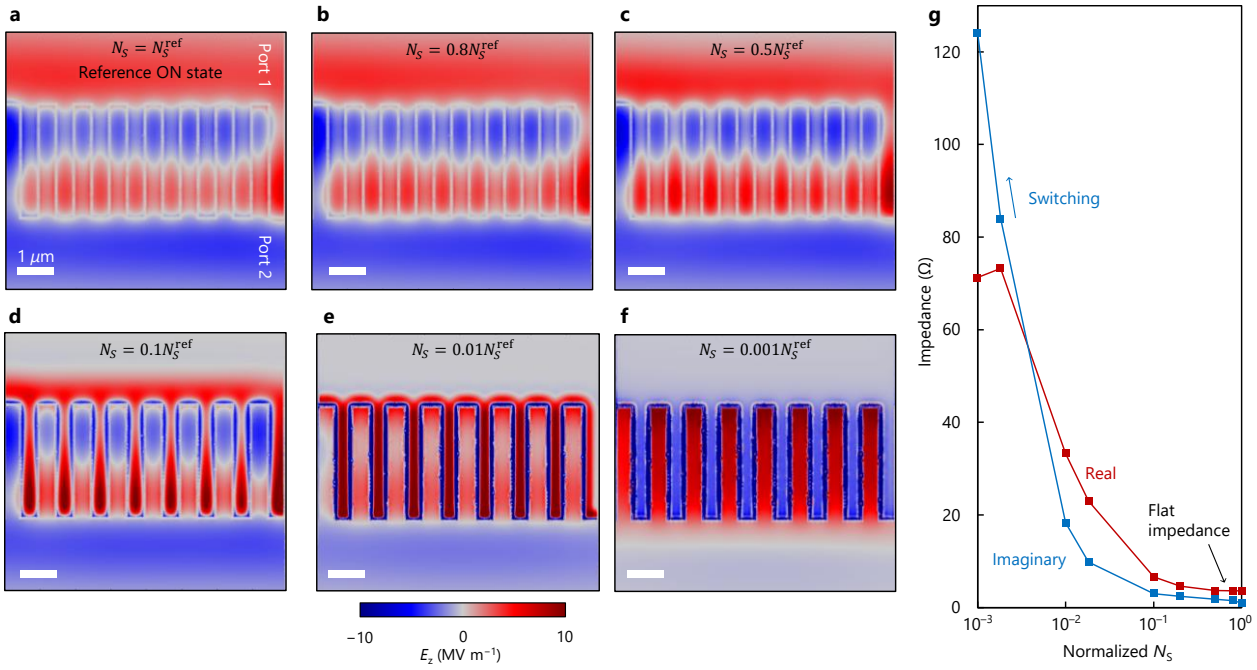

Fig. 2.12 | Electric field patterns and electrical characteristics of metadevices at partial depletion. Simulated vertical electric field (E_z) at the barrier with different electron densities (sheet resistances) under port 1. **a,** $N_S = N_S^{\mathrm{ref}}$ (identical to Fig. 2.2f), **b,** $N_S = 0.8N_S^{\mathrm{ref}}$, **c,** $N_S = 0.5N_S^{\mathrm{ref}}$, **d,** $N_S = 0.1N_S^{\mathrm{ref}}$, **e,** $N_S = 0.01N_S^{\mathrm{ref}}$, **f,** $N_S = 0.001N_S^{\mathrm{ref}}$. **g,** Extracted impedance (real part, red, imaginary part, blue) from simulations at different electron densities. The field distributions and the impedances are quite flat up to ~50% depletion.

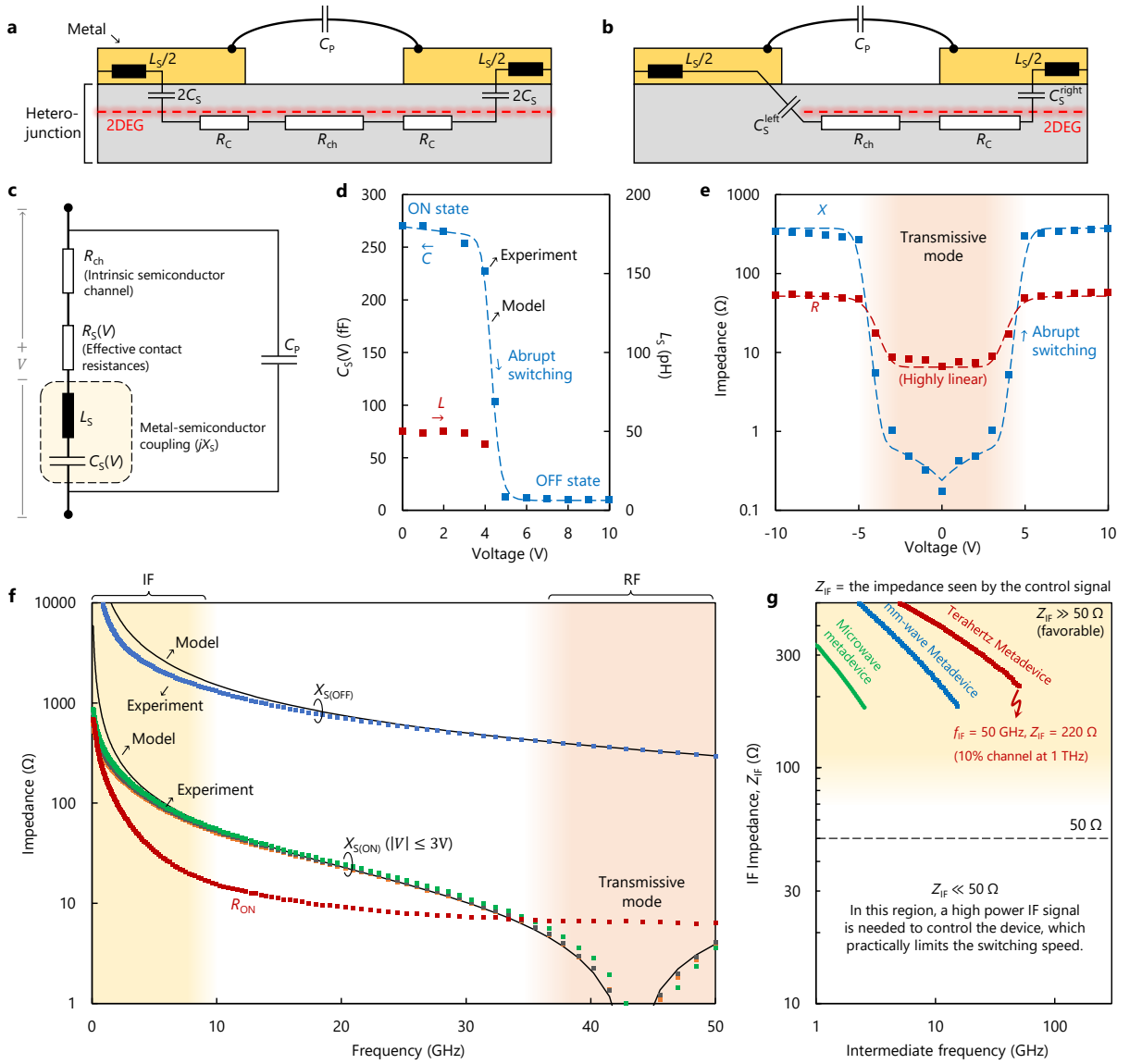

Fig. 2.13 | Circuit model of electronic metadevices. Schematic of the cross section of metadevices in **a,** ON, **b,** OFF states. **c,** Proposed compact circuit model including four elements $R_{\rm ch}$ (channel resistance) R_S (contact resistances), $X_S = L\omega - (C\omega)^{-1}$ (reactive impedance due to the metal-semiconductor coupling), and C_P (capacitance between the interdigital metals). **d,** Extracted C_S and L_S at different voltages (discrete points). The inductance play a negligible role in the OFF-state reactance, and therefore, it can be considered constant ($L_S = 50$ pH) for the entire voltage range. The measured capacitance was empirically fitted by $C_S(V) = 260\left(1 + \frac{1}{25}(|V|/V_{\rm th}) + (V/V_{\rm th})^{20}\right)^{-1} + 9.5$ fF, with $V_{\rm th} = 4.3$ V (dashed line). **e,** Measured (discrete points) and modeled (solid lines) impedances at the resonance frequency ($\omega = \omega_{0S}$). Red (real part), blue (imaginary part). The device exhibits a very linear ON state followed by an abrupt switching. **f,** Broad-band measured impedance of the device in ON ($|V| \leq 3$ V) and OFF states ($V = 10$ V) (discrete points), showing a very good agreement with the model (solid lines). In a wide range of frequencies around the resonance, the imaginary part of the impedance is very small and negligible compared to $R_{\rm ON}$, which shows the wide band nature of the transmissive mode. **g,** Absolute values of the impedance of the 6-stripe microwave metadevice, as well as 4-stripe mm-wave and terahertz metadevices (parameters described in Table 2.1) at intermediate frequencies. Considering data modulation with a 10% bandwidth, the devices show a high impedance for the control (data) signal, while exhibiting a low impedance for the carrier signal. This feature is radically different from conventional devices, and enables high performance large signal switching with low-power control signals.

$$X_S = Z_{0S}\left(\frac{\omega}{\omega_{0S}} - \frac{\omega_{0S}}{\omega}\right) \tag{2.5}$$

Where $\omega_{0S} = (L_S C_S)^{-1/2}$ and $Z_{0S} = (L_S/C_S)^{1/2}$ represent the central frequency and the characteristic impedance of the resonator. We note that $X_S(\omega_{0S}) = 0$, and X_S could be very small (negligible compared to R_{ch}) for a wide range of frequencies, if Z_{0S} is low impedance. This represents the wide-band nature of the mode (Fig. 2.9), which is consistent with s-parameter measurements.

Based on the simulations presented in Fig. 2.12, X_S plays the dominant role in the switching transient. In this case, switching the vertical displacement field at the barrier, totally changes the state of the device. We model this effect by considering a voltage dependence of the series capacitor, $C_S(V)$, where V is the voltage across the device. Due to the symmetry of the proposed devices, $C_S(V)$ is an even function ($C_S(V) = C_S(-V)$).

4. The parallel capacitance C_P: Even without having the semiconductor layer, the stripe array has a capacitance, like interdigital capacitors. So C_P is a linear capacitance parallel to the device terminals.

In fact both C_S and C_P contribute to the OFF-state capacitance of the device (C_{OFF}), however, at moderate voltage biases, where only a small portion of the channel is depleted (Fig. 2.13b), C_S dominates C_P. So in applications like modulators, where the device does not hold very large voltages, only the series impedance

$$Z_S = R_{ch} + R_S(V) + j\left(2\pi f L_S - \frac{1}{2\pi f C_S(V)}\right) \tag{2.6}$$

can be an accurate representation of the device impedance.

We evaluated the proposed circuit model in a metadevice with 8 stripes (L = 10.8 μm, W = 1.28 μm, g = 320 nm). Based on s-parameter measurements we extracted the capacitance and the inductance of the switch, from 0 to 10 V (Fig. 2.13d). Since C_S dominates C_P at moderate voltages, we assigned the entire extracted capacitance to C_S. The capacitance was almost flat up to ~3 V, and then showed an abrupt change. We empirically fitted the obtained values by

$$C_S(V) = \frac{260}{1+\frac{1}{25}(|V|/V_{th})+(V/V_{th})^{20}} \text{ fF} \tag{2.7}$$

where $V_{th} = 4.3\ V$ is the threshold voltage. The series inductance was quite small and only affected the device impedance in the ON state, were it showed the voltage-independent value of 50 pH. As shown in Fig. 2.13e, considering the resonance frequency (~43 GHz), the fixed value of L_S together with the fitted capacitance, well describe the device impedance for a large voltage swing, from −10 V to +10 V. The real part of the impedance ($R_{ON} = R_{ch} + R_S$) was fitted by

$$R_{ON}(V) = 6.5 + \frac{4.5}{1+(V/V_{th})^{-10}}\ \Omega \tag{2.8}$$

The model works well for a broad range of frequencies. Fig. 2.13f shows a very good agreement between the modeled reactance (solid lines) and measurements (discrete points) in both ON and OFF states. The series inductance X_S is negligible compared to R_{ON} for a wide range of frequencies (~20% bandwidth), which shows the wide-band nature of the transmissive mode. Fig. 2.13f also indicates that

R_{ON} can be practically considered to be frequency independent. This is because R_{ON} is almost flat for high frequencies, and for low frequencies, X_S totally dominates R_{ON}. So X_S can solely describe the impedance at low frequencies. In this case, one can assume a fixed value for R_{ON} (corresponding to that of high frequencies).

An important feature of the proposed devices is that they exhibit different impedances at low and high frequency. The transmissive mode offers very low impedances in a wide frequency window (the transmissive mode). At intermediate frequencies, however, X_S becomes large. This can be highly beneficial for the switching performance of the device. For example, schottky diodes exhibit almost identical impedances for low and high frequencies: in this case if the device achieves a low insertion loss at high frequencies, then a high power control signal is needed to switch ON and OFF the device. In metadevices, however, the control signal sees a rather high impedance while the carrier signal sees a low impedance. Considering the intermediate frequencies corresponding to a channel of 10% bandwidth around the resonance frequency, all the different kinds of metadevices realized (microwave, mm-wave, and terahertz devices) show high impedances ($Z_{\mathrm{IF}} \gg 50\ \Omega$) (Fig. 2.13g).

The results obtained by the s-parameter measurements, which were captured by the circuit model, show a great correlation to the microscopic features of the device. In particular, the following points:

1. The device exhibits a very flat response in the ON state. At the highly transmissive mode, the reactive part of the impedance is totally negligible and the measured resistance is almost constant in a large voltage swing between –3 V to +3 V. This level of linearity is an important feature of the proposed devices which is originated from their very fundamental working principle. This is a great benefit for RF switching, since the device does not produce harmonics.

2. The switching is mainly driven by X_S and it is quite dramatic. This is also in agreement with the simulations which showed that X_S plays the most important role in the switching mechanism. The abrupt switching reflects in the steep functionality of $C(V)$ presented in equation (2.7).

3. The transmissive mode is quite wide-band which is reflected in the low impedance of $Z_{0\mathrm{S}}$. For the devices shown in Fig. 2.13g, $Z_{0\mathrm{S}}$ is about ~10 Ω, resulting in $X_{\mathrm{S}} < 2\ \Omega$ for a 20% bandwidth, which is negligible compared to the ON-state resistance of the devices. Scaling up the metadevices further reduces $Z_{0\mathrm{S}}$ and X_{S}.

4. The devices exhibit high impedances for intermediate frequencies, which is highly beneficial for large signal switching. If we apply

$$v_{\mathrm{in}}(t) = A_{\mathrm{IF}} \cos(\omega_{\mathrm{IF}} t) + a_{\mathrm{IF}} \cos(\omega_{\mathrm{RF}} t) \tag{2.9}$$

to the first port (A_{IF} and a_{RF} represent the amplitudes of the intermediate frequency (IF) and RF signals with angular frequencies of ω_{IF} and ω_{RF}) and terminate the second port by a load, then the RF signal will be transmitted without producing a considerable voltage across the terminals (because the device has a low impedance). For the IF signal, however, most of the amplitude A_{IF} will drop across the terminals which switch ON and OFF the device. This is not the case in schottky diodes, for example, were a strong IF signal is needed to switch the device.

2.6 Dynamic performance of electronic metadevices: resilience against trapped carriers

We aim to evaluate the switching performance of electronic metadevices under harsh conditions, at high voltages and high speeds. This is important since trapped carriers under high-voltage stresses can potentially degrade the (trans)conductance of lateral devices [161]. Fig. 2.14 shows a schematic of the experimental setup for accurate characterization of metadevices under harsh switching conditions. The amplified output of a high-speed function generator is applied to one port of the device. The second port is terminated by a VNA, which measures the temporal refection from the device at the fixed frequency of 40 GHz. The reflection coefficient gives the full information about the impedance of the DUT. In this setup, the IF bandwidth of the VNA determines the measurement accuracy. We used the IF frequency of 10 MHz corresponding to one measurement point per 70 ns. This gives almost the best possible measurement speed, as the maximum IF frequency of the VNA was 15 MHz (which led to significant drop in the signal-to-noise ratio). We note that trapping and de-trapping mechanisms are rather slow processes, and having a longer stress time (applying a high voltage while the device is in the OFF state) results in a more significant trapping and memory effect. De-trapping processes can be even slower with characteristic times well over 1 μs [162], [163]. Therefore, the measurement speed that we could achieve is enough to evaluate the trapping-induced memory effect in the devices.

We submitted a metadevice (L = 10.8 μm, W = 1.28 μm, g = 320 nm, and with 8 stripes) to a burst of high amplitude pulses (100 cycles), periodically switched between ON and OFF. The device was relaxed for 10 ms, before the next burst was applied. Fig. 2.14b shows the temporal reflection (magnitude of S_{11}) from the DUT for the case of 20 V pulses. Fig. 2.14c presents the zoomed-in view of the first 10 μs, showing that the device is stressed in the OFF state for 4 μs, and turns ON only for 500 ns for the measurement of the S_{11}, and consequently, to extract the ON resistance. We note that this is a very harsh condition, for three reasons:

1. The device has a threshold voltage of about 4.5 V, while we applied pulses with high amplitudes of 10 V, 15 V, and 20 V, which are much higher than the actual operation voltage of the device. In general, these voltage levels are extremely large for such high-speed devices. We note that at such voltages, the electric fields in the devices are on the order of 1 MV cm^{-1}.

2. The ON/OFF duty cycle is very low (about 10%) meaning that the device is almost constantly under stress, and there is a short time to relax. In a modulator, the duty cycle is about 50%, and so the device has much more time for relaxation.

3. The OFF state time is quite long compared to the realistic operation of the devices, in the gigabits per second regime, for example. In this case, we stress the device for a longer-than-usual time to fill up the possible trap states.

The average resistance over the ON-state periods at each switching cycle was extracted and normalized by that extracted resistance of the fully relaxed device (t < 0 in Fig. 2.14b). The results presented in Fig. 2.14d show a very small increase of the post-stressed ON state resistance. In addition, the device showed a hysteresis-free switching. The device was submitted to a 2-μs-long ramp-up voltage, stressed for 10-μs, and then ramped down again (Fig. 2.14e). The measured reflection coefficient versus applied voltage shows no hysteresis loop (Fig. 2.14f).

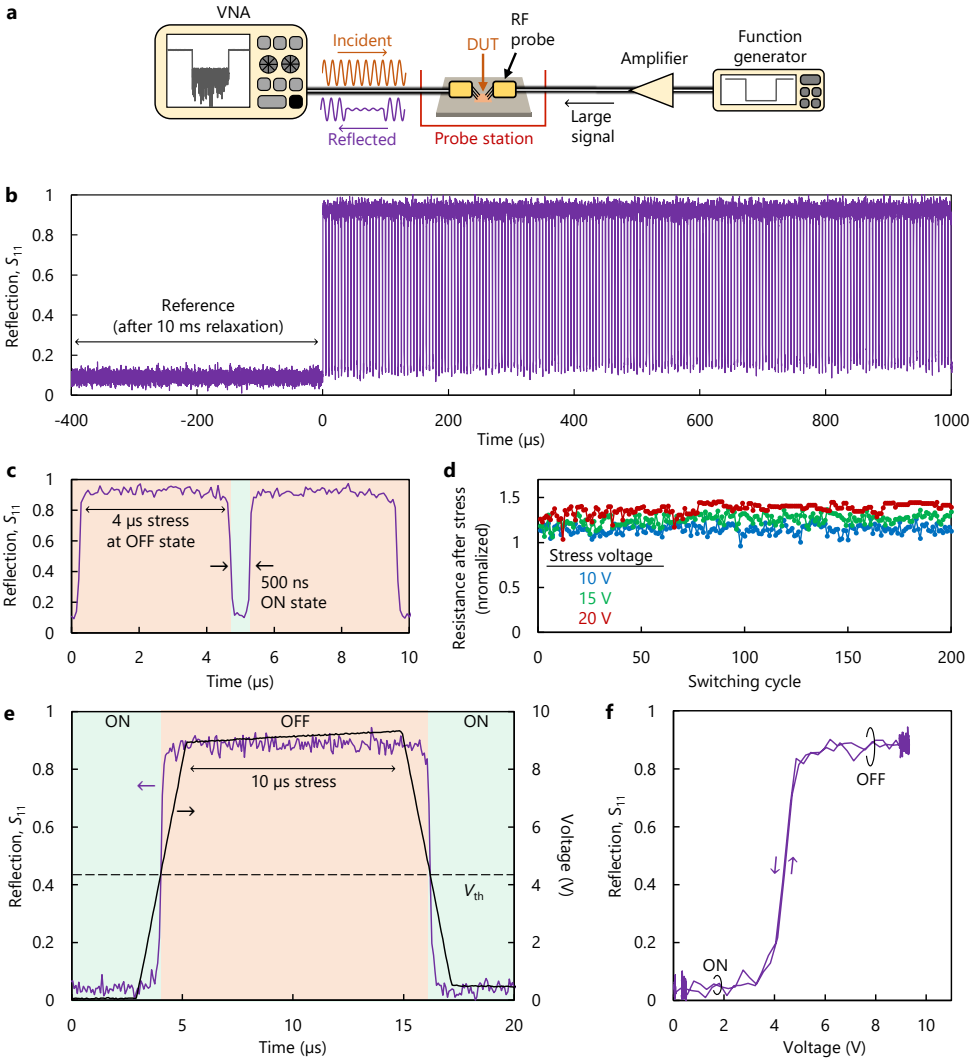

Fig. 2.14 | Dynamic performance of electronic metadevices under harsh switching conditions. a, Schematic of the experimental setup to evaluate the dynamic performance of the metadevices under harsh switching conditions. **b,** Measured reflection (S_{11}) from the device, under burst conditions. The device is relaxed for 10 ms followed by a sequence of 100 switching cycles. The measurement corresponds to the switching amplitude of 20 V. **c,** Measured reflection in a time period of 10 μs. At each period, the device holds a stress for about 4 μs, and then goes to the ON state for about 500 ns. The ON resistance of the device is extracted based on the reflection coefficient. **c,** Extracted ON resistance of the device (normalized by the reference resistance of the relaxed device, as shown in part a) for different amplitudes over the 100 cycles. Without any passivation, the device shows a very good performance with only a negligible R_{ON} degradation. **e,** Waveforms in a double-sweep experiment to evaluate possible hysteresis in the threshold voltage. The device is submitted to a large signal voltage and the reflection is measured in both switching cycles (ramp up and ramp down). **f,** Extracted double-sweep reflection showing a hysteresis-free operation.

We believe that there are two main reasons for such an excellent dynamic performance (even though the device had no passivation layer):

1. Normally, oxide layers can host a high density of trap states, which is a significant source of dynamic R_{ON} degradation in planar HEMTs, for example [164]. Electronic metadevices do not have any oxide layers, which is a benefit.

2. Electronic metadevices transmit RF signals through electromagnetic coupling and not electron injection. One has to see how much trapped carriers can perturbate the transmissive mode of the device. As shown in Figs. 2.12 and 2.13, one important point about the proposed devices is that they have a very flat resistance-versus-voltage and resistance-versus-N_S in the ON state. This can clarify the origin of the excellent dynamic performance: the electrostatic partial depletion of channel due to the trapped carriers can be mimicked by a virtual gate [165]. The fact that small potentials do not degrade the performance of the device, means that the effect from the trapped carriers could be quite negligible too.

Because electronic metadevices show negligible memory effect under harsh switching conditions, one expects that the switching speed has to be solely driven by the field-driven depletion/accumulation of charges which can be extremely fast. For example, HEMT platforms are used for detection of sub-picosecond THz pulses, which shows how fast the electrons can respond to ultrafast electric fields [166]. In case of electronic metadevices, as we discuss in the next section, a flat frequency response up to ~100 Gb s^{-1} (corresponding to picosecond switching times) was experimentally demonstrated, and the device has the potential to operate at much higher speeds.

2.7 THz modulators and mixers based on two-terminal metadevices

To show one application of the presented electronic metadevice, a modulator to map an electrical signal onto a THz carrier was demonstrated, which shows the potential for ultrahigh capacity wireless communication links [19]. As presented in Fig. 2.15a, in a two-terminal scheme, the data signal is applied to one port of a metadevice integrated with coplanar waveguides. A terahertz continuous wave is injected to the second port of the device. The data signal controls the state of the metadevice, and correspondingly changes the reflection of the THz wave. The reflected wave is separated from the incident carrier by a directional coupler and goes to a coherent THz receiver which down-converts the signal to the intermediate frequency (IF). Fig. 2.15b shows received signals with different carrier frequencies, along with the eye diagram of the 520.4 GHz channel shown in Fig. 2.15c. The corresponding spectra presented in Fig. 2.15d shows that the precise modulation by metadevices can provide a platform for ultra-dense allocation of communication channels which enables massive THz wireless networks. The modulation efficiency of the system was examined at very high stream data rates. The data signal was replaced by a sinusoidal source which represents a consecutive sequence of "01". Fig. 2.15e shows the normalized modulation efficiency at the carrier frequency of 0.55 THz which indicates a flat response up to very high data rates. To evaluate the frequency response of the modulator, we fixed the RF frequency at 10.2 GHz corresponding to the output frequency of 550.8 GHz. We applied a sinusoidal wave (at frequency fd) to the second port of the device. At the receiver side we selected LO frequency of f_{LO} = 10.19537 – f_d / 54 GHz to have a fixed IF frequency of 250 MHz after down-conversion.

Ultrafast low-jitter switching dynamic is an important advantage of terahertz switches realized by the metadevice concept with respect to high-cut off frequency switches such as those based on micro-electro-mechanical systems (MEMS) [61], phase-change materials [62], and 2D memristors [63] (Table 2.2). In addition, Fig. 2.16 shows the application of metadevices for ultra-wide-band mixing as another showcase of operation in the THz band. In this case, a 0.526 THz signal was mixed a combination of two radiofrequency signals at 12 GHz and 18 GHz. A power combiner is used to combine the

radiofrequency signals and apply the combination of the two to one port of a metadevice. The terahertz signal is applied to the other port of the device and the reflection is measured by a THz receiver.These results reveals the enormous potential of electronic metadevices for THz applications [167]-[170].

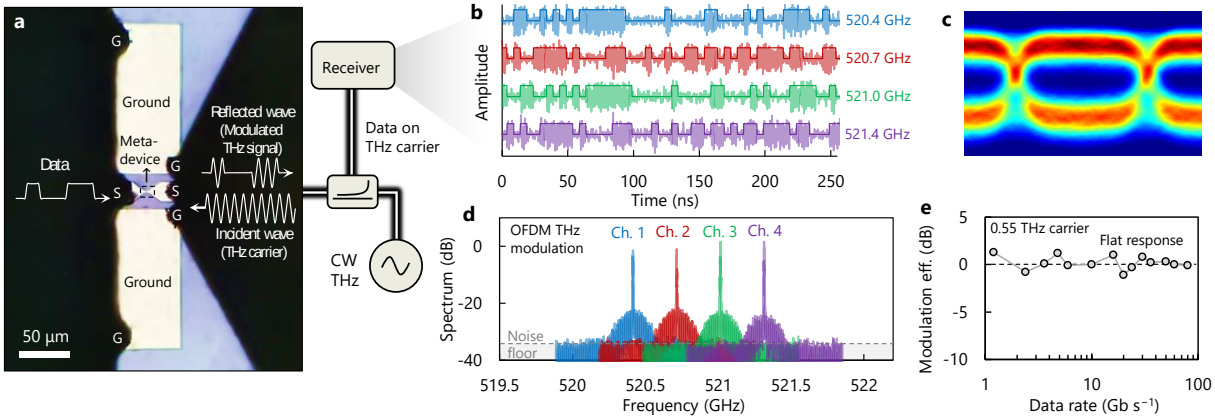

Fig. 2.15 | High-performance THz data transmitters using electronic metadevices. a, Optical microscope image of a metadevice modulator. The data signal, fed into the left port, modulates the incident THz wave injected in the right port. The reflected wave is the data signal on the THz carrier which is received by a coherent receiver. **b,** Received modulated signals with four different carrier frequencies. The very high ON/OFF ratio shows that metadevice modulators are operational at frequencies much above 0.5 THz. **c,** Eye diagram of the 520.4 GHz channel indicating an excellent modulation. **d,** Spectrum of the received signals. The high-performance modulation results in almost zero cross talk between channels which indicates the potential of metadevice modulators for ultra-dense allocation of channels in massive communication networks. **e,** The modulation efficiency versus data rate, indicating an efficient modulation of THz signals with very high data rates.

Table 2.2 | Comparing terahertz switches realized based on metadevice concept with classic devices

Characteristics	Metadevice	FET	Schottky diode	PIN diode	MEMS	Memristor	Phase change
Cutoff frequency FOM, f_{co}	Very high	Moderate	High	Moderate	Very High	Very high	Very high
Dynamic switching	Fast	Fast	Fast	Slow	Very Slow	Moderate	Slow
Jitter (Phase noise)	Low	Low	Low	Low	High	High	High
Operation lifetime	Infinite	Infinite	Infinite	Infinite	Limited	Limited	Limited
Breakdown	High	Low	Low	Moderate	Moderate	Low	-
ON state static power	0	0	High	Very high	0	0	High*
MMIC integration	Yes	Yes	Yes	No	No	No	No

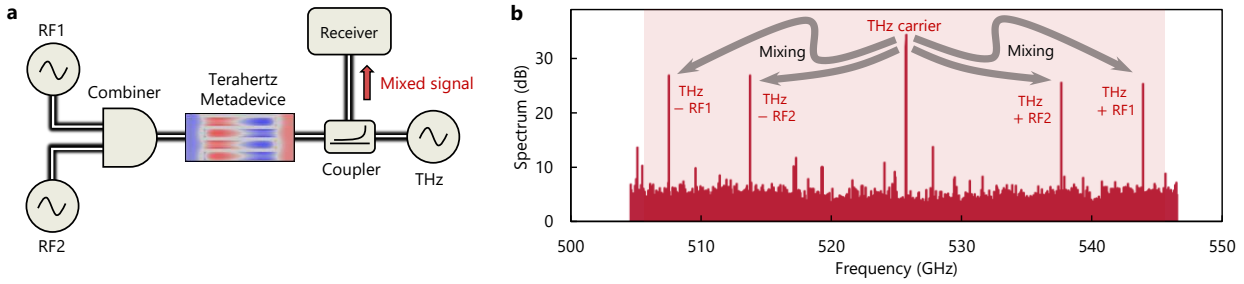

Fig. 2.16 | Ultra-wide-band THz mixers using electronic metadevices. a, Schematic of THz mixing with two RF signals. The RF signals, which are applied to one port of the metadevice through a power combiner, modulate the THz wave coming at the second port. **b,** Spectrum of the mixed signal with f_{THz} = 0.526 THz, f_{RF1} = 18 GHz and f_{RF2} = 12 GHz exhibiting extremely high mixing efficiency of −8 dB which does not degrade from 12 GHz to 18 GHz.

2.8 Three-terminal electronic metadevices and modulators

The concept of electronic metadevice can be extended to three-terminal devices in which the state of the device is controlled by an electrostatic gate (Fig. 2.17a). The gate terminal does not perturbate the electric field pattern over the device layout, and so the device takes the advantage of the electric field manipulation (Fig. 2.17b). By depleting the semiconductor under the gate, the electric fields revert to

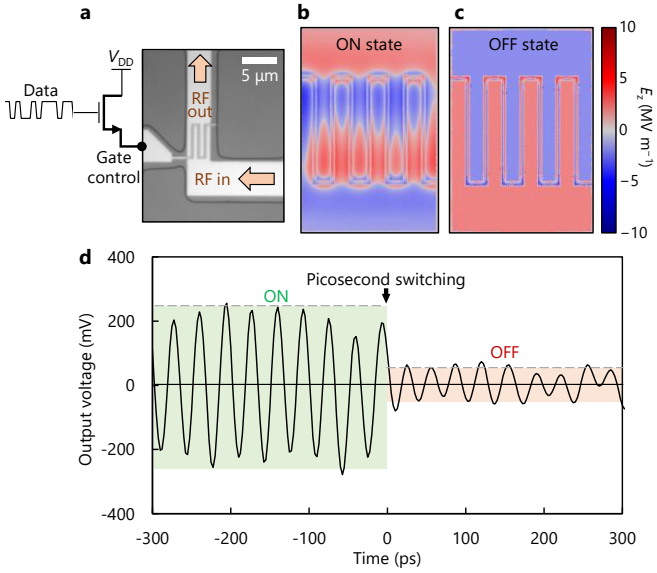

Fig. 2.17 | Three terminal metadevices. a, Micrograph of a fabricated three-terminal metadevice. One terminal is pumped with a radiofrequency signal and the state of the device is controlled by the gate terminal. In an integrated-circuit form factor, the gate terminal of the metadevice can be controlled similarly to a field-effect transistor, by either applying an over-threshold bias or by floating the terminal. **b,** Simulated electric field pattern at the barrier for a gated metadevice in the ON state showing that the gate does not perturb the electric field pattern. **c,** Simulated electric field pattern at the barrier for a gated metadevice in the OFF state, in which the gate electrode depletes the 2DEG underneath it. **d,** Measured output signal of the gated metadevice showing a sub-10 ps switching. The measurement were done using a three-port setup with one GSGSG 67-GHz probe (for the gate and the input RF signals) and one GSG 67-GHz probe (for the output RF signal).

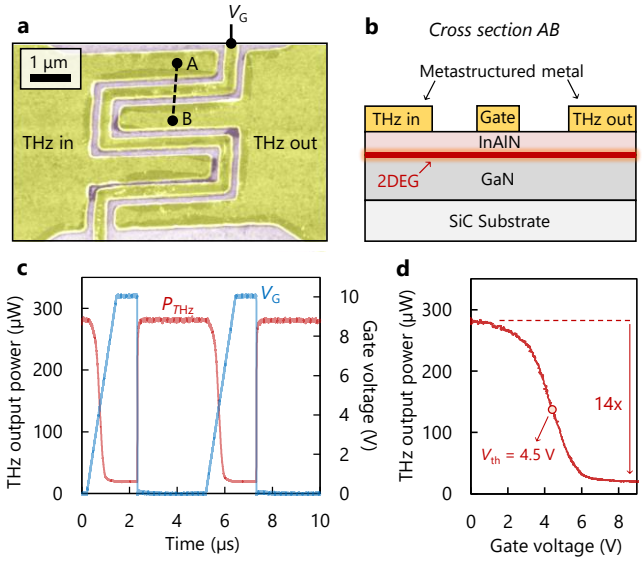

Fig. 2.18 | Thee-terminal metadevices operating at terahertz frequencies. a, Scanning electron microscope (SEM) image of a three-terminal THz metadevice. The device layout includes two metastructured terminals with a gate in between, patterned on a high-electron-mobility platform. **b,** Schematic cross section AB of the device fabricated on an InAlN/GaN epitaxy with a 7.5-nm-thin barrier. **c,** Quasi-static terahertz output power P_{THz} (at 0.23 THz) of the device with a ramp gate signal V_G. **d,** Terahertz output power versus gate voltage, showing a pronounced switching.

the conventional pattern (Fig. 2.17c). In addition, considering the small amount of charge that is needed to charge/accumulate to switch the device, such three-terminal metadevices can exhibit extremely fast switching (Fig. 2.17d).

Three-terminal THz metadevices were fabricated on a high-electron-mobility platform based on InAlN/GaN epitaxy grown on a SiC substrate (Fig. 2.18a and Fig. 2.18b). The fabrication was started by an electron-beam lithography step (PMMA double layer), followed by metal deposition (80 nm Ni / 20 nm Au) to form the metastructured terminals and the gate electrode in a lift-off process. The second step was defining the mesa region by photolithography followed by inductively coupled plasma (ICP) etching. To characterize the quasi-static operation of the fabricated switch, we excited the input terminal of the device by a continuous wave at 0.23 THz and terminated the output port by a down-converter-based THz detector which determines the relative THz power. To scale the detected THz power we measured a through layout on a standard calibration chip and scaled the measured power to the nominal power of the THz source (1 mW). The gate terminal was excited by a function generator which synthesized repetitive pulses with a smooth rising edge and monitored the output THz power at the same time (Fig. 2.18c). From this measurement, the output THz power was extracted as a function of gate voltage (Fig. 2.18d).

The fabricated thee-terminal metadevices were used to build a high-speed THz-band digital modulator (Fig. 2.19a). A frequency up-converter (VNAX276) with multiplication factor 18 was used to synthesize a continuous-wave THz, which is injected into the input port of the device. Using f_{RF} = 15.4 GHz we set

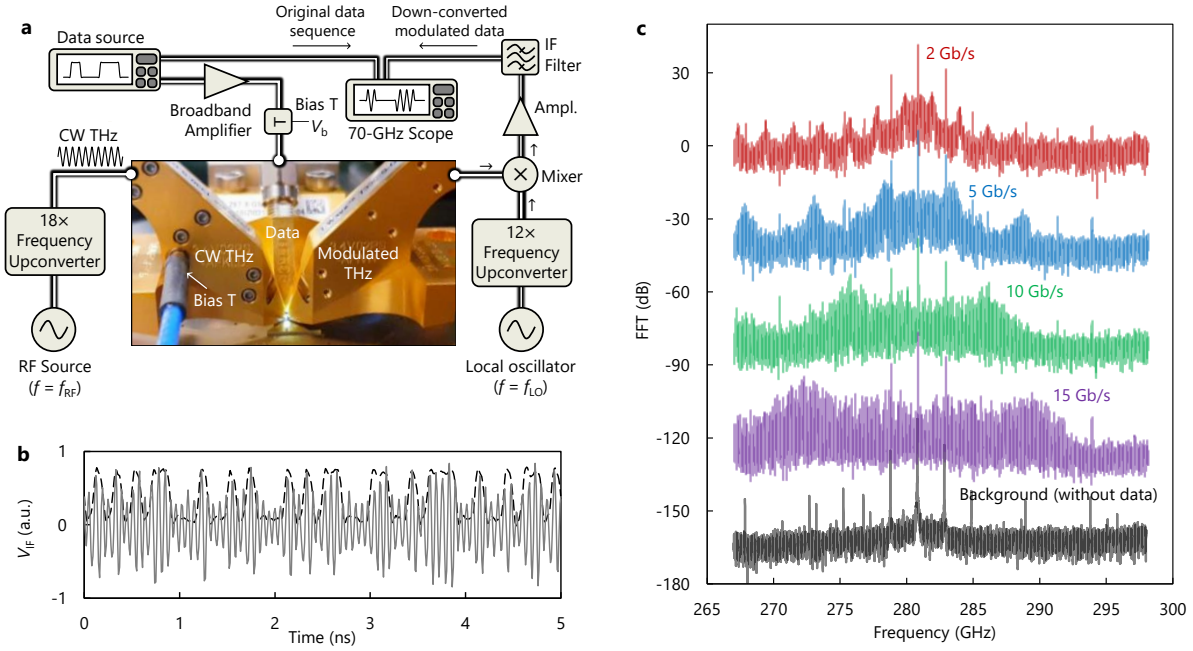

Fig. 2.19 | High-speed three-port THz modulator using three-terminal metadevices. a, Schematic of the experimental setup for the high-speed data modulator based on three-terminal displacement-field nano-switches. The device was accessed through a couple of WR3.4 THz probes (220-330 GHz) for THz input and output, and an RF probe (DC to 67 GHz) to inject the data signal into the gate terminal. **b,** Spectra of the modulated data terminated by the THz receiver, for data rates from 2 Gb/s to 15 Gb/s as well as the background spectrum without data streaming. The spectra were shifted vertically by 40 dB to have a clear plot. **c,** Post-down-conversion of the modulated signal together with the reference data, showing an excellent modulation.

the central frequency of the data transmitter to $f_0 = 18 \times 15.4 = 280.4$ GHz. A Tektronix AWG70000B arbitrary waveform generator was used as the high-speed data streamer. The data source provides two complementary output signals with 0.5-V peak-to-peak amplitudes. One output signal was directly terminated by a Tektronix DPO70000SX 200GS/s 70-GHz oscilloscope to record the reference data. The other output signal was amplified by a broadband 40-GHz amplifier and received a DC offset (V_b = 4.5 V) using a 40-GHz bias-tee to excite the device close to its threshold voltage (Fig. 2.15d). The amplified and DC-leveled data signal was then applied to the gate terminal of the displacement-field nano-switch using a 67-GHz RF probe. The output port of the fabricated modulator was terminated by a coherent receiver that mixed the modulated signal with a 300.8 GHz source which was synthesized using a 12× frequency upconverter driven by a 25.06667 GHz local oscillator. This results in a down-converted IF signal with the central frequency of 20 GHz was measured by the high-frequency oscilloscope.

Fig. 2.20a shows the spectra of the modulated signals corresponding to different data rates up to 15 Gb/s, as well as the background spectrum without data streaming which indicate a dominant peak at 280.4 GHz (the central frequency of the THz source) with two side-peaks at ±1.95 GHz corresponding to a ~10% periodic variation in the THz intensity. The results illustrate very clean spectra, which shows the excellent performance of the realized modulator. Fig. 2.20b presents the received IF signal (solid line) as well as the reference data signal (dashed line), corresponding to 10 Gb/s data rate. The

modulator exhibits an amplitude-phase modulation because the channel impedance varies with respect to the gate voltage. Thanks to the pronounced switching of displacement-field switches with a large ON/OFF ratio, even a simple incoherent envelope detector can reveal the streamed data. The data-rate of the performed experiments was limited by the data streamer and the IF bandwidth of the THz receiver. Time-domain measurements revealed ps-switching capability which would enable much large date rates, above 100 Gb/s.

2.9 Conclusion

This chapter demonstrated that electronic metadevices challenge the fundamental limitations of traditional semiconductor device and extend the operation of electronics to higher speeds, larger voltages, and higher efficiencies. The core idea was that microscopic manipulation of electric fields over an electronic device layout can significantly modify the electronic properties of the device. Switches realized on a high-electron mobility platforms showed ultrahigh cutoff frequency of 18 THz with extremely high breakdown voltage of 30 V. Direct electrical measurements demonstrated giant switching at 1 THz with a contact resistance below the state-of-the-art in tunneling junctions which resolves one of the most fundamental challenges in nano-electroncis.

The high-performance of two-terminal and three-terminal metadevice terahertz switches demonstrated in this chapter potentially offers a large impact on ultrafast electronics and can enable ultrahigh-speed telecommunication systems covering the entire THz band. In a more general view, the electronic metadevice concept can enable variety of functional devices such as gain elements and rectifiers on any material system, ranging from CMOS to 2D materials, with performances far surpassing the state-of-the-art in classic electronics.

3 Nanoplasma picosecond switches: THz electronics on a single metal layer

The broad applications of ultra-wide-band (UWB) signals and THz waves in quantum measurements [171], [172], imaging and sensing techniques [173], [174], advanced biological treatments [175], and very-high data-rate communications [167] have drawn extensive attention to the ultrafast electronics. In such applications, high-speed operation of electronic switches is challenging especially when high-amplitude output signals are required [152]. For instance, although field-effect and bipolar junction devices present good controllability and robust performance, their relatively large output capacitance with respect to their ON-state current significantly limits their switching speed [176]. This chapter demonstrate a novel on-chip all-electronic device concept based on nano-scale plasma (nanoplasma) that enables picosecond switching of electric signals with a wide range of power levels. The very high electric field in the small spatial scale of the nanoplasma leads to an ultra-fast electron transfer, resulting in extremely short time responses. Ultrafast switching speed, higher than 10 V ps^{-1} was achieved, which is about two orders of magnitude larger than that of field-effect transistors and more than ten times faster than the fastest electronic switch nowadays. Extremely short rise-times were measured down to 5-ps which was limited by the employed measurement set-up.

By integrating these devices with dipole antennas, high-power THz signals with Pf^2 = 600 mW.THz^2 were emitted, which is significantly larger than state-of-the-art in solid-state electronics. Using advanced terahertz measurements, terahertz sources operating up to 300 GHz are characterized. This chapter also presents functional millimeter-wave systems in which the integration of nanoplasma devices with linear coplanar networks provides a high-performance scheme for digital modulation on a single metal layer. Tuning by the gap size of nanoplasma devices, they enable switching of signals with at a wide variety of power levels from milliwatts to kilowatts. Ease of integration as well as compactness of the nanoplasma switches could open new horizons in several fields, such as imaging, sensing, communications, and biomedical applications.

3.1 The Pf^2-limit in electronic radiofrequency sources

Nanometer-scale transistors based on III–V compound semiconductors, such as GaAs, InAs, and InP, are at the heart of many high-speed and high-frequency electronic systems [23]. Due to their high electron mobilities, these devices exhibit very high small-signal cut-off frequencies, in the terahertz range [43]. However, the high-frequency large-signal performance of transistors is still a challenge, since it is severely limited by the output capacitance C_{out}, electron saturation velocity and critical electric field [55]. The maximum switching speed of a transistor (Fig. 3.1a) with saturation current I_{max} is limited to

$$\frac{\mathrm{d}v}{\mathrm{d}t}\Big|_{max} = \frac{I_{max}}{2C_{out}}. \tag{3.1}$$

which leads to a power (P)-frequency (f) trade-off, called Pf^2-limit (Fig. 3.1b)

$$Pf^2\Big|_{max} = \frac{(\mathrm{d}v/\mathrm{d}t|_{max})^2}{8\pi^2 Z} \tag{3.2}$$

where Z is the load resistance. Equation (3.1) is a self-normalized term, independent from device size and gate length, that results in almost similar values of less than 1 V ps^{-1}, for either power or RF devices (Fig. 3.1c). For example in lateral devices, normalized saturation currents and output capacitances are in range of 1 mA μm^{-1} and 1 fF μm^{-1}, respectively, resulting in switching speeds of 0.5 V ps^{-1}.

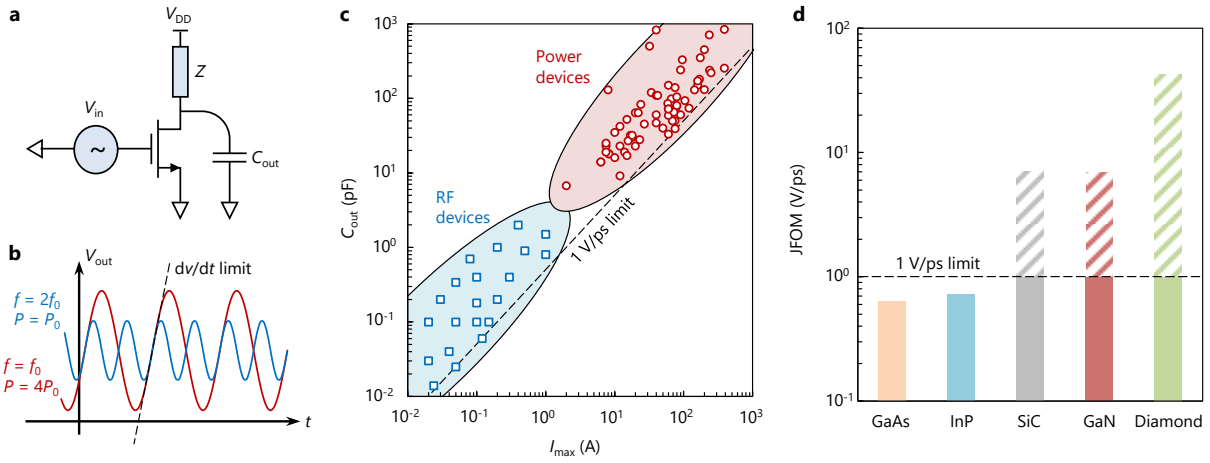

Fig. 3.1 | Switching speed limitation in solid-state electron devices. a, Simple circuit schematic including a transistor with output capacitance C_{out} and load Z. The switching speed of the device is limited to $I_{max}/2C_{out}$. V_{DD} and V_{in} are the drain bias and gate excitation, respectively. **b,** dv/dt limitation causes the Pf^2 limit in solid-state electronics. The red curve has double the amplitude and half the frequency of the blue curve, resulting in the same Pf^2, while both are limited to the switching speed. **c,** Output capacitance C_{out} versus maximum current Imax for commercial and research devices from the literature and datasheets, both for power and radiofrequency applications, showing the 1 V ps^{-1} limit. In practice, switching speeds as high as 0.5 V ps^{-1} have been demonstrated. **d,** JFOM for some of the high-performance semiconductor materials. GaAs and InP are limited to the JFOM, while the C_{out}-limited rise rate of 1 V ps^{-1} restricts the performance of silicon carbide (SiC), gallium nitride (GaN) and diamond.

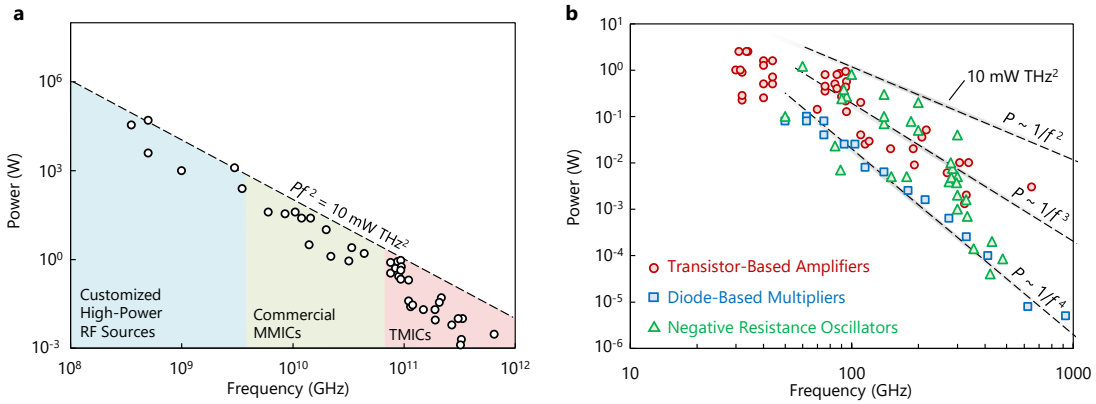

Fig. 3.2 | Benchmark of state-of-the-art power amplifiers. a, Power versus frequency trade-off in power amplifiers reveals a decay of output power as frequency increases, resulting in a constant Pf^2. It should be noted that the limit of 2.5 mW THz^2 in equation (3.2) has been obtained for a single transistor. With power combination techniques in power amplifiers, relatively higher powers (still below about 10 mW THz^2) can be obtained. In the terahertz band, however, such a power combination becomes very challenging, especially if a high bandwidth is required. As an example of state-of-the-art performance in monolithic microwave integrated circuits (MMICs) and terahertz monolithically integrated circuits (TMICs), Radisic *et al.* [178] achieved 1.7 mW at 650 GHz in a single power amplifier corresponding to Pf^2 = 0.7 mW THz^2. Another work presented by Leong *et al.* [179] reported 0.93 mW at 0.85 THz showing Pf^2 = 0.67 mW THz^2. RF, radiofrequency. **b,** Power versus frequency trade-off in different solid-state-based millimeter-wave/terahertz sources showing the generality of the decrease in power at high frequencies. For the references for the data points, please refer to Methods.

Johnson's figure-of-merit (JFOM) [55] takes into account the breakdown voltage and small-signal cut-off frequency of devices, although these parameters are obtained from two different measurements at two separate operating points [177]. As shown in Figure 3.1d, JFOM indicates switching speeds of even less than 1 V ps^{-1} for GaAs and InP, as the semiconductors with the highest electron-motilities and main candidates for ultra-fast electronics (Figure 3.1d). As described in Eq. (3.2), the maximum switching speed of 1 V ps^{-1} corresponds to an output power of 2.5 mW at 1 THz for Z = 50 Ω. Such a limitation can be seen, not only in the performance of power amplifiers, but also in other solid-state-based approaches including frequency multipliers and negative resistance oscillators (Figure 3.2). In practice, several phenomena happening at high-frequency and small-scales, such as RF g_m collapse [56], short-channel effects [57], and surface traps [58] result in considerably lower-than-expected powers at the low-THz band (0.1-1 THz).

3.2 Plasma on a chip: a departure from solid-state electronics

Plasma devices, such as gas discharge tubes, have nearly-ideal ON state providing extremely-high current-densities and do not exhibit the C_{out}-limited switching speed. The dynamic performance of these devices, however, is severely limited by their relatively low electric-field and the considerable electron-scattering between two terminals, which result in nanosecond-range switching times [180]. Here we use formation of nanoplasma (Fig. 3.3a) in atmospheric air to realize an ultra-fast switch that overcomes the switching-speed limitation of solid-state electron devices as well the large-scale plasma

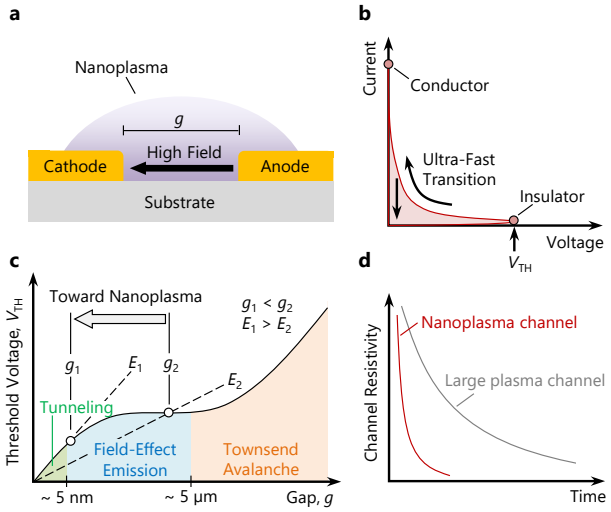

Fig. 3.3 | The concept of a nanoplasma switch. a, Schematic of the structure of a nanoplasma switch with gap length g. The switch is normally OFF and becomes ON at the threshold voltage $V = V_{TH}$ by electron transport in the high-electric field region. **b,** Current–voltage characteristics of a nanoplasma switch. The switch has two stable phases: insulating and conducting. The transition from the insulating phase to the conducting phase is ultrafast, while the conducting to-insulating transition is controlled by the external circuit. **c,** Threshold voltage V_{TH} versus gap distance, corresponding to the modified Paschen law, showing a much larger electric field (E) for devices with nanoscale gaps. Townsend avalanche is the dominant plasma formation mechanism for g > 5 µm, while field-effect emission and tunnelling are dominant for 5 nm < g < 5 µm, and g < 5 nm, respectively [182]. **d,** The higher electric field in a shorter gap distance results in a much faster electron transport for nanoplasma devices.

switches. As shown in Fig. 3.3b, the switch is normally OFF, until a voltage higher than the threshold V_{TH} is applied. The nano-gap allows an extremely rapid electron transport in the very-high-field region, which results in an ultra-fast switching from an isolated to conducting state, with extremely high ON/OFF ratio. Fig. 3.3c presents the modified Paschen curve [181] showing the threshold voltage versus gap distance. For small-scale devices, where the origin of plasma formation is either by electric-field emission (5 nm < g < 5 µm) or tunneling (g < 5 nm), much higher electric fields than in large-scale plasma devices can be achieved [182]. This results in extremely fast time responses, much faster than that in large-scale plasma devices (with normally nanosecond-range switching times) [180] (Fig. 3.3d).

3.3 Picosecond switching in nanoplasma devices

The structure of nanoplasma switches is very simple, consisting of metal pads separated by a nanometer-scale gap (Figs. 3.4a-b), which is compatible with planar fabrication processes and even possible integration to flexible substrates (Figs. 3.4c). A very high bandwidth experimental setup, shown in Figs. 3.4d, was used to characterize the switching dynamics of fabricated nanoplasma devices. A nanosecond pulse generator supplies the input pulse, and once the input signal reaches the V_{TH}, the nanoplasma switch turns ON, passing the signal to the 50-Ω termination of oscilloscope. Figs. 3.4e

shows the measured switching waveforms. Comparing the very sharp switching transients of nanoplasma devices with state-of-the-art switching speed in solid-state electronics, reveals the outstanding performance of these devices for ultra-fast electronics, especially for applications requiring large signals. The measured rise-time (Figs. 3.4f) for small scale devices, with gap lengths down to 20 nm, reached the measurement bandwidth limit of 6-ps, which after de-embedding the effect of cables and attenuators, resulted in a rise-time of 5 ps (Figs. 3.5).

Figs. 3.4g shows measured rise-time versus amplitude for the fabricated devices in comparison to reported data for the fastest electronic switches including field-effect transistors (FETs) and step-recovery diodes (SRDs). While the switching speed of solid-state electronics is below 1 V ps^{-1} (in agreement with the theoretical prediction in Figs. 3.1), nanoplasma devices reached much higher values while they are not limited any more by the parasitic capacitance (Figs. 3.6). In such a comparison we should note that FETs, as three-terminal devices, are capable of turning ON and OFF with the same speed, while in other high-performance electron devices, including step-recovery-diode (SRD) [183] or silicon-avalanche-diode (SAS) [184], as two-terminal devices, a single fast switching-edge is provided. Nanoplasma is also a two-terminal device with an ultra-fast turn-ON transient, however, it provides a significantly faster switching time at higher voltages which enables generating much faster UWB signals at higher power levels.

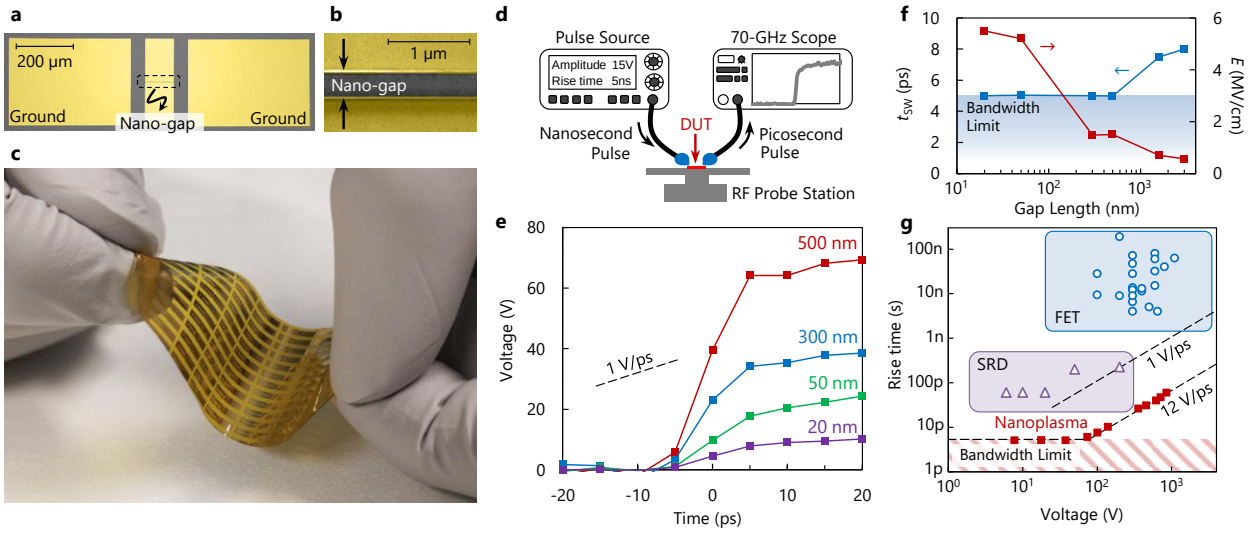

Fig. 3.4 | Implementation of nanoplasma switches. a, Micrograph of a nanoplasma switch integrated with RF pads, and **b,** a scanning electron microscope image (SEM) of the nano-gap. **c,** Fabricated devices on Kapton showing their possible integration to flexible substrates. **d,** Schematic of the experimental set-up for switching characterization of the nanoplasma devices. Time-domain measurements were carried-out with a DPO70000SX 70-GHz Tektronix oscilloscope, which together with the 67 GHz cables and RF probes, limited the rise-time measurements to 6 ps. **e,** Measured switching waveforms showing 6-ps rise time of high voltage signals. **f,** Measured (blue) together with the electric field in the nano-gap (red). After de-embeding the effect of cable and RF probe, a 5-ps rise-time was obtained (Fig. 3.5). Switching-time measurements in time domain are limited by the oscilloscope bandwidth. **g**, Benchmark of the rise-time/switching-voltage of nanoplasma versus other state-of-the-art electronic devices.

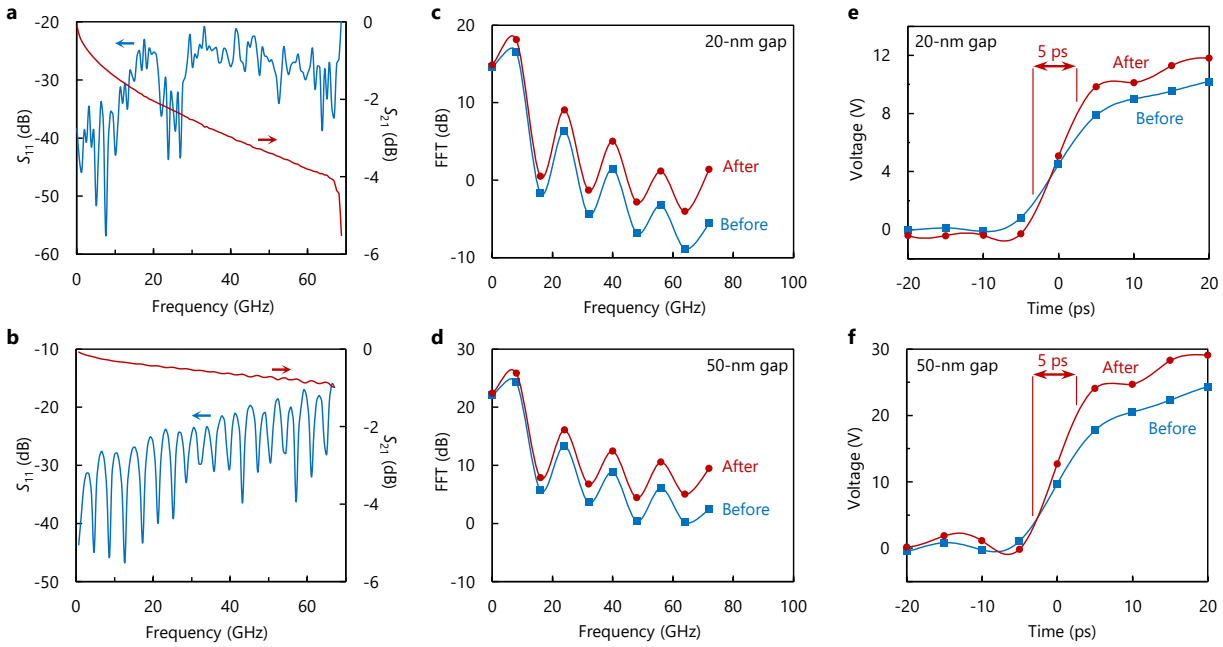

Fig. 3.5 | De-embedding cabling and probing effects from time-domain measurements. Measured reflection and transmission scattering parameters for the used **a,** high-frequency coaxial cable and **b,** ground-signal-ground (GSG) RF probe, reported by the manufacturer. **c, d,** FFT of the measured signal (blue) and the obtained FFT after de-embedding (red) for 20-nm and 50-nm-wide gap devices. **e, f,** The measured (blue) and de-embedded (red) waveforms for 20-nm and 50-nm-wide gap devices showing 5-ps rise-time corresponding to the 70-GHz bandwidth of the oscilloscope.

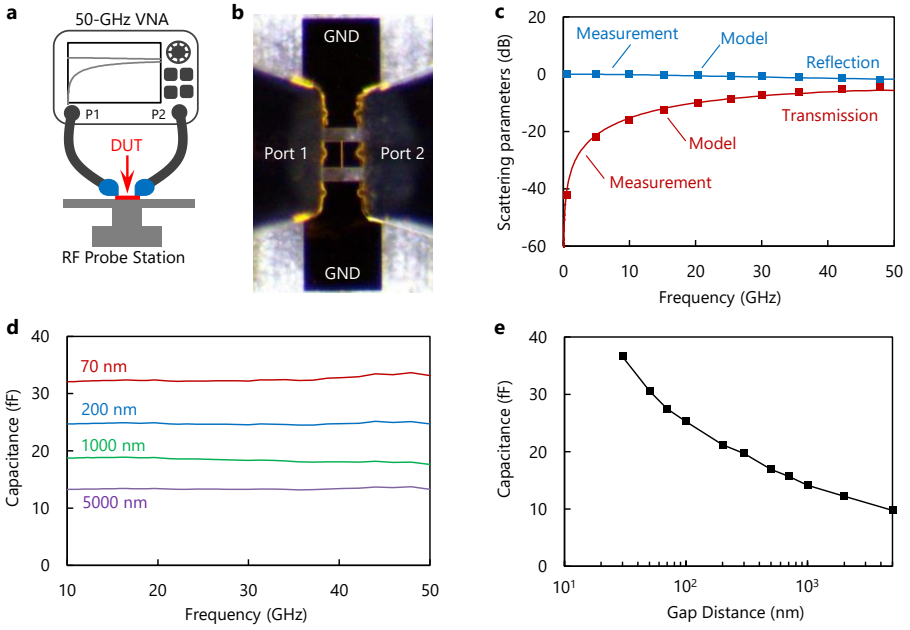

Fig. 3.6 | Parasitic capacitance characterization of nanoplasma devices. a, Schematic of the experimental set-up for capacitance measurement. **b**, Optical image of a device under test. **c**, Measured (solid lines) and modeled (discrete points) reflection (S_{11} = S_{22}) and transmission (S_{21} = S_{12}) coefficients through a 100-nm-gap nanoplasma device. The device was simply modeled as a 25-fF capacitance. **d**, Extracted capacitance versus frequency for devices with different gap sizes. **e**, Extracted capacitance versus gap distance. The small parasitic capacitances lead to very high d*v*/d*t*–limit for nanoplasma devices *e.g.* 42 V ps^{-1} for 500-nm-gap devices.

A good consistency in the switching transient as well as a durable performance under harsh switching conditions are other beneficial aspects of nanoplasma devices for high-power ultrafast electronics (Fig. 3.7). The obtained results shown in Figs. 3.7a-b indicates that the proposed devices with sputtered tungsten pads are capable of withstanding repetitive short circuits, without any specific optimization. The devices with a thicker pads (thus lower current density) provide a more stable performance even at very harsh condition, thus one could expect a very long lifetime in normal operations. In addition, electromigration has a solid background in silicon electronics with several demonstrated solutions, including the use of specific alloys, or single crystalline metals that result in nearly infinite lifetime even for sub-micrometer interconnections [181]. Thus even though the 100-nm-thick devices showed a larger degradation in such extreme condition, they could also be useful in practical applications.

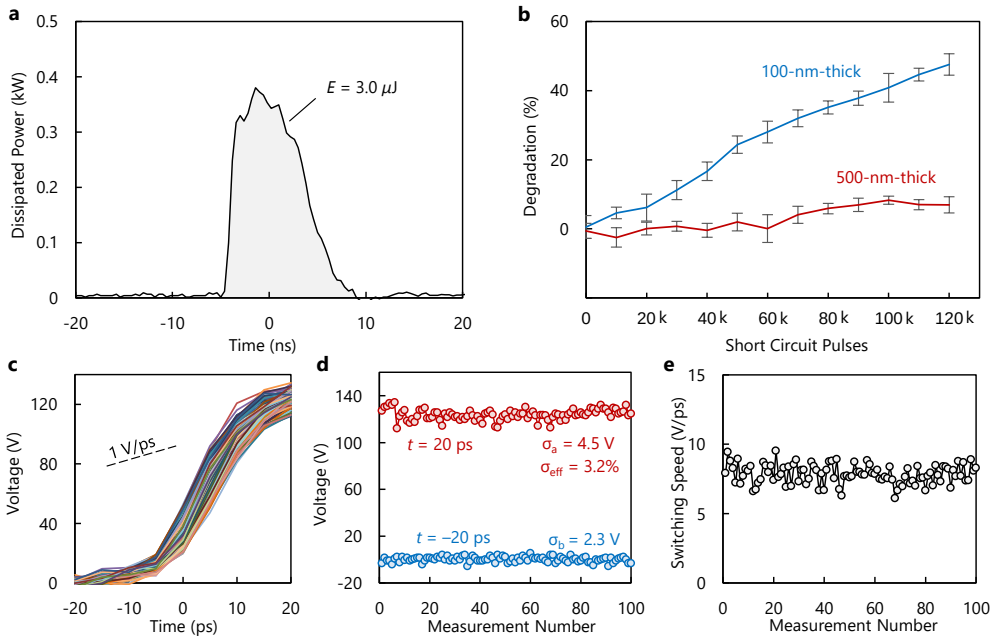

Fig. 3.7 | Lifetime evaluation under harsh switching condition and statistics of the switching performance. a. Dissipated power inside 700-nm-gap nanoplasma switch with tungsten pads under short circuit test resulting in the highest possible current density for lifetime measurements (high current density is the main driver for electromigration). Measurements showed energy and peak power dissipation of 3 μJ and 0.4 kW at each short circuit pulse. Such a high-power and energy dissipation are orders of magnitude higher than in practical applications. **b,** Degradation with the definition of (V_{TH}[n] – V_{TH}[0]) / V_{TH}[0], where V_{TH}[n] is the threshold voltage at nth short circuit. The error bars show ±2σ, where σ is the standard deviation from 10 measurements. **c,** 100 measured switching transients for 1000-nm-gap devices with 500-nm-thick tungsten. **d,** Measured switching voltage at t = 20 ps (with standard deviation σ_a) and measured noise level at t = −20 ps (with standard deviation σ_b) corresponding to the waveforms shown in parts a, b, and c, respectively. The normalized effective standard deviation $\sigma_{\text{eff}} = \left(\sigma_a^2 - \sigma_b^2\right)^{1/2}/V_{\text{SW}}$, where V_{SW} ~ 120-V is the switching voltage, was 3.2%. **e,** Measured maximum dv/dt corresponding to the measured waveforms shown in part c, respectively. Characterization of dv/dt is more subjected to measurement errors because of the limited sampling time (5-ps/sample). It should be noted that the limited sampling time, generally leads to an underestimation of dv/dt, as the sampling does not necessarily pick the maximum of dv/dt. All the results presented are without de-embedding.

3.4 Ultra-wide-band impulse sources using nanoplasma switch

Generation of impulse and square-shape signals is enabled by devices providing a single fast switching transient based on techniques such as discharging the energy stored in a capacitor (Fig. 3.8a), inductor, transmission line, etc., or by utilizing delay-lines [186], [187]. The switching time and voltage/current capability of the switch limits the minimum rise (fall)-time and pulse-width, as well as the maximum peak power of generated signals. Fig. 3.8b shows a simple monolithically integrated circuit fabricated to demonstrate the impulse generation using nanoplasma devices. The delay structure between the excitation port and the nano-gap does not let the input transmission line (including RF probe and cable) to discharge through the gap immediately after switching. The experimental set-up shown in Fig. 3.4d was used to characterize the monolithically integrated circuit. Fig. 3.8c shows an ideal impulse with arbitrary amplitude after passing an ideal 70-GHz low-pass filter (corresponding to the bandwidth of the used oscilloscope), which in fact, is a sinc function. The obtained waveforms for devices with two different gap sizes are shown in Fig. 3.8d. Nanoplasma devices presented a much higher amplitude and shorter pulses than any other electron device in the literature (Fig. 3.8e) which shows their outstanding potential for UWB systems.

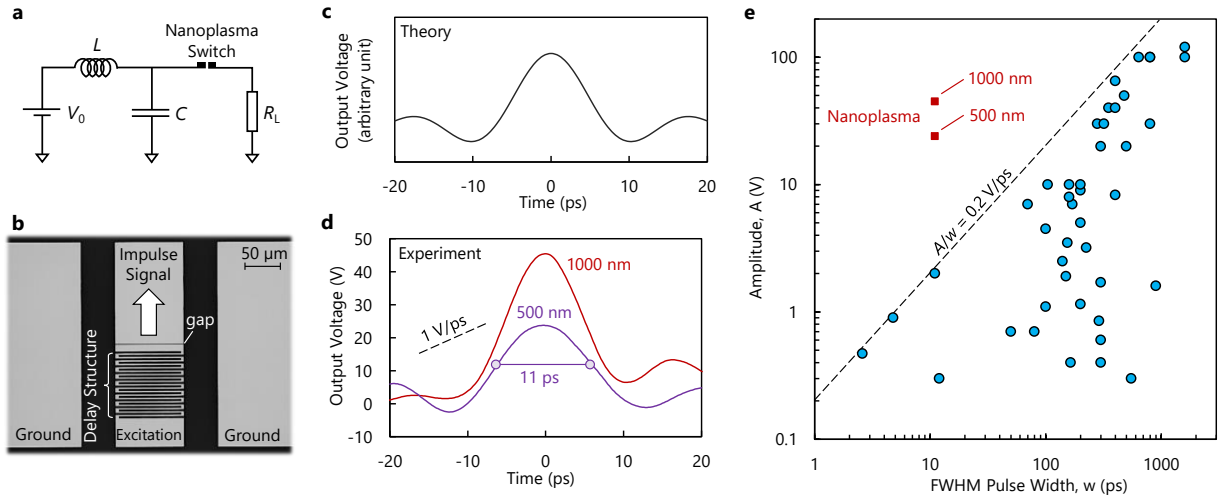

Fig. 3.8 | Impulse generation using nanoplasma switch. a, Simple circuit topology enables nanoplasma to generate ultra-fast impulse signals. The capacitor C is charged through the voltage source V_0 in series with inductor L, up to the V_{TH} of the nanoplasma device. At this point, the energy stored in C is discharged into the load R_L. The time-constant $\sqrt{LC}$ is higher than the output time-constant $R_L C$ so that at a switching event, the capacitor C is discharged alone to the load, without the previous stage being involved (which includes RF probes and cables), resulting in the generation of an impulse. **b,** Optical image of a monolithically integrated circuit fabricated to provide a charging delay time between the gap and the excitation. **c,** An ideal impulse signal with arbitrary amplitude after filtering with an ideal 70-GHz low-pass filter. **d,** Measurement results after de-embedding for devices shown in part b, with two gap sizes 500-nm and 1000-nm, showing a very high amplitude and waveforms close to the ideal impulse (sinc function). **e,** Benchmark of amplitude versus full-width-at-half-maximum (FWHM) of the generated pulses against with reported data in the literature and datasheets. For the references of the data points, please refer the supplementary information.

High repetition rate operation is an import feature of impulse sources. Fig. 3.9 demonstrates nanoplasma devices with high switching frequency. The experimental set-up for high repetition-rate pulse sharpening characterization is shown in Fig. 3.9a. A 10-MHz GaN-based pulse source drives the DUT which is connected to a 1-GHz scope through a stack of attenuators. Fig. 3.9b shows how the output signal of the nanoplasma device follows the input signal. The device turns ON just after the input signal reaches V_{TH}, resulting in a pulse sharpening, which converts the input nanosecond rise-time to a picosecond transition at the output. The switch remains in the ON state until the driver circuit supplies the signal. When the input signal becomes zero, the ultra-fast recombination of ionized molecules in the nanoplasma recovers the OFF state of the switch. The switching frequency of this experiment is limited by the solid-state pulse generator, however we demonstrated a 20-MHz switching frequency at 390-V, together with ultra-fast recombination time of <20-ns which enables to further increase the switching frequency up to 50-MHz (Fig. 3.9). The ultra-high switching speed and the capability of operating at very high repetition rates, unveil the significant potential of nanoplasma switches for ultra-fast electronic systems, especially high-power terahertz sources operating at very high repetition rates.

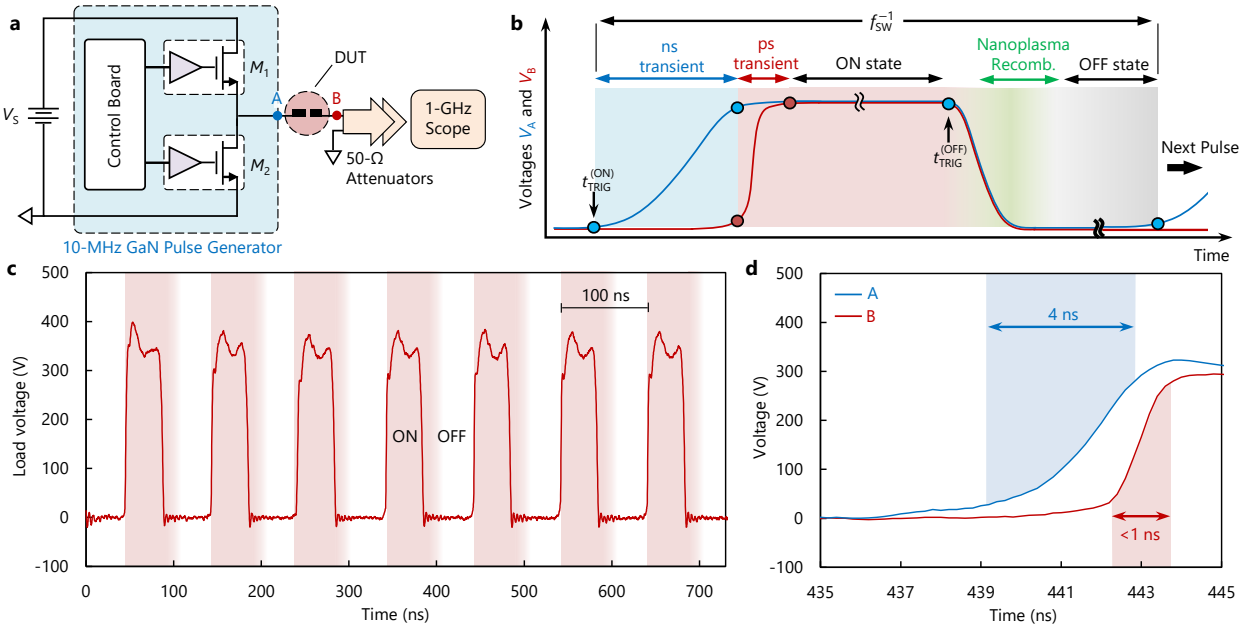

Fig. 3.9 | High-repetition-rate pulse sharpening with nanoplasma switches. a, Schematic of the experimental setup for high-frequency switching using nanoplasma devices. A GaN-based half-bridge circuit drives a nanoplasma device terminated by 50-Ω port of a 1 GHz oscilloscope through a chain of attenuators. **b**, Illustration of waveforms before (V_A) and after the DUT (V_B). At t = $t_{TRIG}^{(ON)}$ the GaN pulser generates a pulse (nanosecond rise-time). The DUT is OFF until the voltage reaches V_{TH}, then it turns ON in a very short time (picosecond rise-time). The DUT maintains its ON state until $t_{TRIG}^{(OFF)}$ when the GaN pulser starts to switches OFF the output voltage. After a recombination time, the DUT retains its OFF state. **c**, Voltage waveform (V_B) over the 50-Ω load demonstrating 10-MHz high-power switching with DUT. **d**, Voltage waveforms V_A and V_B, showing the pulse sharpened V_B by the nanoplasma (limited to the measurement bandwidth).

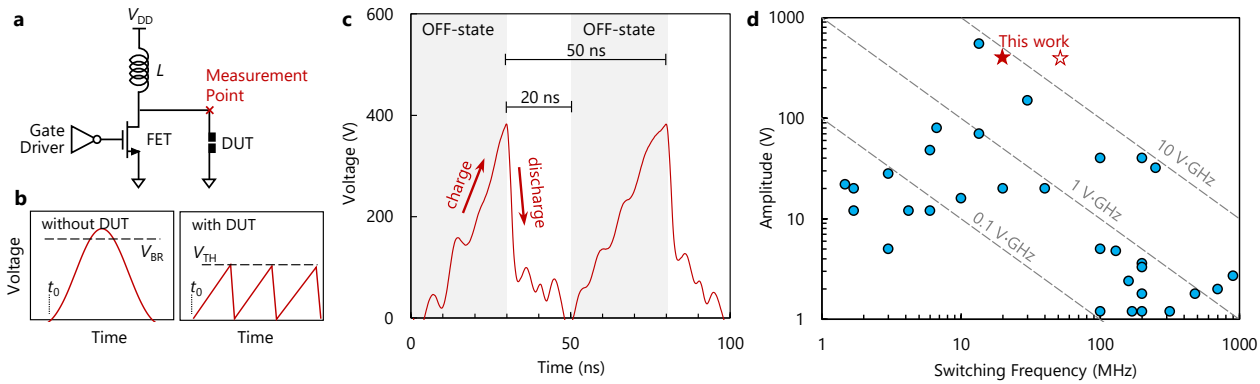

Fig. 3.10 | Sub-20 ns recombination time of nanoplasma. a, Proposed circuit to demonstrate very high repetition-rate switching. The FET is ON for $t < t_0$, charging the inductor L. At $t = t_0$, the transistors turns OFF initiating a resonance between its output capacitance and inductor L. **b,** Without connecting the DUT, a high-amplitude spike is generated. By connecting the DUT, when the voltage reaches the V_{TH} of the switch, the DUT discharges the output capacitance. At this time, the inductor still has current, so it charges again the output capacitance. This charging/discharging process can continue up to several times, depending on the inductor current. **c,** Measured voltage waveform over DUT (g = 6 µm) a small plasma recombination time < 20 ns to reconfigure the transistor back to its operation. This shows a high-switching frequency in the devices. The measured <20-ns recombination-time enables to achieve switching frequency up to 50-MHz (depends on the duty cycle) at 390-V (hollow red marker). In the current circuit however, limited the switching frequency to 20-MHz (solid red marker). **d,** Benchmarking the obtained switching-frequency with state-of-the-art in solid-state electronics. These results shows the potential of the proposed devices, not only in ultrafast dv/dt transients, but also in switching frequency. For the references of the data points, please refer to the supplementary information.

3.5 High-power THz sources based on nanoplasma switches

The ultrafast performance of the proposed nanoplasma devices also enables the generation of mm-wave and THz signals at high peak-power levels. As shown in Fig. 3.11a, a resonator illustrated by an *LC* tank is smoothly charged (Fig. 3.11b). When the output voltage reaches the threshold voltage of the nanoplasma switch, it turns ON, discharging the energy stored in the resonator, as a high-frequency wave-packet, into the load (Fig. 3.11c). The performance of such a mm-wave/THz pulse source is determined by the employed switch as well as the resonator design. Picosecond switching of the nanoplasma enables exciting very high resonance frequencies in the THz range, and the high-amplitude operation of the switch results in large energy stored in the resonator, leading to high output powers. The resonator design determines the resonance frequency as well as the mm-wave/THz pulse energy. Fig. 3.11d shows the schematic of the high band-width experimental set-up used to characterize the wave emission from nanoplasma switches integrated with bowtie antennas, serving as both the resonator and radiating element. An antenna with the same geometry connected to a high frequency oscilloscope was used to receive the radiated wave-packet. Four received waveforms with different antenna sizes resulting in central frequencies of 27, 50, 80, and 109 GHz, are shown in Figs. 3.11e-h, respectively (The maximum chosen frequency was limited by the bandwidth of our 113 GHz oscilloscope). The time scale bars are 50-ps and for the 27-GHz waveform, the second harmonic of the antenna was filtered out. Fig. 3.11i shows the FFT of received signals. Based on frequency-domain characterization of the antennas, and after de-embedding the effect of cables and RF probe an average

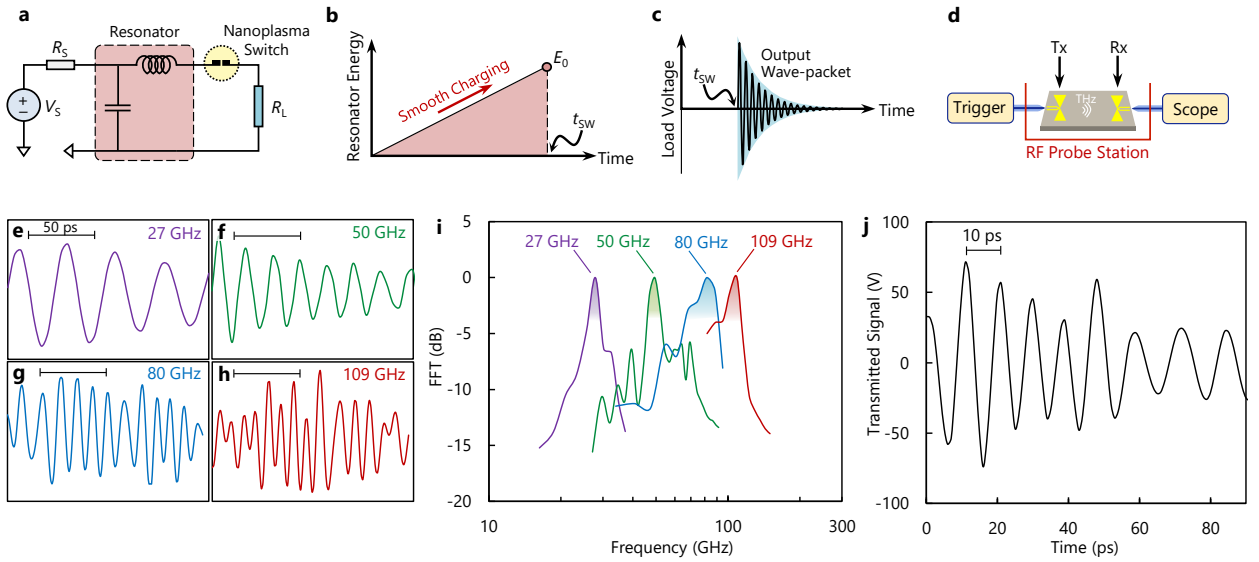

Fig. 3.11 | Nanoplasma-based mm-wave/THz sources. a, Implemented circuit diagram of mm-wave/THz source realized by nanoplasma switch. **b,** The voltage source V_S smoothly charges a fast resonator, which is excited at $V = V_{TH}$ when the nanoplasma switch turns ON with picosecond transition time. The resonance frequency of the resonator determines the central frequency (f_0) of the generated pulse and the switching transition of the nanoplasma switch should be small enough ($\lesssim 1/f_0$) to excite the resonator. The energy is transferred to the load in a short time after switching time t_{SW}. **c**, Illustration of the generated mm-wave/THz pulse at $t = t_{SW}$. **d**, Schematic of the experimental set-up. The THz pulse is emitted by a transmitter antenna connected to the nanoplasma switch and the received wave is measured by an ultra-high-frequency oscilloscope. Measured waveforms with bowtie antennas with different sizes (the transmitter and receiver antennas have the same size) resulting in central frequencies of **e,** 27 GHz, **f,** 50 GHz, **g,** 80 GHz, and **h,** 109 GHz. **i,** Frequency spectrum of the received signals for four different antenna sizes showing the flexibility of the method in generating high-frequency signals at different frequencies, (up to the measurement limit of our set-up). **j,** Calculated radiated signal from the transmitter antenna, based on the measured S_{21} after de-embedding the effect of cables and RF probe, showing a high average peak power of 50-W at 109-GHz.

peak power of 50-W at 109-GHz corresponding to Pf^2 of 600 mW.THz^2 was obtained (Fig. 3.11j). This is more than 200 times larger than the Pf^2 = 2.5 mW.THz^2 limited by 1 V ps^{-1} switching speed in solid-state electronics. In addition, the very high frequency operation of the proposed devices can have also a significant impact in flexible electronics. While 2D semiconductors are showing promising RF performances, their relatively small mobility severely limits the bandwidth of existing flexible electronic systems [188]. Nanoplasma devices increase the bandwidth of flexible integrated electronic systems, from below 10 GHz in 2D semiconductors to the THz band [189].

To evaluate the performance of nanoplasma-based THz sources at frequencies well above 100 GHz, an advanced measurement setup based on high-bandwidth down-converting mixers was used. This is because the best oscilloscopes or spectrum analyzers do not provide bandwidth above ~100 GHz and one needs to down-convert the THz signal into intermediate frequencies using high-bandwidth mixers. Fig. 3.12a shows a schematic of the experimental setup. An ordinary pulse source generates a square signal which is amplified using a 5-MHz 32-dB amplifier. The amplified signal excites a bowtie antenna integrated with a nanoplasma switch at its port (Figs. 3.12b-c). Triggering the nanoplasma device leads

to the generation of a THz signal which is received by a receiver antenna (Rx) with the same shape. The frequency content of the THz signal at the port of the Rx antenna is determined by the coupling between two antennas as they are in the near field. The Rx antenna is terminated by a THz probe which offers a coplanar-to-rectangular waveguide (WR3.4 for 220 GHz – 330 GHz) transition. The waveguide port of the THz probe was connected to a frequency down-converter from VDi which mixes the THz signal to a continuous wave 300 GHz signal (generated by frequency multiplication of a 25 GHz LO). The mixer-based down-converter provide a bandwidth of at least 40 GHz. The output signal after down-conversion was terminated by a 70-GHz oscilloscope.

Fig. 3.12d shows the received signal (generated by the nanoplasma-based THz source with 400-μm-long antennas) after down-conversion. To understand the level of the THz power the receiver, the system was calibrated by a references continuous wave THz source with the nominal power of 1 mW. In this case, the a standard on-chip through feature of a calibration chip was used to directly terminated

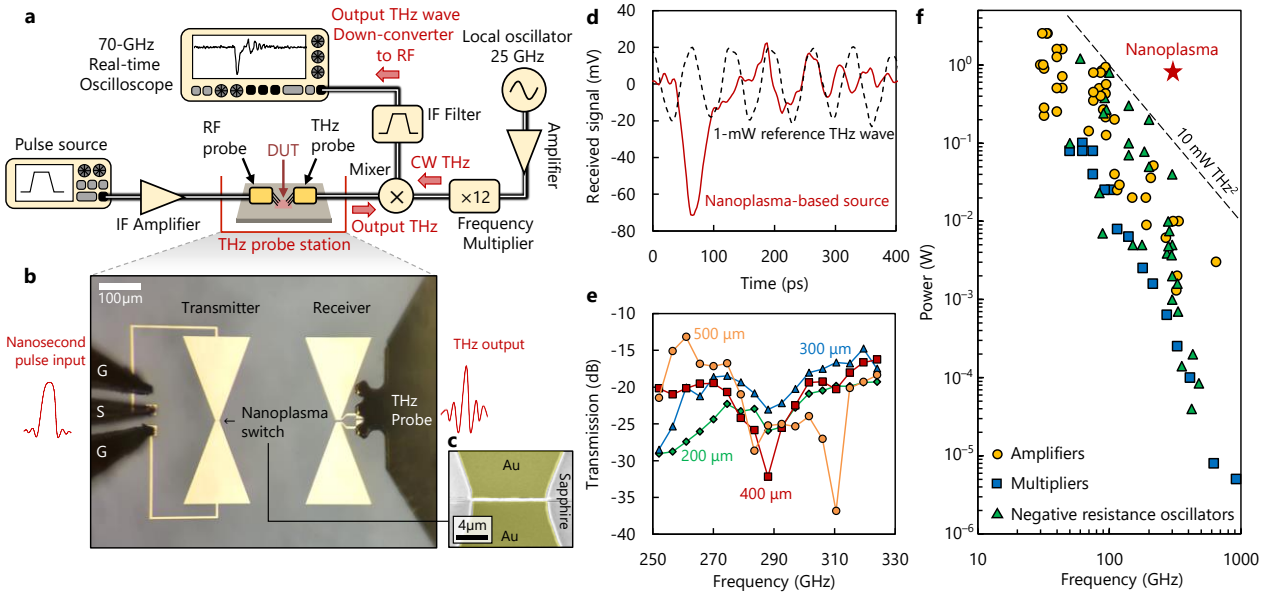

Fig. 3.12 | High-power nanoplasma-based THz source operating at 300 GHz. a, Schematic of the experimental setup for real-time evaluation of nanoplasma-based THz sources. The emitted THz signals are down-converted to intermediate frequencies and measured by a 70-GHz oscilloscope. **b,** Image of the transmitter (Tx) antenna (integrated with a nanoplasma switch) and receiver (Rx) antenna. The transmitter antenna was excited by an ordinary nanosecond pulse using a 67-GHz GSG probe and the receiving antenna was terminated by a THz probe with WR3.4 waveguide port (standard for 220 – 330 GHz). **c,** False-colored SME image of the nanoplasma switch at the middle of the bowtie antenna (transmitter). The device were fabricated by Au (100 nm)/Cr (5 nm) on a sapphire substrate. Transmitter/receiver antennas with different lengths 200 μm, 300 μm, 400 μm, and 500 μm were fabricated. **d,** Received signals after down-conversion of the THz pulse generated by the nanoplasma-based source with a 400 μm-long antenna (red). To understand the level of power, the THz receiver probe was directly terminated by a 1-mW (nominal) continuous wave source using a standard through feature (dashed line). The results indicate that using the nanoplasma-based source, the Rx antenna receives over 10 mW. **e,** Scattering parameters measurement between two couples antennas of different lengths. The results were used to obtain the radiating THz power. **f,** Benchmark of the proposed nanoplasma-based source with respect to the state-of-the-art THz sources.

two THz probes, one connected to the reference THz source and the other connected to the THz down-converter. The results shown in Fig. 3.13d (dashed line) indicate that the received signal generated by the nanoplasma-based has a peak power over 10 mW. Therefore, the power transmitted by the Tx antenna should be well over 10 mW. To estimate the transmitted power, the transmission (S_{21}) between the antennas was measured. In this case, the gap ports of both antennas were probed by two THz probes connected to VNA extended modules (VNAX3.4 of VDi) (Fig. 3.12e). Considering a maximum transmission of –20 dB in case of the 400 µm-long antennas, the radiated power should be in range of ~1 W. These results show that the nanoplasma-based sources significantly outperform the state-of-the-art THz sources (Fig. 2.12f). It should be noted that the proposed nanoplasma sources are able to generate THz pulses with can bypass the need for THz modulators after generating a continuous wave THz.

3.6 Nanoplasma-based data modulators on a single metal layer

Synthesizing and amplifying millimeter-wave (mm-wave) and terahertz signals are challenging in traditional semiconductor electronics [190], [191]. The previous sections discussed about the terahertz gap in general, where it is fundamentally difficult to generate decent powers at THz frequencies. This section addresses a more challenging issue: how to synthesizing/amplify high-frequency signals with a certain frequency contents, so that they can carry information?

For narrow-band systems, including different types of modulators, the classic approach is to use a microwave local oscillator followed by a power amplifier which drives a chain of frequency multipliers [192]. This results in a rather low-power signal (due to the Pf^2 limit) at millimeter or sub-millimeter bands that is delivered to a modulating switch whose cut-off frequency limits the maximum operation frequency of the system. Such technical challenges are more severe for RF systems that require ultra-wide-band (UWB) signals [193], [194]. Digital approaches to synthesize rich-frequency waveforms are bulky and quite limited in terms of bandwidth. Power amplification of such wide-band signals is also very difficult. Alternative analog approaches have been explored to directly generate UWB signals, like impulses [195]. Ultrafast reverse recovery of p-i-n diodes [196] and nonlinear wave-lattice interactions [197] that produces self-compressed electrical pulses [198] are examples of such alternative techniques. Besides the relatively low output power of these approaches, the requirement for specific semiconductor epitaxies can hinder their application in conventional integrated circuits.

This section proposes to use the picosecond threshold firing in nanoplasma devices, integrated with a coplanar patterned metal layer (a linear network with the transfer function H), to generate and modulate mm-wave and terahertz signals at large power levels. As shown in Fig. 3.13a, an ordinary source (which can have a low bandwidth in the range of MHz) injects a pulse to a nanoplasma switch. The switch transfers the input pulse into a signal with a picosecond rise-time which has an ultra-wide bandwidth up to the THz band. This UWB signal passes through a linear network (transfer function H) which shapes it into the desired waveform at the output load. In the case of H being a band-pass filter, the output pulse is a wave-packet, and the entire structure acts an amplitude-shift keying self-modulator.

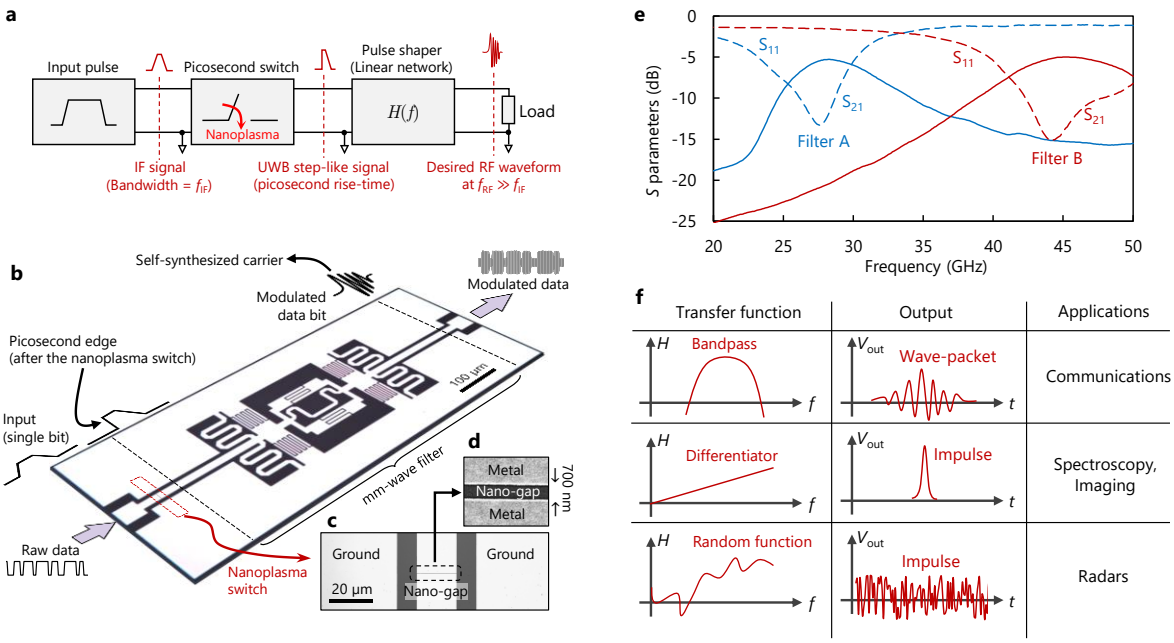

Fig. 3.13 | Nanoplasma-enabled analog synthesizers. a, Schematic of the proposed analog synthesizer based on a picosecond threshold-firing switch (nanoplasma device). **b,** Nanoplasma-based single-metal-layer modulator. The figure illustrates the perspective optical microscope picture of a fabricated modulator. The structure is driven by a sequence of data bits. Data bits corresponding to "1", trigger the nanoplasma device which generates a step-like UWB signal. The UWB signal passes through a coplanar filter that transfers the step-like shape to a wave-packet with the desired frequency content. **c,** Scanning electron microscope (SEM) image of a nanoplasma device integrated on a coplanar waveguide. **d,** SEM image of the nano-gap. **e,** On-wafer scattering parameter characterization of two fabricated bandpass filters designed with central frequencies of 28 GHz (filter A) and 45 GHz (filter B) using a 50-GHz vector network analyzer (VNA). Transmission (S_{21} = S_{11}) shown by solid lines and reflection (S_{11} and S_{22}) shown by dashed lines. **f,** Generalization of the concept to analog synthetization of arbitrary mm-wave/THz signals. Illustration of three examples of transfer functions and their corresponding output waveforms.

This concept relies on a single metal layer (Fig. 3.13b), and integrates several functions together, enabling a simple, compact and low-cost digital data modulator in the millimeter and terahertz bands. The proposed all-metal circuits (in the form of two-port networks) consist of two parts: 1. A nanoplasma switch right after the input port of the network (Fig. 3.13c-d), and 2. A linear coplanar network with a designed transfer function $H(f)$ which shapes the signal generated by the nanoplasma switch. Nanoplasma device is capable of switching signals with amplitudes from a few volts to thousands of volts. Therefore, the proposed concept can provide a wide range of power levels from milliwatts to kilowatts. Recombination rates of less than 20 ns (limited by the experimental setup) have been demonstrated for nanoplasma switches, which can enable high data rates over 100 Mb/s. This section demonstrate a realization of Fig. 3.13a, where H is a bandpass filter (Fig. 3.13e), although the concept can be generally used to synthesize arbitrarily signals with applications in communications, imaging, and radars (Fig. 3.13f).

The nanoplasma-based modulators were fabricated on a 2-inch sapphire substrate. The process flow started with a metal deposition step (500 nm-thin Au, along with 3-nm thin Cr adhesion layers). Nano-

gaps were patterned by e-beam lithography (using ZEP positive resist) followed by ion-beam etching. Coplanar filters were then defined by photolithography, followed by an ion-beam etching step. We characterized the all-metal modulators designed with four different bandpass filters, named filters A, B, C, and D with central frequencies at 28 GHz, 45 GHz, 55 GHz, and 65 GHz, respectively, each of them including three series of coplanar resonators. Fig. 3.13b illustrates one modulator circuit containing filter A (central frequency of 28 GHz). The detailed design of all filters is presented in the supplementary document. Fig. 3.13e shows the measured reflection (dashed lines) and transmission (solid lines) of the fabricated filters with central frequencies of 28 GHz (filter A, blue lines) and 45 GHz (filter B, red lines). For the scattering parameter characterizations, our measurements were limited by the bandwidth of the 50-GHz performance network analyzer (PNA) (Keysight N5225A). The measurements were done on-wafer in which the two coplanar ports of the filters were connected to coaxial cables (terminated by two ports of the PNA) through 67-GHz ground-signal-ground (GSG) RF probes.

The time-domain performance of the fabricated modulators was evaluated using a 70-GHz oscilloscope (DPO77002SX) with an ultrahigh sample rate of 200 GS/s (Fig. 3.14a). Electrical pulses generated by a function generator were amplified by an intermediate frequency (IF) amplifier with 5 MHz bandwidth and 34-dB gain to drive a 700-nm-long gap nanoplasma switch. The output port of the modulator was accessed through a 67-GHz GSG probe connected to a 1.85-mm cable terminated to the 70-GHz port of the oscilloscope with an external 67-GHz 40-dB attenuator. The attenuator was used to downscale the modulated wave into the measurement range of the oscilloscope (~350 mV peak-to-peak). Fig. 3.14b illustrates waveforms at the output port of the modulators, which correspond to the measured waveforms by the oscilloscope multiplied by 100 (to compensate for the 40-dB attenuation). The discrete points correspond to the samples taken by the oscilloscope with interval of 5 ps.

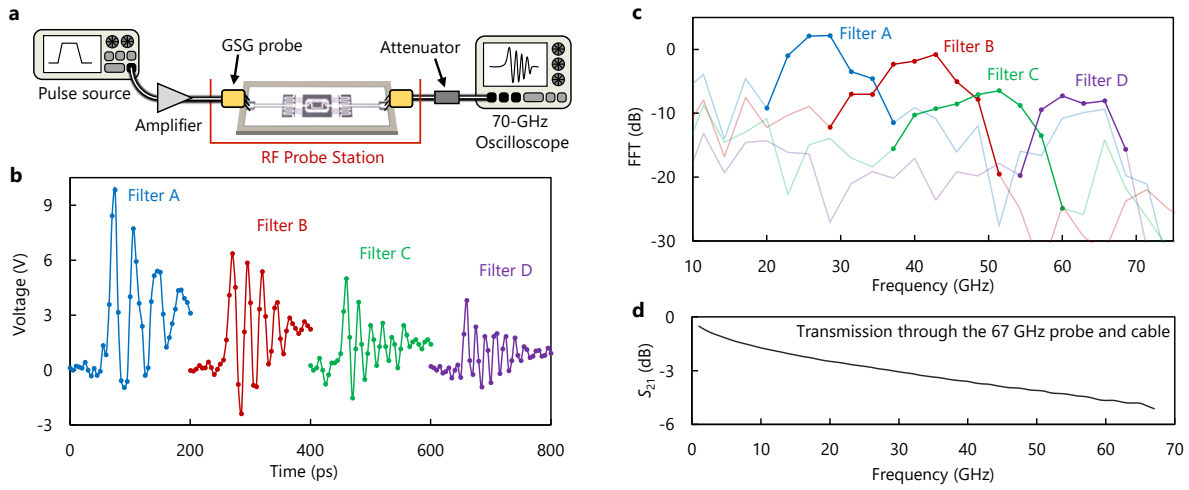

Fig. 3.14 | Nanoplasma-based mm-wave modulators on a single metal layer. a, Schematic of the experimental setup. A function generator with an IF amplifier stage drives the all-metal modulator terminated by a 70-GHz oscilloscope. The input and output ports of the modulator were accessed through 67-GHz ground-signal-ground (GSG) RF probes. **b,** Output voltage of the all-metal modulators with four different filters, designed at 28 GHz, 45 GHz, 55 GHz, and 66 GHz. The points correspond to the digital sampling of the oscilloscope. **c,** FFT of the captured waveforms. **d,** Transmission scattering parameter through the probe and the cable, reported by the datasheets.

The output waveform shape and its frequency content are determined by the design of the coplanar filter. As shown in Fig. 3.14c, the central frequency of the output pulse can be shifted from 28 GHz to over 60 GHz by changing the layout design of the filter (which in this work was limited by our measurement equipment). The modulator provides a high output power level without an RF amplifier stage, which is one of the most costly and challenging parts of millimeter-wave communication systems. In fact, here there is only one IF amplifier to drive the nanoplasma device, which should only support the much lower bandwidth of the data-rate. The picosecond switching capability of the nanoplasma devices can potentially enable modulation into the terahertz band, bridging the gap between RF and optical modulators [199], [200].

The output power of the modulator becomes lower at higher frequencies, since the filter is excited by a step-like signal, whose frequency content (FFT magnitude) is proportional to the inverse of frequency. This behavior is similar to the general power-frequency trade-off in RF sources (Pf^2 = constant, where P and f represent the output power and frequency of the RF source). Despite this general trade-off, the output power of the proposed modulator is quite high. The output voltage level at the 50-Ω load is in range of several volts, which considering the attenuation of the cable and probe (Fig. 3.14d), results in Watt-range power levels. The output power can be further increased by optimization of the designed filters, as they currently exhibit at least a 5 dB insertion loss at their central frequencies (Fig. 3.13e). Another way to adjust the output power is by changing the gap size of the nanoplasma device, which can tune its operation voltage in a very wide range, from a few volts to thousands of volts.

From a more general point of view, the concept proposed can potentially enable synthesizing analog waveforms with designed shapes. This is challenging to do with classic digital sampling methods for two reasons. First, high-frequency signals require ultrahigh sampling rates, which is difficult at the millimeter and submillimeter bands. Second, the amplification of signals with a rich frequency content is a major challenge. For instance, the fast Fourier transform (FFT) of noise-like signals that are interesting for radar applications [201] can cover a wide range of frequencies, much larger than that achievable with UWB amplifiers [202]. Impulse waveforms are other sort of UWB signals with applications in communications [193], radars [203], imaging [204], and broad-band spectroscopy systems [205].

From a general point of view, Fig. 3.13a shows the block diagram of a universal nanoplasma-based analog synthesizer. A nanosecond pulse source, generated by an ordinary electronic circuit, drives a nanoplasma switch in series with a patterned coplanar structure with transfer function H. The amplitude and phase of H precisely controls the shape of the output signal delivered to the load, which can be a radiating element. Fig. 3.13f illustrates some possible transfer functions and the corresponding output signals, showing the potential functionality of the synthesizer. For a bandpass filter, as described in the previous section, the output signal is a wave-packet, and the system operates as a modulator.

Replacing the bandpass filter by a differentiator [206], the system can potentially generate impulse-like signals. The design of the differentiator determines the spectrum of the generated impulses. The nanoplasma devices offer switching times faster than 5 ps (limited by the bandwidth of the state-of-the-art time-domain measurement tools used) which enables generating UWB signals with at least 70-GHz bandwidth. The enormous flexibility in the design of the coplanar network, which can be precisely implemented by highly accurate fabrication tools can enable a wideband randomly-shaped transfer

function, resulting in a noise-like signal. In all of these potential examples, the system directly delivers the signal at large power levels, without the need for a post-amplification stage, which bypasses a major challenge in high-frequency electronics.

3.7 Microplasma picosecond switches for pulsed-power applications

Pulsed-power is the technology of storing energy a period of time and releasing it instantly through one or multiple high-power fast switches [207]. Such high-power pulses have opened promising pathways to address some of the most important challenges of the current century, such as the conversion of greenhouse gases like CO_2 and CH_4 to value-added products [208] and cancer treatment [209]. The fast switching dynamics of nanoplasma devices (Fig. 3.15a) together with their high-frequency switching capability, over 20 MHz, and extremely high ON-state current that can go beyond 300 A mm^{-1} (Fig. 3.15a, inset), make them outstanding candidates for pulsed-power sources, where the switch plays a key role [210]-[213]. Conventional semiconductor devices, such as MOSFETs and HEMTs, although exhibit a versatile functionality with a practically infinite lifetime, suffer from a low on-state conductivity and a limited switching speed, below 1 kV ns−1 [214] ,[215]. IGBTs are more widely used in pulsed power, however, their switching speed is very slow [216]. There are other electron devices than conventional transistors with fast switching capability, which are specifically developed for pulsed-power applications. For instance, the reverse recovery in drift-step-recovery diodes (DSRDs) interrupts the reverse current in a short time, thus acting as a fast switch [217].

In this section, the application of scaled-up on-chip plasma switches with gap sizes in the micrometer range (microplasma switch) is demonstrated for pulsed-power circuits. The devices are low-cost, easy-to-fabricate, and do not rely on multilayered epitaxies and special materials. In addition, although the switch can be used as discrete device (Fig. 3.15b), it offers the capability of integration, opening avenues for the future ultrahigh power density pulsed-power systems. A sub-100-ps fast switching speed reaching 14 kV ns^{-1} at 15 kW peak power is demonstrated.

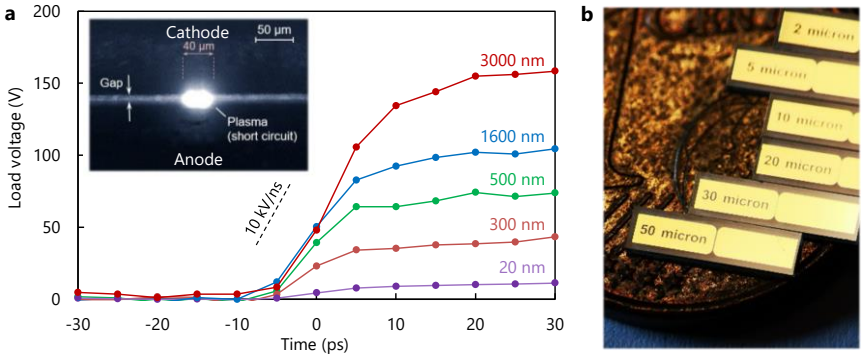

Fig. 3.15 | Extension of nanoplasma switches to high-power microplasma devices. a, On-wafer characterization of switching transient in nanoplasma devices with different gap sizes. The inset shows an optical image of plasma formation in a micro-gap. The switch carries a 13-A peak current which considering the 40 μm width of the plasma indicates a 325 A mm^{-1} current density. **b,** Photograph of discrete switches with various gap distances.

Fig. 3.15a shows the on-wafer switching characterization of nano- and microplasma devices with different gap sizes (*g*), ranging from 20 nm to 3000 nm, showing the capability of the device in operating above 100 V for micrometer-range gaps, while the switching time is still in the picosecond range. In case of the 3,000-nm gap, a 160-V 3.2-A switching corresponding to a 0.5 kW peak power was achieved. The power level can be further increased by increasing the gap distance, however, the voltage and current levels go well beyond the limitations of the employed radiofrequency probes. To demonstrate the high-power switching capability of the plasma devices, scaled-up switches with 1-mm wide channel and different gap distances were fabricated, and the devices were employed in an ultra-compact pulsed-power source. The scaled-up devices were fabricated on a 1-μm-thick tungsten deposited by sputtering on a 2-inch Sapphire substrate. The device layout was patterned by a single photolithography step followed by IBE. Then the wafer was diced into separate discrete devices. Based on such a simple fabrication process, the mass production of these switches can be very fast and low-cost.

Fig. 3.16a shows the experimental setup to evaluate the pulsed-power source utilizing the fabricated switches. A driver circuit generates a bipolar waveform which is used as the excitation of the pulsed-power circuit (Fig. 3.16b and Fig. 3.16c). As shown in Fig. 3.16d, the initial stage of the pulsed-power circuit is an impulse generator which compresses the input bipolar pulse into a high-amplitude short unipolar signal (Fig. 3.16e). The negative part of the bipolar signal biases the diode *D* in the ON state. When the input signal turns positive, the diode *D* does not immediately block the signal, because of

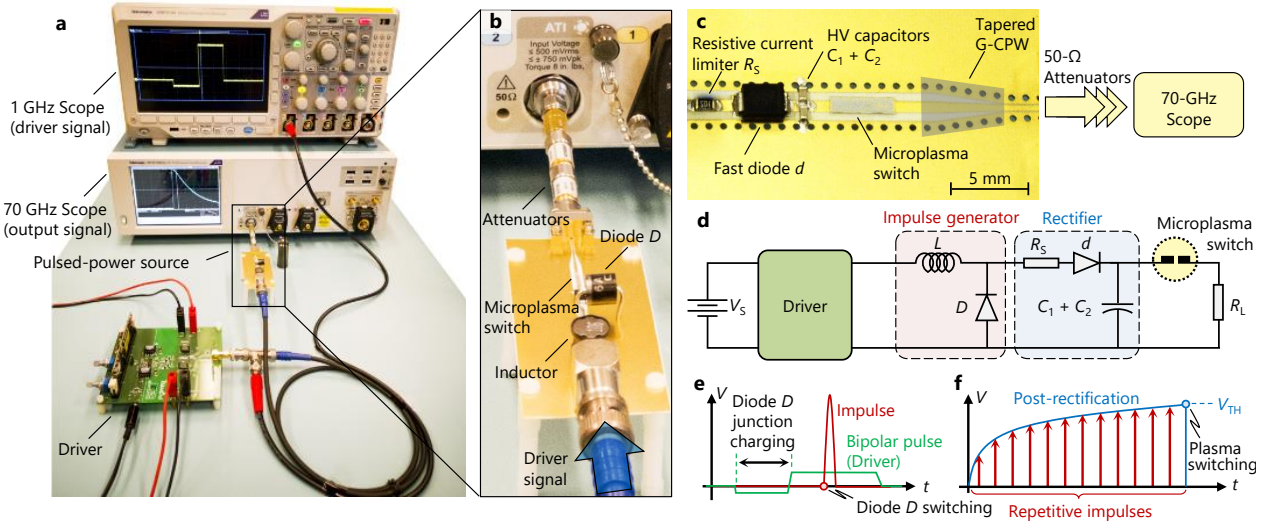

Fig. 3.16 | High-performance pulsed-power circuit using fabricate microplasma devices. a, Photograph of the experimental setup to characterize **b,** the ultra-compact pulsed-power source utilizing the fabricated plasma switches. Measurements were carried out with a 70-GHz real-time Tektronix DPO77002SX oscilloscope. **c,** The top view of the circuit showing the current limiter resistor RS, fast diode d, high-voltage capacitors C_1 and C_2, microplasma switch, and a tapered G-CPW for output termination. **d,** The schematic of the setup illustrating the driver circuit (the green PCB in part a), impulse generator, rectifier, microplasma switch, and the load R_L = 50 Ω. Schematic of the **e,** driver signal, impulse generated by the inductor-diode resonance, and **f,** charging the HV capacitors by repetitive impulses until the micro-plasma switching.

the minority carriers stored in the junction [218]. When the charges are removed, the diode interrupts the current which initiates a resonance between inductor *L* and the capacitance of the diode *D*, leading to the generation of impulse signals. The impulses charge the high-voltage capacitors through a rectifier stage (Fig. 3.16f).

The fabricated switch is then connected to the high-voltage capacitors. When the voltage across the capacitors reaches the threshold voltage (V_{TH}) of the plasma switch, it triggers the device and injects a high-speed pulse into the output port. The circuit is designed based on a grounded coplanar waveguide (GCPW) and the plasma switch is placed face-down, such that two ports of the device are in contact with the signal pads patterned in the printed circuit board (PCB). A 1.85-mm connector rated for 67-GHz bandwidth connects the GCPW to 67-GHz coaxial attenuators with a total attenuation of 60-dB. The signal is finally terminated by the 50-Ω port of a 70-GHz oscilloscope.

Fig. 3.17a shows the output pulses generated by the pulsed-power circuit. We employed switches with different gap distances ranging from 5 μm to 50 μm. The pulsed-power source generates very fast rising-edge output pulses at the 50-Ω terminal, with a high dv/dt reaching 14 kV ns^{-1}, thanks to the high-speed operation of microplasma switches (Figs. 3.17b-c). The output voltage reaches 870 V which corresponds to a peak current and power of 17.4 A and 15.1 kW, respectively. For simplicity, we performed measurements on the ambient air, however, encapsulating the device under modified pressures [219] can be used to manipulate the threshold voltage, which would enable achieving higher powers in small gaps. In addition, a lower load resistance could be employed to absorb a much higher instantaneous power [220]; this is in particular interesting for microplasma switches as they can handle very high current levels.

It should be noted that, although the PCB is well designed, the parasitics in the path of output signal – from high-voltage capacitors to the coaxial connection – still affect the picosecond switching transient. For instance, measurements with ultra-low parasitic radiofrequency probes shows that the dv/dt achieved by 3-μm-gap devices exceeds 11 kV ns^{-1} (Fig. 3.15a), which is about two-times higher than the measured values in the compact pulsed-power source (Fig. 3.17c). This highlights the importance

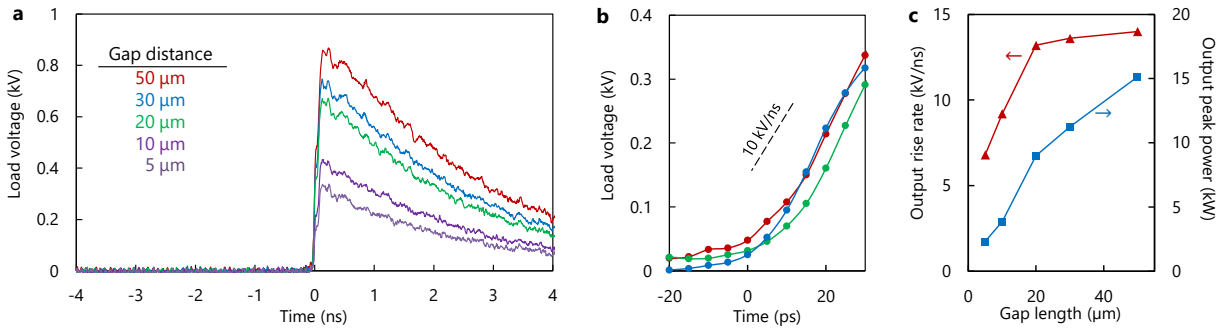

Fig. 3.17 | Characterization of the microplasma-based pulsed-power source. a, Voltage waveforms generated by the pulsed-power circuit. **b,** Rising edge of the signals shown a high value of dv/dt = 14 kV ns^{-1}. (c) Output dv/dt and peak power for different gap lengths.

of the planar structure of on-chip plasma switches which enables a full integration to microwave components, such as transmission lines and antenna, to directly deliver the generated signal to the load.

3.8 Conclusion

This chapter propose an integrable device concept that enables picosecond switching of high-amplitude signals which overcomes the Pf^2 limit in solid-state electronics. In addition to its simplicity and low fabrication cost, its performance surpasses that of current ultrahigh-speed electronic devices. With a proper circuit design, nanoplasma devices enable the generation of ultrafast high-power step and impulse signals, which are key elements for ultra-wide-band systems. The use of nanoplasma devices in high-power terahertz pulse generation was demonstrated, where ~1 W pulses were emitted at 300 GHz, by simply integrating the device with a bowtie antenna. The tunability of V_{TH} together with a high-current capability and low capacitance enable the nanoplasma devices to operate as a high-performance, ultrafast low-parasitic protection unit at the front end of radiofrequency systems.

This chapter also revealed the potential of nanoplasma picosecond switches integrated with coplanar linear networks for millimeter-wave and terahertz modulators in a single metal layer without a need for high-frequency amplifiers. The fabricated modulators provide large output powers (~30 dBm) at high frequencies up to 66 GHz (limited by the bandwidth of the experimental setup). The ease of integration enables the implementation of the proposed concept on almost any platform, including flexible substrates, CMOS, and III-V compounds.

The high performance and simplicity of the proposed devices offer new horizons for future chip-scale ultrafast electronics and terahertz sources with applications in communications, imaging, sensing and biomedicine, among others.

4 Glass-like electronics in Vanadium Dioxide for high-performance data storage and processing

Metal-oxide-semiconductor junctions constitute the building block of today's logic electronics, providing a platform to achieve a variety of functionalities, from memories to computing [221]-[223]. This technology, however, faces fundamental constraints for further miniaturization and compatibility with post von Neumann computing architectures, which has stimulated research on new materials and devices [224]-[226]. Manipulation of structural, rather than electronic, states could provide a pathway towards ultra-scaled low-power functional devices, however, the electrical control of such states is not trivial. This chapter reports on electronically accessible long-lived structural states in Vanadium Dioxide that can offer a scheme for data storage and processing. Such states can be arbitrarily manipulated in short time scales and tracked beyond 10,000 seconds after excitation, exhibiting similar features of glasses, which are beyond the classic metastability in Mott systems [227]. In two-terminal devices with channel lengths down to 50 nm, sub-nanosecond electrical excitation can take place with energy consumption down to 100 femto joules. In addition, the state of the device is determined by a nonlinear superposition of multiple excitations, which enables processing of a sequence of data bits. These glass-like functional devices can outperform conventional metal-oxide-semiconductor electronics in terms of speed, energy consumption, and miniaturization, and open avenues for neuromorphic computation and multi-level memories.

4.1 Strongly correlated electronic systems for the post-CMOS era

Strongly-correlated materials, in which several physical interactions involving spin, charge, lattice, and orbital are simultaneously active, display notable electrical properties [228]. Among them, the first-order insulator-metal transition (IMT) in vanadium dioxide (VO_2) happening close to room temperature has attracted considerable interest [229]-[233]. From a physical point of view, understanding the

underlying mechanism of phase switching in VO_2 is still a challenge in condensed matter physics, as several models ranging from Peierls- to Mott-Hubbard-type were not successful in explaining the broad range of phenomena occurring in the material [234]. Different types of excitations such as temperature, electric field, and doping can induce IMT, which makes the understanding of the phase switching more challenging [229], [235]. From a technological point of view, the bulk conductivity and abrupt phase transition in VO_2 can potentially overcome some of the fundamental limitations in conventional metal-oxide-semiconductor electronics, such as the limited conductance imposed by Thomas–Fermi screening [92] and the thermionic subthreshold-slope limit imposed by Boltzmann–tyranny [236].

Besides the application of phase change materials in traditional electronics, the rich variety of phenomena in vanadium dioxide [237]-[241] can provide completely novel functionalities that enable new schemes for the future of electronics. This chapter demonstrates an exotic property of Vanadium Dioxide—electrically controllable glass-like states—which can offer a platform for information processing and storage. We show that a two-terminal device exhibits a continuous spectrum of lattice-originated states that can be revealed by the incubation time of the IMT: the time at which the nucleation of phase transition percolates to form the first conductive filament between two terminals of the switch. The state can be imposed by a sequence of binary switching events and can be tracked hours after the excitation. The system exhibits features of a glasses, presenting a memory effect much longer than that induced by classic metastability in Mott insulators [227], [241].

4.2 Observation of a quasi-nonvolatile memory effect in VO_2

A 100-nm-thick film VO_2 synthesized by sputtering on a high resistivity silicon substrate (Fig. 4.1a). A Vanadium target (99.95% pure) was used in a plasma chamber with pressure of 0.007 mbar, Oxygen flow of 22.1 sccm and Argon flow of 12.5 sccm. The substrate temperature was at 600 °C during the deposition. Two terminal devices fabricated on the synthesized VO_2 film exhibited sharp IMT driven by temperature (Fig. 4.1b), as well as consistent voltage-driven switching (Fig. 4.1c).

Fig. 4.2a shows an ultrahigh sample-rate time-domain experimental setup that can precisely collect temporal response of a two-terminal VO_2 switch (inset). The device was integrated with radiofrequency pads (ground-signal-ground configuration) which together with high-frequency probes enable accurate measurements with time resolutions down to ~5 ps. A square pulse generator applies repetitive 10-μs-long pulses with a fixed amplitude (set voltage V_{set} = 2.1 V) to a two-port 3-μm long VO_2 switch. The waveform of the current passing through the device is measured at the 50-Ω port of a high-frequency oscilloscope, and the transient conductance of the device is extracted. Following an applied pulse, the VO_2 film exhibits initially an insulating behavior, and only after an incubation time tinc, it undergoes IMT (Fig. 4.2b). The measurements indicate that the incubation time strongly depends on the history of the previous phase transitions. The very first switching curve presented in Fig. 4.2b shows an incubation time of ~1.4 μs. Triggering an IMT and measuring the incubation time after a 10-ms-long relaxation time (T) results in a 10-time shorter incubation time. Longer relaxation times after the first phase transition cause longer incubation times, however, the value of t_{inc} is still lower than that of the very first switching, even after T = 10,000 s.

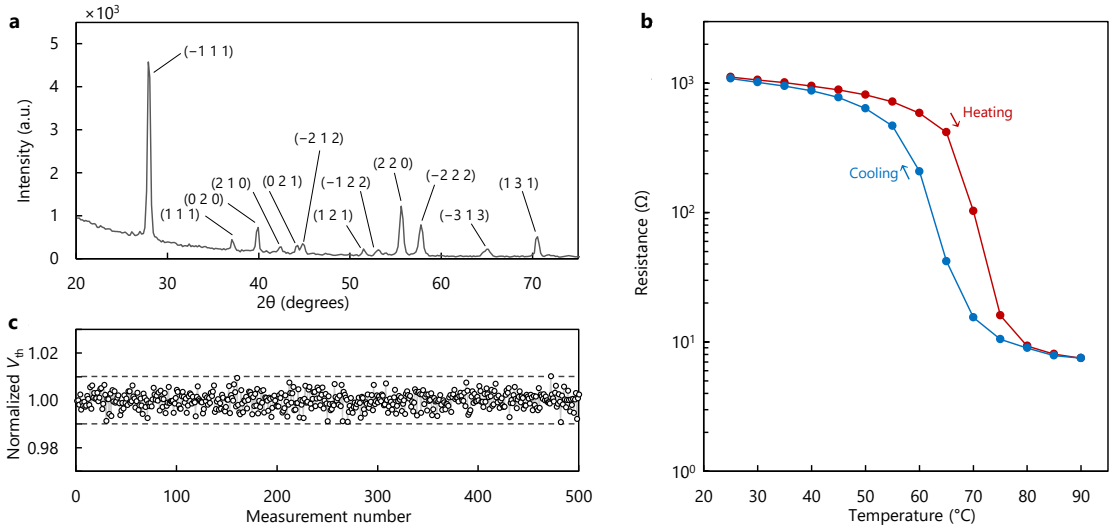

Fig. 4.1 | Demonstration of a single monoclinic phase and consistent IMT switching in the VO_2 film. a, The thin film structure was determined by X-ray diffraction (XRD) analysis using an Empyrean X-ray diffractometer with monochromatic Cu Kα radiation (λ = 0.154056 nm). The $\theta - 2\theta$ diffraction pattern, recorded in the 20° – 75° (2θ) range. The result indicates that the sample is crystallized in the single monoclinic phase as all diffraction peaks are indexed to monoclinic VO_2 (M1) crystal structure according to PDF 04-003-4401 (Space group $P2_1/c$, a = 5.75 Å, b = 4.52 Å, c = 5.38 Å, β = 122.6°). **b,** Resistance versus temperature of a two-port VO_2 switch showing a sharp reduction at the critical temperature of VO_2. **c,** Threshold consistency indicating no degradation. A 3-µm-long VO_2 switch was excited by a voltage ramp and the threshold voltage at each IMT triggering was monitored. The results indicate less than ±1% variation with no drift, indicating no degradation in the film.

Incubation time versus relaxation time, shown in Fig. 4.2c, indicates a logarithmic relation t_{inc} = (78 ns) log(T/(160 μs)). Although t_{inc} has a strong dependence on the previous switching events, the device conductance Gins in the insulating-state shows very small variations that become undetectable after ~1 s (Fig. 4.2d). The observed effect is qualitatively identical in micrometer- and nanometer-long devices. Fig. 4.2e shows incubation time versus the relative increase in conductivity for a 100-nm-long channel device. The values of incubation times are well distinguishable while the conductivity shows a very small variation, which completely relaxes after 1 second. The thermal relaxation of the device is quite fast (~100 ns, see section 4.3), and therefore, the heat accumulation does not play any role in these observations (inset of Fig. 4.2e). The memory effect observed in t_{inc} is reversible and is not due to any degradation in the film (Fig. 4.2f). The results were reproduced in devices with different metal contacts (Fig. 4.3). The fabricated devices show a high device-to-deice consistency (Fig. 4.4).

The results were reproduced on devices fabricated on single-crystal VO_2 films, which indicates the generality of the observation (Fig. 4.5). The VO_2 films were grown on the (001) TiO_2 (Fig. 4.5a) and (0001) Al_2O_3 (Fig. 4.5b) substrates by pulsed laser deposition (PLD). For fabricating ceramic target for growing stoichiometric VO_2 films, stoichiometric V_2O_5 (99.99%, Sigma Aldrich) powder was sintered at 600°C for 18 hours. (001) TiO_2 and (0001) Al_2O_3 substrates were loaded in to high-vacuum PLD chamber and evacuated to a base pressure of ~ 1×10^{-6} Torr. Then, the prepared V_2O_5 ceramic target was ablated by focusing KrF excimer laser (λ = 248 nm) at laser fluence of 1 J/cm^2 and laser frequency of 1

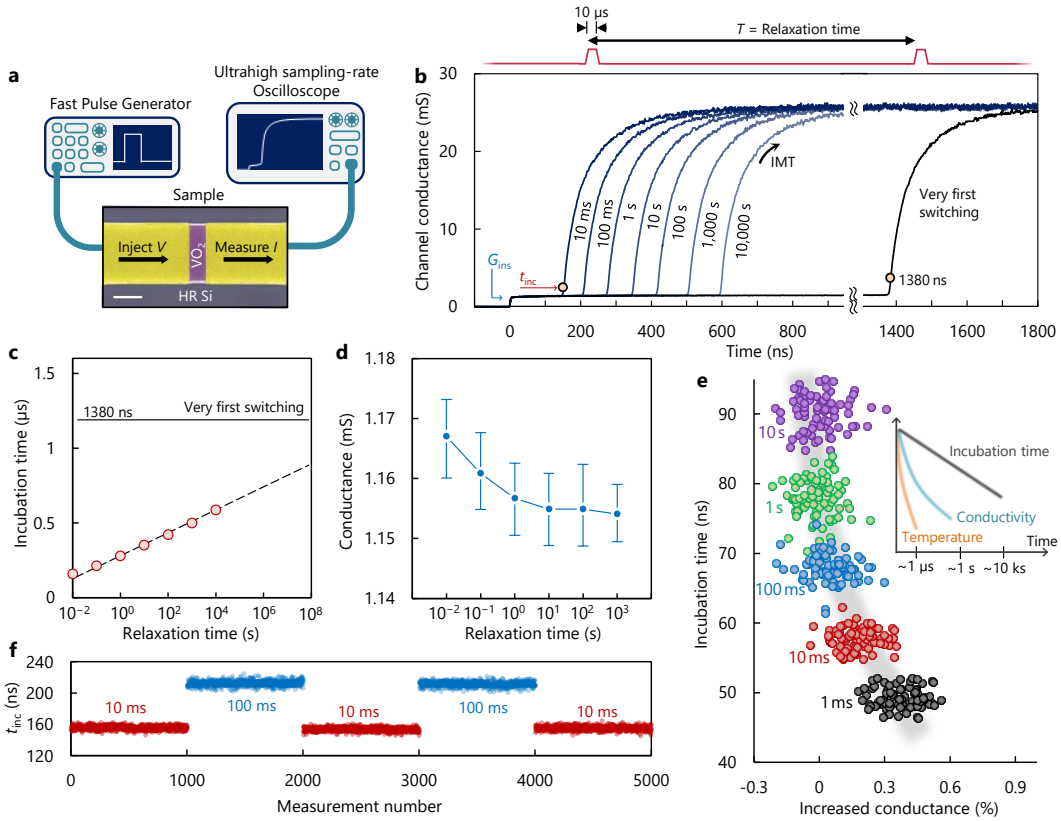

Fig. 4.2 | Tracing state dynamics of VO_2 switches with incubation time. a, Schematic of the experimental ultrafast time domain setup. The SEM image shows the VO_2 switch (scale bar corresponds to 5 μm). Here the devices investigated had lengths varying from 50 nm to 3 μm. **b,** Transient conductance of the VO_2 channel corresponding to different relaxation times T, as well as the very first switching cycle. Incubation time (t_{inc}) corresponds to the interval between the applied pulse and the onset of the change in conductance due to IMT. The insulating-state conductance G_{ins} corresponds to the average of conductance in the time interval between 20 ns and 120 ns. **c,** Incubation time versus relaxation time. t_{inc} shows a logarithmic function of T. The error bars are smaller than the point dimension. **d,** Conductance of the insulating state versus relaxation time. After ~1 s, variations in the conductance can no longer be detectable. **e,** Incubation time versus increased conductance, showing the reproducibility of the results in nano-devices. The inset illustrate the fast relaxation of temperature and resistance, and the slow dynamics of incubation time. **f,** Monitored incubation time for 5,000 measurements, showing that the effect is reversible and consistent.

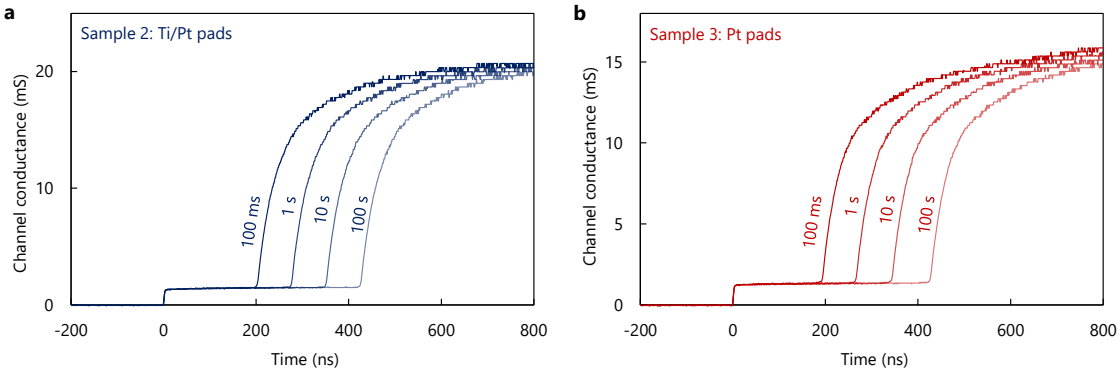

Fig. 4.3 | Reproducibility of the results in devices with other metallic pads. Two-port switches fabricated on the high resistivity silicon substrate, based on **a,** VO_2 / Ti (10 nm) / Pt (200 nm) and **b,** VO_2 / Pt (200 nm) structures exhibit identical memory behavior. The results indicate that the observation is independent from metal-VO_2 interface.

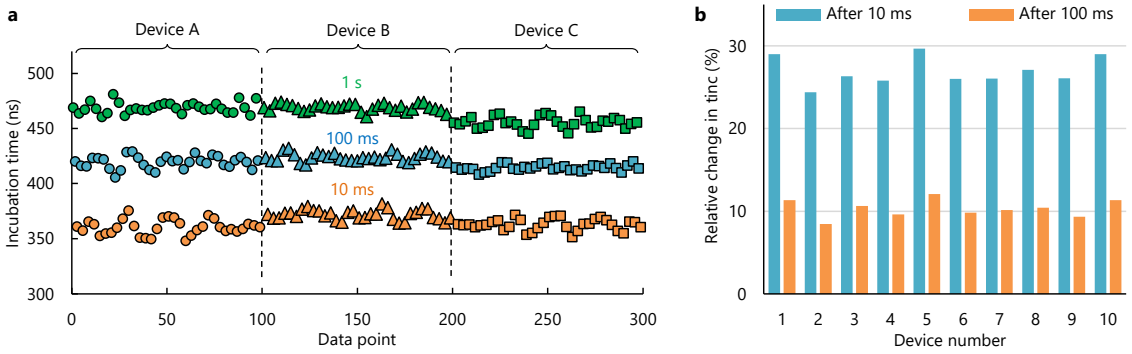

Fig. 4.4 | Consistency of the observed memory effect. Applying repetitive pulses (V_{set} = 1.9 V) to a 500-nm-long channel device with periodically changing the separation times between 1s, 100 ms, and 10 ms, and monitoring the incubation time corresponding to each value of relaxation time. **a,** Measured incubation times over 100 consecutive measurements for three devices with identical geometries. **b,** Consistency of the memory effect defined as $m = t_{\mathrm{inc}}^{\mathrm{ref}}/t_{\mathrm{inc}} - 1$ for ten devices with the same geometry. $t_{\mathrm{inc}}^{\mathrm{ref}}$ is the incubation of the reference pulse (corresponding to 1 second relaxation) and t_{inc} represents the incubation time corresponding to pulses with 10 ms (blue columns) or 100 ms (orange columns) relaxation times.

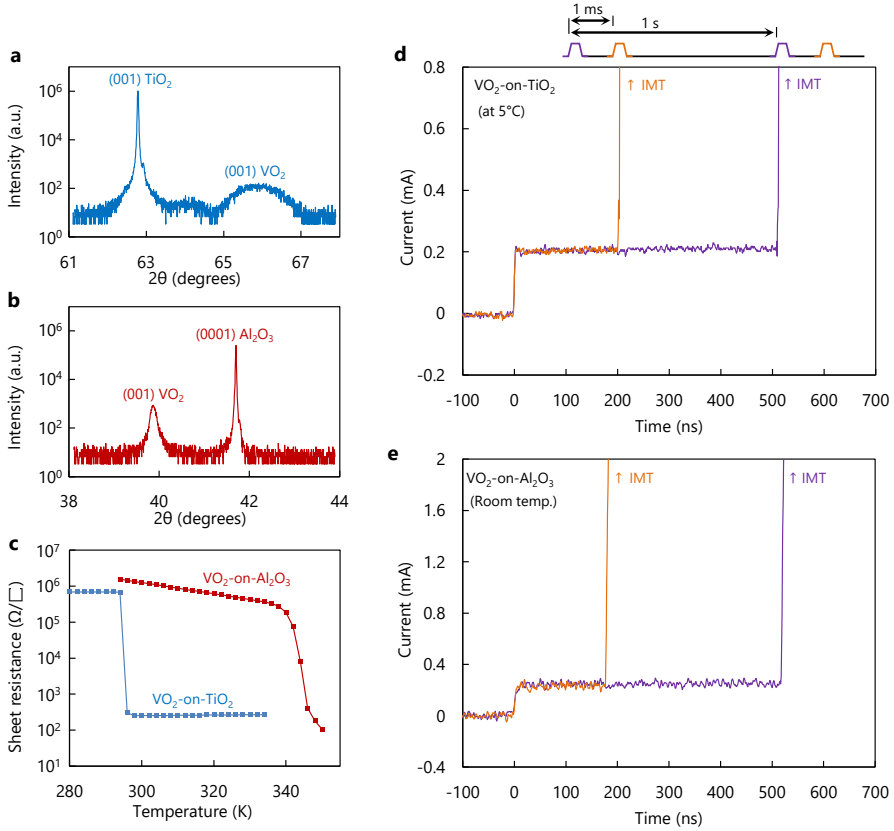

Fig. 4.5 | Reproducibility of the results on a single-crystal VO_2 samples on TiO_2 and Al_2O_3 substrates. Symmetrical 2θ-θ XRD scan on the **a,** 10 nm-thick VO_2 film grown on (001) TiO_2 substrate (VO_2-on-TiO_2), and **b,** 100 nm thick VO_2 film grown on (0001) Al_2O_3 (VO_2-on-Al_2O_3). **c,** Sheet resistance measurements on VO_2-on-TiO_2 and VO_2-on-Al_2O_3 samples in the heating cycle. In case of VO_2 grown on the (001) TiO_2 substrate, which is strained along the c-axis by -1.2%, the transition temperature is shifted from ~340 K to ~292 K. **d, e,** Pulsed-measurements with two relaxation times - 1-ms and 1-s - on VO_2-on-TiO_2 and VO_2-on-Al_2O_3 samples, showing the strong dependence of t_{inc} on the relaxation time. In case of the VO_2-on-TiO_2 sample, the stage temperature was 5 °C to ensure that the film reverts back to the insulating state after removing the excitation.

Hz. VO_2 films were grown on the (001) TiO_2 substrates at TG (substrate temperature) ~ 300°C with p_{O2} (oxygen partial pressure) of 18 mTorr and on the (0001) Al_2O_3 substrates at T_G ~ 450°C with p_{O2} ~ 30mTorr, respectively. After growth, both samples were cooled down to room temperature at 20 °C/min. Symmetric 2θ-ω scans was performed by using high-resolution x-ray diffractometer (D8 Discover, Bruker, λ = 0.15406 nm) at Materials Imaging & Analysis Center of POSTECH (Pohang, South Korea). And temperature-dependent sheet resistance during heating and cooling cycles was measured at a van der Pauw geometry by using Hall measurement system. The synthesized films exhibit around 4 orders of magnitude resistive switching (Fig. 4.5c), and the devices showed pronounced voltage-driven switching with the memory embedded in the incubation times (Fig. 4.5d-e).

4.3 Arbitrary manipulation of VO_2 using a burst of electrical pulses

In a following experiment, the devices were excited with a packet of N identical pulses (V_{set} = 2.1 V) and t_{inc} was monitored after a relaxation time T = 1 s (Fig. 4.6a). The total duration of the excitation including N pulses (ΔT = 1 ms) was much shorter than the relaxation time T. Different pulse packets result in different values of t_{inc}, indicating that such multi-pulse excitation can be used to manipulate the state of the device. Fig. 4.6b shows the summary of the observed results in which the measured values of t_{inc} for different values of N are presented for 60 consecutive acquisitions. These results indicate a fully-electrical scheme to manipulate and sense a Mott system (Fig. 4.6c). Such electrical manipulation concept can enable multi-level memories. In addition to that, one can see that multiple excitation can further decrease the incubation time of the IMT switching, which can open avenues for brain-inspired computation (see section 4.6).

It is worth noting that the excited state does not depend on ΔT, and so the state can be induced in very short time scales (Fig. 4.7). To examine this feature, a VO_2 switch was first submitted to a sequence of

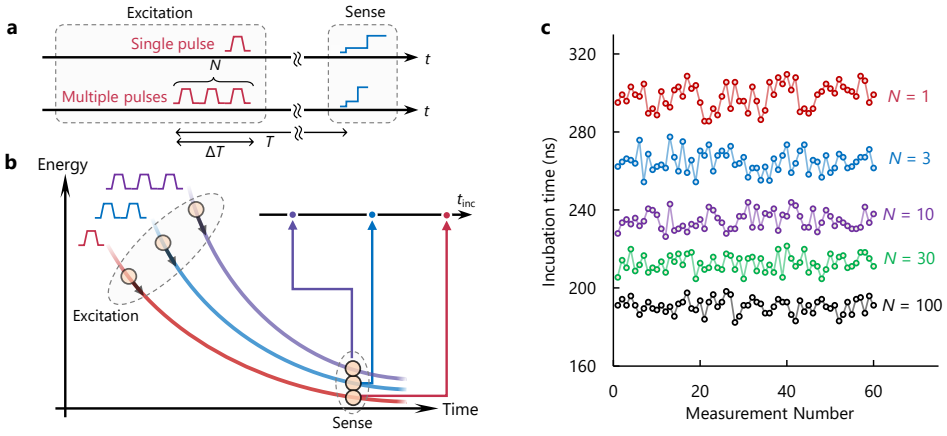

Fig. 4.6 | Manipulation of post-firing state of VO_2 switches. a, Schematic showing excitation of the VO_2 switch with single or multiple pulses and monitoring of the t_{inc} at the sensing pulse after a long relaxation time. **b,** After multiple pulses, the film undergoes different relaxation trajectories, and monitoring t_{inc} can well identify the different original excitations. **c,** Measured t_{inc} for different excitation pulse numbers (N) for ΔT = 1 ms and T = 1 s.

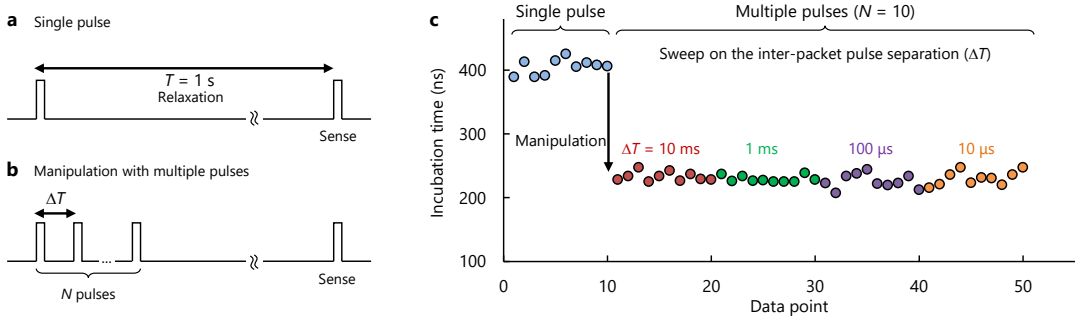

Fig. 4.7 | Effect of inter-packet pulse separation on manipulation of the device state. a, Schematic of waveform corresponding to a single-pulse excitation (V_{set} = 2.7 V and 1-μs pulse width) and sensing incubation time after the relaxation time T = 1 s. **b,** Schematic of waveform corresponding to N-pulse excitation (identical pulses to part a) with inter-packet pulse separation ΔT and sensing the incubation time after the relaxation time T = 1 s. **c,** Measured incubation time on a 500-nm-long channel device for single pulse excitation and multiple pulse excitation (N = 10) with different ΔT = 10 ms, 1 ms, 100 µs, 10 µs. The results clearly shows the state manipulation capability with multiple pulse excitation, however the inter-packet pulse separation plays no role in the state manipulation.

single pulses and the incubation time was monitored (Fig. 4.7a). Then repetitive sequences of 10 pulse packets with inter-packet pulse separation of 10 ms to 10 µs were considered (Fig. 4.7b). The incubation times were identical in all cases of inter-packet pulse separations, while being much lower than the incubation time corresponding to the single pulse excitation. Incubation time in the evaluated devices also did not show any dependence on the width of excitation pulses and the state manipulation was achieved only through the number of triggering events (Fig. 4.7c).

4.4 Exploration of possible physical mechanisms

A. Thermal effects

Vanadium dioxide is sensitive to temperature and one can argue that the memory effect could be due to a temperature rise in the film. However, there are multiple arguments showing that the device is cooled very fast after the excitation:

A1. Double sweep pulsed IV measurements were carried out on the VO_2 devices to identify the cooling rate of the device, as VO_2 exhibits temperature-dependent resistivity. The results presented in Fig. 4.8a shows that the metal-to-insulator transition (from point B to A) takes place in about 100 ns. Noting the high current of the device in the metallic phase, one expects to have a temperature notably above the IMT, however, the device cools down below the critical temperature in short time scales. In addition, the resistance of the insulating phase before and after the switching are very close (inset of Fig. 4.8a) suggesting that the device cooling completes in microsecond time scales.

A2. Electrical pulsed measurements at the same time with IR micro-imaging were carried out to monitor possible temperature rise on the VO_2 film. The VO_2 switch was examined by

repetitive 10-μs pulses with different frequencies 0.1 Hz, 1 Hz, and 10 Hz. The device temperature was captured during the experiment with an integration time of 10 seconds. Because the duty cycles are very low (maximum 0.01% in case of 10 Hz excitation), the averaged thermal image gives the post-firing temperature. Fig. 4.8b shows the device temperature on the illustrated cutline (inset). The small peak and valley close to the gap (position = 0 μm) are due to the metallic edge. As it can be seen, the temperature close to the gap is very similar and the variations are in range of measurement errors, although repetition rates were orders of magnitude different.

A3. If the observed memory is driven by a temperature rise, then one expects to see a more pronounced change in the incubation time if the device is excited by stronger pulses (higher amplitudes). The results presented in Fig. 4.8c-d show the exact opposite: the change in the incubation time does not depend on the amplitude of the exciting pulse. These results disprove any contribution from thermal effects on the observed memory.

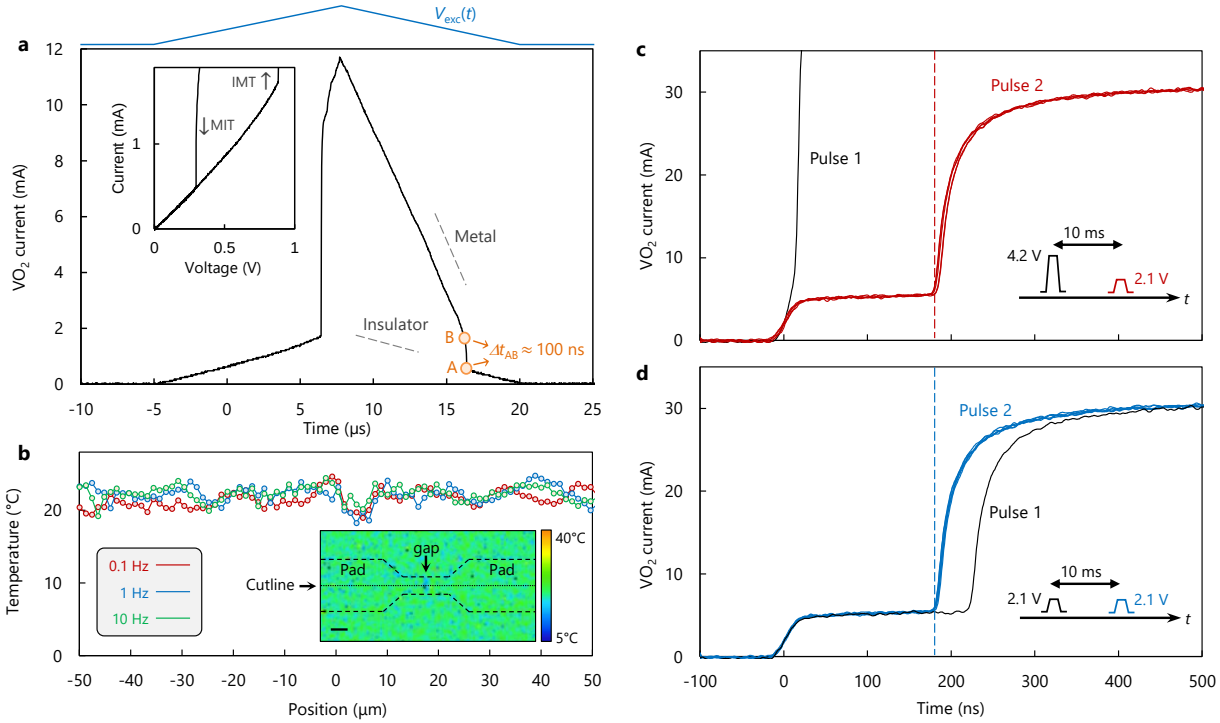

Fig. 4.8 | Investigation on the possible effect of temperature rise on the observed memory effect. a, Measured current of a VO_2 switch under triangular excitation. The MIT transition happens between points A and B with a short time separation of $\Delta t_{AB} \approx 100$ ns. The inset presents the extracted resistance of the device in the IMT and MIT cycles showing that post excitation resistance is close (within 1%) to the pre-IMT resistance. This is another indication of the fast sub-microsecond cooling. **b,** Thermal microscopy of a two-terminal VO_2 switch triggered by 10-μs pulses (V_{set} = 2.1 V) with three different frequencies 0.1 Hz, 1 Hz, and 10 Hz. The captured average temperature over the device does not show any noticible difference between the three cases. This indicates that given the long time duration of our observed memory, this memory effect cannot be originated from thermal effects. **c, d,** Investigation of the memory effect for different excitation amplitudes V_{set} = 4.2 V and 2.1 V, respectively. If thermal effects induced the memory effect, then the 4.2 V excitation should result in a more pronounced change in the incubation time, because it leads to a higher temperature rise comparing to 2.1 V excitation. The measured incubation times, however, are identical, which disproves the role of thermal effects in our observed memory.

B. Electromigration

The second possible hypothesis was whether the electric current in the film induced the observed memory. This is a critical aspect because quasi-non-volatile memories induced by long high-current biases have been observed [242]. However this is not the case in the here-presented case, as the memory effect is independent from the excitation type and can also be induced purely by heat. Fig. 4.9a shows synchronized measurements in which IMT is achieved by a pulsed heater that is electrically isolated from the VO_2 switch. Every two seconds, a 20-µs-long pulse triggers IMT in the electrically isolated heaters, which ensures a temperature-driven IMT in the VO_2 switch at the middle of two heaters (Fig. 4.9b-c). We electrically triggered the middle VO_2 switch with a period of one second and monitored the incubation time. The electrical excitation had a 20-ms time lag with respect to the heater signal (Fig. 4.9d). Therefore, in one electrical measurement, the VO_2 switch had a 20-ms relaxation time after a thermal-IMT, and in the next electrical measurement, the switch had a much longer relaxation (1 second) which is considered to be the reference measurement (without memory).

The results indicate that the thermally-driven IMT also induces a change in incubation time (Fig. 4.9e). This suggests the generality of the effect, as it can be driven not only by voltage/current, but also by heat. At the same time, the results show that the electric current in the film, which could induce excitation or movement of ions, does not play any role in the memory effect since there was no current flowing in the device during the thermally-driven IMT.

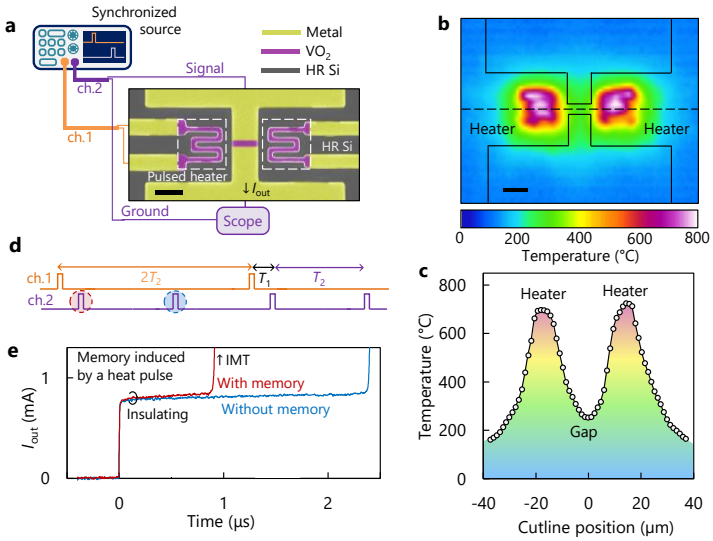

Fig. 4.9 | Exploration on possible mechanisms behind the long memory. a, Schematic of an experimental setup for a synchronized measurement in which the memory is induced by a heat pulse, without flowing current through the VO_2 device. **b,** Captured thermal micrograph of the device with the heaters are triggered at their threshold voltage (18 V). The scale bar corresponds to 10 μm. **c,** Measured temperature over the cutline shown in part B indicating that the temperature at the middle switch (gap) considerably surpasses the IMT temperature. **d,** Illustration of waveforms in the synchronized measurement. Channel 1 triggers the IMT in electrically-insulated pulsed heaters which ensure thermal-driven phase transition in the middle switch. 20-ms after thermal IMT, the middle switch is triggered by a voltage pulse and the incubation time (dashed red circle) is compared with the case of no thermal-driven IMT (dashed blue circle). After 20 ms, the switch was back to room temperature, because of the very small excitation duty cycle (0.1%), which is also reflected by the similar insulating state conductivities with and without memory effect. **e,** Measurements for three consecutive cycles indicate that the memory can be induced by thermal IMT, showing the generality of the effect.

C. Influence from Metal-VO_2 junction

VO_2 is an oxygen-rich thin-film and so its junction with the top metal pads forms a metal-oxide interface which could potentially exhibit non-volatile switching, as observed in TiO_2 for example [94]. In addition, metal atoms could potentially diffuse in the VO_2 film, resulting in persistent changes in the device. Nevertheless, our experiments showed that the metal-VO_2 junction plays no role in the observed memory for the following reasons. First, we found that the effect is independent from the metal type: Ti/Au (Fig. 4.2), Pt, and Ti/Pt (Fig. 4.3). Second, we reproduced the memory effect in a cross structure (Fig. 3d), which enables triggering IMT only in the central portion of the VO_2 channel, without activating the metal-VO_2 interface.

As shown in Fig. 4.10a we fabricated four-terminal cross structures and examined whether triggering of VO_2 from the horizontal terminals can modify the incubation time of the vertical path. We made sure that the region of phase transition due to the horizontal triggering does not reach to the vertical metallic pads. We repetitively triggered IMT in the vertical path with the period of 10 s and captured the incubation times. For odd periods we triggered IMT in the horizontal path, 1-s before the vertical excitation. The even periods do not have this horizontal excitation (Fig. 4.10b-c). We considered the even cycle as the reference and examined whether the odd periods show a different incubation time. Our results show that the horizontal triggering reduces the incubation time on the vertical path (Fig. 4.10d).

As a control experiment, Fig. 4.10e presents the measured current at terminal 4 (I_{out}) while triggering the horizontal path. This is to make sure that the area of phase transition in the horizontal path does not reach the vertical metallic pads. We always apply V_{low} = 0.5 V to the terminal 1 to track the vertical channel resistance. Fig. 4.10e shows that the current at terminal 4 corresponds to the resistance of the insulating state and the two spikes with different polarities (exactly happening at the rising and falling edges of voltage waveforms) are due to capacitance coupling, since the integration over the curves results in no net charge transfer. This control experiment confirms that the change in the incubation time presented in Fig. 4.10d is only due to modification of the VO_2 channel, and not the metal-VO_2 junction.

This experiment rules out the possibility of the metal-VO_2 interface to play a role in the observed memory effect. In addition, accessing the memory effect in a cross structure shows an interesting possible implementation of this material for memory devices as well as programmable computational devices.

D. Long-lived metallic domains

Post-IMT intermediate super-cooled metallic domains [243] that can potentially persist considerably below the transition temperature is another possible mechanism that could lead to memory effects in VO2. Using ultrafast electron diffraction and infrared transmissivity experiments researchers have reported a metastable monoclinic metallic state that can persist a few picoseconds after destroying the ground state by an optical pulse [244]. Electrical measurements have suggested such metallic domains can persist up to a few milliseconds at temperatures below the IMT [227]. This was described by the classic metastability in first-order transitions [245] which is known to persist up to milliseconds [241].

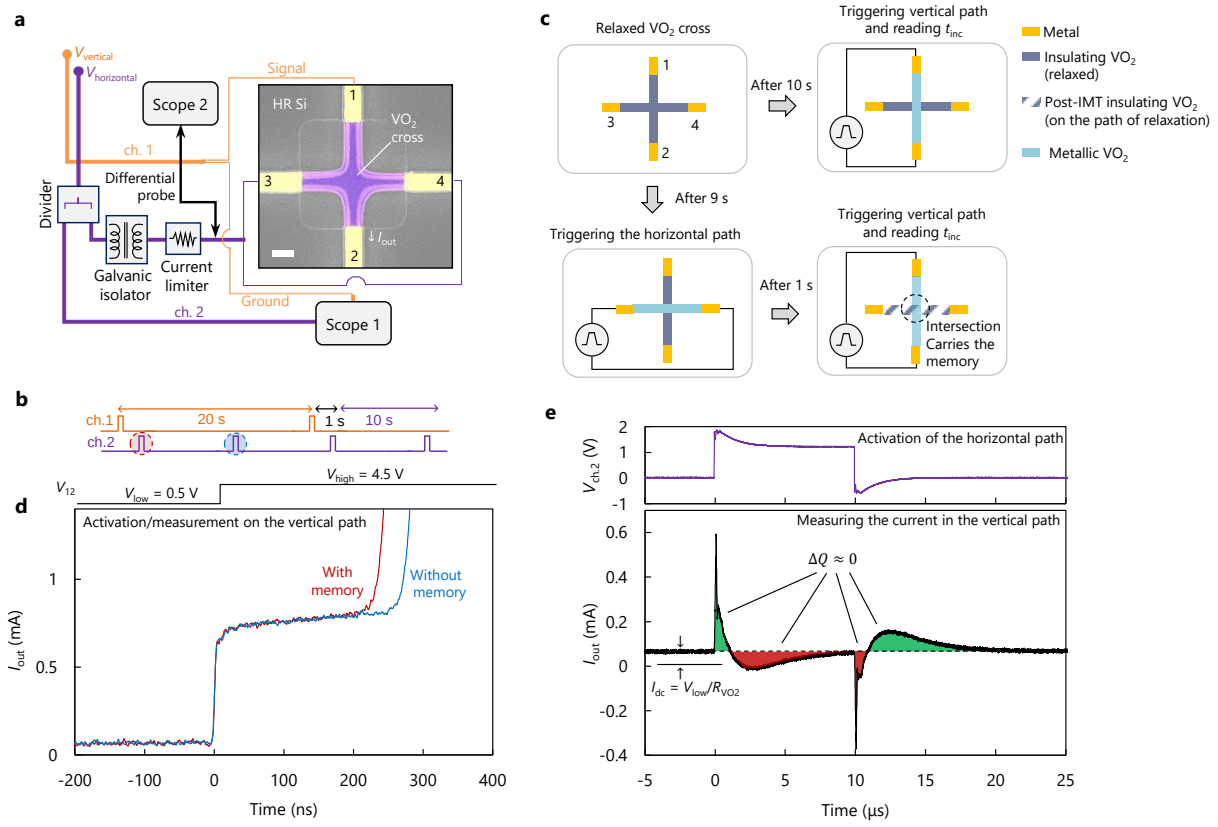

Fig. 4.10 | Synchronized electrical characterization of a four terminal VO_2 cross structure. a, Schematic of the experimental setup. A signal source generates two synchronized trains of pulses at channels 1 and 2. Channel 1 triggers the vertical path (terminal 1) while terminal 2 is connected to a high speed scope. Terminals 3 and 4 are differentially activated by channel 2. A transformer was used to galvanically isolate the vertical and horizontal paths of the cross. In this case, the charges forced into the terminal 1 must exit from the terminal 2, and the input charges forced into the terminal 3 must exit from the terminal 4. The scale bar corresponds to 2 μm. **b,** Schematic of the applied signal to the cross structure. Channel 1 generates a sequence of pulses with period of 10 s. Channel 2 generates a sequence of pulses with period of 20 s, which is 1-second lagged with respect to channel 1. Looking at the excitation of terminal 1, in cycle the cross has a 1-second activation history on the horizontal direction, and in the other cycle, has a 10-second activation history on the vertical direction. Here we consider the 10-second history case as the reference relaxed film. **c,** Schematic of the VO_2 cross structure in two different cycles. In one cycle, the vertical path is triggered after 10 second relaxation to measure the reference incubation time (named as no memory). In another cycle, the vertical path is triggered 1 second after triggering the horizontal path (names as with memory). **d,** Output measured current at terminal 2, with and without memory, showing that the horizontal triggering modifies the incubation time of the vertical path. In this measurement, the applied pulses to the terminal 1 has the minimum voltage of V_{low} = 0.5 V which enables a real time resistance measurement in the vertical path, to make sure that the phase transition region in the horizontal triggering does not reach to the pads of terminals 1 and 2 (vertical path remains in the insulating regime). **e,** Measured current on terminal 4 while triggering the horizontal path. The small dc current corresponds to $I_{dc} = V_{low}/R_{ins}$ where R_{ins} (≈ 10 kΩ) represents the insulating state resistance of the device. The current measurement at terminal 4 indicates that the vertical switch remains in the insulating state and the two damping spikes on the current measurement correspond to capacitive coupling between terminals as the integration over these variations result in no net charge transfer.

However, the time scales involved in our observed memory are orders-of-magnitude longer than what is reported for such long-lived metallic domains. Thus, if metallic domains were related to such memory effect, conventional microscopy techniques used to monitor the lattice structures [246] or electronic properties [247] should be able to directly reveal possible metallic domains that survive for hours at room temperature. Such ultra-long lasting domains, however, have not been observed in the literature, nor in our in-situ Kelvin probe force microscopy (KPFM) measurements (Fig. 4.11).

We explored more in-depth the relation between long-lived metallic domains and our observations. The VO_2 cross experiment presented in Fig. 4.10 shows that such possible long-lived metallic domains have to be in the VO_2 channel and not at the metal-VO_2 junction. In this case, the change in incubation time should be more pronounced for devices with shorter channels, as the channel length approaches to the size of the largest metallic domains. In the extreme case, where the channel size becomes shorter than the size of a metallic domain, the incubation time becomes zero. Such metallic domains are also expected to show a larger change in the conductance in shorter channel devices, considering the film as a resistive network. The results presented in Fig. 4.12 show that devices with smaller channel lengths down to 50 nm exhibit a higher increase in the conductance which could be due to possible long-lived metallic domains that could persist in millisecond time scales [227]. The memory embedded in the incubation time, however, was nearly constant for all gap lengths (Fig. 4.12) which shows that the effect does not originate from possible long-lived metallic domains.

We also examined the IMT threshold voltage of the devices which is known to be more sensitive to the presence of long-lived metallic domains than the channel resistance [227]. The results presented in Fig. 4.12e show that the threshold voltage and resistance follow the same trend, and totally relax after a few seconds, while the incubation time shows a logarithmic relaxation which keeps relaxing for orders of magnitude longer times. These measurements show that the incubation times are independent from threshold voltage and resistance changes, and thus that the long-lived metallic domains are unlikely related to our memory observation.

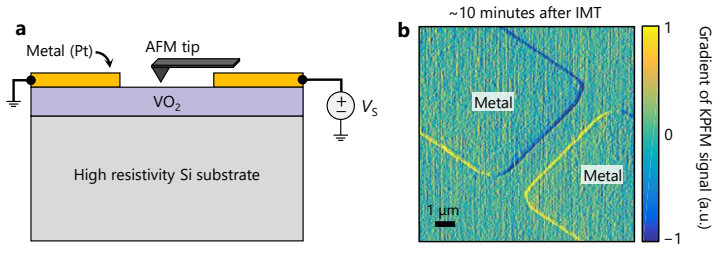

Fig. 4.11 | In-situ kelvin probe force microscopy to observe possible long-lived metallic domains. a, Illustration of the KPFM experimental setup with in-situ electrical excitation to monitor possible long-lived metallic domains after electrically-driven IMT. If some metallic domains can possibly survive at room temperature and are responsible for the hours-long memory, one expects to capture a nonuniform surface potential map [247]. **b,** Gradient of the KPFM signal corresponding to the post-IMT scanning indicates visually no difference between the VO_2 layer and the metallic pads (serving as reference), which is not supportive for long-lived metallic domains at the resolution of the KPFM scan (~30 nm) to be responsible for the observed memory.

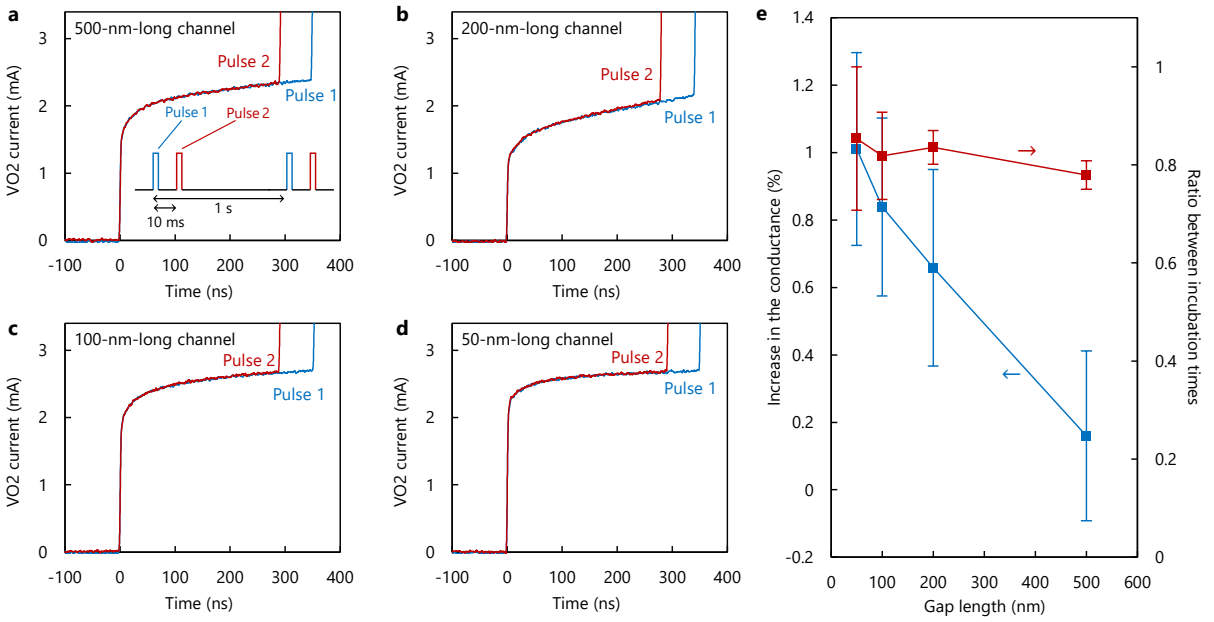

Fig. 4.12 | Examining the hypothesis of mesoscopic states being responsible for our observation. VO_2 switches with different channel lengths ranging from 500 nm down to 50 nm and fixed width of 20 µm were investigated. The memory effect was probed by applying double pulses with relaxation times of 1 s and 10 ms. The measured VO_2 current for **a,** 500-nm-long channel VO_2 switch (V_{set} = 2.8 V). **b,** 200-nm-long channel VO_2 switch (V_{set} = 1.65 V). **c,** 100-nm-long channel VO_2 switch (V_{set} = 1.25 V). **d,** 50-nm-long channel VO_2 switch (V_{set} = 0.95 V). The voltage of each device was set to result in almost identical incubation times in the first reference pulse (blue curves). These results show that the memory effect is identical among devices, and not a strong function of channel length. This suggests that the observed phenomena are not attributed to any mesoscopic length scale. **e,** Increased conductance of pulse 2 with respect to pulse 1 versus gap length, showing a notable increase for devices with shorter channel lengths, which is possibly due to the existence of long-lived metallic domains. The memory effect in the incubation time, however, is almost constant.

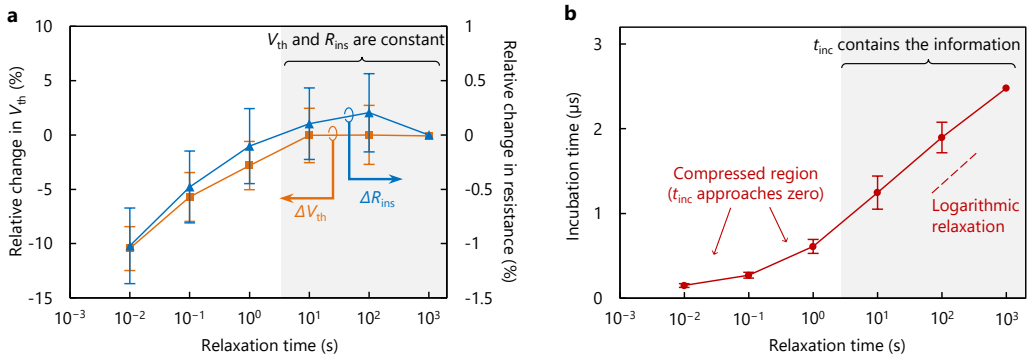

Fig. 4.13 | Evaluation of threshold voltage, resistance, and the incubation time of a VO_2 switch. a, IMT threshold voltage and resistance of 1-µm-long channel VO_2 switch were measured at different relaxation times. Both parameters show similar trends, although the change in the threshold voltage is ten times larger than that of the resistance. Both parameters stabilize at in a few seconds and do not show logarithmic relaxation. We note that the MIT threshold voltage was totally independent from the relaxation time. **b,** Measured incubation revealed the information of previous switching events when the threshold and resistance are constant. Each data point corresponds to at least 20 measurements (error bars defined) with the exception of the T = 1000 s where we collected three data points. The results show that the memory effect embedded in the incubation time is independent from the changes in the threshold voltage and the resistance of the channel.

4.5 Structural glass-like features of the memory effect

To identify the origin of the observed memory effect in VO_2, we examined whether electronic states could be responsible for our observation. We evaluated the memory effect under a continuous-wave (CW) laser pumping with relatively high energy photons (2.33 eV), larger than the material band gap [248]. The measurements under laser excitation show a considerably higher conductivity with respect to those under dark, however, the memory effect is not affected (Fig. 4.14a-b). This observation does not support scenarios that explain the memory effect based on excitation of electronic states, such as orbital switching [249] or trapped carrier in defects, because the laser light continuously reshuffles the electronic state occupancies. In fact, logarithmic or stretched exponential relaxations are quite slow processes for electronic states, nevertheless, such long relaxation times are one of the main features of glassy states with configurational transitions [250]. The IMT in VO_2 is a structural switching, and therefore, slow glass-like configurational changes driven by bond lengths or vacancies could be a possible explanation. These are scale-less processes which is consistent with the results presented in Fig. 4.12.

To investigate the possible scenario of a glass-like structural relaxation, we evaluated the memory effect at elevated temperatures to examine an important feature of glasses: the system becomes more mobile

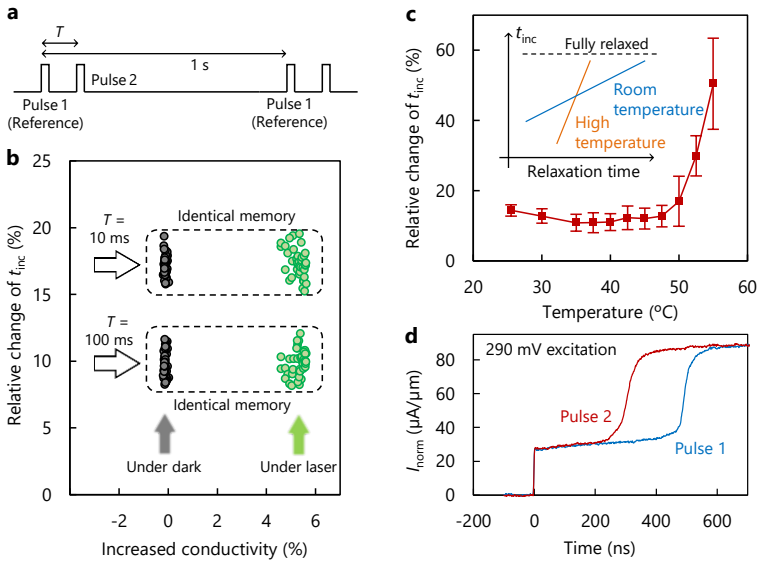

Fig. 4.14 | Evidence of glass-like dynamics. a, Illustration of excitation signal of a VO_2 switch for measurements under laser light. Every second, two identical pulses with the time separation T are applied to the device and incubation times are monitored (t_{inc}^{ref} and t_{inc}, respectively). **b,** Relative change in the incubation time ($(t_{inc} - t_{inc}^{ref})/t_{inc}^{ref}$) versus increased insulating-state conductance in a 200-nm-long channel VO_2 switch. Measurements under a continuous-wave 532-nm laser light with ~100 W cm^{-2} power density show a considerably higher conductivity, however, the memory effect is unchanged for both different relaxations times T = 10 ms and 100 ms. The experiment shows that memory effect is likely structural and not electronic. **c,** Relative change in the incubation time after T = 10 ms with respect to reference pulses with relaxation time of T = 1 s at different temperatures. The more pronounced change in t_{inc} when the temperature becomes close to the IMT temperature indicates a faster relaxation (inset). **d,** Transient current density of the VO_2 switch corresponding to two consecutive triggering with V_{set} = 290 mV at chuck temperature of 55 °C. The results show a notable change in t_{inc} close to the IMT.

close to the transition temperature [251]. In this case, an excitation signal can more easily perturbate the system, and the system relaxes faster after removing the excitation. To examine this feature, we monitored the change in incubation times between periodic pulses with separation of 1 s (reference pulses) and pulses with separations of 10 ms over a temperature sweep from room temperature to 55 °C (Fig. 4.14a). At each temperature, we set the excitation amplitude to result in t_{inc} = 500 ns for the reference pulse and monitored the incubation of the second pulse. We observed a much more pronounced change in the incubation times close to the IMT (Fig. 4.14c-d). This difference in the incubation times is proportional to the slope of t_{inc} over relaxation time (for example 78 ns/dec in Fig. 1c). Therefore, our results show a faster relaxation at higher temperatures (inset of Fig. 4.14c) which is an important feature of glass-like systems.

Glass transitions are also reversible (which is analogous to the results presented in Fig. 4.2f) and can undergo new phase paths if they are heated before a complete relaxation, which can explain the capability of electrical manipulation in the VO_2 switches (Fig. 4.6). It should be noted that the identical memory effect under vacuum of 10−4 mbar, which shows that such off-stoichiometric mechanism must be purely configurational, without any exchange with the ambient. Even though more investigations may be needed to identify in-depth the microscopic details of this process, the observed effect certainly shares important features of glasses, thus can be considered as glass-like dynamics. In this case, the state of a glass-like system is controlled and read electrically.

4.6 Potential applications in computation and data storage

The concept of electrically accessible glass-like dynamics can offer opportunities in electronics. An important aspect of the observed effect is that, at constant amplitude, t_D is proportional to the energy required to activate IMT. Therefore, the history of a device determines the switching energy barrier (E_{bar}) in the future: the higher the number and frequency of switching events, the lower the energy barrier (Figs. 4.15a-b). One can model E_{bar} at $t = t_0$ in the transient regime after n pulses occurring at t_k ($1 \le k \le n$) by

$$E_{\mathrm{bar}} = E_0 - E_1 \ln\left(\sum_{k=1}^{n} \frac{T_0}{t_0 - t_{\mathrm{k}}}\right), \tag{4.1}$$

where E_0 is the energy barrier of the device which is relaxed for $T = T_0$, and E_1 is a constant. The second term in the right hand side of the equation represents the reduced energy barrier due to the film history. Equation (4.1) captures the dynamic changes in the t_{inc} both for uniform (Fig. 4.15a) and non-uniform pulse patterns (see Appendix B). This functionality can enable highly dynamic classifiers with a computation-free training, which cannot be achieved in classic classifiers based on nonlinear resistive elements [252]. To show this, we can consider a neural network with one hidden layer, in which a VO_2 switch has been placed between each two nodes (Fig. 4.15c). At time t, the network can be fully described by matrices $E_{\mathrm{bar}}^{\mathrm{A}}(i,j,t)$ and $E_{\mathrm{bar}}^{\mathrm{B}}(j,k,t)$ representing the reduced energy barrier of A_i-X_j and X_j-B_k switches, respectively. The product of these two matrices corresponds to the correlation between inputs and outputs, enabling an energy-based classification: for each set of inputs, the output with the minimum energy required for IMT triggering at the interconnections will be activated.

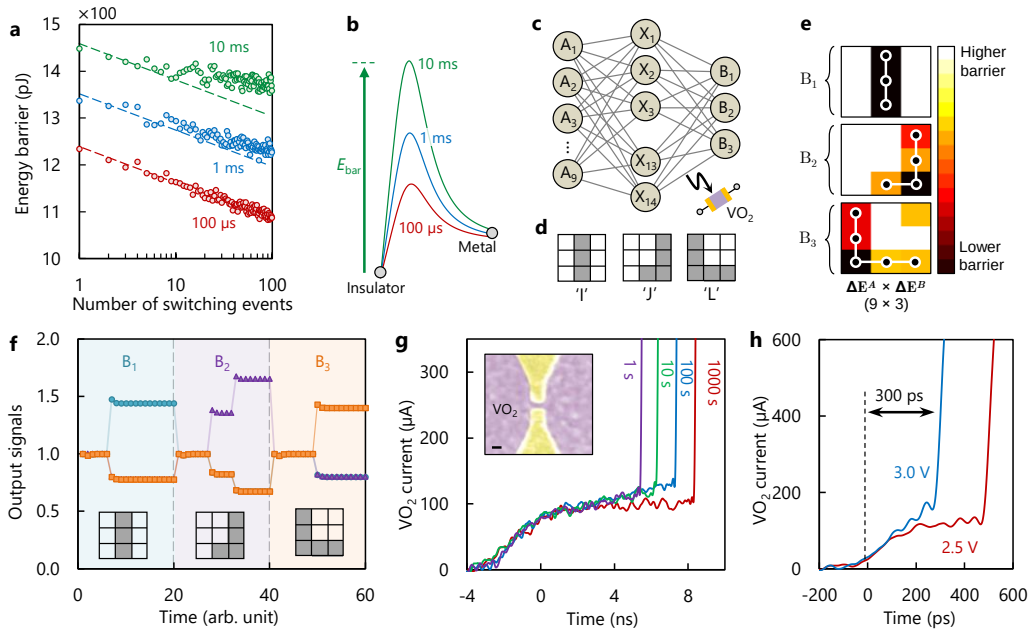

Fig. 4.15 | Electrical control of glass-like dynamics for computation and data storage. a, Dynamic change in energy barrier (E_{bar}) of a 2-µm-long VO_2 switch with the number of switching events for different pulse separations. **b,** Schematic showing that shorter pulse separations result in a lower E_{bar}. **c,** Considered neural network. A VO_2 switch is placed in the interconnection between each two nodes. ΔE^A and ΔE^B matrices represent the reduced energy barriers corresponding to A_i-X_j and X_j-B_k interconnections. **d,** Labels used to train a 3 × 3 pixel network for image classification. **e,** Post-training $\Delta E^A \times \Delta E^B$ matrix represents the effective reduced energy barrier corresponding to each output. **f,** Output signals at the three nodes B_1 (circles), B_2 (triangles), and B_3 (squares). Exposing the network to the inputs and monitoring the output currents successfully classifies the samples. **g,** Measured current of a VO_2 nano-device with different memories showing the potential of glass-like relaxation for ultra-scaled memory devices. The inset shows the false-colored scanning microscope image of the VO2 switch. The scale bar correspond to 100 nm. **h,** Measured current of a VO_2 nano-device with different memories showing the potential of glass-like relaxation for ultrafast memory nano-devices (V_{set} = 2 V). The inset shows the false-colored scanning microscope image of the VO_2 switch. The scale bar correspond to 100 nm. **h,** Measured current of the VO_2 nano-device (represented in the inset of part **g**) excited with V_{set} = 2.5 V (red line) and V_{set} = 3.0 V (blue line), showing that electrically induced memory can take place in sub-nanosecond time scales.

This concept provides two important features. First, training of the network can be done purely based on hardware. There is no need for calculation of weights and also no need to physically induce them, for example to manipulate the resistivity of elements [252]. We show this feature in classification of three characters "I", "J", and "L" provided in 3×3 pixels (Fig. 4.15d). Application of electric currents to the input nodes (A_i) corresponding to each image label, and grounded the equivalent output, can simply train the network. For example, to train the shown network with sample "J", the input nodes A_2, A_4, A_7, A_8, and A_9 are activated and B_2 is grounded, while all other nodes are floating. This reduces the energy barrier for some of the pathways connecting each set of inputs to the corresponding output. Fig. 4.15e illustrates the $E_{\mathrm{bar}}^{\mathrm{A}} \times E_{\mathrm{bar}}^{\mathrm{B}}$ matrix with a color map, representing the effective reduced energy barrier from inputs to outputs. For example in case of sample "J", the nodes A_2, A_4, A_7, A_8, and A_9 have a lower energy barrier to fire IMTs towards output B_2 (corresponds to "J"). In this case, if one activates the above-mentioned nodes, a higher current will be collected in node B_2. This approach yields a

Table 4.1 | Comparison between the structural state-based memory and other technologies

Parameter	Glass-like memory	Memristor	SRAM	DRAM	Flash	Disk
Density (F^2)	< 4	4	120 – 200	6 – 12	4 – 6	2/3
Operating voltage (V)	290 mV*	Nonmetric bipolar, ~2	3.3 – 5	3.3	3.3 – 5	5 – 12
Energy / bit (pJ)	≲ 0.1	0.1 – 3	~0.1	2	10000	>10,000,000
Read time (ns)	~10	10 – 100	10 – 30	10 – 50	25,000	~10,000,000
Write time (ns)	~1	~10	13 – 95	10 – 50	200,000	~10,000,000
Retention time	> 2 hr	100 s to years	Power sup.	4 – 64 ms	Years	Years

* Record for elevated temperatures. The concept is operational for voltages below 1 V at room temperature.

successful classification of the characters (Fig. 4.15f). The second feature provided by a glassy neural network is its self-tuning capability. The system is operational after an initial training, however, it fine tunes itself as it is exposed to the classification samples, because each sample would induce switching events at the correct nodes, reducing their energy barriers. This can self-optimize the network during the classification process, only relying on a small training set.

The concept of electrically-accessible glass-like states can also enable high-performance data storage platforms (Table 4.1). This is because the triggering process is fast, the relaxation is quite slow, and the manipulation capability enables storing multi-bits on a single physical bit. In addition, the memory effect can be accessed at very low voltages (≪ 500 mV) which is beneficial for energy efficient electronics [11] (Fig. 4.15d). Furthermore, the concept – relying on two-terminal devices – is compatible with a cross-bar configuration which offers extremely high data-storage densities [95]. The inset of Fig. 4.15g shows a 50 nm × 200 nm VO_2 nano-switch, in which the device history can be read in sub-10 ns (Fig. 4.15g). The writing process (triggering the IMT which induces the memory) can take place in sub-nanosecond time scales with low energy cost ~100 fJ (Fig. 4.15h). We note that a considerable portion of the measured current in the device shown in the inset of Figs. 4.15g-h is from fringing current that can be eliminated by defining a mesa region around the device. Therefore, the writing energy cost can go well below 100 fJ. In addition, the demonstration of the memory effect in four-terminal cross structures open possibilities in implementations for computational and memory devices. For neural networks, the vertical direction (Fig. 4.10a) can be considered as the signal propagation path and the device can be programmed through independent horizontal terminals. For memory devices, this four terminal configuration enables reading and writing process to take place from different ports.

4.7 Conclusion

This chapter demonstrated electrically accessible glass-like dynamics in VO_2 that can be excited in sub-nanosecond time scales and monitored during several orders of magnitudes in time, from sub millisecond to hours. A two-terminal or multi-terminal switch undergoes complex but fully reversible dynamics, induced by a series of excitations. From a technological point of view, the presented results show that the response of these structural dynamics to a sequence of excitations can enable new schemes for data storage and processing. The proposed functional devices can potentially meet some of the continuous demands in electronics such as downscaling, fast operation, and decreasing the voltage supply level. From a physical point of view, the results revealed extremely long memories in VO_2 that can be only revealed by the incubation time. Monitoring the incubation times as a sensitive measure nano-scale lattice and electronic phases can set the stage to study out-of-equilibrium phase dynamics in other material systems.

5 Mitigating the efficiency-frequency trade-off in power electronics: the role of C_{OSS} losses

The two first parts of this thesis focused on new device technologies for high-speed radiofrequency and logic electronics. Several high-frequency measurement schemes were presented to evaluate the performance of the proposed devices. Such measurement methods are often used to characterize high-frequency devices. In the last part of the thesis, we show how some of these methods can be used to measure important properties of power devices. In particular, this part of the thesis focuses on new methods to characterize output capacitance losses in power transistors, which is currently a major limitation on increasing the frequency and reducing the size of power converters.

5.1 C_{OSS} losses in power transistors: a brief history

Increasing the switching frequency of power devices directly reduces the energy storage requirements of power converters, which in principle enables their downscaling [253]. To achieve dramatic increases in switching frequency, it is necessary to mitigate frequency-dependent device loss mechanisms including switching loss and gating loss [120]. There are well-known circuit-level solutions to do so. Zero-voltage switching [16] are used to reduce capacitive discharge loss and voltage/current overlap losses at the switching transitions, and resonant gating [254] can diminish losses resulting from charging and discharging device gates. Other than these two types of *classic* frequency-dependent losses, researchers have found anomalous non-recoverable energy loss associated with high-frequency charging and discharging the output capacitance of power devices, which are intrinsically linked to the device and cannot be diminished by modifying the power circuits.

The non-recoverable energy loss in the output capacitance of power transistors was observed for the first time for Si Superjunction (SJ) devices. The SJ device concept can significantly reduce the conduction losses, and therefore, it is a strong candidate to realize highly efficient power

converters [255]. However, in 2014, Fedison and his colleagues observed higher-than-expected energy loss in the output capacitance of these power devices [256]. Interestingly, the more advanced devices (the ones with lower specific ON resistance) exhibited higher unexpected losses. Two years later, in 2016, Fadison and Harrison reported that the large-signal C_{OSS} of SJ devices show a large hysteresis [257]. Followed by these observations, there has been numerous studies to measure [258]-[260] and microscopic model of such losses [261]-[263] to ultimately mitigate them.

The lower-than-expected efficiencies in soft-switching power converters based on wide-band-gap (WBG) transistors, again initiated investigations on C_{OSS}-losses [130]. Zulauf *et al.* characterized C_{OSS} charging/discharging energy dissipation (E_{DISS}) in GaN transistors using Sawyer Tower (ST) method, where the results showed frequency-dependent losses [132]. Guacci *et al.* used a thermal approach to study C_{OSS}-losses in GaN transistors and observed dv/dt-dependent energy dissipation [135]. The ST-based E_{DISS} measurement of some of the commercial SiC transistors, however, presented a weak dependence on frequency and dv/dt [134].

Although several measurements showed an effect from voltage-swing, frequency and dv/dt on C_{OSS} -losses in SiC and enhancement-mode GaN transistors, the dependence of E_{DISS} on these parameters is still not clear [135]. Zulauf *et al.* [134] used the empirical relation

$$E_{\mathrm{DISS}}^{\mathrm{Ref\ [1]}} = k \cdot f^{\alpha} \cdot V^{\beta}, \tag{5.1}$$

to fit the experimental data, where f is the frequency, V is the charging voltage, and k, α, and β are constants. For some of the evaluated transistors, values of $\alpha < 1$ and $\beta < 2$ were obtained [264]. Although curve fitting from large-signal measurements shows the behavior of C_{OSS}-losses, it requires excessive experiments with high-voltage and high-frequency power amplifiers at several operation points at different voltages and frequencies. Moreover, the need for a high-voltage RF power amplifier (PA) can severely limit the maximum voltage and frequency applied to the device under test (DUT).

This chapter aims to propose new measurement methods to meet the high-frequency and high-dv/dt requirements for GaN devices. These techniques reveals new aspects of C_{OSS} losses in wide-band-gap power transistors, and set the stage for on-wafer evaluation of such non-recoverable soft-switching losses.

5.2 Nonlinear resonance technique: capturing C_{OSS} losses in nanosecond time scales

Sawyer-Tower is a typical electrical measurement method used to evaluate large-signal output capacitance of transistors and diodes [266]. In this method, the gate and source of the transistor are shorted to turn OFF the device, and a high-amplitude sinusoidal waveform is applied to the series connection of the device under test (DUT) and a reference linear capacitor (C_{REF}). The stored charge in the C_{OSS} of the transistor is assumed to be equal to the charge stored in the reference capacitor. This assumption is valid when the leakage current in DUT is much smaller than the displacement current, otherwise it may lead to the observation of spurious hysteresis [267]. The choice of C_{REF} is crucial in the ST method, since it depends on the range of interest for C_{OSS}, which however has a significant nonlinearity leading to a variation by a few orders of magnitude when changing drain-to-source bias.

As a result, a fixed value of C_{REF} is not always suitable to capture such large nonlinearity. Another major limitation of the ST method, is that the measurements are performed in steady-state regime. In case of devices with C_{OSS} hysteresis, the junction can significantly heat up due to hysteresis losses, which could potentially affect the measurement accuracy. For instance, the leakage current is much larger at higher temperatures, and can become comparable to the displacement currents in C_{OSS} and C_{REF}, resulting in an incorrect C_{OSS} measurement [267]. Another restriction caused by any steady-state measurement is the limitation of voltage-swing/frequency applied to the DUT before thermal runaway [135]. In addition, the need for high-amplitude sinusoidal voltage source in the ST method constrains the maximum voltage and frequency that can be applied to characterize large-signal C_{OSS}, and the typical values of dv/dt in switching transients, especially for GaN transistors, can only be achieved at very high frequencies, in the range of tens of megahertz [135].

In this section we present a simple and robust measurement method to capture large-signal C_{OSS} as well as C_{OSS} energy dissipation during a single charging/discharging process (E_{DISS}). The method works based on the nonlinear resonance between a pre-calibrated inductor and the output capacitance of the DUT. By changing the circuit parameters, it is possible to tune the dv/dt (above 100 V ns^{-1}), frequency (above 40 MHz), and the voltage swing (above 1 kV), even though the method relies only on a low-voltage DC source, without the need for RF power amplifiers. In addition, large-signal C_{OSS} as well as E_{DISS} can be measured in steady-state regime as well as under a single pulse condition, which eliminates the effect of self-heating from the measurement, and does not thermally limit the maximum voltage swing, frequency, and dv/dt applied to the DUT.

Fig. 5.1a illustrates the proposed circuit for large-signal C_{OSS} and E_{DISS} measurement. The transistor M is ON for $t < t_0$, charging the inductor L with the current I_0. By turning OFF the transistor at $t = t_0$, the inductor resonates with C_{OSS} and the parasitic capacitances C_{par}. This results in the generation of a pulse with an amplitude V_{max} at the output node. By measuring the drain-source voltage waveform (v_{DS}), and knowing the values of L and C_{par}, one can simply extract large-signal C_{OSS} as well as E_{DISS}. The circuit has a high step-up which enables to probe C_{OSS} and E_{DISS} at very large voltages. It is important to note that the resonant nature of the circuit guarantees lossless soft switching at $t = t_0$. In addition, the losses related to the internal gate resistance of transistor and the sink resistance of the gate driver are negligible. The governing equation of the circuit shown in Fig. 5.1a is

$$LC(v_{DS})\frac{\mathrm{d}v_{DS}}{\mathrm{d}t} = LI_0 - \int_{t_0}^{t} v_{DS}(t)\,\mathrm{d}t, \tag{5.2}$$

where $C = C_{OSS} + C_{par}$ is the total nonlinear voltage-dependent capacitance at the output node. When v_{DS} peaks at $t = 0$, the inductor has zero current, so the inductor flux ($\varphi = LI_0$) can be calculated by integration of its voltage. Since $v_{DD} \ll v_{DS}$:

$$LI_0 = \int_{t_0}^{0} v_{DS}(t)\,\mathrm{d}t. \tag{5.3}$$

Replacing (5.3) into (5.2), yields

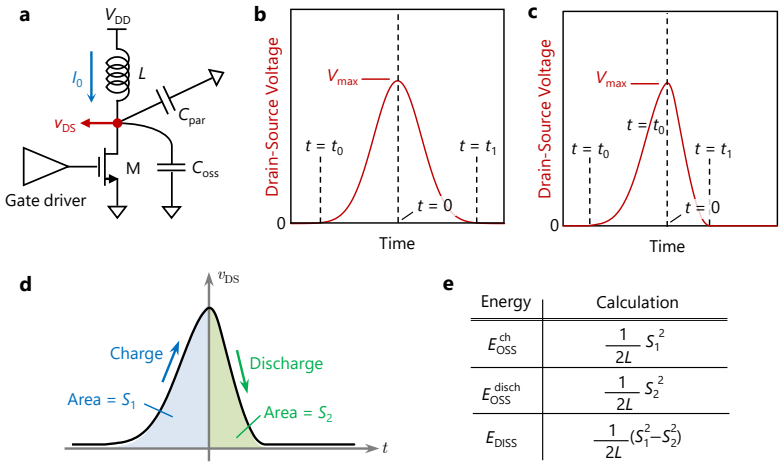

Fig. 5.1 | Nonlinear resonance method to capture large-signal C_{oss} and C_{oss} losses. a, The circuit, and samples for v_{DS} voltage waveforms for devices with **b,** lossless and **c,** lossy C_{OSS} charging/discharging processes. **d,** Areas below v_{DS} waveform for charging (S_1) and discharging (S_2) processes translates to **e,** C_{OSS} charging/discharging energies as well as the dissipated energy E_{DISS}.

$$C(v_{DS}) = \frac{\int_{t_0}^{0} v_{DS}(t)\,\mathrm{d}t - \int_{t_0}^{t} v_{DS}(t)\,\mathrm{d}t}{L\dfrac{\mathrm{d}v_{DS}}{\mathrm{d}t}}. \tag{5.4}$$

Equation (5.4) presents the expression of the capacitance C exclusively as a function of v_{DS}. The inductance value of L in the denominator of (5.4) should be properly measured to accurately extract the large-signal C_{OSS}. It should be noted that v_{DS} starts from 0 at $t = t_0$, increases to the maximum value of V_{max} at $t = 0$, and then again, decreases to 0. This results in a double-sweep large-signal measurement of output capacitance for each pulse. In the case of devices without C_{OSS} hysteresis, the measured v_{DS} has a symmetric waveform (Fig. 5.1b), while devices with C_{OSS} hysteresis present a non-symmetric waveform (Fig. 5.1c).

Equation (5.4) can be used to calculate the energy transferred to (or recovered from) C_{OSS} during a time interval T

$$E_T = \int_T v_{DS} C(v_{DS})\,\mathrm{d}v_{DS}. \tag{5.5}$$

After replacing (5.4) into (5.5), the C_{OSS} charging ($T = [t_0,0]$) and discharging ($T = [0,t_1]$) energies can be extracted as

$$E_{OSS}^{ch} = \frac{1}{2L}\left(\int_{t_0}^{0} v_{DS}(t)\,\mathrm{d}t\right)^2 \tag{5.6}$$

and

$$E_{\mathrm{OSS}}^{\mathrm{disch}} = \frac{1}{2L}\left(\int_0^{t_1} v_{\mathrm{DS}}(t)\,\mathrm{d}t\right)^2 \tag{5.7}$$

respectively. The difference between (5.6) and (5.7) gives the energy dissipated in C_{OSS}

$$E_{\mathrm{DISS}} = \frac{1}{2L}\left(\left(\int_{t_0}^{0} v_{\mathrm{DS}}(t)\,\mathrm{d}t\right)^2 - \left(\int_0^{t_1} v_{\mathrm{DS}}(t)\,\mathrm{d}t\right)^2\right) \tag{5.8}$$

Figs. 5.1d and 5.1e depict the correspondence of the C_{OSS} charging/discharging/dissipated energies to the areas below the v_{DS} curve. This makes the method numerically convenient since it just relies on the integration of a single voltage waveform, which can be accurately measured even at ultra-fast charging/discharging cycles, even below 10 ns. It should be noted that the use of a high-Q inductor L leads to negligible deformation of v_{DS} waveform, even below the measurement accuracy of typical oscilloscopes.

We demonstrate the applicability of the proposed method for large-signal C_{OSS} measurement as well as to extract E_{DISS} for different transistors (listed on Table 5.1). Fig. 5.2a shows the experimental set-up with different test boards compatible with different transistor packages. The captured v_{DS} and v_{GS} waveforms verify the soft switching in the circuit since the transistor turns OFF (v_{GS} = 0) before building-up the v_{DS} voltage. A test board with 1-mH inductor is shown in Fig. 5.2b. The impedance of the employed inductor was measured using a Keysight E4990A impedance analyzer, as shown in Fig. 5.2c.

Based on this measurement, we extracted and de-embedded the parasitic capacitance of the inductor (inset of Fig. 5.2c). The results for M1 (SiC) and M2 (Si SJ) using 1-mH inductor, shown in Figs. 5.3a and 5.3c, respectively, illustrate the shape of the v_{DS} pulse for these two transistors, which translates into large-signal C_{OSS} (Figs. 5.3b and 5.3d, respectively). The obtained large-signal C_{OSS} were verified with

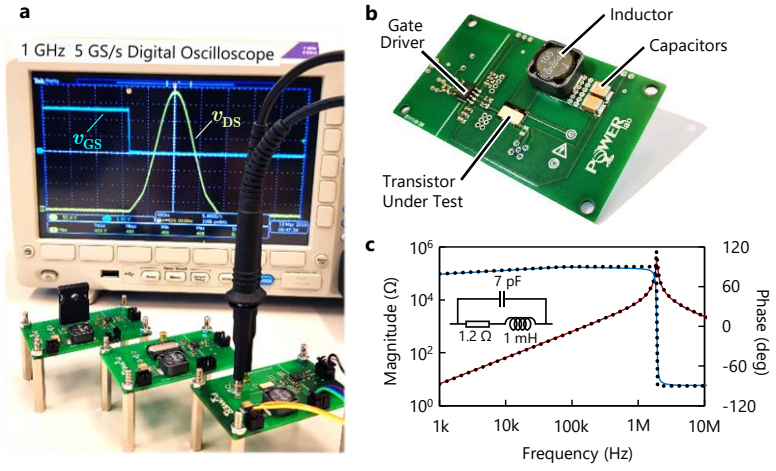

Fig. 5.2 | Implementation of the Nonlinear resonance method. a, Photographs of the experimental set-up. **b,** Photographs of the a nonlinear resonance test board. **c,** Measured (solid lines) and modeled (dotted lines) impedance of a 1-mH inductor. The inset shows the equivalent circuit model of the inductor.

Table 5.1 | Specifications of the evaluated transistors using Nonlinear resonance method

No.	Technology	Voltage/Current Ratings		Reported E_{OSS} at 400 V (μJ)
		Voltage (V)	Current (A)	
M1	SiC	0650	93	22.0
M2	Si SJ	0650	60	17.5
M3	SiC	0900	36	08.5
M4	GaN	0650	65	15.5
M5	GaN	0650	65	07.0

ST method performed at 300 kHz (dashed lines in 5.3b and 5.3d). It should be noted that although the measurements were done at V_{max} = 100 V, the supply voltage v_{DD} was very small, e.g. v_{DD} = 100 mV in Fig. 5.3a.

The large values of inductor L result in relatively small resonance frequencies, *e.g.* 300 kHz for M1 (SiC) in Fig. 5.4a, however, much higher frequencies and dv/dt values can be obtained with smaller inductors. Fig. 5.4b shows measurement results for M2 (Si SJ) with a 500-nH air-core inductor. By changing the small voltage v_{DD}, the peak voltage V_{max} was tuned at 250 V, 450 V, and 650 V. Fig. 5.4c shows the

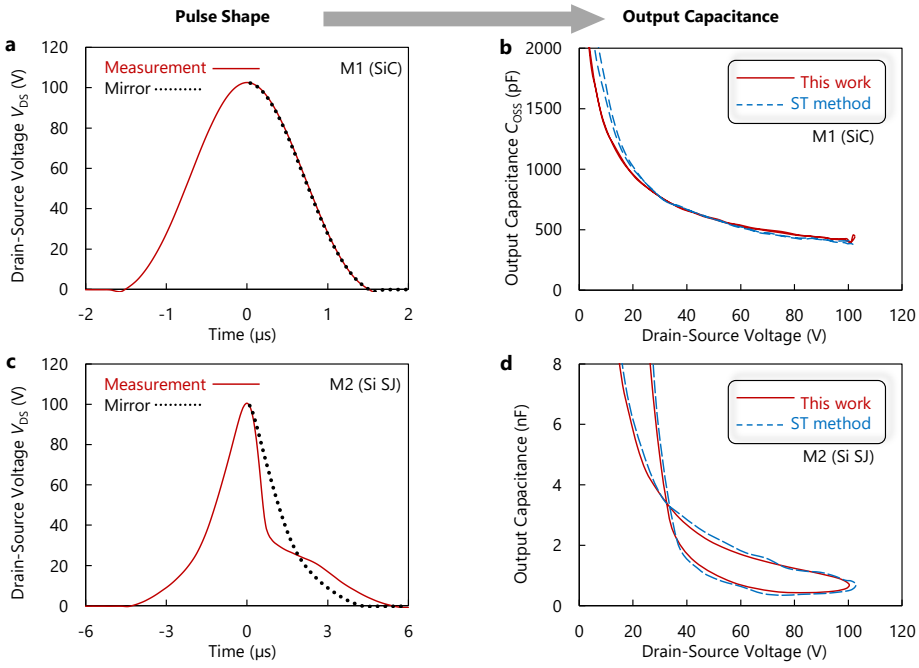

Fig. 5.3 | Validation of the Nonlinear resonance method. a, Measured v_{DS} (solid line) and mirrored waveform (dotted line) for M1. **b,** Extracted C_{OSS} for M1 using the proposed method (solid line) and by ST method (dashed line). **c,** Measured v_{DS} (solid line) and mirrored waveform (dotted line) for M2 shows a non-symmetrical charging/discharging process. (d) Extracted COSS for M1 using the proposed method (solid line) and by ST method (dashed line).

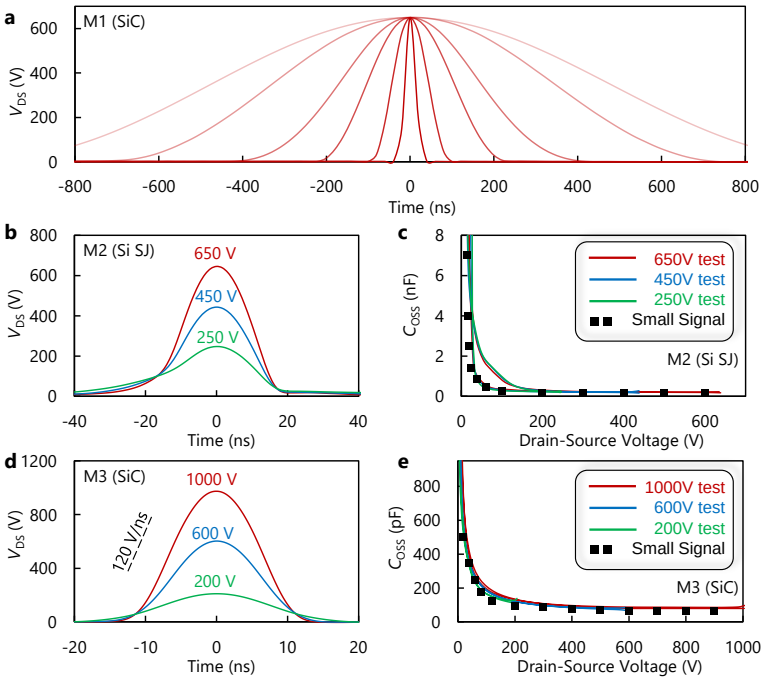

Fig. 5.4 | High d*v*/d*t* operation of the Nonlinear resonance method. a, Measured v_{DS} for M1 using different values of *L* showing the possibility of capturing large-signal C_{OSS} and E_{DISS} at very frequencies. (b) Measured v_{DS} for M2 at V_{max} = 250 V, 450 V, and 650 3V, and (c) the corresponding large-signal C_{OSS}. (d) Measured v_{DS} for M3 at V_{max} = 200 V, 600 V, and 1000 V, and (e) the corresponding large-signal C_{OSS}. Discrete points show small signal C_{OSS} reported in datasheets.

extracted large-signal C_{OSS}, presenting considerable hysteresis loops. The reported small-signal C_{OSS} from the device datasheet (discrete points in Fig. 5.4c) closely match the extracted large-signal C_{OSS} in the discharge cycle.

The method is capable of being performed at high voltage levels. Fig. 5.4d shows the measured v_{DS} waveforms with L = 500 nH at three different voltage 200 V, 600 V, and 1000 V, and the corresponding large-signal capacitances are shown in Fig. 5.4e. For the 1000 V measurement, a resonance frequency of 40 MHz and d*v*/d*t* of 120 V/ns show the potential of the method in operating at very high frequencies and amplitudes, at the same time, without the risk of thermal runaway. To put these numbers in perspective, with the same measurement specifications for a device with an output capacitance of ~100 pF, the amplifier in the ST method would require to provide ~3 kVA of reactive power at 40 MHz.

5.3 Large signal C_{oss} losses in Cascode and enhancement-mode GaN devices

The use of GaN-on-Si HEMTs in high-frequency converters is rapidly growing, due to their outstanding features such as low R_{ON} and small gate charge. Unexpected losses in soft-switched GaN-based power converters initiated studies on C_{OSS} losses in these devices. Figs. 5.5a and 5.5b show the measured voltage waveforms over a cascode GaN transistor (M4), at low and high d*v*/d*t* values, respectively. At 150-V tests, the generated v_{DS} waveforms are almost symmetrical for both low and high d*v*/d*t* tests. At a higher voltage V_{max} = 650 V, however, there is a significant asymmetry in both waveforms. Fig. 5.5c

presents the extracted large-signal C_{OSS} for V_{max} = 150 V, 350 V, and 650 V, showing that the hysteresis loop becomes drastically larger at higher voltages. This indicates a fundamentally different loss mechanism than that in SJ devices, since the device becomes significantly lossy at high voltages. The extracted E_{OSS} and C_{OSS} losses at different voltage levels are shown in Figs. 5.5d. The significant increase in C_{OSS} losses appearing for v_{DS} > 250 V, is in agreement with the previously measured C_{OSS} losses for cascode GaN devices [132].

The extracted E_{DISS} based on the proposed method, were verified with thermal method and ST measurements performed at a wide range of different frequencies from 10 kHz to 300 kHz. The agreement between E_{OSS} reported in datasheet (dashed line in Figs. 5.5d) and the extracted E_{OSS} from (5) (Δ in Figs. 5.5d) is another indication of the accuracy of the proposed method. At the highest test voltage of 650-V, 26% of E_{OSS} is dissipated during charging and discharging processes. Although dv/dt-dependent losses have been observed in some of the advanced GaN HEMTs [132], [135], as it can be seen in Figs. 5.5a and 5.5b, the proposed method did not show any significant difference for different values of dv/dt for the cascode GaN device M4, which opens opportunities for further investigation of these effects on different devices.

We also used the Nonlinear resonance method with drain-source current measurement to evaluate a GaN HEMT (M5). Figs. 5.6a and 5.6b, respectively show measured v_{DS} and i_L waveforms for the

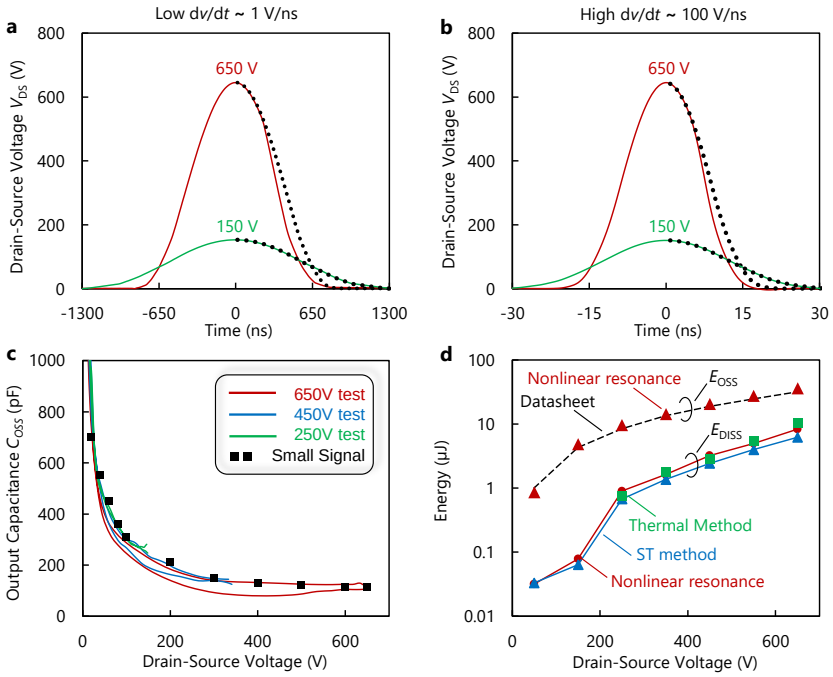

Fig. 5.5 | Anomalous C_{OSS} losses in a cascode GaN transistor. a, Low and **b,** high dv/dt measurements with L = 1 mH and L = 500 nH inductors, respectively. The mirrors (dotted lines) show symmetry at low voltage tests (150 V) and non-symmetry at high voltage tests (650 V). Large signal C_{OSS} and E_{DISS} are not functions of dv/dt in this GaN transistor. **c,** Extracted large signal C_{OSS} for V_{max} = 150 V, 350 V, and 650 V. The device exhibits a large frequency-independent hysteresis for voltages greater than ~300 V. **d,** Extracted losses from the proposed technique, validated with ST and thermal method.

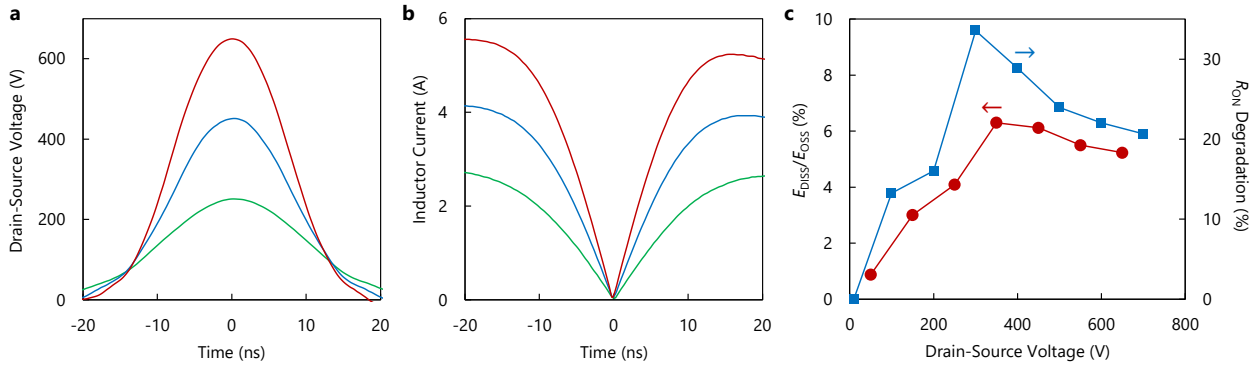

Fig. 5.6 | Possible correlation between C_{OSS} losses and R_{ON} degradation in GaN HEMTs. a, Measured v_{DS} at three different voltage levels for an enhancement-mode GaN HEMT (M5) together with (b) current waveforms. (c) Extracted E_{DISS} and measured ON resistance degradation. The results show a possible correlation between C_{OSS} losses and R_{ON} degradation suggesting an identical microscopic origin for both effects.

enhancement-mode transistor. The extracted C_{OSS} energy dissipation, as well as R_{ON} degradation (measured with AMCAD pulsed IV system) are shown in Figs. 5.6c. The R_{ON} degradation rises until 300-V and then it becomes smaller. Such effect has been previously observed [268]. Interestingly, the percentage of C_{OSS}-losses also decreases at almost the same voltage, suggesting a possible relationship between these two effects [135].

5.4 Small-signal approach to predict large-signal C_{OSS} losses in wide-band-gap transistors

A. Description

This section aims to propose a small-signal modeling approach to extract large-signal C_{OSS}-losses of WBG transistors on a wide range of operation points. The device is simply modeled by a nonlinear capacitance C_{OSS} in series with a frequency-dependent resistance R_S. This modeling decouples the frequency and voltage dependence of losses, enabling to solve a large-signal problem with a small-signal approach. Using an impedance measurement to measure values of R_S at different frequencies, together with the presented output capacitance versus voltage from datasheets, we present a general relationship for C_{OSS}-losses in different voltages and frequencies. As a result, just one simple small-signal measurement (instead of several different measurements in large-signal methods) leads to a general view of the C_{OSS}-losses. The method does not suffer from some of the shortcomings of large-signal measurements such as limitation in applied voltage/frequency (*e.g.* due to power amplifier), or signal distortion at high-frequencies. The proposed method gives insights on dependence of E_{DISS} on frequency, voltage, and dv/dt value.

Fig. 5.7a shows a model for output capacitance of transistors, including a nonlinear capacitance C_{OSS} in series with resistance R_S and in parallel with resistance R_P, representative for losses at high and low frequencies, respectively. The quality-factor (Q-factor) of output capacitance can be defined as [see Figs. 5.7b and 5.7c]

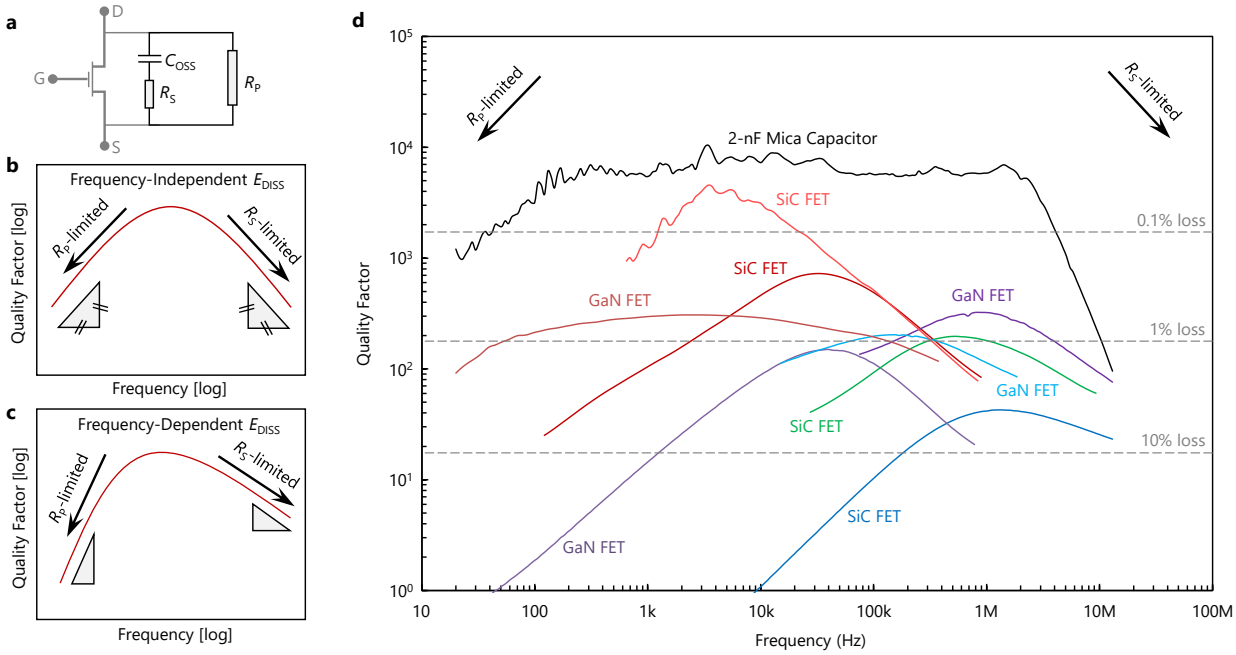

Fig. 5.7 | Small-signal modeling of frequency-dependent C_{OSS} losses. a, Circuit model for output capacitance of transistors. Quality-factor versus frequency for transistors with **b,** fixed, and **c,** frequency-dependent R_S and R_P. **d,** Measured quality-factor of C_{OSS} of different commercial WBG transistors versus frequency at V_{DS} = 40 V. The gate and source of transistors were shorted (C_{OSS} = C_{DS} + C_{GD}).

$$Q = \frac{1}{R_S C_{OSS}\omega + (R_P C_{OSS}\omega)^{-1}} \tag{5.9}$$

The effect of R_P (mainly corresponding to the leakage current) is dominant at DC, while R_S significantly contributes to the switching dynamics and C_{OSS}-losses. As illustrated in Fig. 5.7d, small-signal measurements show a considerable lossy behavior for C_{OSS} of WBG transistors. For instance, the levels of losses are considerably higher than a reference low-loss mica capacitor. The small-signal extracted values of losses for frequencies higher than 1 MHz, are in range of 1-10% which is in agreement with the previously measured large-signal losses [132], [134]. This indicates the possibility of evaluating large-signal losses with a proper small-signal modeling. Fig. 5.7d also shows that for frequencies higher than 1 MHz (which covers the switching bandwidth of WBG transistors), the Q-factor of all the considered transistors is limited by R_S.

For a linear capacitor with frequency-independent R_S and R_P, (2) fully describes the charging and discharging energy dissipation as

$$E_{DISS} = \frac{\pi}{2Q} E_{OSS} \tag{5.10}$$

where E_{OSS} is the total energy stored in C_{OSS}. In practice, however, C_{OSS} is nonlinear and R_S and R_P can change with frequency [see Fig. 5.7b and 5.7c]. The non-unity slope of the Q-factor versus frequency

for several different WBG transistors, shown in Fig. 5.7d (measured with Keysight E4990A impedance analyzer, with a very high accuracy), confirms the frequency-dependent nature of R_S and R_P.

We use the model presented in Fig. 5.7a to extract C_{OSS} charging /discharging energy dissipation. As mentioned, R_S is the origin of C_{OSS}-losses in switching dynamics, as R_P just limits the Q-factor at low frequencies. By applying voltage v(t) to the output capacitance, and considering R_S as a perturbation element, the power loss in R_S can be written as

$$P_{\text{loss}} = R_S(C_{OSS}\frac{\mathrm{d}v}{\mathrm{d}t})^2 \tag{5.11}$$

Assuming v(t) represents a switching transient from 0 to V, the total energy loss during a single switching transient time t_{SW} is

$$E_{\text{loss}} = \int_0^{t_{SW}} R_S(C_{OSS}\frac{\mathrm{d}v}{\mathrm{d}t})^2\mathrm{d}t \tag{5.12}$$

In a charging and discharging process, however, E_{loss} is dissipated two times (E_{DISS} = 2 E_{loss}). Considering a constant switching-speed dv/dt ≅ V/t$_{SW}$, which is very accurate for trapezoidal waveforms and also can be used for sinusoidal waveforms, we write

$$E_{DISS} = 2R_S(\frac{\mathrm{d}v}{\mathrm{d}t})\int_0^V C_{OSS}^2\,\mathrm{d}v \tag{5.13}$$

which clearly shows dv/dt-dependence of C_{OSS}-losses [132]. Equation (5.13) can be rewritten as

$$E_{DISS} = 2R_S(\frac{\mathrm{d}v}{\mathrm{d}t})VC_{OSS}^{\text{eff }2} \tag{5.14}$$

in which we introduced the new term which is the root mean square (rms) of C$_{OSS}$ from 0 to V, representing the average C$_{OSS}$ value that contributes to power dissipation in the device output capacitance

$$C_{OSS}^{\text{eff}} = \sqrt{\frac{1}{V}\int_0^V C_{OSS}^2\,\mathrm{d}v} \tag{5.15}$$

One can use f = 1/(2t_{SW}) to rewrite (5.13) as

$$E_{DISS} = 4R_S f V^2 C_{OSS}^{\text{eff }2} \tag{5.16}$$

Comparing (5.16) with the experimental model (5.1) reveals two main points:

1) α = 1 for a fixed and frequency-independent R_S, however, non-unity values of α have been reported in [132] and [264]. This agrees with the measurement results presented in Fig. 5.7d, showing frequency-dependent R_S.

2) The obtained values of β, extracted by curve fitting in [264], were always less than 2. This is in agreement with (5.16) since when rising the voltage V, the rms value of C_{OSS} decreases. As a result, although square of V is seen in (5.16), the C_{OSS}-related term leads to a β < 2.

B. Validation

Here we show how large-signal C_{OSS}-losses can be extracted from the small-signal model. This sub-section also validates the applicability of the proposed method to evaluate C_{OSS}-losses, by comparing the extracted E_{DISS} values with the ST method [132] ,[134]. The first step to extract the general relation of (5.16) is to obtain the effective C_{OSS}. This can be done by using data reported in datasheets. Figs. 5.8a and 5.8b show the reported C_{OSS} in datasheet of transistors M1 (36-A-rated SiC FET with R_{ON} = 80 mΩ) and M2 (30-A-rated e-mode GaN HEMT with R_{ON} = 50 mΩ), respectively. the effective C_{OSS} values were obtained using (5.15) [see Figs. 5.8a-b]. One can directly use these values, however, here we applied a curve fitting to obtain closed-form relations [dashed lines in Figs. 5.8a and 5.8b]:

$$C_{\mathrm{OSS}}^{\mathrm{eff}} = (2850\ \mathrm{pF}) \times (V\ [\mathrm{V}])^{-0.38} \tag{5.17}$$

and

$$C_{\mathrm{OSS}}^{\mathrm{eff}} = (2350\ \mathrm{nF}) \times (V\ [\mathrm{V}])^{-0.42} \tag{5.18}$$

for M1 and M2, respectively.

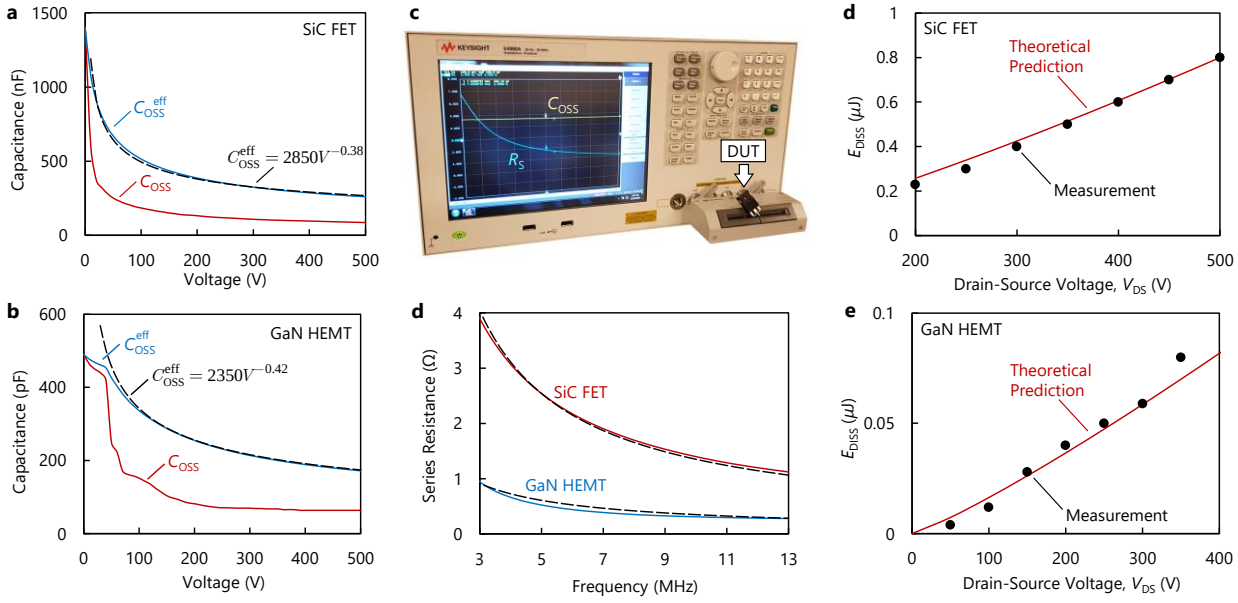

Fig. 5.8 | Verification of the small-signal model of frequency-dependent C_{OSS} losses. C_{OSS} versus drain-source voltage at 1 MHz reported in datasheet (red lines) as well as the extracted effective C_{OSS} (blue lines) for transistors **a,** M1 (SiC FET) and **b,** M2 (GaN HEMT). **c,** Photograph of the experimental set-up to measure R_S using a Keysight E4990A high accuracy impedance analyzer. **d,** Measured R_S versus frequency (V_{DS} = 40 V) for transistors M1 and M2. **e,** Predicted C_{OSS} losses based on (5.21) for transistor M1 (solid line) against large-signal measurement results (discrete points). **f,** Predicted C_{OSS} losses based on (5.22) for transistor M2 (solid line) against large-signal measurement results (discrete points). The level of losses in M1 and M2 are considerably different, showing the applicability of the proposed approach to extract C_{OSS} losses for a wide range of E_{DISS} values.

After extraction of the effective C_{OSS}, the series resistance R_S was measured using a Keysight E4990A impedance analyzer [see Fig. 5.8c]. The R_S, as a key element in C_{OSS}-losses, as a function of frequency is not typically reported by manufacturers in datasheets. Fig. 5.8d illustrates the R_S for transistors M1 and M2 (solid lines). Unlike C_{OSS}, which is strong function of voltage, R_S is almost constant with voltage; and therefore it can be assumed as linear parameter. On the other hand, C_{OSS} is not a function of frequency, while R_S is highly frequency-dependent [see Fig. 5.8d]. For M1 and M2 we have

$$R_S = (11\,\Omega)\times(f\ [\mathrm{MHz}])^{-0.91} \tag{5.19}$$

and

$$R_S = (2.2\,\Omega)\times(f\ [\mathrm{MHz}])^{-0.8} \tag{5.20}$$

respectively. It should be noted that the level of R_S, as the effective series resistance of C_{OSS}, is significantly higher than the device on-resistance (*e.g.* in GaN devices it includes the buffer and Si substrate instead of the two-dimensional electron gas [269]). Replacing (10)-(13) into (9) results in

$$E_{DISS} = 0.357\times f^{0.09}\times V^{1.24}\ \ [\mathrm{nJ}],\quad \text{for SiC FET} \tag{5.21}$$

and

$$E_{DISS} = 0.049\times f^{0.2}\times V^{1.16}\ \ [\mathrm{nJ}],\quad \text{for GaN HEMT} \tag{5.22}$$

where f and V are in MHz and Volts, respectively, showing losses at different operation points just by performing two measurements. The obtained relations were verified with measurement results using ST method with sinusoidal waveforms performed at 1 MHz for M1 [134] and at 10 MHz for M2 [132]. As shown in Fig. 5.8, good agreements were obtained for both transistors. It should be noted that the level of losses in these transistors are considerably different, showing the applicability of the proposed approach to extract C_{OSS}-losses for a wide range of E_{DISS} values.

C. Discussions

The proposed model can predict the frequency-dependent C_{OSS} losses in transistors. In case of devices with static hysteresis loops, such as SJ and Cascode devices, this frequency-dependent loss has to be added with a constant loss to give a complete description of C_{OSS} losses. Here we separately discuss about applicability of the method for two other types of devices:

1) SJ devices: The dominant part of C_{OSS}-loss in SJ transistors is due to the charge-trapping which causes frequency-independent energy dissipation. SJ devices, however, can potentially have a limited Q-factor. In this case, a frequency-dependent loss is added to the total energy dissipation. This might be the reason of previously observed frequency-dependent losses in some of SJ transistors [270]. In this case, a low frequency ST measurement (frequency-independent losses) together with the proposed method (frequency-dependent losses) give a complete view of C_{OSS} energy dissipation.

2) Cascode devices: A type of frequency-independent losses, different from that is happening for SJ devices, was observed in cascode transistors [144], [271]. Some of the commercial

cascode GaN (integrated with a low-voltage Si device) devices showed considerably higher loss for voltages larger than ~200 V [132], [144]. As a result, one can separately characterize frequency-independent (using ST method at the frequency corresponding to peak of *Q*-factor) and frequency-dependent (using the proposed method) C_{OSS}-losses. Adding these different component gives the general behavior of energy dissipation in the output capacitance.

Based on the proposed model, it is suggested to manufacturers to present RS-versus-frequency (at least for frequencies above 1 MHz) for WBG transistors. This curve, together with gives a general view on C_{OSS}-losses.

5.5 Selection of devices with lowest C_{OSS} losses

The small-signal method to evaluate E_{DISS} is a simple technique showing a general view of C_{OSS} losses in WBG transistors and, therefore, can be used to select low-loss devices. Among WBG transistors within the same R_{ON} and voltage rating, the values of C_{OSS} are generally the same; hence, the value of R_S determines the level of C_{OSS} losses. As a result, a single measurement determines the device with lowest amount of C_{OSS} losses, which is preferable for high switching frequency power circuits.

We selected four WBG transistors with similar current capability of ~30-A based on GaN (devices A and B) and SiC (devices C and D). A detailed description of the selected devices is presented in Table 5.2. Figs. 5.9a-d represent the measured C_{OSS} versus voltage at two different frequencies 1-MHz and 10-MHz, for devices A-D, respectively. These figures show that all of the selected devices have the same range of C_{OSS} values, and the measurement results agree with the values reported in datasheet. Fig. 5.9e shows the measured R_S at V_{DS} = 40 V versus frequency for devices A-D. Device A (GaN) exhibits the lowest R_S, which corresponds to the lowest E_{DISS}. The method predicts the largest C_{OSS} losses for device D (SiC). To verify the prediction, we submitted devices C and D (with the same package) to a 75-V peak-to-peak sine-wave at three different frequencies (1-MHz, 2-MHz, and 3-MHz) showing significantly higher losses in device D, as predicted by the method (Figs. 5.9f-g).

Table 5.2 | Specifications of the evaluated transistors using the small-signal approach

Device	Type	Voltage and current rating		R_{ON}** (mΩ)	C_{OSS} (pF) at 400-V
		Voltage (V)	Current* (A)		
A	GaN HEMT	600	31	55	72
B			26	56	71
C	SiC FET	650	30	80	66
D			31	80	64

* Continuous current at 25 ºC. ** Typical ON resistance at 25 ºC.

5.6 Relevance of the developed methodology in energy-efficient power converters

This section aims to demonstrate the relevance of the proposed methodology in the design of energy-efficient power converters. We show how selecting devices with low C_{OSS} losses enable ultrahigh step up operation of boost converters in the impulse rectification regime.

A. The ultrahigh step-up impulse-rectification boost converter: operation principle

Fig. 5.10a shows a boost converter topology separated into two main stages. The first stage, including an inductor and a field-effect transistor (FET), converts the input dc voltage to a stream of high-voltage repetitive impulses. As shown in Fig. 5.10b, when FET is ON ($t_0 < t < t_1$), the inductor is smoothly charged by the input voltage V_{in}. At $t = t_2$, the FET is turned OFF. The resonance between L and C_{OSS} provides a zero turn-OFF loss (ZTL) [272]: because the switching time (Δt_{SW}) is much faster than $(LC_{OSS})^{1/2}$ time

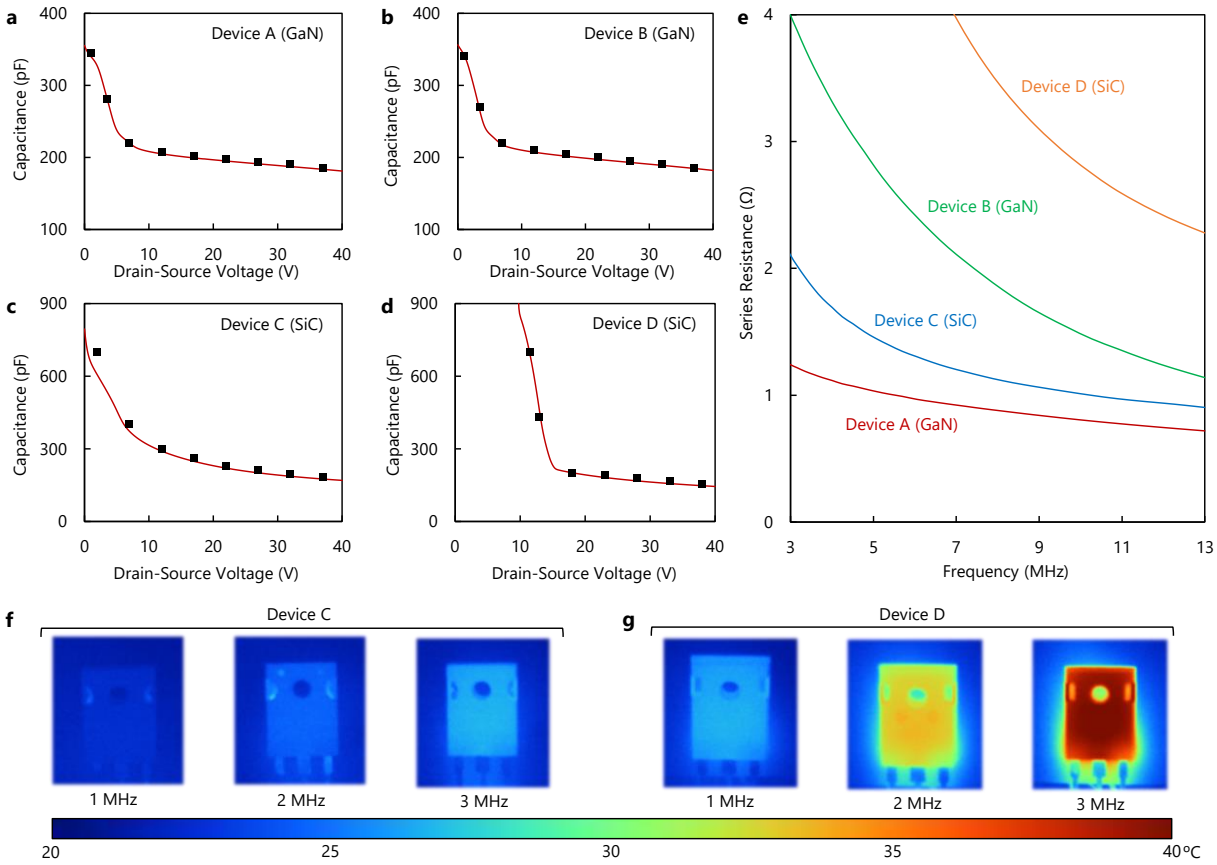

Fig. 5.9 | Selection of low-loss devices with small-signal measurements. Measured C_{OSS} versus drain-source voltage at 1 MHz (solid red line) and 10 MHz (dashed blue line) as well as data reported in datasheet (discrete points) for **a,** device A (GaN), **b,** device B (GaN), **c,** device C (SiC), and **d,** device D (SiC), all 600/650-V rated with ~30-A current rating (Table 5.2). The figures show consistency of C_{OSS} over frequency as the valid assumption of the proposed method. **e,** Series resistance (R_S) of the four devices versus frequency. The method simply predicts lowest and highest losses for devices A and D, respectively. Thermographs of **f,** device C and **g,** device D (gate and source shorted), both with the same package, submitted to 75-V peak-to-peak sinusoidal waveform (charging and discharging C_{OSS}) at three different frequencies 1 MHz, 2 MHz, and 3 MHz. Device D shows considerably higher losses, as predicted by the proposed method.

constant, the cross product of the channel current (i_{ch}) and drain-source voltage (v_{DS}) is completely negligible. The resonance between L and C_{OSS} results in the formation of an impulse waveform over drain-source terminals of the FET, as the inductor current passes through C_{OSS} ($i_L = i_{OSS}$). The drain-source impulse gets clamped at $t = t_2$, when the voltage level reaches the output dc link voltage level V_{out}. During $t_2 < t < t_3$, the second stage shown in Fig. 5.10a rectifies the impulse and the inductor energy is injected to the output dc link. At $t = t_3$, when the inductor current reaches zero, the output voltage starts reducing. During $t_3 < t < t_4$, the energy stored in C_{OSS} is restored, which results in a negative current in the inductor. At $t = t_4$, the v_{DS} reaches zero and the FET turns ON, resulting in a zero

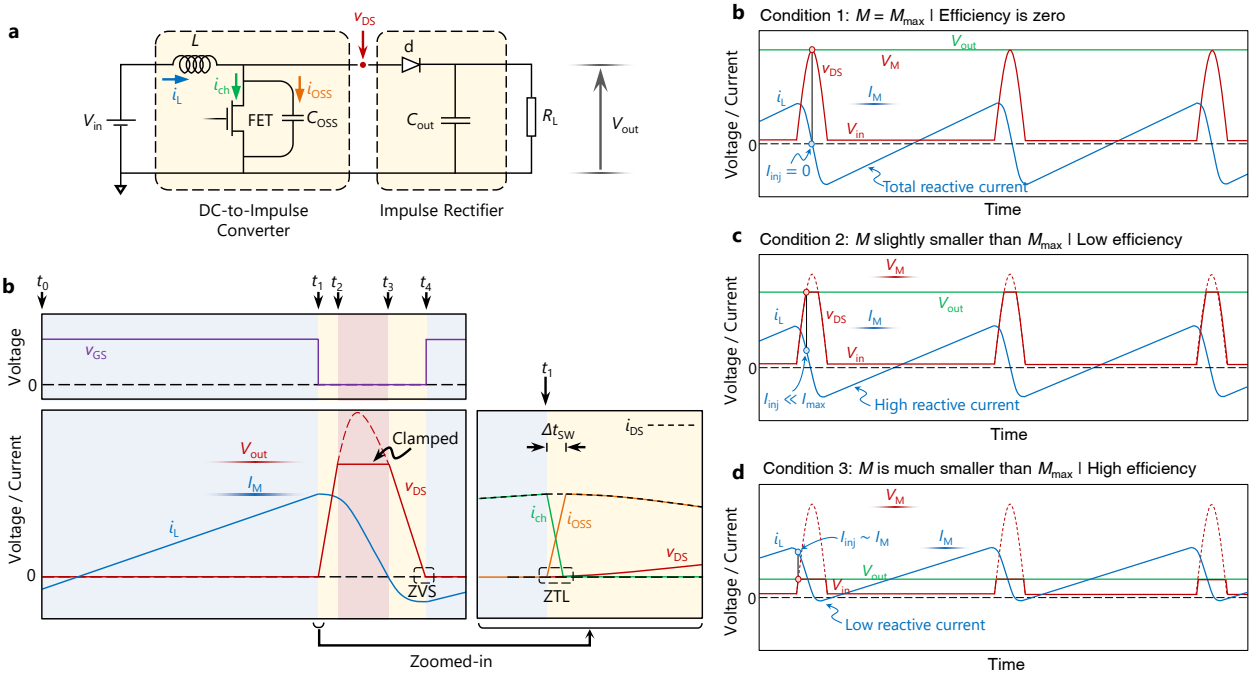

Fig. 5.10 | Impulse rectification boost converter. a, Boost converter topology, together with **b,** illustration of the main waveforms v_{GS}, v_{DS}, i_L, and $i_{DS} = i_{ch} + i_{OSS}$. Operation of boost converter in three conditions: **c,** Maximum possible step-up ($M = M_{max}$), **d,** high step-up ($M \lesssim M_{max}$), and **e,** low step-up ($M \ll M_{max}$).

Table 5.3 | Summary of the operation principle of ultrahigh step-up boost converters

Interval	FET	Diode d	Description
$t_0 < t < t_1$	ON	OFF	Inductor L is being charged
$t_1 < t < t_2$	OFF	OFF	Drain-source impulse starts to build-up (Energy transfer from inductor to C_{OSS})
$t_2 < t < t_3$	OFF	ON	Power transfer period (the impulse is clamped at V_{out})
$t_3 < t < t_4$	OFF	OFF	Restoring the energy of C_{OSS} resulting in a negative inductor current

voltage switching (ZVS). If the FET turns ON after $t = t_4$, then the inductor current flows through the body diode of the FET, resulting in a higher power dissipation due to reverse conduction losses. A turn-ON switching before $t = t_4$ is not favorable as it leads to a hard switching. Table 5.3 summarizes the discussed operation principle. Figs. 5.10b-d show schematic of voltage and current waveforms in three scenarios of maximum possible step-up ratio, high step-up ratio, and low step-up ratio. $M_{max} \triangleq V_M/V_{in}$ represents the maximum voltage gain

$$M_{\max} = \frac{\sqrt{L/C_{\mathrm{OSS}}^{er}}}{R_{\mathrm{ind}}+R_{\mathrm{ON}}}. \tag{5.22}$$

Where $C_{\mathrm{OSS}}^{\mathrm{er}}$ is the energy-related effective C_{OSS}, which is a fixed equivalent capacitance that would give the same stored energy as C_{OSS} for v_{DS} rising from 0 V to the stated V_M, R_{ON} is the ON-resistance of the FET, and R_{ind} the series resistance of the inductor.

The maximum output power of the converter can be written as

$$P_{\max} = \frac{1}{2} L I_{\mathrm{M}}^2 f_{\mathrm{SW}}, \tag{5.23}$$

and the power dissipated in the C_{OSS} is as follows

$$P_{\max} = \frac{1}{2} E_{\mathrm{DISS}} f_{\mathrm{SW}}. \tag{5.23}$$

B. Implementation and evaluation of an ultrahigh step-up boost converter: Impact of C_{OSS} losses

We experimentally demonstrate an efficient high-step-up power conversion using boost converters based on the proposed operation (Fig. 5.11a) using a fixed 10-μH inductor (Fig. 5.11b) and two different SiC FETs (Table 5.4). Figs. 5.11c-d present the main characteristics of the power converter based on FET1. At a fixed voltage gain, the efficiency-versus-switching frequency exhibits a parabolic shape. At low frequencies the peak of inductor current becomes large which results in significant hysteresis losses at the core (Fig. 5.11b). At high-frequencies, the efficiency is limited by the non-recoverable C_{OSS} losses. Fig. 5.11d shows the transferred power at different voltage gain values, from 5 to 200. Based on these power level one can see the significance of the C_{OSS} losses on the energy efficiency of the entire power converter. As shown in Table 5.4, the SiC FET1 exhibits 0.3 μJ per resonantly charging/discharging cycle which corresponds to 0.3 W power dissipation for the switching frequency of 1 MHz. For a ~10 W transferred power (Fig. 5.11d) this results in a 3% lower-than-expected efficiency, which is quite significant. One can experimentally observe the impact of C_{OSS} losses on the energy efficiency of the power converter.

In fact, balancing the trade-off between conduction losses and output capacitance losses is crucial. Whereas R_{ON} contributes to conduction losses, selecting a device with a very small R_{ON} (lower than ac resistance of the inductor) results in a high E_{OSS} and high reactive-power to charge and discharge C_{OSS} losses (Fig. 5.12a) which limits the efficiency. Fig. 5.12b shows the measured efficiency of the circuit

shown in Fig. 5.11a, for two SiC switches within a same family but with two different R_{ON}. The classic view of the circuit may predict a higher efficiency for SiC FET2, which has a lower R_{ON}. However, SiC FET1 shows a consideably higher efficiency which is due to its lower E_{DISS}. It should be noted that lower efficiency in case of SiC FET2 is not due to additional switching losses (as ZVS is achieved in the turn-ON), but because of the higher reactive power in the circuit and corresponding C_{OSS} losses.

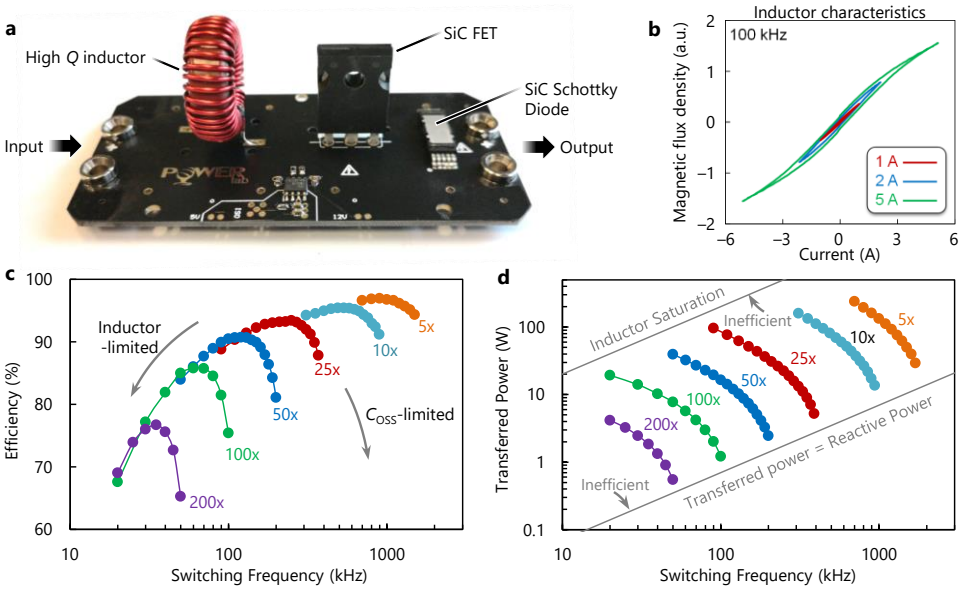

Fig. 5.11 | Implementation and evaluation of an ultrahigh step-up impulse rectification boost converter. a, Prototype of an ultra-high step-up boost converter based on the impulse rectification concept. **b,** Large signal hysteresis characterization of the 10-μH inductor. **c,** Power conversion efficiency, and **d,** transferred power, versus switching frequency for different voltage gain values, ranging from 5 to 200. The power convert exhibit a high energy efficient when the reactive power corresponding to charging and discharging of C_{OSS} is low, and the inductor is not close to saturation.

Table 5.4 | Contribution of the C_{OSS} losses on the energy efficiency of the converter

Device	R_{ON} (mΩ)	C_{OSS}^{er} (pF)	E_{OSS} (μJ) at 400 V	E_{DISS} (μJ) at 400 V	Contribution of the C_{OSS} loss in the efficiency of the converter*
SiC FET1	80	88	7	0.3	–3%
SiC FET2	22	275	22	1.0	–10%

*Operation condition: P_{out} = 10 W, f = 1 MHz, V_{out} = 400 V

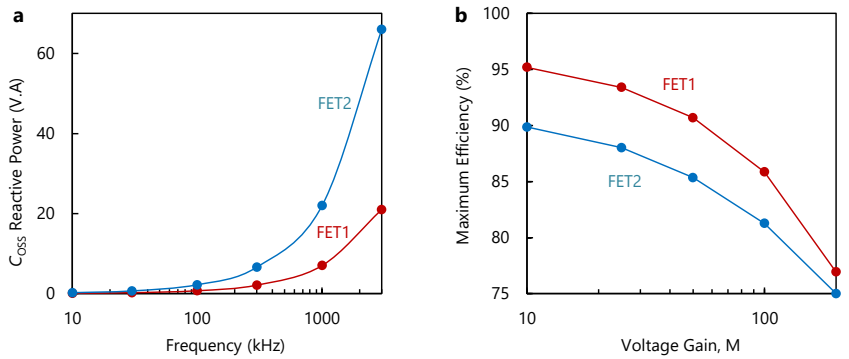

Fig. 5.12 | Impact of C_{OSS} losses in the energy efficiency of the power converter. a, Reactive power versus switching frequency for two different devices FET1 and FET2. **b,** Maximum obtained efficiencies versus voltage gain, for converters utilizing FET1 and FET2. Although FET2 has a lower R_{ON}, it corresponds to a lower efficiency because of higher reactive power and corresponding C_{OSS} losses.

5.7 Conclusions

This chapter presented two new measurement techniques to evaluate and select low C_{OSS} loss devices for miniaturized high-frequency power converters. The first method, Nonlinear resonance, has several advantages, which are as follows:

1) Using a low-voltage dc source, high voltage swings (>1000 V), high frequencies (> 40 MHz), and high values of dv/dt (> 120 V ns^{-1}) can be obtained.

2) The method can be performed in single-pulse mode, which eliminates thermal issues like thermal runaway or increasing leakage at high temperatures, even at very high voltage swings and high values of dv/dt.

3) Unlike ST, where the circuit is not representative of the operating conditions of a device in a switching circuit, the nature of the proposed circuit has similarities to the concept of resonant converters.

4) The simplicity of the circuit, relying on just two main elements (inductor and DUT), minimizes the parasitic effects in waveforms. For instance, any kind of voltage ringing over DUT in more complicated circuits leads to partial C_{OSS} charging/discharging that causes additional losses. These ringings are more dominant in high dv/dt values and can potentially affect the accuracy of measurement. For the proposed method, however, there is always one smooth charging and discharging curve, without any ringing.

Evaluation of a cascode GaN transistor with the proposed method, showed dv/dt-independent C_{OSS} loss that was drastically increased after 250 V, reaching 26% of E_{OSS} at the maximum rating voltage of 650 V. Measurements on enhancement-mode power HEMTs suggested a correlation between C_{OSS} losses and R_{ON} degradation. The simplicity and consistency of the proposed method enables the study of large-signal C_{OSS} and C_{OSS} losses of transistors.

This chapter also proposed a new method to extract C_{OSS}-losses for WBG transistors at different voltages and time/frequency frames, just by performing one small-signal measurements: R_S-versus-frequency. This measurement together with the reported C_{OSS}-versus-V_{DS} reveals the general C_{OSS}-loss behavior of the device. The method helps to clear the voltage and frequency dependence of EDISS, and can be used to compare and benchmark different semiconductor devices. The results also led to a categorization of C_{OSS}-loss in different types of transistors. The E_{DISS} in e-mode GaN and SiC transistors is mainly caused by the limited Q-factor of C_{OSS}, which was not observed in SJ and cascode devices. The generality and robustness of this method make it possible to quantify C_{OSS}-losses of WBG transistors as a crucial source of losses in soft switch power converters, especially those operating at high frequencies. Using the proposed paradigm, low loss devices were selected and the impact on the efficiency of power converter was shown.

6 Precise evaluation of power epitaxies for energy-efficient high-frequency power electronics

6.1 C_{oss} losses from packaged devices to the epitaxy

GaN-on-Si high-electron-mobility transistors (HEMTs) exhibit excellent properties for efficient power conversion. Nevertheless, a considerable energy loss associated with the charging and discharging of the output capacitance (C_{OSS}) in these transistors severely limits their application at high switching frequencies. The previous section proposed new measurement techniques to capture C_{OSS} losses in packaged power devices. The proposed methods enabled selecting devices with lowest losses to realize energy-efficient compact power circuits. However, these package-level methods are less relevant to optimize C_{OSS} losses. This is because packaging in the very last step of the device development, while the power epitaxy is the main source of such losses. This chapter aims to propose new wafer-level measurement methods to evaluate power epitaxies. Using the new technique, we report the observation of unexpected resonances in GaN-on-Si HEMTs. These high-frequency resonances lead to considerable energy losses in fast charging and discharging of the C_{OSS} during switching transients. We propose a simple wafer-level measurement technique to evaluate such losses at the epitaxy level, prior to the transistor fabrication. Experimental results from this technique revealed that the Silicon substrate is the main origin of these losses. Such wafer-level evaluation of C_{OSS} losses opens opportunities to characterize and optimize epitaxies for future power devices, especially those operating at high switching frequencies.

The proposed method enables measurements up to very high frequencies, well above 100 MHz. Low parasitic-capacitances of GaN power transistors enable ultrafast nanosecond switching times [128], [273], resulting in extremely high-frequency harmonics. Nevertheless, practical considerations limit the frequency characterization of C_{OSS} losses to typically less than 40 MHz. Packaging and external-connection parasitics are other limitations hindering the accurate measurement of C_{OSS} losses at very high frequencies. The proposed method uses an on-wafer small-signal modeling approach to evaluate

large-signal C_{OSS} losses, which quantifies frequency-dependent energy dissipation in the C_{OSS}. The extremely low parasitics provided by this method using ground-signal-ground (GSG) RF probes enables the measurement of C_{OSS}-related losses at very high frequencies. This provides a general characterization method of epitaxial structures, enabling their optimization prior to the transistor fabrication.

6.2 On-wafer C_{OSS} loss measurement: Methodology

The output capacitance of a power HEMT mainly consists of three parts: gate-drain capacitance (C_{GD}), drain-substrate capacitance through the vertical epitaxial structure (C_{epi}), and drain-source capacitance through the two-dimensional electron gas (2DEG) (C_{lat}). In power (MOS)HEMTs, C_{GD} is significantly smaller than the two other terms, so that one can consider $C_{OSS} = C_{epi} + C_{lat}$ (Fig. 6.1a). By applying drain-source voltage in the OFF-state, the 2DEG under the gate is depleted, resulting in a considerable reduction in C_{lat} and C_{OSS}. At high enough drain-source voltages, C_{OSS} becomes constant, approximately equal to C_{epi} (Fig. 6.1b) [274]. C_{epi} has been presented as the significant part of C_{OSS} and also the main source of C_{OSS} losses in power HEMTs [274]. This is a vertical capacitance sandwiched between drain pad and silicon substrate, so the capacitance mainly depends on the area of the drain pad, independent from the device layout. Although the characterization of high-frequency losses of RF epitaxies has been proposed in the literature [275], there is little knowledge on high-frequency losses of power epitaxies.

This section presents a wafer-level measurement method based on a simple proposed test structure (Fig. 6.2a) including a signal and ground pads to extract losses due to the epitaxial structure, which is the main source of C_{OSS} losses. The signal pad dimensions should be considerably larger than thickness of the insulating epitaxy so that the effect of fringing fields can be neglected. The RF signal pad is surrounded by a considerably larger ground pad. The ground pad forms a giant capacitance (C_{∞}) with the substrate, which grounds the doped silicon substrate at radio frequencies (Fig. 6.2b). The test structure shown is examined with an incident wave with amplitude V_{inc}, and the reflection coefficient $\Gamma = V_{ref}/V_{inc}$, in which V_{ref} is the reflected wave amplitude, is measured by a network analyzer (Fig. 6.2c). A frequency sweep of V_{inc} gives full information on the behavior of the device under test (DUT), including its circuit model and losses. A lossless C_{epi} results in the total reflection of the incident wave,

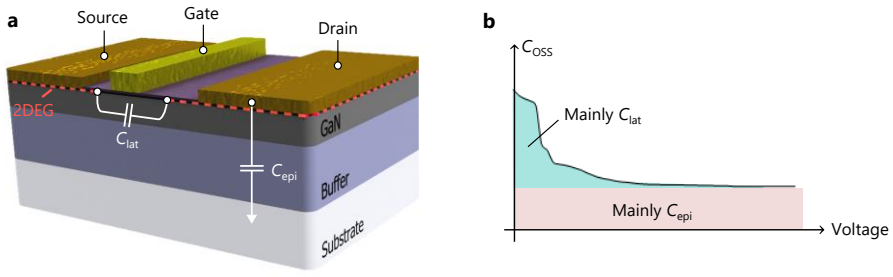

Fig. 6.1 | Nonlinear output capacitance in high-electron-mobility GaN power transistors. a, Simplified structure of an AlGaN/GaN HEMT showing its output capacitance $C_{OSS} = C_{GD} + C_{epi} + C_{lat}$. In practice the effect of $C_{GD} \ll C_{OSS}$ is negligible. **b,** C_{OSS} versus V_{DS} curve for a commercial device showing that C_{epi} dominates at high drain-source voltages.

thus Γ is equal to 0 dB (Fig. 6.2d). Whereas a lossy C_{epi} results in a partial reflection of the incident wave, thus in negative values of Γ (Fig. 6.2e)

One can extract the impedance of the DUT using

$$Z = Z_0 (1+\Gamma)/(1-\Gamma). \tag{6.1}$$

where Z_0 = 50 Ω is the measurement port characteristic impedance. The quality factor Q of the capacitor is obtained as

$$Q = \mathrm{Im}(Z)/\mathrm{Re}(Z) \tag{6.2}$$

where Im(Z) and Re(Z) represent the imaginary and real parts of Z, respectively. For a capacitive element, the amount of charging/discharging losses (between 0 to V) is inversely proportional to its Q, as

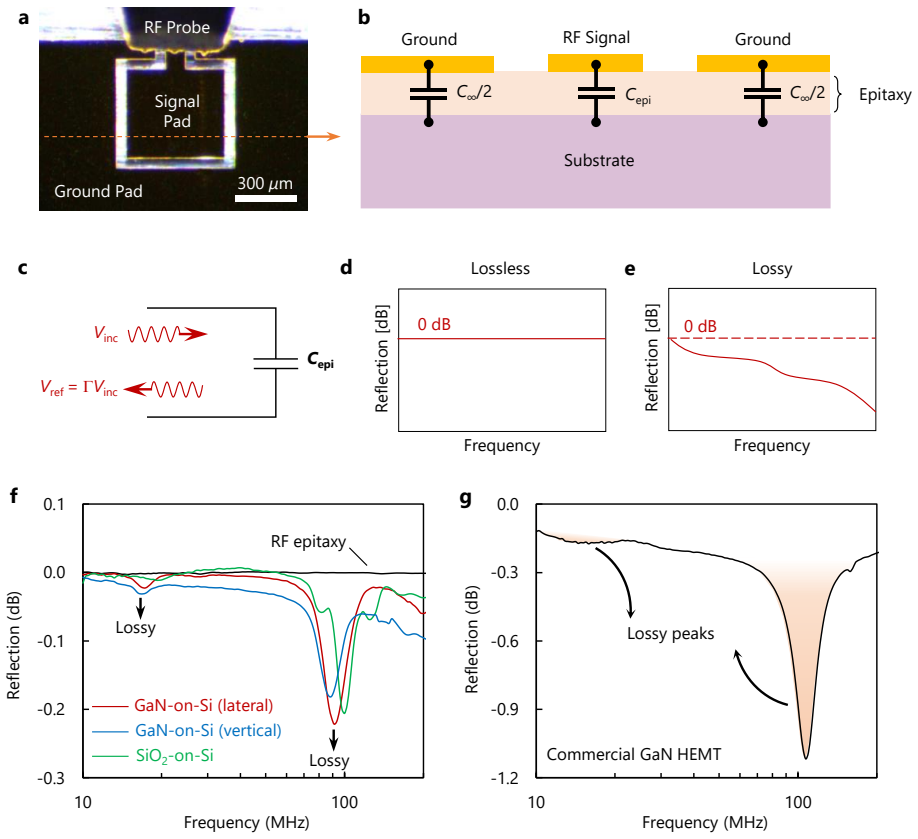

Fig. 6.2 | On-wafer measurement method to evaluate output capacitance losses in power epitaxies. a, Optical image of the test structure measured with an RF probe. **b,** Cross-section illustration of the proposed test structure. **c,** Measurement method to extract losses from output capacitance to characterize epitaxial structures. Illustration of reflection coefficient for **d,** lossless, and **e,** lossy epitaxies. **f,** Measurement results for an RF epitaxy (GaN-on-SiC), together with two GaN-on-Si power epitaxies (corresponding to a lateral HEMT and a vertical MOSFET), as well as a SiO_2-on-Si test structure. **g,** Measurement results for a 600-V-rated commercial device showing similar lossy peaks.

$$E_{\text{diss}} = \frac{\pi}{2Q} E_{\text{tot}} \tag{6.3}$$

where $E_{\text{tot}} = ½CV^2$ is the total energy stored in the capacitor when charged to the voltage V. Thus $\pi/(2Q)$ represents the percentage of energy losses.

Fig. 6.2a shows the fabricated experimental structure. The size of the signal and ground pads are 0.24 mm^2 and 3.7 mm^2, respectively, and the thickness of the pads is 300-nm (270-nm gold with 30-nm titanium adhesion layer). A ground-signal-ground (GSG) RF probe connected to a network analyzer (Keysight N5225A) was used to measure the reflection coefficient at different frequencies, with the lowest possible parasitics and an extremely high bandwidth of 50 GHz. Fig. 6.2f shows the measured reflection coefficient from test structures fabricated on four different epitaxies: GaN-on-SiC RF epitaxy, GaN-on-Si power epitaxies for lateral HEMTs and vertical MOSFETs, and a test SiO_2-on-Si wafer. In all cases, we fabricated devices on 2 cm × 1.8 cm chips diced from 6-inch wafers. All samples on Si substrates (p-type with a resistivity of ~ 0.02 Ω cm) exhibited considerably higher losses with respect to the reference RF epitaxy, with two pronounced peaks at ~17 MHz and ~90 MHz. The presence of lossy peaks (especially the larger one at higher frequency) for the SiO_2-on-Si sample (with no GaN layer) suggests that that the Si substrate is a potential origin of C_{OSS} losses in GaN-on-Si HEMTs. We also observed very similar lossy peaks in some commercial GaN-on-Si power HEMTs (Fig. 6.2g). In this case —in an off-chip measurement — we measured the reflection coefficient from drain-source of the commercial transistor, while the gate was shorted to the source. The vertical GaN-on-Si epitaxy also presented similar lossy peaks. In this case, the drift layer is lightly doped which results in a leakage current between the signal and the ground pads. This causes a lossy behavior over all frequencies and so a lower Q factor. This effect can be seen in Fig. 6.2f, where the vertical epitaxy (blue) shows higher background losses. Therefore, the proposed method reveals all sorts of power dissipations including resonant and leakage losses.

6.3 Evaluation of GaN-on-Si power epitaxies: observation of anomalous resonances

We used the proposed method to quantify the amount of output capacitance losses due to these resonances for epitaxies with different buffer thicknesses. Using (6.1) and (6.3), we extracted the capacitance as well as the losses related to C_{epi}, for two GaN-on-Si power epitaxies 4-μm (Fig. 6.3a) and 5-μm (Fig. 6.3b) buffer thicknesses (similar to the lateral GaN-on-Si epitaxy shown in Fig. 6.2f). There are two distinct peaks corresponding to losses for both epitaxies. Exactly at these peaks, abrupt changes in capacitance are observed, which shows a resonance happening in the epitaxial structure. Although the second epitaxy is 25% thicker than the first one, the resonance frequencies are very close, showing a material dependency of such resonances. As expected, the thicker buffer has a lower capacitance and so a lower stored energy while the dominant part of losses due to the substrate is about the same. This results in a higher relative losses for the thicker epitaxy.

Fig. 6.3 shows the importance of characterizing C_{OSS} losses at high frequencies, since a low frequency test, for instance up to 10 MHz, would not show such significant frequency-dependent losses happening at high frequencies. This could be a potential reason of higher measured losses with pulse excitation (containing higher harmonics) in comparison to sine-wave in ST method [132]. For instance,

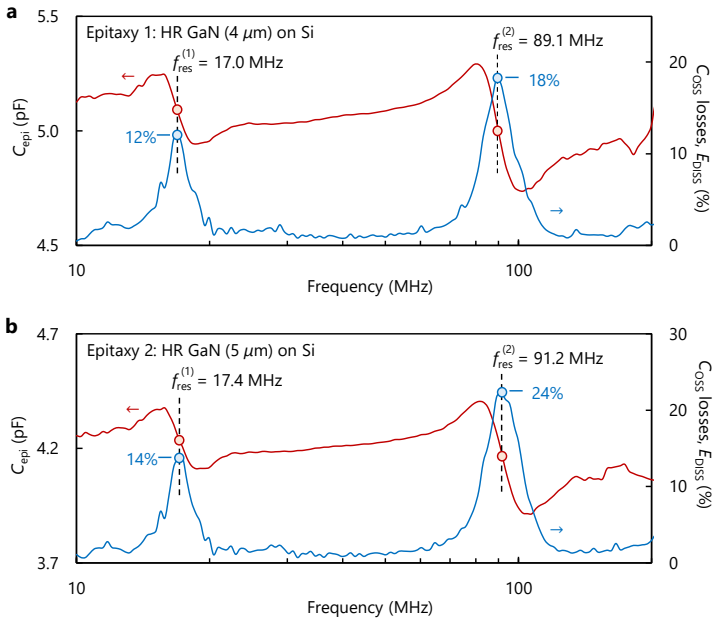

Fig. 6.3 | Evaluation of two GaN-on-Si power epitaxies. Extracted capacitance and losses of the test capacitor on **a,** 4-μm-thick, and **b,** 5-μm-thick carbon-doped high-resistive (HR) GaN buffers. In both cases, there are lossy resonances at ~17 MHz, and ~90 MHz.

at 10-MHz, the employed pulse waveform in [132] had a 5-ns rise-time, and the C_{OSS} losses corresponding to this waveform was not limited to the fundamental frequency of 10-MHz, but it included all the frequency content of the pulse, exceeding 100-MHz. This also shows that single-tone ST measurements, previously performed up to 35 MHz [132], [134], should be performed at much higher frequencies to cover the typical switching harmonics of wide-band-gap transistors. In addition, Fig. 6.3 shows a 1-2% loss over a wide frequency range, which indicates the ability of the proposed method in capturing background C_{epi} losses, caused by other phenomena such as the resistivity of substrate.

6.4 Circuit modeling of epitaxial losses

A circuit model of the C_{epi} can be extracted from the results shown in Fig. 6.3. The model includes a lossless capacitor C_0 in parallel with two lossy *RLC* resonant branches (Fig. 6.4a). Fig. 6.4b shows the extracted circuit parameters for the 4-μm-thick buffer. Fig. 6.4c presents the measured and modeled C_{epi} power dissipation, showing a good agreement between them. We employed the model presented in Fig. 6.4a in a circuit-level simulation with LTspice to extract the amount of C_{OSS} losses due to these resonances for different switching times. Fig. 6.4d shows the power dissipated in R1 and R2 (Fig. 6.4a) representing the low-frequency and high-frequency resonances. The switching time and voltage are 2-ns and 400-V, respectively. The results for 5-ns switching at the same switching voltage level are shown in Fig. 6.4e. As expected, the high-frequency resonance leads to much higher losses for the faster

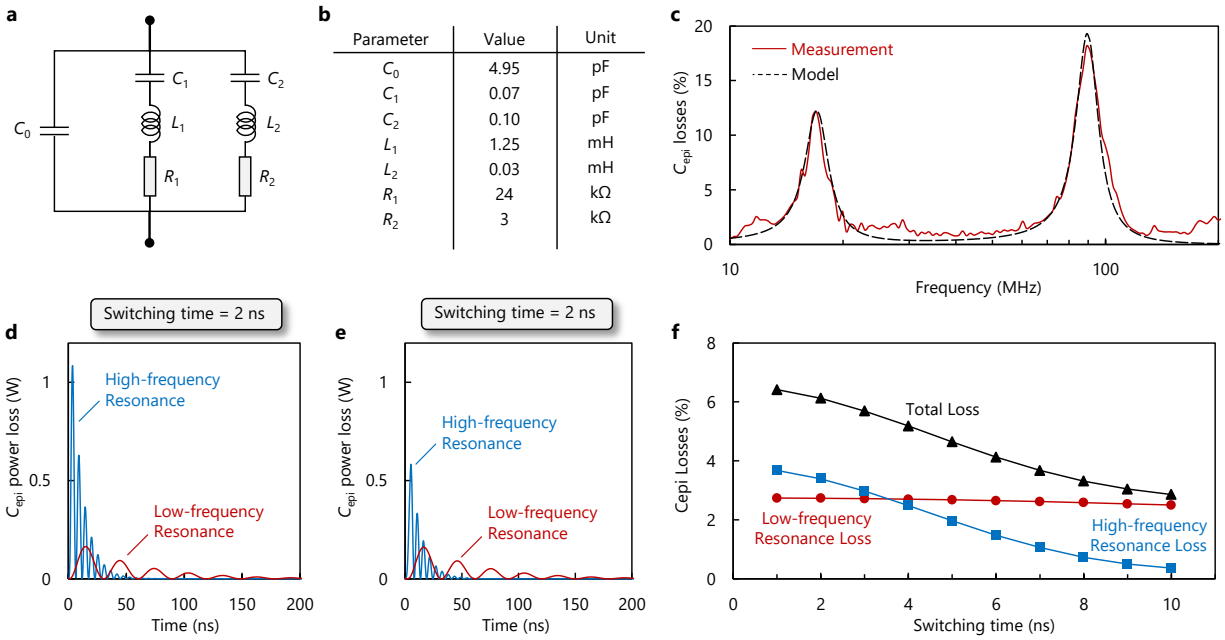

Fig. 6.4 | Circuit modeling and simulation of epitaxial losses. a, Proposed circuit model for output capacitance losses, together with **b,** circuit parameters of the 4-μm-thick buffer sample. **c,** Measured (solid line) and modeled (dashed line) C_{epi} losses. Simulated C_{OSS} power losses of the 4-μm-thick buffer sample for 400-V **d,** 2-ns, and **e,** 5-ns switching transients. The plots show separately the power loss representative for the low- and high-frequencies resonates. **f,** Extracted C_{OSS} energy dissipation corresponding to the low- and high-frequencies resonates, as well as the total loss.

switching transient. The low-frequency resonance, however, is considerably slower than the typical switching transient of a GaN transistor, so both switching times of 2-ns and 5-ns lead to an almost equal power loss. It should be noted that the power loss continues happening after the switching transient is finished. For example for low-frequency resonance, there is a considerable power loss even 100-ns after the switching transient. This cannot be observed in the previous simplified models of output capacitance losses [269], since they do not show any resonances. Fig. 6.4f shows the C_{OSS}-related energy dissipation versus switching time for 400-V switching, from 1 to 10 ns, as well as the share of each resonance in the total loss. For fast switching transients, about 6% of the stored energy is dissipated during charging and discharging. This number is higher for the 5-µm-thick buffer and can reach to about 8% of the stored energy, showing that C_{OSS} losses can be potentially more severe for devices with a higher blocking voltage capability.

6.5 Conclusion

This chapter proposed an on-wafer test method to characterize C_{OSS}-related non-recoverable losses in power epitaxies. Measurements on different GaN-on-Si power epitaxies revealed new insights on C_{OSS} losses in GaN power HEMTs. Two lossy resonances at 17 MHz and 90 MHz were observed, which are of very different nature from previously proposed models and opens opportunities for further

investigations. A reference measurement was done on a test structure fabricated on a GaN-on-SiC RF epitaxy, which showed a flat response without any resonances.

Using a SiO_2-on-Si test epitaxy we showed that the Si substrate has a significant role on the unexpected lossy resonances. Performing measurements on Si substrates with different doping types and doping levels is a future step to minimize such unwanted losses. The proposed method can be used to evaluate and optimize power wafers at the epitaxial level, prior to the device fabrication, which is essential to design the future power electronic devices operating at high switching frequencies.

7 Conclusion and outlook

7.1 Next generation terahertz electronics using nanoplasma switches and electronic metadevices

Next-generation wireless services will demand massive increases in data traffic, requiring access to signals at higher frequencies than are presently used [276]. The future 6G as well as modern non-ionizing imaging and civil radar systems will operation at terahertz frequencies which provide high bandwidths and high spatial resolutions. The novel nanoplasma picosecond switches and electronic metadevices are potentially of great importance as they overcome fundamental limits of classic devices.

The nanoplasma device enable picosecond switching at high amplitudes which leads to generating large powers at terahertz frequencies. Using this new technology we demonstrated the following:

- Extremely fast switching speeds beyond 10 V ps^{-1}, which is over 10 times higher than the state-of-the-art in classic electronics. The output amplitude can vary from 10 V to 1,000 V.
- High-power THz generation. A nanoplasma-based prototype showed ~1 W at 300 GHz. Without any circuit optimization we obtained 10 times larger power comparing to solid-state sources.
- Concept of mm-wave/THz all-metal modulators. A 66-GHz prototype was demonstrated using the state-of-the-art measurement tools. The concept is also applicable to synthesize different types of analog signals such as impulses and noise-like waveforms with applications in imaging and radar systems.

The future steps to further develop nanoplasma devices include:

- Design of terahertz resonators with high energy storage to integrate with nanoplasma switches to achieve higher THz powers.

- Exploration on vertical nanoplasma devices to achieve nanogaps and bring the threshold voltage of the device to ~1 V to operate with CMOS-level voltages.

Electronic metadevices can offer a totally new paradigm for high-performance THz electronics. We showed that microscopic manipulation of radiofrequency fields over the device layout can significantly enhance the device properties. We demonstrate the following points in this thesis:

- Terahertz switches with the cutoff frequency of 18 THz, which is significantly higher than state-of-the-art semiconductor devices. We experimentally demonstrated the switching capability of the devices at 1 THz.

- Proposing a new device concept to achieve ultrahigh conductance values close to the quantum limit. This resolves one of the major challenges in Nanoelectronics which is applicable to any material system (CMOS, III-V, 2D, etc.)

- Thanks to the extremely high performance of the devices we demonstrated a THz modulator operating above 0.5 THz with a flat response up to ultrahigh data rates of 100 Gb/s which is notably higher than what can be currently achieved in 5G system.

- Demonstration of an ideal electronic device at 1 THz The breakdown-conductance characteristics of our THz devices is very close to an ideal device, being two orders of magnitude better than the state-of-the-art in the literature.

The concept of electronic metadevices is more general than THz switches. The future step is extend the concept to amplifiers, rectifiers, etc.

7.2 Data storage and processing based on glass-like electronics

There is a never-ending push for logic electronics to provide faster operation speeds and higher energy efficiencies at smaller scales. Metal-oxide-semiconductors are the main platform of electronics, however, face fundamental constrains for further miniaturization, faster operation, and power reduction, which has stimulated research on complementary or even alternative approaches. This thesis demonstrated electronically accessible long-lived structural states in Vanadium Dioxide that can open new paradigms for widespread applications such as data storage and processing. The structural state of two-terminal nanodevices can be electrically arbitrarily manipulated at low energy costs in sub-nanosecond time scales and probed beyond 10,000 seconds after the excitation. Furthermore, the vanadium dioxide device undergoes complex structural transient phases that can offer a platform to analog data processing.

From the physical point of view, we demonstrated that this memory effect is beyond the classic metastability in Mott systems, but shows features similar to glasses. We demonstrated that these structural glass-like states can be induced and sensed electronically which is a new concept at the frontier of electronics and condense matter physics. From a technological point of view we show the following points:

● Sub-1 ns writing time and sub-10 ns reading time. We believe this extends the state-of-the-art for non-volatile memory devices. We also show sub 100 fJ operation energy cost.

● Ultralow voltage supply down to 290 mV at elevated temperatures and ~800 mV at room temperature. This outperforms the theoretical limits of conventional MOS-based devices.

● Very high cycle-to-cycle, device-to-device, and film-to-film consistency. Poor consistency is a major issue in memristors, which has hindered their potential in large-scale neural networks.

● This is a scale-less effect. We show the same effect can be scaled down to 50-nm-long channel devices, in a two terminal device, which is compatible with ultra-dense cross bar configurations.

● The device can be arbitrarily manipulated at will. We show that this interesting functionality enables multi-level memories and new schemes for brain-inspired computation with unsupervised learning.

The future steps to further develop glass-like electronics include:

● Demonstration of the memory effect in a cross-bar configuration and implementation of an ultra-dense memory.

● Simulations indicate that glass-like electronics has a great potential for brain-inspired computation. Experimental demonstration of a neuromorphic chip based on the proposed glass-like electronics is an important future step.

7.3 Towards low-loss power epitaxies for the next generation power electronics

Enhancing the energy-efficiency and miniaturization of power converters is of great importance in power electronics. GaN-on-Si HEMTs provide a low ON resistance and small gate capacitance which enables them to operate at high frequencies, resulting in a reduction in the overall size of power circuits, however, anomalous losses in their output capacitance hinder their energy-efficient performance. This thesis presented new measurement techniques to precisely evaluate C_{OSS} losses in power transistors to select the devices with lowest losses:

● Nonlinear resonance method to capture large-signal C_{OSS} losses at very high frequencies (40 MHz). This new method revealed new aspects of C_{OSS} losses in GaN cascode devices. In case of enhancement-mode devices, the new technique suggested a correlation between C_{OSS} losses and R_{ON} degradation.

● Small-signal model to predict large signal frequency-dependent C_{OSS} losses. Based on this model we selected low-loss devices only based on a small-signal measurement and realized an energy-efficient dc-dc power converter with voltage gains up to 200.

● On-wafer measurement technique to evaluate C_{OSS} losses in power epitaxies prior to the device fabrication. The method showed unexpected lossy resonances in GaN-on-Si power

epitaxies. We showed that these resonance contribute to the C_{OSS} losses, especially at fast switching transients.

The on-wafer measurement technique can set the stage to minimize the output capacitance losses in the epitaxial levels. As a future work, applying this new measurement techniques to Si substrates and GaN buffers with different doping types and doping levels can give insights to the contribution of these parameters on the non-recoverable output capacitance losses.

A Analytical derivation of the subwavelength TM mode on a thin meta-insulator-semiconductor

Writing the vectorial wave equation at the barrier ($\nabla \times \nabla \times E - \xi^2 E = 0$, with $\xi^2 = \omega^2 \mu\varepsilon$, where ω, μ, and ε are angular frequency, permeability and permittivity of the barrier, respectively), considering the symmetry of structure in the y direction ($\partial/\partial y = 0$) (Fig. A1a) results in

$$\frac{\partial^2}{\partial z^2} E_{\mathrm{x}} - \frac{\partial^2}{\partial x \partial z} E_{\mathrm{z}} + \xi^2 E_{\mathrm{x}} = 0, \tag{A1}$$

$$\frac{\partial^2}{\partial x^2} E_{\mathrm{y}} + \frac{\partial^2}{\partial z^2} E_{\mathrm{y}} + \xi^2 E_{\mathrm{y}} = 0, \tag{A2}$$

and

$$\frac{\partial^2}{\partial x^2} E_{\mathrm{z}} - \frac{\partial^2}{\partial x \partial z} E_{\mathrm{x}} + \xi^2 E_{\mathrm{z}} = 0. \tag{A3}$$

Equation (A2) is independent from two other equations, and E_y cannot get activated based on the excitation in our system. Assuming E_z to be uniform along z direction at the very thin barrier (Fig. A1b-g), equation (A1) can be rewritten as

$$\frac{\partial^2}{\partial z^2} E_{\mathrm{x}} + \xi^2 E_{\mathrm{x}} = 0, \tag{A4}$$

which results in

$$E_{\mathrm{x}}(x,z) = E_0(x)\ e^{-j\xi z} + A e^{j\xi z}\ , \tag{A5}$$

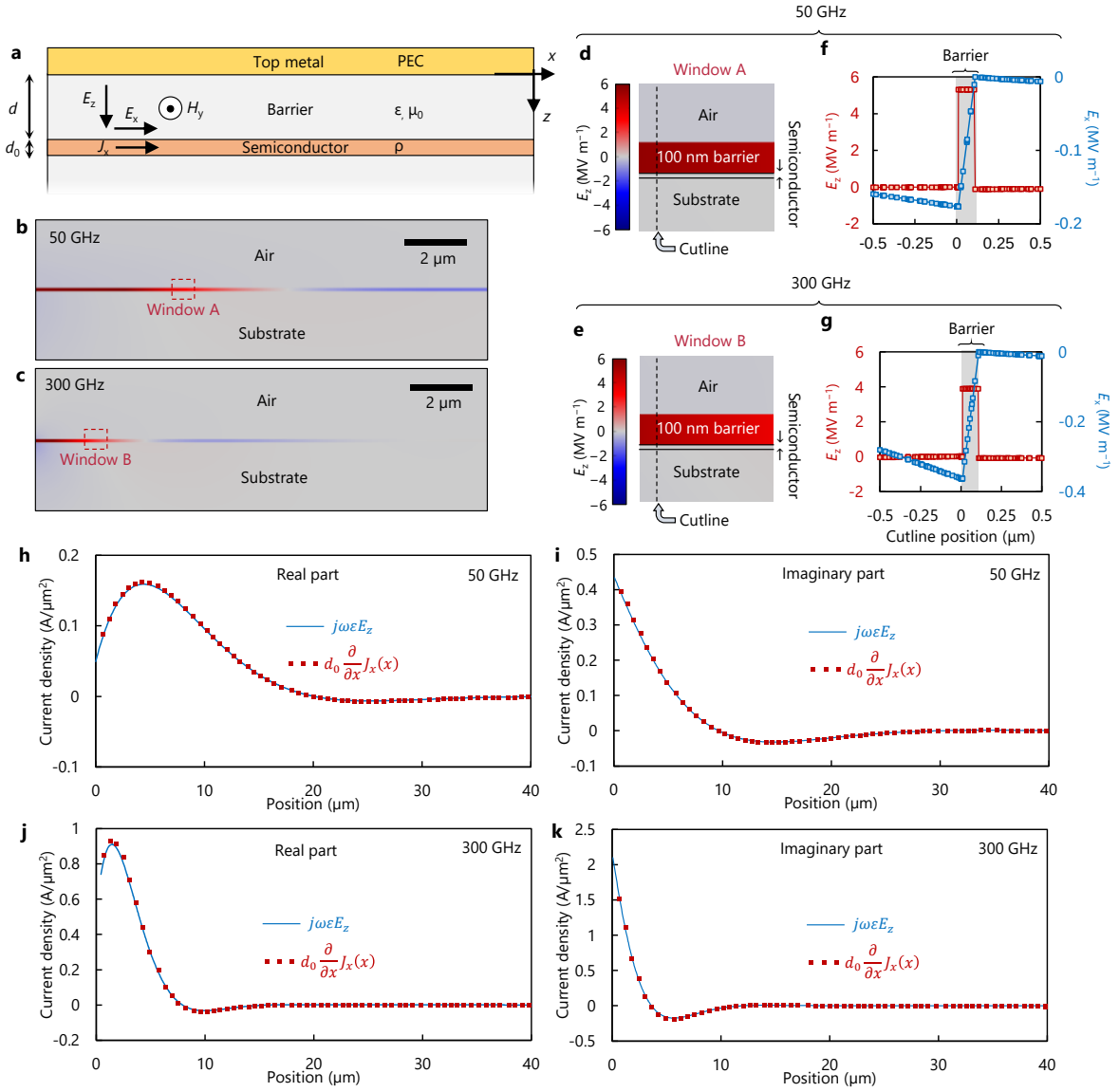

Fig. A1 | Validation of the theoretical description for the subwavelength mode at the metal-semiconductor junction. a, Schematic of a thin MIS structure showing the direction of electromagnetic fields. **b, c,** Simulated electric field E_z (cross section) with d = 100 nm (we considered a larger-than-usual thickness to have more data points in our numerical model which is used to support our analytical approach) at 50 GHz and 300 GHz, respectively. The structure is excited from the left end and terminated from the right end. **d, e,** Simulated electric field E_z (cross section) at 50 GHz and 300 GHz at the windows A and B of parts **b** and **c**, respectively. The results show a uniform E_z at the thin barrier, which is one of the assumptions in our theoretical modeling. The semiconductor layer (10 nm thin) is just below the barrier. **f, g,** Simulated electric field components E_z and E_x in the cutline shown in parts **c** and **d** at 50 GHz and 300 GHz, respectively, indicating a uniform E_z and a linear E_x at the barrier which is in agreement with the theoretical calculation of equation (A10). **h, i,** Simulated displacement current at the barrier and derivation of current in the semiconductor layer (real and imaginary parts, respectively) validating the current continuity in equation (A11). The results are presented at 50 GHz. **j, k,** Simulated displacement current at the barrier and derivation of current in the semiconductor layer (real and imaginary parts, respectively) at 300 GHz validating equation (A11).

where $j=\sqrt{-1}$, $E_0(x)$ represents the functionality from x, and A is a constant. Equation (A5) has to meet boundary conditions at the PEC and the semiconductor layer:

$$E_{\mathrm{x}}(0,z)=0, \tag{A6}$$

$$E_{\mathrm{x}}(d,z)=\rho J_{\mathrm{x}}(x) \tag{A7}$$

where J_x represents the current density in the thin semiconductor layer. Substituting (A6) in (A5) imposes $A=-1$. Then substituting boundary condition (10) in (8) results in

$$E_0(x)(e^{-j\xi d}-e^{j\xi d})=\rho J_{\mathrm{x}}(x). \tag{A8}$$

Therefore we can re-write (A5) as following

$$E_{\mathrm{x}}(x,z)=\rho\frac{e^{-j\xi z}-e^{j\xi z}}{e^{-j\xi d}-e^{j\xi d}}J_{\mathrm{x}}(x). \tag{A9}$$

The barrier thickness is many orders of magnitude shorter than the wavelength. For example, the wavelength of 1 THz is in range of ~100 μm (depending on the dielectric constant), while the barrier is ~10 nm thin. This guarantees $\xi z \ll 1$ and so $e^{j\xi z}$ can be simplified as $1+j\xi z$. In this case (A9) results in

$$E_{\mathrm{x}}(x,z)=\frac{\rho z}{d}J_{\mathrm{x}}(x). \tag{A10}$$

This linear functionality can be seen in the simulations results presented in Fig. A1e and A1f. Substituting equation (A10) into (A3) results in (2.1). We then apply current continuity at the semiconductor layer which imposes a matching between the displacement current in the metal-semiconductor junction, and the ohmic current at the semiconductor:

$$j\omega\varepsilon E_{\mathrm{z}}=d_0\frac{\partial}{\partial x}J_{\mathrm{x}}(x) \tag{A11}$$

This is valid because the electric fields are closed between the top metal and the semiconductor layer (Fig. A1c-f). We have further demonstrated the validity of equation (A11) in Fig. 9g-j. Substituting (A11) into (2.1) noting that $\rho/d_0=R_{\mathrm{sh}}$ (the sheet resistance of the semiconductor layer) results in

$$\frac{\partial^2}{\partial x^2}E_{\mathrm{z}}-j\frac{\omega\varepsilon R_{\mathrm{sh}}}{d}E_{\mathrm{z}}+\xi^2E_{\mathrm{z}}=0. \tag{A12}$$

One can easily conclude that the second term of (A12) dominates the third term for the condition of our devices. For example, considering $R_{\mathrm{sh}}=300\ \Omega/\square$ and $d=10\ \mathrm{nm}$ and $f=1\ \mathrm{THz}$, then the second term of (A12) is 3,800 times larger than the third term. Therefore, equation (A12) can be simplified to equation (2.2) which leads to a dissipative mode with a subwavelength oscillatory nature with subwavelength (2.3). We note that this subwavelength mode has major differences compared to slow-waves, which are also subwavelength modes on MIS platforms [277]. Beside the different structure of our devices with coplanar slow-waves, the subwavelength mode described by equation (2.2) is a

stationary mode driven by the diffusion equation, different from slow-waves that have propagating nature. The stationary nature of the here-presented modes can be seen in the simulations, in which identical fields patterns are obtained at different values of permeability.

B High-frequency Modeling and De-embedding Based on *S*-parameter Measurements

For measurements at mm-wave frequencies, we utilized extended VNA modules from Virginia Diodes (VNAX276 and VNAX277) together with terahertz probes (220-330 GHz) from Cascade. The modules were driven by a radiofrequency (RF) (at frequency f_{RF}) and a local oscillator (LO) (at frequency f_{LO}). Using an amplifier/frequency multiplier chain, the VNAX276 module generates a terahertz signal at $18\times f_{RF}$ which is applied to the device-under-test (DUT). The signal before application to the DUT (reference signal) and the reflection from the DUT (reflection signal) were then mixed with $24\times f_{LO}$ to be down-converted to intermediate frequencies and measured. The complex ratio of the reflection and the reference signal results in the reflection scattering parameter S_{11}. The RF and LO signals are swept together, to fix the intermediate frequency at 279 MHz, which is optimized for the VNAX modules. The LO signal is also applied to the VNAX277 module which mixes the transmitted signal through the DUT with $24\times f_{LO}$ to downconvert the transmitted signal to the same intermediate frequency of 279 MHz. The complex ratio of the transmitted and the reference signals results in the transmission scattering parameter S_{21}.

Higher frequency measurements were done at 500-750 GHz and 750-1,100 GHz bands. We used frequency extender modules from Virginia Diodes connected to a four port Keysight PNA-X. In both cases, the system was calibrated by a standard through-reflect-line (TRL) chips. We used THz probes with embedded bias-tee corresponding to each frequency band to terminate the waveguide ports to coplanar port of the DUT.

Scattering parameters were measured in a two port measurement setup, and the ABCD scattering matrix parameters were extracted. The parameter B in the ABCD matrix equals the series impedance $Z(\omega)$, from which we extracted the R_{ON} in the ON state and $1/(jC_{OFF}\omega)$ in the OFF state. We also conducted de-embedding on the measured R_{ON}. For each device, a short circuit feature with the same

pad size and thickness was fabricated to measure the short-circuit resistance, including two probe-pad contact resistances and also the resistance of metallic pads outside the active area of the device.

Transfer length method (TLM) measurements is normally used to extract the contact resistance of electronic devices. For the mm-wave and terahertz devices, however, the situation was special as g becomes comparable with W, and therefore, a sweep in g would change the field pattern in the device. To avoid this issue, we extracted the total R_{ON} and then excluded the channel resistance to obtain the contact resistances from two sides of the channel.

C Layout and Simulation of Coplanar Filters in Nanoplasma-based Modulators

Nanoplasma-based millimeter-wave and terahertz modulators only rely on a single metal layer, where the entire circuit can be patterned in single photolithography step. The thesis presents the modulator performance for four different bandpass filter designs. Fig. C1 shows a comparison between measured and simulated results of scattering parameters corresponding to filter A is presented in. The layout corresponding to each filer is represented in Fig. C2.

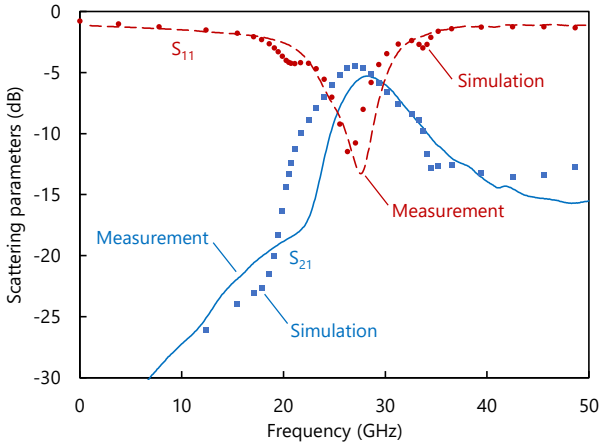

Fig. C1. Measurements (solid and dashed lines) and simulation results (discrete points) corresponding to design A.

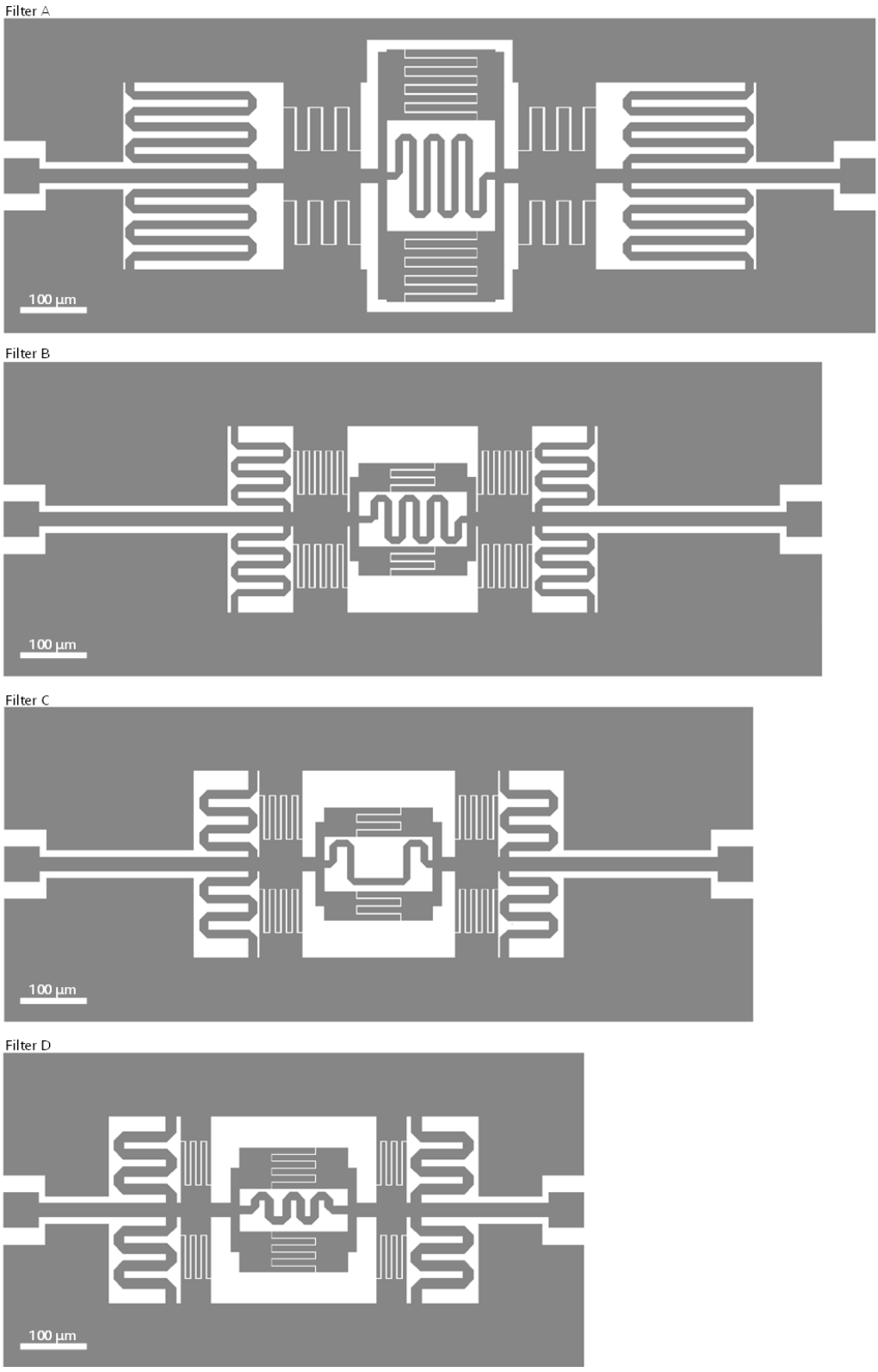

Fig. C2. Layout designs corresponding to filters A, B, C, and D.

D Mathematical prediction of VO_2 glass-like dynamics in a non-uniform pattern of excitation

The empirical equation (4.1) presented the switching barrier of a VO_2 switching after n switching events. The equation was found in the case of repetitive pulse packets in which the time interval between two consecutive pulses remains fixed. In this section we demonstrate that this equation is valid even for a nonuniform pulse pattern. Our results suggest that the glass-like dynamics on VO_2 is mathematically predictable with high accuracy. We use a non-uniform patter of pulses with the following separations: 1s, 10ms, 1ms, 100ms, 1ms, 1ms, 1ms. We periodically repeated this pattern and measured the corresponding incubation times.

Equation (4.1) can be equivalently written for the incubation times:

$$t_{\mathrm{inc}} = t_{\mathrm{inc},0} - t_1 \ln\left(\sum_{k=1}^{n} \frac{T_0}{t_0 - t_{\mathrm{k}}}\right), \tag{D1}$$

where $t_{\mathrm{inc},0}$ represents the incubation time of the switch relaxed for $T = T_0$ after n excitations. In this case we consider the pulse after the longest relaxation (T_0 = 1 s) as the reference pulse (with incubation time $t_{\mathrm{inc},0}$). Using (B1) we write the reduced incubation time of each pulse with respect to the reference pulse:

$$t_{\mathrm{inc},0} - t_{\mathrm{inc}}^{\mathrm{pulse}\ 1} = t_1 \log\left(\frac{1}{0.01}\right) = 2t_1 \tag{D2}$$

$$t_{\mathrm{inc},0} - t_{\mathrm{inc}}^{\mathrm{pulse}\ 2} = t_1 \log\left(\frac{1}{0.001} + \frac{1}{0.011}\right) = 3.038t_1 \tag{D3}$$

$$t_{\mathrm{inc},0} - t_{\mathrm{inc}}^{\mathrm{pulse}\ 3} = t_1 \log\left(\frac{1}{0.1} + \frac{1}{0.101} + \frac{1}{0.111}\right) = 1.461t_1 \tag{D4}$$

Table D1 | Verification of the empirical model presented in Eq. 4.1 in a non-uniform pattern

Pulse no.	Relaxation time (ms)	Measured t_{inc} (ns)	Reduction in the incubation time with respect to the reference pulse		
			Measurement (ns)	Analytical model (ns)	Error (%)
0 (Reference)	1000	778.4	-	-	-
1	10	639.1	139.3	137.0	1.7%
2	1	571.2	207.2	208.1	0.4%
3	100	680.1	98.3	100.1	1.8%
4	1	572.7	205.7	206.3	0.3%
5	1	559.9	218.5	218.2	0.2%
6	1	552.5	225.9	224.0	0.9%

$$t_{\mathrm{inc},0} - t_{\mathrm{inc}}^{\mathrm{pulse\ 4}} = t_1 \log\left(\frac{1}{0.001+0.101+0.102+0.112}\right) = 3.012 t_1 \tag{D5}$$

$$t_{\mathrm{inc},0} - t_{\mathrm{inc}}^{\mathrm{pulse\ 5}} = t_1 \log\left(\frac{1}{0.001} + \frac{1}{0.002} + \frac{1}{0.102} + \frac{1}{0.103} + \frac{1}{0.113}\right) = 3.184 t_1 \tag{D6}$$

$$t_{\mathrm{inc},0} - t_{\mathrm{inc}}^{\mathrm{pulse\ 6}} = t_1 \log\left(\frac{1}{0.001} + \frac{1}{0.002} + \frac{1}{0.003} + \frac{1}{0.103} + \frac{1}{0.104} + \frac{1}{0.114}\right) = 3.27 t_1 \tag{D7}$$

Based on these calculations, the only parameter describing the transient change in the incubation times is t_1 which is equal to the change of incubation time by one decade change in the relaxation time. Using t_1 = 68.5 ns we have the values reported in Table D1 which show excellent agreements with the measurement results. Such an excellent predictability together with a high device-to-device consistency enables system-level designs for a variety of applications.

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