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Integrated Electronics for Deep Implants to Remotely Monitor Hemodynamics

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To my parents, my brother, my sister,
and
To my wife, Sevdenur . . .

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Abstract

The integration of technology in the medical field has greatly improved accuracy in diagnoses, thus leading to more effective treatments. Wearable and implantable medical devices offer great potential for remote patient monitoring, particularly for heart failure (HF) patients. Continuous and accurate monitoring of the patient's hemodynamics, especially pulmonary artery pressure (PAP) and cardiac output (CO), is essential for adapting treatments and reducing repeated hospital admissions. This thesis presents an implantable wireless system for remote hemodynamic monitoring, which enables direct, continuous (24/7), and simultaneous measurement of the PAP and cross-sectional area (CSA) of the artery, that is necessary to accurately calculate the CO.

The implantable system is designed to minimize clinical issues by reducing its dimensions and power consumption. Techniques for designing low-power, miniature circuits and systems to measure pressure and artery diameter are presented. An energy-efficient bridge-to-digital converter (BDC) for pressure measurements is introduced and exploits duty cycling to reduce the power consumption of the piezoresistive sensor and the instrumentation amplifier (IA) in the sensor readout, while inherently cancelling the IA's offset and 1/f noise thanks to a novel spinning method. Thus, it avoids the need for complex IAs that foresee offset-reduction techniques or calibration. This novel architecture enables high resolution and ultra-low energy consumption in bridge sensor systems, representing state-of-the-art performance in energy efficiency.

An innovative method is developed to directly measure the diameter and CSA of an artery. The method exploits the inductive characteristic of an implant's anchoring loops and provides a direct and accurate measurement of the artery's CSA. The anchoring loop is used for both the fixation of the implantable system in the artery and the measurement of the artery's CSA. The deformation of the loop changes its inductance, which is correlated to the artery's diameter and CSA. An oscillator-based inductive readout circuit that measures the inductance change of a nitinol anchoring loop is presented. It enables remote monitoring of the artery's CSA and improves by a factor of four the lateral resolution of echocardiography.

Ultrasound (US) is the most efficient method for powering miniature implants at great depths. To meet the requirements for a small form factor, a single implantable piezoelectric transducer is used for simultaneous power and uplink data transfer. The US powering through an 8.5 cm

tissue phantom provides sufficient link efficiency, enabling wireless powering with an acoustic intensity much lower than the Food and Drug Administration (FDA) safety limit. The parallel uplink data transfer, using amplitude-shift keying (ASK) modulation, achieves a high modulation index, thus providing a robust communication link. Prototype integrated circuits (ICs) are designed and implemented in a standard 180-nm CMOS technology. A biocompatible, hermetic glass packaging approach is developed to enable long-lasting and low-cost implants. The size of the glass-packaged implantable system is 3.2 mm × 2 mm × 10 mm. The challenges of powering the glass-packaged implant are discussed, and the system's performance is verified in an *in vitro* experimental setup that emulates the arterial blood flow.

Keywords: Implantable medical device (IMD), remote patient monitoring (RPM), hemodynamic monitoring of heart failure (HF) patients, pressure sensor, energy-efficient, CMOS, instrumentation amplifier (IA), analog-to-digital converter (ADC), bridge-to-digital converter (BDC), wireless ultrasonic power and data transfer.

Résumé

L'intégration de la technologie dans le domaine médical a considérablement amélioré la précision des diagnostics et a permis des traitements plus efficaces. Les dispositifs médicaux portables et implantables offrent un grand potentiel pour la surveillance à distance des patients, en particulier pour les patients souffrant d'insuffisance cardiaque (IC). La surveillance continue et précise de l'hémodynamique du patient, en particulier de la pression artérielle pulmonaire (PAP) et du débit cardiaque (DC), est essentielle pour adapter les traitements et réduire les admissions répétées à l'hôpital. Cette thèse présente un système sans fil implantable pour la surveillance hémodynamique à distance, permettant une mesure directe, continue (24/7) et simultanée de la PAP et de la surface de section transversale (SST) des artères, ce qui est nécessaire afin de calculer précisément le DC.

Le système implantable est conçu pour minimiser les problèmes cliniques en réduisant ses dimensions et sa consommation d'énergie. Des techniques pour concevoir des circuits et des systèmes miniaturisés à faible consommation d'énergie servant à mesurer la pression et le diamètre des artères sont présentées. Un convertisseur pont numérique (CPN) à faible consommation d'énergie pour les mesures de pression est présenté. Le CPN met à profit le cycle de fonctionnement pour réduire la consommation d'énergie du capteur piézorésistif et de l'amplificateur d'instrumentation (AI) dans la lecture du capteur, tout en annulant implicitement le décalage et le bruit 1/f de l'AI grâce à une méthode innovante de rotation. Cela évite les AIs complexes qui prévoient des techniques de réduction de décalage ou nécessitent un calibrage. Cette architecture innovante permet une résolution élevée et une très faible consommation d'énergie dans les systèmes de capteur en pont, représentant une performance de pointe en terme d'efficacité énergétique.

Une méthode innovante est développée pour mesurer directement le diamètre et la SST d'une artère. La méthode exploite la caractéristique inductive des boucles d'ancrage de l'implant et fournit une mesure plus précise et directe de la SST de l'artère. La boucle d'ancrage est utilisée à la fois pour le placement du système implantable dans l'artère et pour la mesure de la SST de l'artère. La déformation de la boucle change son inductance, qui est corrélée au diamètre et à la SST de l'artère. Un circuit de lecture inductif à base d'oscillateur qui mesure le changement d'inductance d'une boucle d'ancrage en nitinol est présenté. Il permet la surveillance à distance de la SST de l'artère et améliore d'un facteur quatre la résolution latérale de l'échocardiographie.

Résumé

L'ultrason est la méthode la plus efficace pour alimenter les implants miniaturisés à grande profondeur. Pour répondre aux exigences d'un petit facteur de forme, un seul transducteur piézoélectrique implantable est utilisé pour le transfert simultané de puissance et de données de liaison ascendante. L'alimentation en ultrasons à travers un fantôme de tissu de 8,5 cm offre une efficacité de liaison suffisante, permettant une alimentation sans fil avec une intensité acoustique beaucoup plus faible que la limite de sécurité de la FDA (Food and Drug Administration). Le transfert de données de liaison ascendante parallèle utilisant la modulation d'amplitude (ASK) atteint un indice de modulation élevé, offrant ainsi une liaison robuste. Des circuits intégrés prototypes (CI) sont conçus et mis en œuvre dans une technologie CMOS standard de 180 nm. Une encapsulation en verre biocompatible hermétique est développée pour permettre des implants à longue durée de vie et à faible coût. La taille du système implantable encapsulé en verre est de 3,2 mm x 2 mm x 10 mm. Les challenges liés à l'alimentation de l'implant encapsulé en verre sont discutés et les performances du système sont vérifiées grâce à une plateforme expérimental in vitro qui émule le flux sanguin artériel.

Mots clés : Dispositif médicaux implantables (DMI), surveillance à distance des patients (SDP), surveillance hémodynamique des patients atteints d'insuffisance cardiaque (IC), capteur de pression, économie d'énergie, CMOS, amplificateur d'instrumentation (AI), convertisseur analogique-numérique (CAN), convertisseur pont-numérique (CPN), transfert par ultrason sans fil d'énergie et de données.

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1 Introduction

Technology advancements have a significant impact on the diagnosis and treatment of diseases. The incorporation of technology in the medical field has greatly improved the accuracy of diagnoses, leading to more successful treatments. Today, mobile health technologies have enormous potential for enhancing patient care and reducing healthcare costs. Wearable and implantable devices are driving a transformation in the mobile health era and are receiving increasing attention in various biomedical applications such as medical diagnostics, clinical therapy, and personal healthcare [1].

Wearable devices that can continuously monitor patients' vital signs are widely available in the form of smart watches, glasses, and arm bands. These devices are capable of monitoring a range of physiological parameters, including heart rate, blood pressure, respiration rate, blood oxygen saturation level, and body temperature [1]. Additionally, there is a growing demand for implantable medical devices and electronics among both patients and clinicians. Since the first pacemaker implant in 1958, a variety of implantable devices such as pacemakers, cardioverter defibrillators, cochlear implants, and deep brain stimulators have been developed and are used to treat millions of patients [2, 3]. According to a report by Allied Market Research [4], the implantable medical devices market was valued at $91.9 billion in 2020 and is expected to reach $179 billion by 2030.

Recent advancements in fabrication and packaging techniques have made it possible to embed multiple microelectronic and micromechanical sensors very sensitively into a small and cost-effective area, allowing for the efficient integration of various sensing capabilities into wearable and implantable devices. In addition, improvements in wireless communication technology have enabled high data rates and expanded broadband wireless networks to reach rural and low-income areas [1]. According to a report by the International Telecommunication Union [5], in 2021, 95% of the world's population had access to mobile broadband networks and 4G network coverage reached 88% of the global population. The widespread availability of broadband wireless networks worldwide offers great promise for the use of wearable and implantable sensors in remote and continuous monitoring of patients, which has the potential to greatly improve patient care while significantly reducing healthcare costs.

Remote patient monitoring (RPM), also known as telemonitoring, refers to the monitoring and evaluation of a patient's health parameters remotely. RPM systems wirelessly transfer the patient's physiological data to healthcare providers, allowing for more frequent and sensitive assessment of the patient's clinical status. Utilizing advances in digital technology, RPM offers many benefits to the healthcare system, such as saving time for both healthcare providers and patients, the ability to continuously monitor patients, the prevention of worsening illnesses and untimely deaths, reduced hospitalizations and costs, and more accurate readings while allowing patients to continue with their usual daily activities [6]. It is also useful in situations where patients have mobility issues or when physical interactions are risky, such as during a pandemic. During the Covid-19 pandemic, the popularity of RPM increased and several applications were developed to help reduce hospitalization rates [7]. One of the main areas where wearable and implantable devices can be effectively used for RPM is remote hemodynamic monitoring of heart failure (HF) patients, allowing healthcare providers to continuously track key indicators of their condition and intervene proactively to prevent deterioration, reducing the risk of repeated hospitalizations. This thesis presents the design and development of an implantable system for remote and long-term hemodynamic monitoring of HF patients.

1.1 Heart Failure (HF)

Heart Failure is a severe and progressive clinical condition in which the heart is unable to pump enough blood to meet the needs of the body. It is one of the leading causes of death, disability, and healthcare costs in the 21^{st} century [8, 9, 10]. One of the defining characteristics of HF is a high incidence of hospital admission and readmission, with HF causing the highest rate of rehospitalization compared to all other medical conditions [9]. High rate of HF hospitalization (HFH) results in a significant economic burden to the health care system and decreases the quality of life of millions of patients. HF patients suffer from progressively declining functional status and impaired quality of life, leading to death within 5 years of diagnosis for approximately 42% of them [11]. HF is diagnosed by monitoring a patient's heart function. Monitoring of hemodynamics, which is the dynamics of the blood flow, plays a crucial role in the management of HF [12, 13]. The continuous (24/7) and accurate monitoring of the patient's hemodynamics, particularly pulmonary artery (PA) pressure and cardiac output (CO), is essential for adapting treatments based on the patient's reactions to the prescribed medications and reducing repeated hospital admissions.

1.1.1 Societal and Economic Impact

The global impact of cardiovascular diseases (CVDs) is burdensome as reported by the World Health Organization (WHO) [14]: they are the leading cause of death globally, accounting for 32% of all deaths, killing about 17.9 million people every year worldwide. Focusing on HF, it is a global epidemic, affecting more than 64 million people worldwide, with rates increasing due to population growth and aging [15].

In the United States, the prevalence of HF is projected to increase by 46% from 2012 to 2030, and it is estimated that more than 8 million adults older than 18 years will suffer from HF in 2030 [16, 17]. The total percentage of the population with HF is expected to rise from 2.4% in 2012 to 3% in 2030. Hospitalization is inevitable to treat acute complications of HF. This places a growing burden on national healthcare systems and is becoming increasingly unsustainable. In 2018, HF hospitalizations in the United States exceeded 1.2 million, and the number of deaths due to HF in 2019 was more than 86,000 [17]. In Switzerland, the overall HF prevalence is estimated at 2.5%, representing more than 200,000 people [18, 19]. According to the Swiss Federal Office of Statistics, among all causes of death, cardiovascular mortality in 2020 was 26.9%, and more than 62,000 men and 44,000 women were hospitalized for CVDs [20].

As the population is aging, the prevalence of HF continues to rise and its economic burden on healthcare systems significantly increases, with the cost of care becoming unsustainable. The global economic burden of HF in 2012 was estimated to be $108 billion per year, and this value is expected to continue to rise further with the aging and increasing global population [21]. In the United States, the estimated total cost of HF in 2020 is $43.6 billion, and the annual total cost of care is projected to increase by 60% to $69.7 billion by 2030 [16]. HFH is a major contributor to the high cost of HF care. The annual median total cost for HF care per patient was estimated at $24,383, with HFH driving costs at $15,879 per patient [22].

1.1.2 Diagnosis and Monitoring

The journey of HF patients is complex and difficult, beginning with the onset of initial symptoms and progressing to a decline in physical status, which can vary in its severity, and may lead to death. Medical management aims to stabilize the disease and treat acute decompensation leading to hospitalization. When the HF process of congestion [23] and decompensation begins, the earliest change in a physiologic parameter is an increase in cardiac filling and PA pressure (PAP), which could be detected weeks before hospitalization [13]. A recent study [24] showed that even small changes in PAP can predict mortality in patients with chronic HF. In a 6 months period, a 3 mmHg reduction in estimated PA diastolic pressure was associated with a 19.2% reduction in mortality risk whereas 5 mmHg reduction was associated with a 30% reduction. Contrarily, a rise of 3 mmHg in the estimated PA diastolic pressure was associated with 23.8% increase in mortality risk while an increase of 5 mmHg after 6 months was associated with a 42.8% increase in mortality risk.

Cardiac output is the volume of blood that the heart pumps in a time interval of one minute [25]. The changes in cardiac function associated with HF result in a decrease in CO [13]. According to the definition of European Society of Cardiology, HF is due to a structural and/or functional abnormality of the heart that results in elevated intracardiac pressures and/or inadequate cardiac output at rest and/or during exercise [13]. Therefore, two essential physiological parameters to assess the early development of HF are PAP and CO.

1.2 State-of-the-Art Hemodynamic Monitoring

Hemodynamic monitoring plays a crucial role in the management of HF patients. The pulmonary artery catheter (PAC) [26] is the current "gold standard" for measuring the PAP and CO directly and simultaneously [27]. However, this invasive technique is limited to intensive care settings and operating rooms and is not suitable for RPM. There are also other hemodynamic monitoring systems such as pulse wave analysis, echocardiography, Doppler ultrasonography, carbon dioxide rebreathing, and bioimpedance [12, 27]. However, these methods are limited in accuracy as they do not directly measure the CO and are also not suitable for RPM, outside of the critical care or in-hospital environment. The demand for remote hemodynamic monitoring has led to the development of devices such as the CardioMEMS^{TM} HF System, Cordella^{TM} HF System, and the USCOM device. These devices will be explained and compared in the following sections. The current state-of-the-art implantable remote hemodynamic monitoring device in the market is CardioMEMS^{TM} HF System. By providing accurate PAP measurements during the CHAMPION trial [9], it showed a 37% reduction in the relative risk of HF hospitalizations and a significant improvement in the quality of life of HF patients.

1.2.1 Pulmonary Artery Catheter (PAC)

The pulmonary artery catheter (PAC) is a thin, flexible tube with a small balloon at the tip that is inserted into a PA during a procedure called pulmonary artery catheterization or right heart catheterization. Fig. 1.1 illustrates the process of PAC. The technique was introduced by Drs. Swan and Ganz in 1970 [26] and is the current "gold standard" in hemodynamic monitoring [12, 27]. It has a key advantage over many other systems in that it provides simultaneous measurements of other hemodynamic parameters in addition to CO, including PAP, right-sided and left-sided filling pressures, and mixed venous oxygen saturation [12].

The thermodilution technique computes CO by timing the temperature change of a set volume of cold injectate as it travels a set distance to the PAC temperature sensor [12]. This technique offers a direct and accurate CO measurement, combined with other useful indicators. The drawbacks include invasive equipment carrying potential severe complications and requiring complex calibrations, making it unsuitable outside of highly monitored environments, technical factors affecting measurements, and intermittent measurements [27]. Most importantly, it is not suitable for telemonitoring.

1.2.2 CardioMEMS^{TM} HF System

CardioMEMS^{TM} HF System [29] from Abbott is the state-of-the-art PAP-guided remote hemodynamic monitoring device in the market. The system is passive and consists of a capacitive pressure sensor and an inductor [30]. Pressure applied to the capacitive sensor leads to a characteristic shift in the resonant frequency, and by applying electromagnetic signals from an external station, this data is transmitted to the external base station. Fig. 1.2(a) shows the

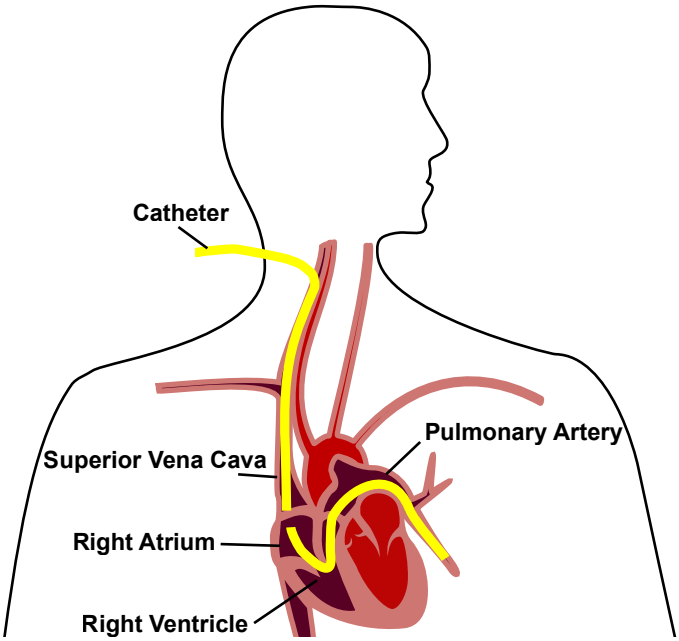


Figure 1.1: Process of pulmonary artery catheter. Adapted from [28].

implantable sensor unit hermetically sealed by glass and having two nitinol loops to permanently anchor the implant in a branch of the PA. It is small in size, measuring 3.5 mm × 2 mm × 15 mm, suitable for endovascular delivery and permanent implantation [31].

Several clinical trials demonstrated its long-term safety and clinical efficacy [32, 33], and Food and Drug Administration (FDA) approved it in 2014 for PAP monitoring in HF patients. The system has a small size, a good safety profile, a simple implantation procedure, and provides an accurate PAP measurement comparable to the Swan-Ganz method [31, 34]. In the CHAMPION trial, CardioMEMS^{TM} guided therapy led to a 37% reduction in HFHs at 1 year [32]. The extended efficacy of pressure-directed HF therapy was demonstrated using CHAMPION trial data, with HFHs reduced by 33% over the randomized access process and 48% over the open access process over 31 months follow-up [34]. Despite its undeniable advantage for remote hemodynamic monitoring, CardioMEMS^{TM} relies only on PAP to assess cardiovascular status, giving a limited understanding of the HF mechanism. Recently, it was used to estimate the CO using a software algorithm calculating CO based on the analysis of pressure waveforms [35]. However, it does not measure the CO directly, only estimates it based on pressure waveforms.

1.2.3 Cordella^{TM} PAP Sensor

The Cordella^{TM} PAP Sensor from Endotronix is a prototype device and is not currently approved for clinical use in any region. Similar to CardioMEMS^{TM}, it is a PAP-guided HF management system [36, 37]. Cordella^{TM} is a passive system consisting of a capacitive pressure sensor and an inductor [38]. The pressure data from the capacitive sensor is transmitted to an

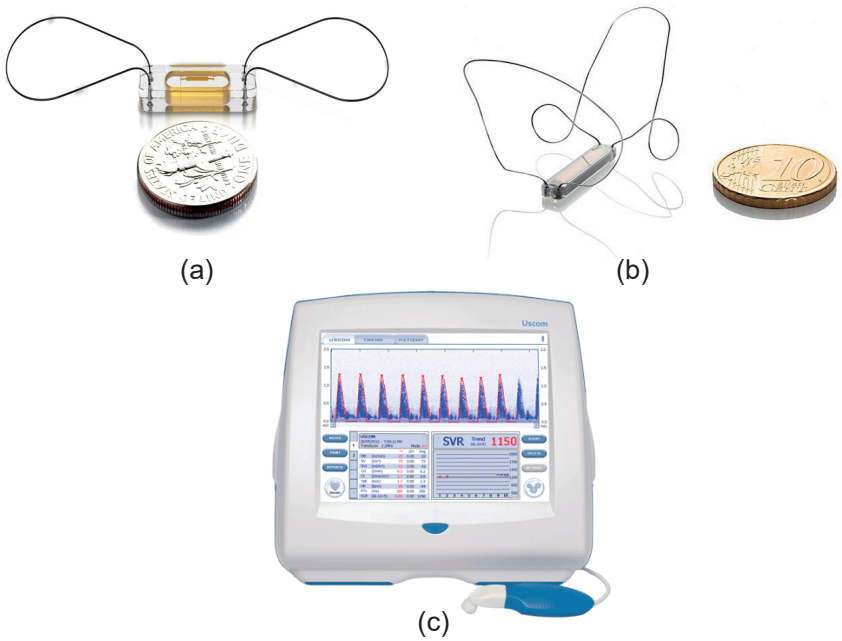


Figure 1.2: Existing remote hemodynamic monitoring devices: (a) CardioMEMS^{TM} HF System of Abbott, the state-of-the-art PAP-guided implantable hemodynamic monitoring device in the market. (b) Cordella^{TM} PAP Sensor of Endotronix, an investigational device similar to CardioMEMS^{TM}. (c) Ultrasound Cardiac Output Monitor (USCOM) device for non-invasive CO monitor based on Doppler ultrasound technology. Photos from [29],[39],[40]

external base station using electromagnetic signals via inductive coupling. Fig. 1.2(b) shows the hermetically sealed implantable sensor having two nitinol anchoring loops.

The results of the first-in-human clinical study (SIRONA) [36] showed that the implantation of the Cordella^{TM} sensor was safe, feasible, and provided accurate PAP measurements that were comparable to those obtained with the Swan-Ganz catheter. However, the rates of HF hospitalization were found to be higher than those seen with the CardioMEMS^{TM}. The PROACTIVE-HF clinical studies [37] are currently underway to evaluate the effectiveness of the system. In December 2021, the FDA approved changing the trial to a single-arm study with pre-specified safety and effectiveness endpoints, in order to provide objective evidence of a similar risk-benefit profile to the CardioMEMS^{TM}. Like the CardioMEMS^{TM}, Cordella^{TM} sensor relies on PAP to assess the cardiovascular status and does not measure the CO, giving a limited understanding of the HF mechanism.

1.2.4 Ultrasound Cardiac Output Monitor (USCOM)

The Ultrasound Cardiac Output Monitor (USCOM) device is a non-invasive CO monitor based on continuous wave Doppler ultrasound (US) technology [41]. The device can measure CO from the pulmonary or aortic valve by measuring blood flow velocity through the valve using the Doppler effect. When measured by echocardiography, CO is defined as the product of

stroke volume (SV) and heart rate (HR), where SV is velocity time integral (VTI) multiplied by the cross-sectional area (CSA) of the artery or valve [25]:

$$CO_{[\frac{ml}{min}]} = VTI_{[\frac{cm}{beat}]} \times CSA_{[cm^2]} \times HR_{[\frac{beats}{min}]}. \tag{1.1}$$

For cardiac output measurement at the pulmonary valve, the ultrasound probe is placed on the patient's chest and directed at the pulmonary valve [42]. Blood flow velocity is measured by the Doppler effect, but the CSA of the valve is only estimated based on the patient's age and weight [42, 43]. Fig. 1.2(c) shows the USCOM device with its ultrasound probe.

This non-invasive device was approved by FDA in 2005, but has been found to have poor agreement with the CO measurements obtained using the pulmonary artery catheter method [42]. This is likely due to the fact that the USCOM device does not directly measure the cross-sectional area of the valve, which is a significant source of error in CO measurements [25, 42]. To measure the CO accurately, the CSA should be directly measured.

1.3 Thesis Goal

The goal of this thesis is to develop an advanced, implantable wireless system for remote hemodynamic monitoring of HF patients. This system aims to enable direct, continuous (24/7), and simultaneous measurement of the PA pressure and artery cross-sectional area, using ultrasound technology for wireless power transfer and data communication. The main advancements of this thesis include:

1. Development of a miniaturized and energy-efficient bridge-to-digital converter enabling duty-cycling of the piezoresistive pressure sensors to achieve an ultra-low power pressure sensing system for direct and continuous (24/7) PAP measurement.

2. Development of a novel method for direct and continuous (24/7) measurement of the CSA of an artery, based on the inductance change of the anchoring loops mounted on a miniaturized system implanted in a section of the artery.

3. Development of a wireless ultrasonic power and data platform for efficient powering and robust communication of deeply implanted medical devices.

4. Integration of the system in a miniaturized biocompatible package enabling permanent implantation in the pulmonary artery.

1.3.1 System Overview

In this thesis, an implantable active system for direct and remote hemodynamic monitoring, specifically for PAP and artery CSA measurements, is developed. Fig. 1.3(a) illustrates the concept of the deep implantable system placed in a branch of the pulmonary artery. A wireless

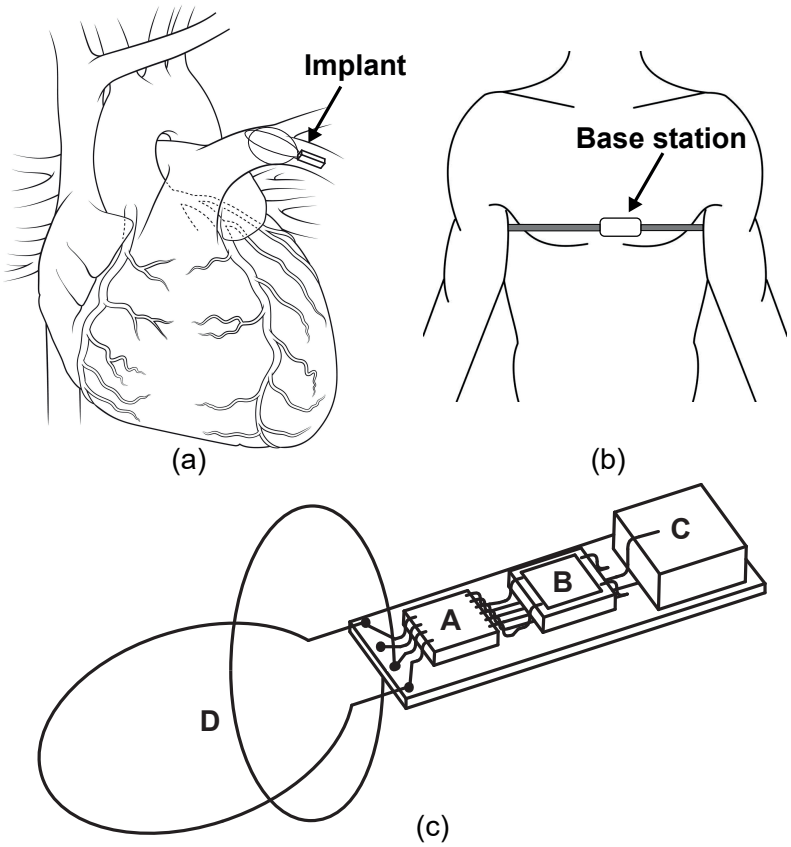


Figure 1.3: (a) Conceptual view of the remotely powered deep implant placed in the PA. (b) An example of placement for the external base station for wireless power and data transfer. (c) The implantable system consisting of (A) a piezoelectric transducer, (B) a piezoresistive pressure sensor, (C) an ASIC, and (D) two conductive anchoring loops.

ultrasonic power transfer solution is used with the deep implant, with an external piezoelectric transducer placed over the implanted unit. Fig. 1.3(b) shows an example of a placement for the external unit.

The proposed system requires low power consumption for remote powering and a small volume for implantation in the PA. As demonstrated in Fig. 1.3(c), the implantable system comprises a piezoelectric transducer, a piezoresistive pressure sensor, an application-specific integrated circuit (ASIC), and two conductive anchoring loops. Ultrasound is the most efficient method to power small-volume implants at great depths and achieves state-of-the-art performance in depth/volume ratio [44, 45]. In this thesis, a single piezoelectric transducer is used in the implant as a transceiver for both power harvesting and data communication. Piezoresistive pressure sensors, implemented as microelectromechanical systems (MEMS) and configured in a Wheatstone bridge, are widely used to measure pressure thanks to their small size and high accuracy [46, 47, 48, 49, 50, 51]. A miniature piezoresistive pressure sensor is employed to accurately measure the pressure. The ASIC consists of sensor readout circuits,

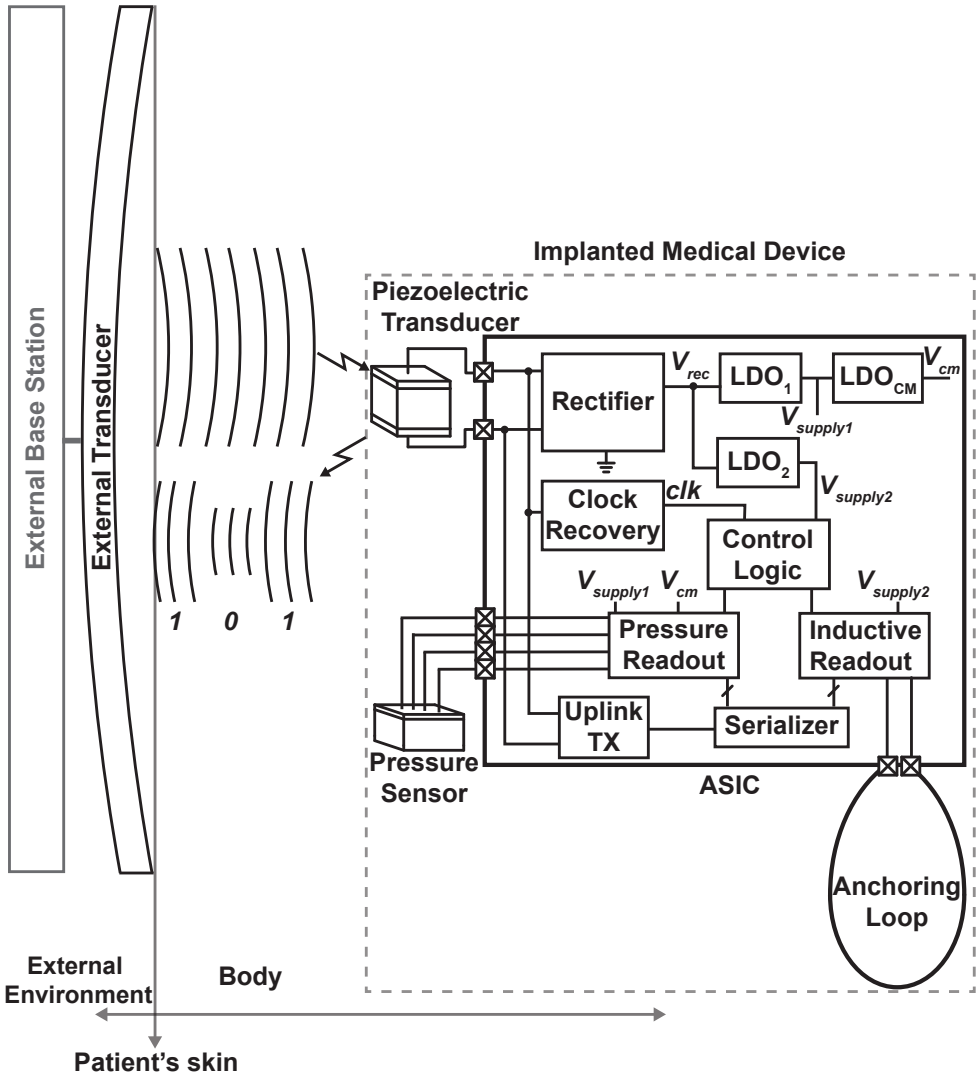


Figure 1.4: Block diagram of the complete system with the US link.

power management, and communication blocks. Implantable hemodynamic monitoring devices such as CardioMEMS^{TM} and Cordella^{TM} use nitinol-based anchoring loops for implant placement in the PA. This work employs conductive anchoring loops for both fixing the implant in the PA and measuring its cross-sectional area, by exploiting the inductive characteristic of the conductive anchoring loops.

Fig. 1.4 shows the complete system with the US link. An external transducer, which is an annular array transducer consisting of 10 rings, converts electrical power into acoustic power and transmits the acoustic power toward the implant. Hence, a second transducer, which is in the implant, converts the acoustic power into electrical power to energize the implanted device. Then, the implanted device sends the data relative to the sensor activity back to the external transducer by backscattering. The external base station is not in the scope of this thesis and waveform generators are used to drive the external transducer.

1.3.2 System Specifications

Deep implantation of the proposed system in the PA presents certain physical limitations. To minimize blockage of blood flow in the PA, it is essential that the implant occupies a small volume. The dimensions of the implant are designed to be 3.2 mm × 2 mm × 10 mm, which is comparable to FDA-approved implantable devices. Additionally, the system should consume low power for remote powering at great depths.

The system will be powered by ultrasound and must comply with FDA safety regulations, that is, the maximum acoustic intensity must not exceed 7.2 mW/mm^2 [52]. Since US signals experience low tissue attenuation [53], milliwatt power levels can be safely transferred. To stay safe within FDA regulations, the system's total power budget is aimed to be less than 100 µW. The system requires significant implantation depths, which can range from 5 cm to 12 cm depending on the patient. For this study, the powering distance is set to be around 8.5 cm.

Patients are considered at risk for HFH if their pressures are higher than 35 mmHg for systolic, 15-20 mmHg for diastolic, and 20-25 mmHg for mean PAP [9]. To cover high-pressure limits and allow calibration for atmospheric pressure, the pressure range is selected to be from –135 mmHg to +135 mmHg. To achieve accurate PAP monitoring by detecting fast peaks of systolic and diastolic pressure changes, the pressure resolution is set to be higher than 0.5 mmHg, and the system's bandwidth ranges from 0 to 450 Hz. Therefore, the pressure readout circuit requires a 10-bit analog-to-digital converter (ADC) with a sampling rate of 1 kilo-samples-per-second (kS/s). In a study involving 3171 volunteers [54], the mean PA diameter was measured to be 25.1 ± 2.8 mm and can be as high as 30 mm. In addition, the lateral resolution of echocardiography, which is the clinical standard for artery CSA measurement, is typically around 1 mm [55]. As an improvement, the resolution of the diameter measurement is set to 0.25 mm in a diameter range from 20 mm to 30 mm. An oscillator-based inductive readout circuit is designed and uses a 12-bit counter to achieve sufficient resolution. The pressure readout creates a 10-bit output code per conversion while the inductive readout generates 12-bit output code. To cover the 22-bit sensor output and some additional bits for preambles, the data rate is set to 40 kilo-bits-per-second (kbps). Overall system specifications are summarized in Table 1.1. In order to meet these specifications, the ASIC was designed and fabricated using a 180-nm standard CMOS technology. This technology node is chosen thanks to its low cost and sufficiently high core and IO voltages to supply the piezoresistive sensors and power management circuits. Since the input voltage of the rectifier is always lower than 3.3 V peak-to-peak, there is no need to use a high-voltage (HV) CMOS technology.

1.4 Thesis Contributions

The building blocks of the proposed system shown in Fig. 1.4 are presented in the following chapters. The main contributions of this thesis consist of proposing a novel energy-efficient bridge-to-digital converter enabling ultra-low conversion energy in piezoresistive sensor systems, an innovative system to directly measure the CSA of an artery based on the inductance

Table 1.1: System specifications for the remote hemodynamic monitoring implant.

Implant Volume (mm^3)	3.2 × 2 × 10
Power Budget (μW)	100
Powering Distance (cm)	~ 8.5
Pressure Range (mmHg)	–135 to +135
Pressure Resolution (mmHg)	0.5
Artery Diameter Range (mm)	20 to 30
Diameter Resolution (mm)	0.25
Data Rate (kbps)	40

change of the implant's anchoring loops, a wireless ultrasonic power and data platform for powering and communication of deeply implanted medical devices, and a biocompatible and hermetic glass packaging approach for low-cost and long-lasting implants. In this collaborative work, Dr. Kerim Türe from the EPFL Radio Frequency Integrated Circuits Group designed the wireless powering and communication circuits, and some blocks of the inductive readout. The implantable and external piezoelectric transducers were designed and fabricated by IMASONIC, whereas Yalosys developed the glass package for the implant.

1.5 Thesis Outline

This thesis is organized as follows:

- In Chapter 2, an energy and area-efficient capacitively-coupled chopper instrumentation amplifier (CCCIA) for implantable bridge sensor systems is proposed.
- In Chapter 3, an innovative energy-efficient bridge-to-digital converter for pressure-sensing implants is presented. This chapter introduces a novel spinning method exploiting duty cycling to reduce the power consumption of the bridge sensor and the instrumentation amplifier (IA) while inherently cancelling the IA's offset and 1/f noise.
- In Chapter 4, a novel system for direct measurement of the artery CSA is proposed. This system exploits the inductive characteristic of an anchoring loop that mounts the implant in a branch of the artery.
- In Chapter 5, a wireless ultrasonic power and data platform is introduced for efficient powering and robust data communication of deeply implanted medical devices.
- In Chapter 6, a biocompatible and hermetic glass packaging approach is discussed and *in vitro* experimental results are presented.
- In Chapter 7, the thesis conclusion and potential future research are discussed.

2 Energy and Area-Efficient Capacitively-Coupled Chopper IA

This chapter presents an energy and area-efficient capacitively-coupled chopper instrumentation amplifier (CCCIA) dedicated to implantable bridge sensor systems. Its target application is an implantable pressure sensing system used to measure the pulmonary artery pressure (PAP), which is particularly relevant for monitoring heart failure (HF) and pulmonary hypertension (PH) patients. The CCCIA employs chopper stabilization to decrease its offset and 1/f noise. The resulting ripple due to the up-modulated offset and 1/f noise is suppressed by a switched-capacitor (SC) ripple reduction loop (RRL). The gain of the instrumentation amplifier (IA) is defined by a programmable capacitive feedback network with a gain range from 40 V/V to 116 V/V, making it suitable for use with bridge sensors having different output voltages. The proposed CCCIA was designed and fabricated in a standard 180-nm CMOS technology. It achieves an input-referred noise density of 88.2 nV/$\sqrt{\text{Hz}}$, a worst-case input offset of 5 µV, and a noise efficiency factor (NEF) of 6.2 while drawing 3.3 µA current from a 1.2 V supply. The SC RRL suppresses the output ripple to less than 185 µV at all harmonics. The CCCIA achieves state-of-the-art performance in terms of small area, occupying only 0.17 mm^2. The results make the system suitable for implantable bridge sensor systems. Some parts of this chapter were published in [56, 57].

This chapter is organized as follows: Section 2.1 provides an overview of instrumentation amplifiers. Section 2.2 describes the design and implementation of the proposed CCCIA, whereas the details of the implemented ripple reduction loop are presented in Section 2.3. Section 2.4 summarizes the measurement results and Section 2.5 concludes the chapter.

2.1 Overview of Instrumentation Amplifiers

Instrumentation amplifiers are commonly used to detect low-amplitude signals from sensors. A typical implantable sensing system is composed of a bridge sensor and its readout circuit, which consists of an IA followed by an analog-to-digital converter (ADC). Fig. 2.1 shows the conventional readout circuit for piezoresistive sensors configured in a Wheatstone bridge. To accurately amplify low-amplitude output signals of sensors in an energy-efficient way, the IA

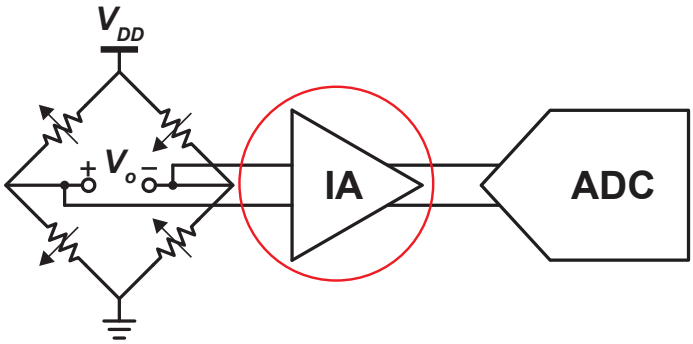


Figure 2.1: Conventional readout circuit for Wheatstone bridge sensors.

should have low offset, low noise, and low power consumption [58, 51, 59, 60, 61, 62, 63]. Since most sensor applications operate near DC with a bandwidth of a few hundred Hz, the IA's offset and 1/f noise significantly degrade the amplifier performance. Fig. 2.2 shows the low-frequency noise spectrum of CMOS amplifiers. The worst-case offset of a CMOS differential amplifier can be as large as 10 mV. Additionally, the 1/f noise dominates the low-frequency spectrum and is inversely proportional to the frequency, with a typical 1/f noise corner of a few kHz to tens of kHz [64]. To achieve accurate and energy-efficient measurements, several techniques such as auto-zeroing, correlated double sampling, and chopping have been used for low-frequency noise and offset cancellation [64]. The chopping technique is superior to other techniques since it provides a continuous-time output and does not cause noise folding. Moreover, it is more energy-efficient than other dynamic offset cancellation techniques.

The IA determines the system's energy efficiency since the main noise contribution comes from its input stage. The classic 3-Opamp IA and the current-feedback IA have two noise-critical input stages, while the capacitively-coupled IA (CCIA) has only one [65]. Therefore, the CCIA delivers the best performance in terms of both accuracy and energy efficiency [62]. It achieves a high gain accuracy without any extra cost since on-chip capacitors have excellent matching characteristics. In addition, the input capacitors of the CCIA block the common-mode (CM) input voltages of the Wheatstone bridge and allow using different supply voltages for the resistive bridge and the readout circuit [50].

Although the capacitively-coupled chopper instrumentation amplifier provides highly accurate and energy-efficient measurements, it has two main drawbacks. Firstly, the up-modulated offset and 1/f noise of the amplifier generates a large ripple at the output of the IA. Several ripple-reduction techniques have been proposed to suppress the output ripple [62, 66, 67, 68]. Secondly, the chopping technique reduces the input impedance of the IA to less than 10 MΩ at typical chopping frequencies. This input impedance is high enough for most of the resistive bridges since their equivalent resistances are usually lower than 10 kΩ. For the applications requiring very-high input impedance, a positive feedback loop has been proposed to boost the CCCIA's input impedance [62].

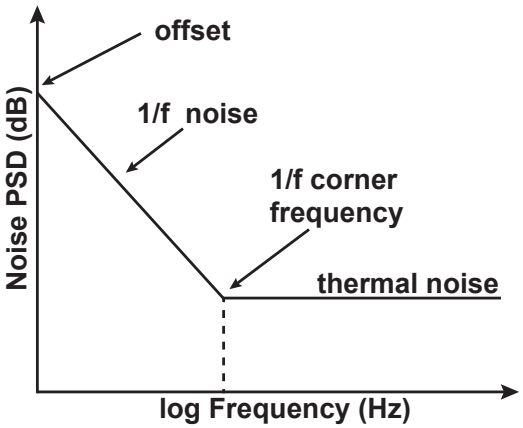


Figure 2.2: Low-frequency noise spectrum for CMOS amplifiers.

2.2 Design of an Energy and Area-Efficient CCCIA

An energy and area-efficient CCCIA was designed and implemented to be used in implantable bridge sensor systems. It amplifies the output of a bridge sensor accurately and energy-efficiently to profit from the full input range of the succeeding ADC.

2.2.1 Topology and Design Considerations

Fig. 2.3 shows the schematic of the CCCIA consisting of a two-stage Miller-compensated operational transconductance amplifier (OTA) (G_{m1} and G_{m2}), a programmable capacitive feedback network to set the gain (C_{in} and C_{fb}), three chopper switches (CH_{in}, CH_{out} and CH_{fb}), and high-value pseudo-resistors (R_b and R_{fb}) to set input common-mode (CM) level. The IA's gain is accurately defined by C_{in}/C_{fb}, where C_{fb} are 3-bit programmable capacitor arrays. It is a 3-bit controlled variable gain amplifier (VGA) that enables tuning the input range of the IA for different bridge sensors and avoids the saturation of the IA output arising from the bridge offset.

Chopper modulation enables the cancellation of the amplifier's 1/f noise and input offset. The DC and low-frequency signals at the output of the bridge are converted to higher-frequency AC signals by input chopper switches (CH_{in}) and then capacitively coupled to the input of G_{m1}. The up-modulated input signals are amplified by G_{m1} and then demodulated back to the baseband by output chopper switches (CH_{out}), while the 1/f noise and offset of G_{m1} is up-modulated away from the signal band. As a result, the IA can achieve very low input noise and input offset, thus enabling a high accuracy at low frequencies [64]. Thanks to G_{m1}'s high gain, the noise and offset contributions of the following stages are negligible. The DC gain (A_0) of the OTA is designed to be larger than 100 dB to achieve a high gain accuracy. In order to obtain such a high gain, a two-stage Miller compensated amplifier is employed (G_{m1} and G_{m2}).

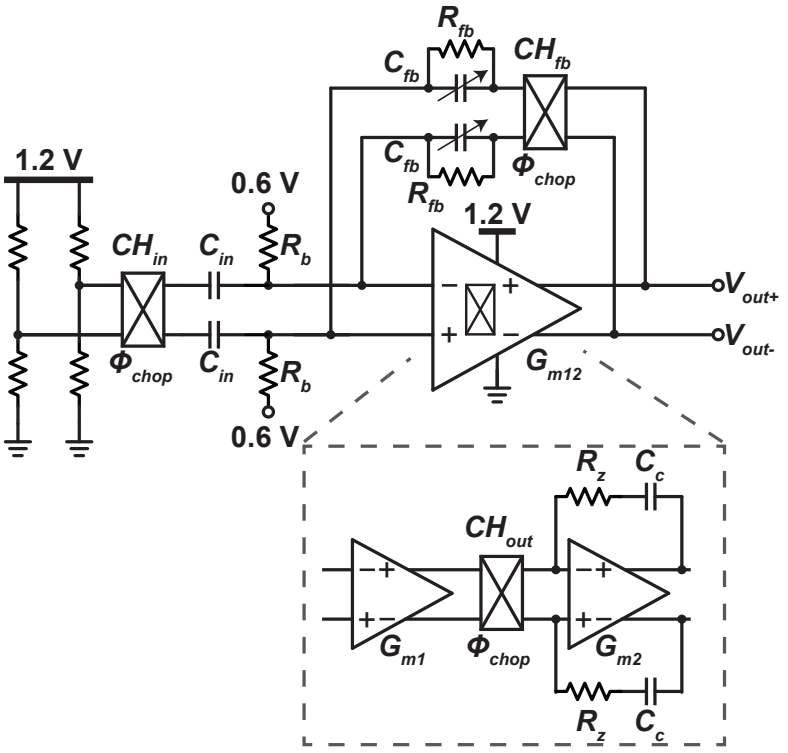


Figure 2.3: Schematic of the CCCIA with a bridge sensor.

Chopper stabilization provides continuous-time operation and can achieve microvolt offset and very low 1/f noise. However, this technique has two main drawbacks. Firstly, the up-modulated offset and 1/f noise of G_{m1} inevitably appear as an output ripple. The amplitude of the ripple can be estimated [62] by

$$V_{ripple} = \frac{V_{os} \times G_{m1}}{2 \times f_{chop} \times C_c}, \tag{2.1}$$

where V_{os} is G_{m1}'s offset. The output ripple voltage can consume too much headroom at low supply voltages and has to be removed. Thus, this ripple is suppressed by an additional ripple reduction loop (RRL). Secondly, the input impedance of the CCCIA at DC is defined [62] by a switched-capacitor (SC) resistor formed by CH_{in} and input capacitors (C_{in}):

$$Z_{in,DC} = \frac{1}{2 \times f_{chop} \times C_{in}}. \tag{2.2}$$

Since C_{in} is usually in the order of a few pF, the input impedance of a chopped amplifier is limited to ~10 MΩ, which is lower than the DC input impedance of non-chopped amplifiers.

The chopper frequency, f_{chop}, is one of the most important design parameters. It must be higher than the 1/f noise corner of G_{m1} to eliminate the 1/f noise completely. On the

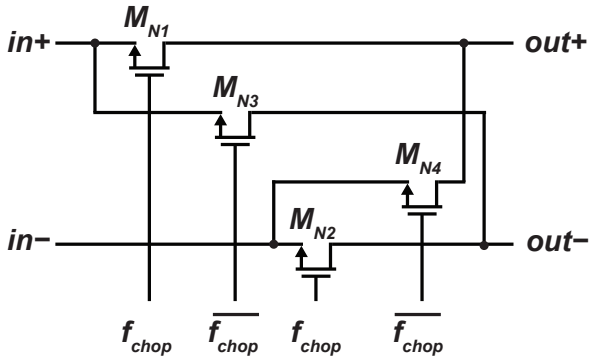


Figure 2.4: Schematic of a chopper switch based on four NMOS transistors.

other hand, the charge injection and clock feedthrough at the CH_{in} lead to a residual offset proportional to f_{chop} [64]. Therefore, f_{chop} must be carefully chosen since increasing f_{chop} reduces the input noise but also increases the residual offset. In addition, increasing f_{chop} reduces the amplitude of the output ripple whereas it decreases the DC input impedance of the CCCIA. Therefore, the chopper frequency has to be carefully selected in a precise frequency range.

2.2.2 Implementation

The chopper frequency is selected to be 10 kHz in order to be higher than the 1/f noise corner frequency of G_{m1} and to be low enough to achieve a low residual offset and high input impedance. To apply chopper modulation and demodulation, polarity-reversing chopper switches are implemented. As shown in Fig. 2.4, the chopper switches are made of four NMOS switches driven by clock signals with two complementary phases at f_{chop}. The size of the NMOS switches should be minimized to suppress the charge injection and clock feedthrough errors [64]. However, the noise of the on-resistor of the input chopper switches has to be low enough for low-noise operation. As a compromise, NMOS switches with a width (W) of 880 nm and length (L) of 180 nm are employed. In order to achieve effective offset cancellation, the two complementary chopping clocks must have a 50% duty cycle and have transitions at the same time. A D-flip-flop-based divider-by-two circuit is placed very close to each chopper switch to ensure a 50% duty cycle[69]. Two buffers are used at the outputs of clock dividers to drive the nearby chopper switches with complementary clock signals having very low rise and fall times.

The gain of the CCCIA is defined by the capacitive ratio C_{in}/C_{fb}. The feedback capacitors are programmed by 3 configuration bits and the gain settings are 40, 44, 48, 54, 69, 80, 96, and 116 V/V, thus making the IA flexible for different bridge sensors. Apart from f_{chop}, the value of input capacitors, C_{in}, is also an important design parameter. It has to be minimized to save the chip area and to keep the input impedance of the CCCIA as high as possible. In addition, the transient settling of the CCCIA is limited by the time constant determined by the pseudo

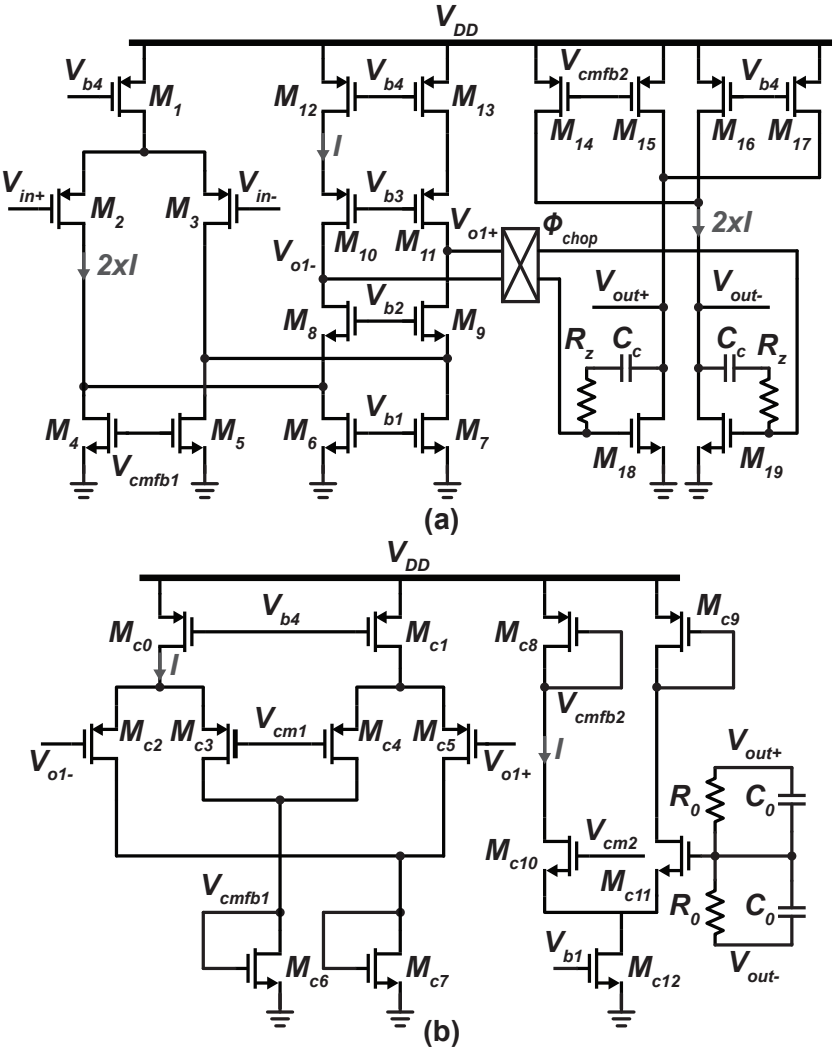


Figure 2.5: Schematic of (a) the two-stage Miller OTA (G_{m1} and G_{m2}) with (b) two seperate CMFB circuits.

resistors and input capacitors. C_{in} has to be low enough to achieve a sufficient settling. On the other hand, C_{in} should be high to suppress the input-referred noise of the biasing resistors and to limit the error caused by parasitic terms in the low-value feedback capacitors. As a compromise, C_{in} is selected to be 5 pF. If the parasitics are neglected, the selected f_{chop} and C_{in} result in a DC input impedance of about 10 MΩ, which is high enough for most of the resistive bridges since their equivalent resistances are usually lower than 10 kΩ. High-value pseudo resistors [70] (R_b and R_{fb}) based on MOS transistors operating in the sub-threshold region are employed for the input biasing of the OTA since they occupy a considerably smaller area than physical resistors.

The DC gain of the CCCIA OTA has to be high enough to suppress the gain error. The closed loop gain (A_{CL}) of the CCCIA is defined as:

$$A_{CL} = \frac{A_0}{1 + (A_0 \times \frac{C_{fb}}{C_{in}})}, \tag{2.3}$$

where A_0 is the DC open-loop gain of the OTA. To ensure a gain error less than 0.1% for a closed-loop gain of 100 V/V (40 dB), a fully differential two-stage RC compensated Miller OTA with a DC gain of about 100 dB is designed. Fig. 2.5 shows the schematic of the CCCIA OTA with its CM feedback (CMFB) circuits. For a high DC gain, G_{m1} is implemented as a folded-cascode amplifier with a PMOS input pair biased in weak inversion. For a large output swing, G_{m2} is implemented as a common-source amplifier in the succeeding stage. The currents that circulate in the folded and common-source branches are scaled by a factor of two to improve the noise efficiency, and the unity current (I) in Fig. 2.5 is 200 nA. To avoid instability in any mismatch and process variation conditions, RC compensation is employed. G_{m1} is 12.3 µS and the Miller capacitors C_c are selected to be 11.4 pF, which results in a unity-gain frequency of 170 kHz.

As shown in Fig. 2.5(b), two separate CMFB circuits are implemented to properly set the output CM voltages of the first and second stages. The first stage employs an amplifier with two differential pairs [71], while the second stage faces the large swing of the differential output with a resistive divider and an amplifier [72]. The divider uses relatively large resistors, R_0 = 2.5 MΩ, to avoid limiting G_{m2}'s output resistance. To achieve the maximum output swing at a 1.2 V supply voltage, the CM voltages of both stages (V_{cm1} and V_{cm2}) are set to 0.6 V.

2.3 Ripple Reduction Loop (RRL)

The up-modulated offset and 1/f noise of G_{m1} create an output ripple. The output ripple can be as high as the supply voltage and has to be removed. A low-pass filter (LPF) could be used to suppress the ripple, but it would require large resistors and capacitors, and a first-order LPF cannot sufficiently suppress such a large output ripple when f_{chop} is not very high [56]. Therefore, a switched-capacitor (SC) RRL [62] is designed and implemented.

2.3.1 Topology and Design Considerations

In the designed CCCIA, G_{m1} = 12.3 µS, f_{chop} = 10 kHz, and C_c = 11.4 pF. If the worst-case offset of G_{m1} is estimated to be 10 mV, the output ripple is approximately

$$V_{ripple} = \frac{V_{os} \times G_{m1}}{2 \times f_{chop} \times C_c} = \frac{10mV \times 12.3\mu S}{2 \times 10kHz \times 11.4pF} = 540mV. \tag{2.4}$$

Such a high voltage level would consume too much headroom for a 1.2 V supply and has to be removed. Fig. 2.6 shows the block diagram of the SC RRL to effectively suppress the large output ripple.

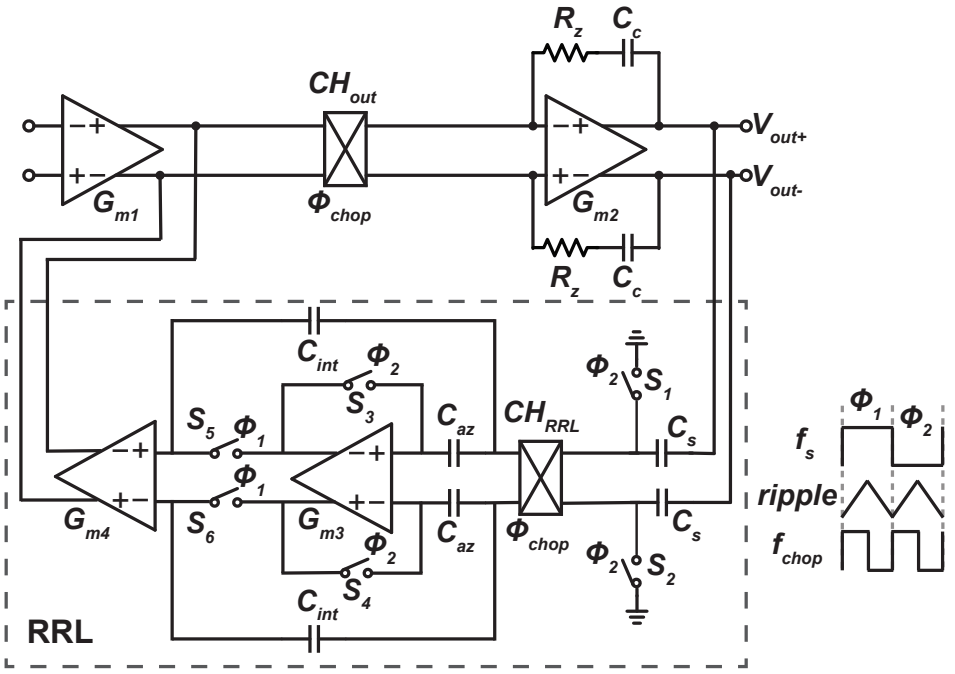


Figure 2.6: Schematic and timing diagram of the SC RRL.

The output ripple appears at the chopping frequency. In this design, the switching frequency (f_s) is selected to be half of f_{chop}, which is equal to 5 kHz. The first half cycle of f_s serves as an integration phase (Φ_1) whereas the second half cycle acts as an auto-zero phase (Φ_2) [62]. During Φ_1, the output ripple voltage is converted into an AC current by the sampling capacitors (C_s), and then the RRL switches (CH_{RRL}) demodulate this AC current back to DC. After that, this current is integrated by the integrator, which is built around G_{m3}, into a voltage and then G_{m4} converts this voltage into a current that compensates the offset current of G_{m1}.

Although the offset of G_{m1} is sufficiently suppressed, G_{m3}'s offset generates an error voltage at the output of the integrator, which appears as an additional ripple at the CCCIA's output. Therefore, the auto-zero technique is adopted during Φ_2 to eliminate the introduced ripple by G_{m3}'s offset. During Φ_2, C_s are shorted to the ground to prevent the integration of any ripple current. G_{m3} is configured in unity-gain, and its offset is sampled and stored in auto-zero capacitors, C_{az}. Integration capacitors, C_{int}, are disconnected from the output of G_{m3} to hold the voltage at the end of Φ_1, and they are connected to G_{m4}'s input. This solution provides the correct injection of a compensating current into G_{m1} during both phases and eliminates the output ripple [62].

2.3.2 Implementation

The SC RRL shown in Fig. 2.6 creates a notch in the transfer function of the CCCIA. The center frequency of the notch is equal to the chopper frequency, and the main design parameters of the SC RRL are the notch width ($2f_{0RRL}$) and the ripple suppression factor (F). Half of the

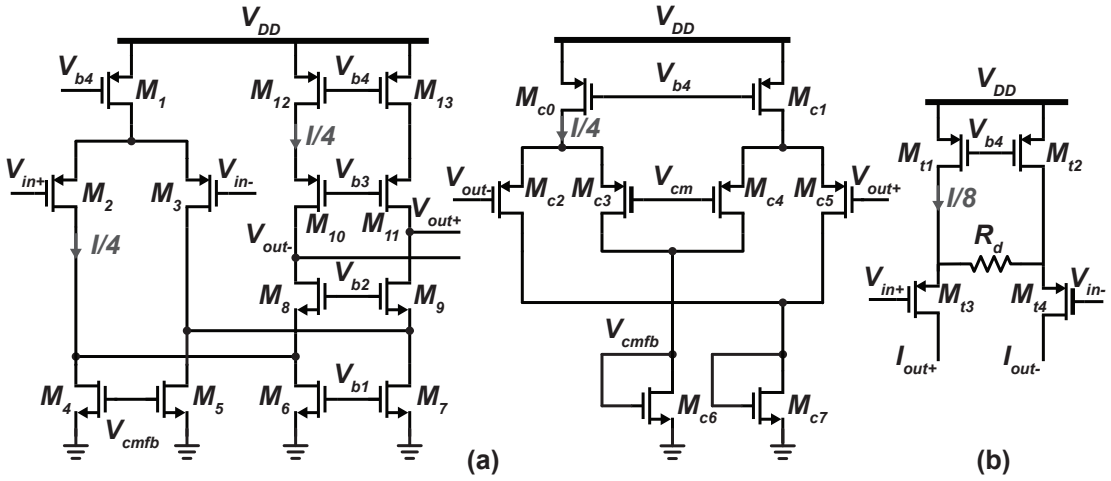


Figure 2.7: Schematic of the (a) SC RRL integrator OTA (G_{m3}) with its CMFB circuit, and (b) the compensation transconductor (G_{m4}).

notch width is defined [62] as

$$f_{0RRL} = \frac{G_{m4} \times C_s}{2\pi \times C_c \times C_{int}}. \tag{2.5}$$

The RRL injects noise into the CCCIA via the transconductor G_{m4}. To minimize the noise contribution of the SC RRL, G_{m4} has to be much smaller than G_{m1}. In this work, G_{m1} is 12.3 µS, and G_{m4} is designed to be 0.65 µS, which is 19 times smaller than G_{m1}. In addition, the generated notch must be outside of the CCCIA's signal band. In the CCCIA, C_s is 11.4 pF, and to save chip area, C_s and C_{int} are selected to be 0.72 pF and 2.87 pF, respectively. As a result, f_{0RRL} is equal to 2.28 kHz, and the notch is well outside of the signal bandwidth.

The second design parameter is the ripple suppression factor [62], which is

$$F = \frac{A_{Gm3} \times G_{m4}}{2 \times C_c \times f_{chop}}, \tag{2.6}$$

where A_{Gm3} is the DC open-loop gain of G_{m3}. Eq. 2.4 shows that the assumed ripple for the worst case is 540 mV. A_{Gm3} has to be high to sufficiently suppress this worst-case ripple.

Fig. 2.7 shows the schematics of (a) G_{m3} and (b) G_{m4}. To achieve a high DC gain, G_{m3} employs a folded-cascode OTA with its CMFB circuit. The simulated A_{Gm3} is about 74 dB, resulting in a suppression factor of 83 dB. To make the noise contribution of the RRL negligible, G_{m4} must be much smaller than G_{m1}. However, G_{m4} should provide sufficient current to compensate for the maximum offset current of G_{m1}. Therefore, source degeneration is applied to G_{m4}, and G_{m4} = 0.65 µS.

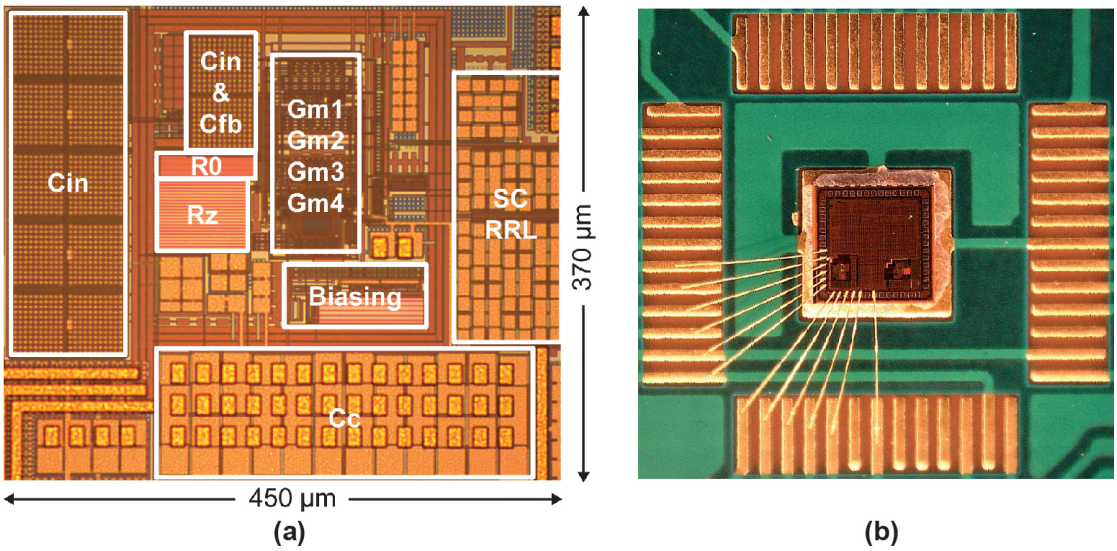


Figure 2.8: (a) Die micrograph of the CCCIA and (b) photo of the test PCB with the wire-bonded IC.

To ensure an efficient design, the current consumption of the RRL should be smaller than that of the CCCIA. Therefore, the currents flowing through the branches of G_{m3} and G_{m4} are respectively 8 and 16 times lower than the current flowing through the input devices of G_{m1}. To achieve a high area efficiency, the RRL capacitors are smaller than C_c, which has a value of 11.4 pF. The SC RRL has a total capacitance of 10 pF and consumes only 350 nA current. Therefore, its area and power consumptions are negligible compared to the CCCIA. Moreover, the RRL eliminates the need of using an LPF [56], which requires a large chip area.

2.4 Measurement Results

The CCCIA was designed and fabricated in a 180-nm standard CMOS process. Fig. 2.8(a) shows the die micrograph, whose core area is 0.17 mm^2. The IC was wire-bonded to a test PCB, as shown in Fig. 2.8(b). The total current consumption of the IC is 6.3 µA from a 1.2 V supply. However, when the consumption of the current reference circuit for biasing is not considered, the CCCIA draws only 3.3 µA current.

Fig. 2.9(a) shows the closed-loop frequency response of the CCCIA for different gain configurations. The gain can be adjusted between 32.1 dB (40 V/V) and 41.3 dB (116 V/V) by trimming the feedback capacitor C_{fb}. This allows for tuning the input range of the IA from ±4 mV to ±12 mV for different bridge sensors and to handle the bridge offset not to saturate the output of the IA. To measure the output noise spectrum density of the CCCIA, an external low-noise amplifier (LNA) with a gain of 1.3 V/V is connected to the output of the CCCIA and acts as a differential to single-ended buffer to drive the spectrum analyzer. Fig. 2.9(b) shows that the measured output noise at the highest gain configuration is 13.3 µV/$\sqrt{\text{Hz}}$, which

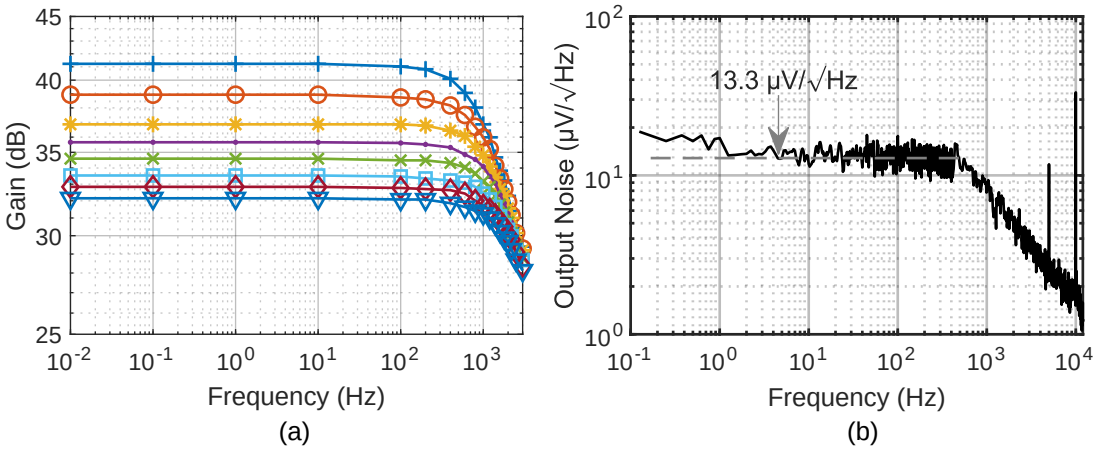


Figure 2.9: (a) Measured frequency response for different gain configurations and (b) output noise spectrum at the highest gain configuration.

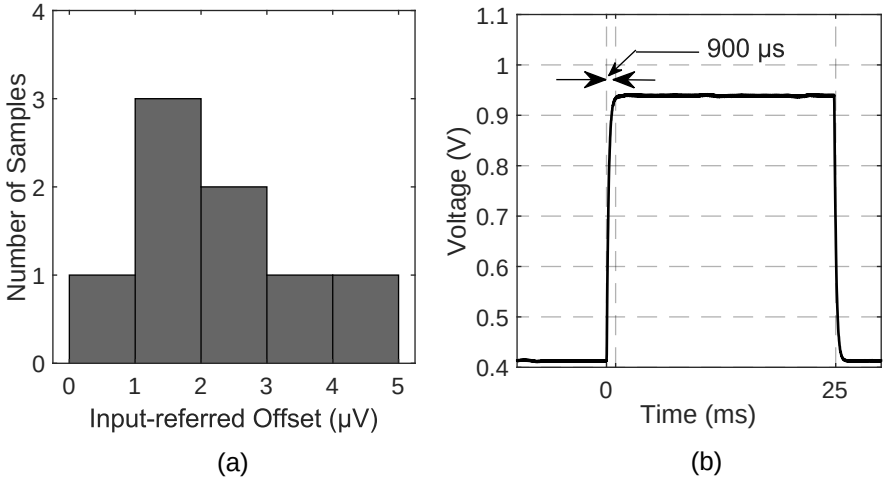


Figure 2.10: Measured (a) input-referred offset and (b) transient step response.

is equivalent to an input-referred noise of 88.2 nV/$\sqrt{\text{Hz}}$ when the gains of the CCCIA and LNA are 116 V/V and 1.3 V/V, respectively. Additionally, the output noise is almost flat until 100 mHz, demonstrating effective cancellation of the 1/f noise. The measured input-referred noise density ($v_{n,in}$) and the current consumption result in a noise efficiency factor given by

$$NEF = v_{n,in}\sqrt{\frac{2I_{tot}}{\pi U_T 4kT}} = 6.2. \tag{2.7}$$

A histogram of the measured input-referred offset is represented in Fig. 2.10(a). For 8 samples operating at f_{chop} = 10 kHz, the CCCIA's measured offset is lower than 5 μV. Fig. 2.10(b) demonstrates that the settling time of the CCCIA is equal to 900 μs when a 5 mV input step is

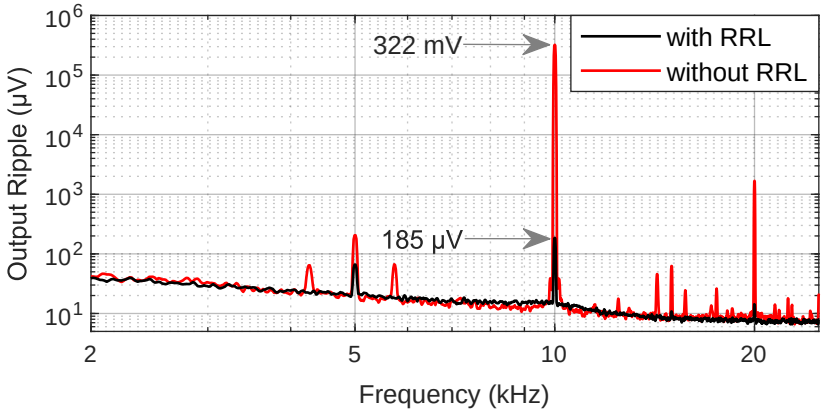


Figure 2.11: Measured output ripple with and without the RRL.

Table 2.1: CCCIA's performance summary and comparison with the state of the art.

	ISSCC 2013[58]	JSSC 2017[59]	TCAS1 2021[60]	JSSC 2022[61]	**This Work**
Technology (nm)	700	180	180	180	**180**
Supply Voltage (V)	5	2.7-3.6	1.2	1.8	**1.2**
Supply Current (µA)	8	75	0.6	210	**3.3**
Gain Range (V/V)	>20	1-128	100	-	**40-116**
Input Offset (µV)	3	<3.5	-	0.4	**<5**
Input Noise (nV/$\sqrt{\text{Hz}}$)	55	19	190	20	**88.2**
NEF	6.1	6.4	3.5	7.3	**6.2**
Chip Area (mm^2)	1.35	0.53	0.57	0.55	**0.17**

applied. Fig. 2.11 shows the spectrum of the output ripple with and without the RRL. The SC RRL suppresses the amplitude of the output ripple by about 65 dB, from 322 mV to 185 µV.

The performance of the designed CCCIA is summarized and compared with the state-of-the-art IAs in Table 2.1. This work achieves the smallest area and has a very low power consumption that makes it suitable for use in implantable sensor systems. Besides, the 3-bit controlled programmable gain with a range from 40 V/V to 116 V/V enables tuning the input range of the IA for different bridge sensors. It achieves a competitive NEF equal to 6.2 and its input noise, offset and output ripple are low enough for most implantable bridge sensor applications.

2.5 Conclusion

This chapter presented an energy and area-efficient CCCIA for implantable bridge sensor systems. The proposed CCCIA was designed and fabricated in a 180-nm standard CMOS technology. It has a core area of 0.17 mm^2 and consumes only 3.3 µA current from a 1.2 V supply. With a 3-bit controlled variable gain ranging from 40 V/V to 116 V/V, it is suitable for use with different bridge sensors, while also avoiding the saturation of the IA output caused by the bridge offset. The CCCIA achieves an input-referred noise density of 88.2 nV/$\sqrt{\text{Hz}}$, an input offset of less than 5 µV, and a NEF of 6.2. The SC RRL effectively suppresses the output ripple to less than 185 µV at all harmonics, achieving a suppression rate of 65 dB. Overall, the CCCIA presents state-of-the-art performance in terms of small area, and its power consumption, input noise, input offset, and output ripple values are low enough to be used in implantable bridge sensor systems.

3 Energy-Efficient Bridge-to-Digital Converter for Pressure Monitoring

This chapter presents an energy-efficient, duty-cycled, and spinning excitation bridge-to-digital converter (BDC) for use in implantable pressure sensing systems. The circuit provides the measure of the pulmonary artery (PA) pressure, which is particularly relevant for the monitoring of heart failure (HF) and pulmonary hypertension (PH) patients. The BDC is composed of a piezoresistive pressure sensor and a readout integrated circuit (IC) consisting of an instrumentation amplifier (IA) followed by an analog-to-digital converter (ADC). The proposed design spins both the bridge excitation and the ADC's sampling input voltages simultaneously and exploits duty cycling to reduce the static power consumption of the bridge sensor and IA while cancelling the IA's offset and 1/f noise at the same time. The readout IC was designed and fabricated in a standard 180-nm CMOS process and achieves 8.4 effective number of bits (ENOB) at 1 kHz sampling rate, while drawing 0.53 μA current from a 1.2 V supply. The BDC, built with the readout IC and a differential pressure sensor having 5 kΩ bridge resistances, achieves 0.44 mmHg resolution in a 270 mmHg pressure range at 1 ms conversion time. The current consumption of the bridge sensor is reduced by 99.8% by employing duty cycling, thus becoming 0.39 μA from a 1.2 V supply. The total conversion energy of the pressure sensing system is 1.1 nJ, achieving a figure-of-merit (FoM) of 3.3 pJ/conversion, which both values represent the state of the art. Some parts of this chapter were published in [73, 74].

The organization of the chapter is as follows: Section 3.1 provides an overview of the building blocks of implantable pressure sensing systems, whereas the working principle of the proposed duty-cycled and spinning excitation BDC is described in Section 3.2. Section 3.3 summarizes the BDC system design with its specifications. The design and implementation details of the IA and SAR ADC are explained in Sections 3.4 and 3.5, respectively. Section 3.6 reports the experimental results and Section 3.7 provides the conclusion.

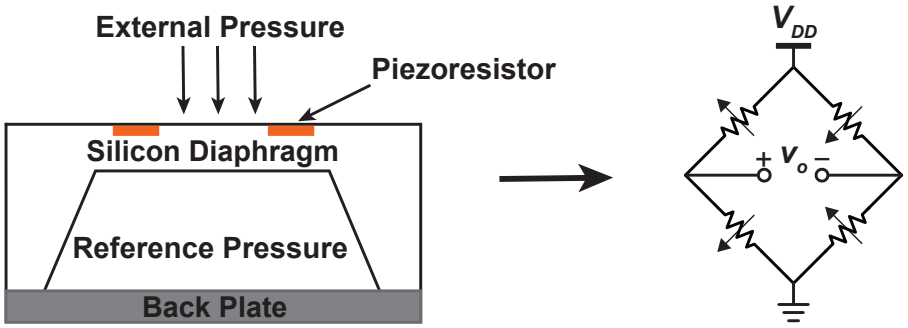


Figure 3.1: Schematic view of a piezoresistive pressure sensor.

3.1 Overview of Implantable Pressure Sensing Systems

Several pressure monitoring systems for implantable and wearable medical devices have been reported in the literature [75, 76, 46, 47, 48]. Implantable and wearable systems require sensors having small volume due to the limited space. Miniature pressure sensors are implemented as microelectromechanical systems (MEMS), combining silicon based microelectronics and micromachining technology. Piezoresistive and capacitive MEMS pressure sensors are widely used for their high accuracy in a space-limited region [77, 78].

Capacitive sensors have the advantages of low energy consumption and low temperature drift, but suffer from non-linearity of the output response. Moreover, they provide lower output signals and require complex readout electronics [79]. Piezoresistive sensors configured in a Wheatstone bridge are an effective solution and widely used to measure pressure, temperature, and humidity, thanks to their small size and high accuracy [46, 47, 48, 49, 50, 51, 80]. In addition, they have a highly-linear output and simpler readout circuit compared to capacitive sensors. However, resistive sensors are power-hungry and have the drawbacks of zero-pressure offset voltage and thermal drift [79].

In this thesis, a piezoresistive pressure sensor is chosen due to its simplicity, small size, and high accuracy. Since the pressure sensor in this application is intended to measure the blood pressure in the PA, it will operate under stable temperature conditions, and the temperature drift will be negligible. In order to handle the zero-pressure offset and to decrease the power consumption, special circuit techniques are used in the sensor interface.

As shown in Fig. 3.1, a typical piezoresistive pressure sensor consists of four piezoresistors diffused on the silicon diaphragm and connected in a Wheatstone bridge configuration. The pressure difference between the external and reference pressures deforms the flexible silicon membrane, and the amount of this deformation is converted to an electrical signal by the bridge [78, 79]. The pressure sensor in Fig. 3.1 has a back plate to fix the reference pressure of the sensor. If the reference pressure is vacuum enclosed in the sensor, such devices are known as absolute pressure sensors. To measure the difference between any two pressures, the back plate can be removed, and two different pressures can be applied from two sides of the silicon

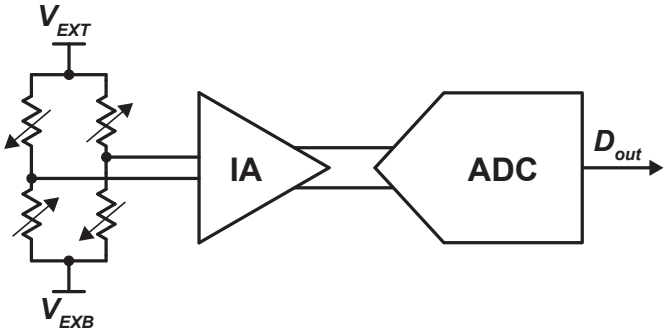


Figure 3.2: Conventional bridge-to-digital converter (BDC).

diaphragm. Such sensors are known as differential pressure sensors. If the reference part of the sensor is exposed to ambient pressure, it is known as a relative (gauge) pressure sensor and determines the external pressure with respect to ambient or atmospheric pressure [78].

Piezoresistive sensors typically generate low amplitude signals in the millivolt range. In order to monitor pressure values, these small signals must be amplified and converted into a digital output. Fig. 3.2 shows a conventional bridge sensor readout, also known as a bridge-to-digital converter (BDC). The BDC consists of an instrumentation amplifier (IA) followed by an analog-to-digital converter (ADC). In conventional BDCs, the top excitation voltage (V_{EXT}) of the bridge is connected to a DC biasing voltage, while the bottom excitation (V_{EXB}) is grounded. In addition, the IA should have low noise, low offset, and low power consumption to accurately and energy-efficiently amplify the bridge sensor's output, in order to utilize the full input range of the succeeding ADC [65]. While the bridge measurement can achieve high resolution and accuracy, the bridge itself tends to be the most power-hungry block of the analog front-end. The excitation energy consumption of the bridge is higher than the interface circuit's conversion energy due to low bridge resistances, thus limiting the overall sensor energy efficiency [50]. Recent works, such as [47, 49, 51, 80] have used duty-cycling of the bridge to reduce its energy consumption.

Apart from the bridge sensor, a low-noise and low-power readout IC is required to achieve an energy-efficient BDC. Several techniques such as auto-zeroing, correlated double sampling, and chopping have been widely used for noise and offset cancellation [64]. The IA typically determines the energy efficiency of the readout circuit since the main noise contribution arises from its input stage. As explained in Chapter 2, capacitively-coupled chopper IA (CCCIA) delivers the best performance in accuracy and energy efficiency [65]. However, the CCCIA generates a large ripple at the output; an additional circuitry such as a ripple reduction loop is required to eliminate this drawback [62]. This solution increases the energy consumption, chip area, and design complexity of the system.

This thesis proposes a novel technique that involves applying duty cycling to the bridge sensor while simultaneously spinning its excitation voltage. The sensor's excitation energy consumption is reduced by a factor of 640 times. Additionally, this system avoids complex

IAs that foresee offset-reduction techniques or need calibration. A novel spinning method simultaneously applied to the bridge sensor and the capacitive digital-to-analog converter (DAC) of the successive-approximation-register (SAR) ADC inherently suppresses the 1/f noise and offset of the IA, eliminating the need for offset-reduction techniques such as chopper modulation. The IA is also duty-cycled to decrease its power consumption by a factor of 427 times. This novel architecture enables to achieve very low energy consumption in the bridge sensor and readout circuit at the same time and makes the bridge sensor suitable for implantable medical devices.

3.2 Duty-Cycled and Spinning Excitation BDC

The proposed BDC consists of a duty-cycled and spinning excitation bridge sensor, a duty-cycled IA, and a spinning SAR ADC. Fig. 3.3 shows its circuit diagram. The spinning and duty cycling operation uses switches controlled by the amp, $spin+$, and $spin-$ signals. The switches controlled by $spin+$ and $spin-$ signals simultaneously spin both the bridge excitation (V_{EXT}, V_{EXB}) and the capacitive DAC's sampling inputs (V_{OP}, V_{ON}). These switches reverse the supply connections of the bridge so that during one phase, the bridge's output is $+V_{BR}$, and during the other phase, the output is equal and opposite, $-V_{BR}$. The duty-cycled IA is active when the amp signal is high.

The excitation switches of the bridge sensor operate like the modulation switches of the chopping technique as they reverse the signal at the output. The IA amplifies the modulated signal and the low-frequency spurs made by the IA offset and the 1/f noise component. Indeed, the amplification of the IA offset (V_{OS}) and the 1/f noise component also make the IA's output. Instead of using a demodulating chopper for cancelling the low-frequency spurs, the circuit implements the following scheme. During the first spin, half of the positive DAC array charges to V_{OP} while half of the negative DAC array charges to V_{ON}. When the bridge excitation reverses, the second half of the positive DAC array charges to V_{ON}, and the second half of the negative DAC array charges to V_{OP}. The bridge is 640 times duty-cycled in 1 ms conversion time, and $spin+$ and $spin-$ are high for 781.25 ns. Since the time separation of the two spinning phases is less than 800 ns and the estimated 1/f noise corner is 20 kHz, there is a strong correlation between the 1/f noise components sampled on the two halves of the DAC array. As a result, the total charge on the capacitive DAC arrays depends only on the bridge signal and compensates for the 1/f noise and offset.

This method not only avoids a second chopper but also directly eliminates the offset contribution, without requiring the use of a digital filter used to remove the spur components caused by the square wave modulation of the offset and the 1/f noise at the chopping frequency. The mismatch between the two halves of the capacitive arrays may lead to a residual offset. Still, this error is minimal if the circuit uses relatively large unity capacitors in the DAC array. It becomes negligible when it is less than the step resolved by the SAR ADC.

The timing diagram shown in Fig. 3.3 describes the working principle of this innovative

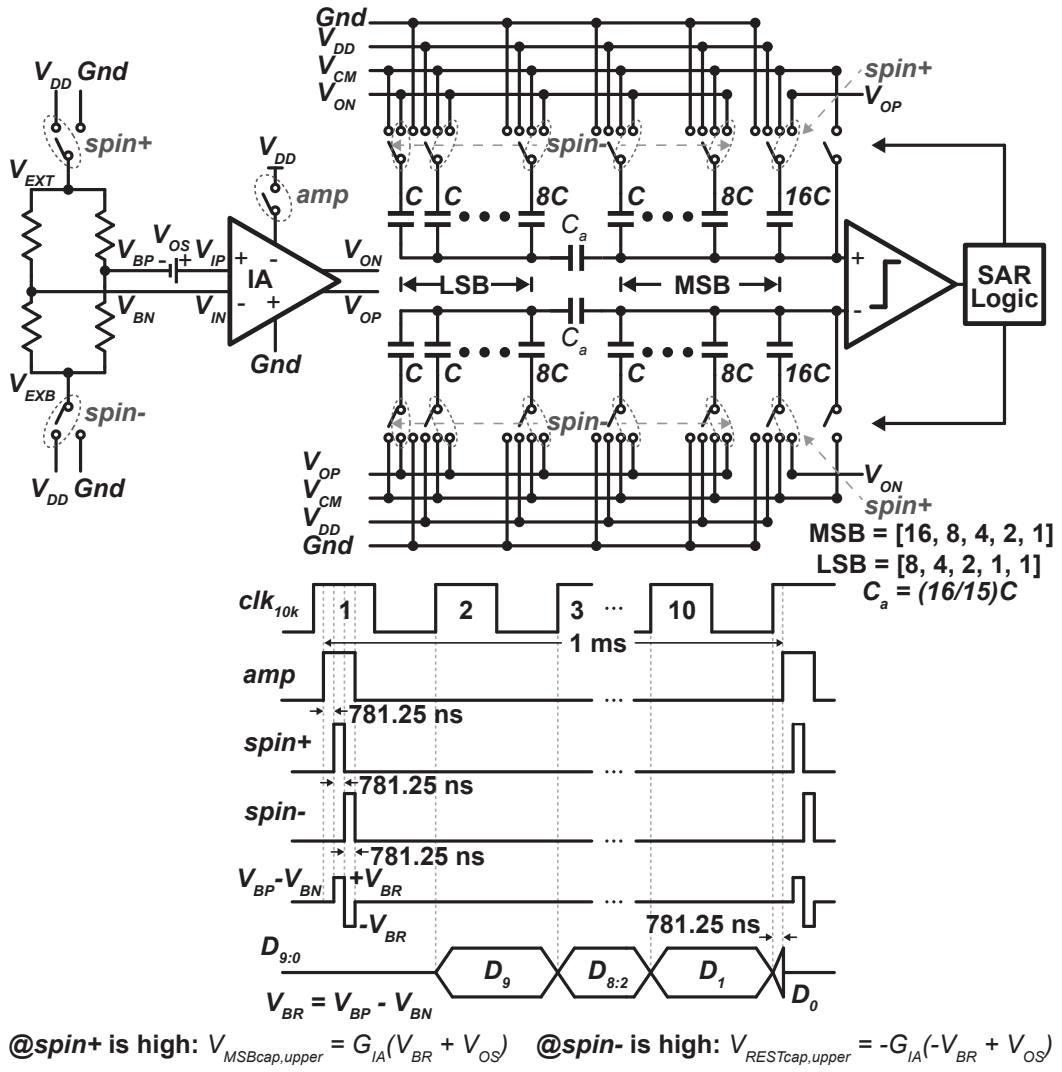


Figure 3.3: Circuit diagram of the highly duty-cycled and spinning excitation BDC, and its timing diagram.

topology in detail. The bridge sensor and the IA are not active at the beginning of a conversion cycle. Then, the IA is powered up starting from the rising edge of the amp signal, 781.25 ns ahead of the activation of the bridge. After that, $spin+$ is high for 781.25 ns to connect the top excitation voltage (V_{EXT}) of the bridge to V_{DD} while the bottom excitation voltage (V_{EXB}) goes to ground to generate the bridge output $+V_{BR}$. To prevent a short circuit in the bridge, $spin+$ becomes low before $spin-$ rises, and then $spin-$ is high for another 781.25 ns for generating the bridge output $-V_{BR}$. The bridge is active for only 1.5625 µs when either $spin+$ or $spin-$ is high, and the IA is active for 2.3437 µs out of 1 ms conversion time when amp is high. Therefore, the energy consumption of the bridge and the IA are respectively 640 and 427 times less than an equivalent static DC biasing.

When $spin+$ is high, the most significant bit (MSB) capacitor ($16C$) of the DAC positive array

is charged to V_{OP}, while the DAC negative array's MSB capacitor ($16C$) is charged to V_{ON}. All the other DAC capacitors remain floating during $spin+$. When $spin-$ is high, the remaining capacitors of the DAC positive array, which are equivalent to $16C$, are charged to V_{ON} while the MSB capacitor is floating. Similarly, V_{OP} charges the remaining capacitors of the DAC negative array, and the MSB capacitor is floating. As a result, the total charges in the positive and negative DAC arrays depend only on the two phases of the bridge signal ($+V_{BR}$ and $-V_{BR}$). The operation acts as a correlated double sampling over the IA offset and compensates for it since the MSB capacitor and the remaining capacitors' array are equal.

3.3 System Design

The proposed BDC requires low energy consumption to be remotely powered and a small size to be implanted in the body. As depicted in Fig. 3.3, it consists of a piezoresistive pressure sensor, an IA, and a succeeding SAR ADC.

Patients are considered at risk for HF hospitalization if their pressures are higher than 35 mmHg for systolic, 15-20 mmHg for diastolic, and 20-25 mmHg for mean PAP [9], and PH is defined by a mean PAP of 20 mmHg or more at rest [81]. To cover high-pressure limits, the pressure range of the system is selected to be from 0 to 135 mmHg. Since the atmospheric pressure decreases with increasing altitude, an additional margin in the negative pressure is also necessary. Therefore, the overall pressure range with respect to the reference pressure (1 atm = 760 mmHg) is chosen to be from –135 to +135 mmHg, enabling calibration of the BDC with respect to the ambient pressure. For accurate PAP monitoring, the pressure resolution is higher than 0.5 mmHg. The system's bandwidth ranges from 0 to 450 Hz to precisely detect fast peaks of systolic and diastolic pressure changes.

Bridge sensors typically generate low-amplitude signals in the millivolt range, and a typical readout circuit uses an IA before the ADC. Highly duty-cycled bridge sensor requires higher bandwidth, which increases the power consumption of the IA. Lowering the duty cycle could decrease the IA's power dissipation, but it would not be sufficient to keep the bridge's average power consumption below 1 µW. To solve this issue, the IA is also duty-cycled. The clock input frequency is 1.28 MHz and the highest possible duty cycle with the used clock is 1/640. The bandwidth and settling time requirements of the IA suggest a more prudent duty cycle of 1/427. As a result, the bridge sensor and the IA are duty-cycled by 640 and 427 times, respectively.

A circuit solution that provides accurate amplification of the bridge sensor's output uses two IA stages, which are capacitively coupled. The first stage ensures low-noise operation, whereas a programmable capacitive feedback network defines the gain of the second stage for exploiting the full input range of the ADC. The variable gain also enables tuning of the IA input range for different bridge sensors and avoids the saturation of the IA's output caused by the bridge offset. For ensuring a pressure resolution of at least 0.5 mmHg and a bandwidth of 450 Hz, the system uses a 10-bit SAR ADC with a sampling rate of 1 kilo-samples-per-second (kS/s). A spinning control logic generates the necessary control signals for the system. As shown in

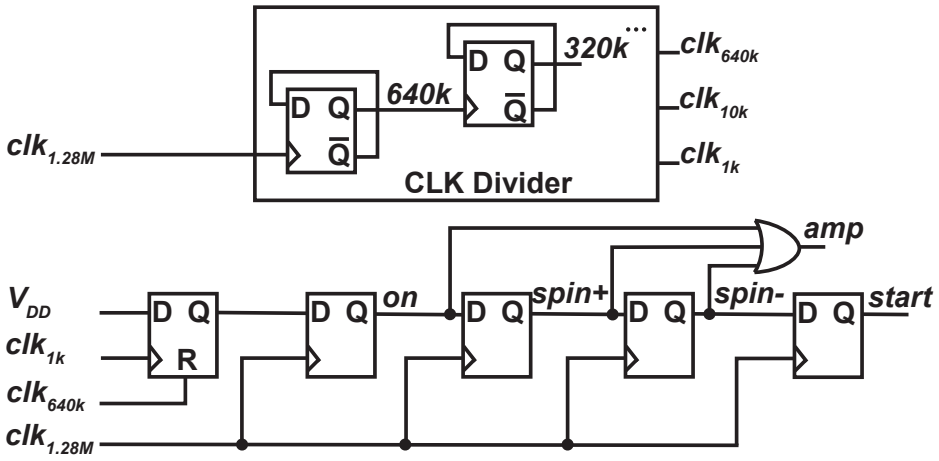


Figure 3.4: Simplified circuit diagram of the spinning control logic.

Fig. 3.4, it consists of a conventional D flip-flop-based clock divider and a set of shift registers. The clock input frequency is 1.28 MHz, which will be recovered from the acoustic waves used for wireless powering. The logic block uses the 1.28 MHz input clock to generate amp, $spin+$, $spin-$, $start$, and the two clock signals at 1 kHz and 10 kHz.

3.4 Capacivitely-Coupled Instrumentation Amplifier (CCIA)

Piezoresistive pressure sensors typically generate low-amplitude signals and these signals should be accurately amplified to profit from the full input range of the succeeding ADC. The gain of the amplification stage is determined by the output range of the sensor. In this work, SM30D [82] differential pressure sensor is used thanks to its small size and pressure range matching well the system's specifications. When biased at 1.2 V, the selected pressure sensor provides a minimum and a maximum full-scale voltages of 14.4 mV and 28.8 mV, respectively. An IA biased at 1.2 V usually has an output swing of 900 mV due to the saturation voltages of NMOS and PMOS transistors at the output stage. To cover the minimum and maximum output voltages of the selected sensor, a programmable capacitive feedback is employed to define the gain of the amplification stage within the gain range of 29 V/V to 72 V/V, thus maximizing the dynamic range of the ADC. The variable gain enables tuning of the IA's input range for different bridge sensors and prevents the saturation of the IA's output caused by the bridge offset.

A CCIA offers the best performance in terms of both accuracy and energy efficiency [62]. Fig. 3.5 shows the distribution of the gain along two stages to optimize the area and power consumption. A single-stage implementation would require larger capacitors and larger bandwidth, which increase the silicon area and the power consumption significantly. The first stage amplifier interfacing with the sensor is critical because of the stringent noise and power consumption request. Thus, a low noise amplifier (LNA) with a mid-band gain of 9 V/V is implemented to optimize the trade-offs between noise, power, and area. The second stage

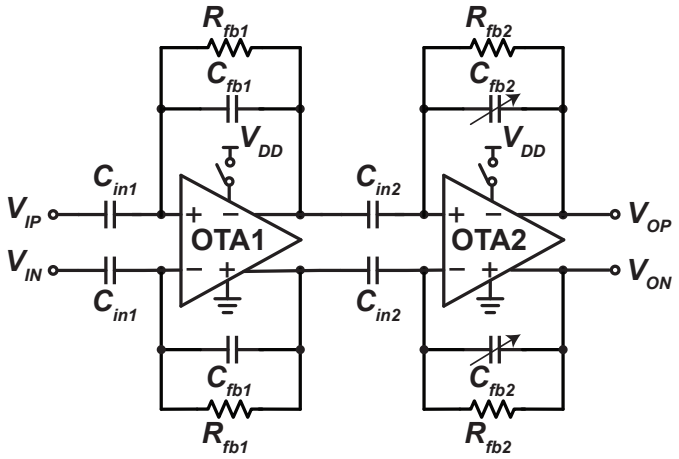


Figure 3.5: Circuit diagram of the capacitively-coupled IA consisting of two gain stages.

is a variable gain amplifier (VGA) maximizing the signal at the input of the ADC. The gain of the VGA is controlled by two bits and varies from 3.2 V/V to 8 V/V.

Since the bridge sensor is 640 times duty-cycled in a 1 ms conversion time and active only for 1.5625 µs, the bandwidth of the CCIA is approximately 1 MHz, which is sufficient to handle high-frequency input components. In addition, the novel spinning method suppresses the offset and 1/f noise, and the IA does not require any offset and low-frequency noise reduction techniques [64]. However, the high bandwidth of the IA imposes a large static current that affects the energy efficiency of the BDC. To address this issue, the 427 times duty cycling makes the CCIA active only for 2.3437 µs in a 1 ms conversion time.

3.4.1 First Stage: Low-Noise Amplifier (LNA)

The mid-band gain of the LNA depends on the capacitive ratio C_{in1}/C_{fb1} and is set to 9 V/V. The minimum value of C_{fb1} is limited by parasitic capacitors in the feedback line, and an increase in the value of C_{in} decreases the input-referred noise of the analog front-end. Fig. 3.6(a) shows the schematic of the LNA. The unity capacitance, C, forming C_{in} and C_{fb1} is chosen to be 56 fF. Therefore, C_{in} and C_{fb1} are respectively 1 pF and 112 fF, relatively large values that decrease the input-referred noise and limit the error caused by parasitic terms.

High-value feedback resistors (R_{fb1}) provide input biasing of the operational transconductance amplifier (OTA) and ensure a high-pass cut-off frequency lower than 3 Hz for all gain configurations. Pseudo-resistors [70] based on two diode-connected PMOS devices in their sub-threshold region are employed to achieve a very high resistance by occupying a small area.

OTA1 requires a high open-loop gain (A_0) to achieve a high gain-accuracy in the closed-loop

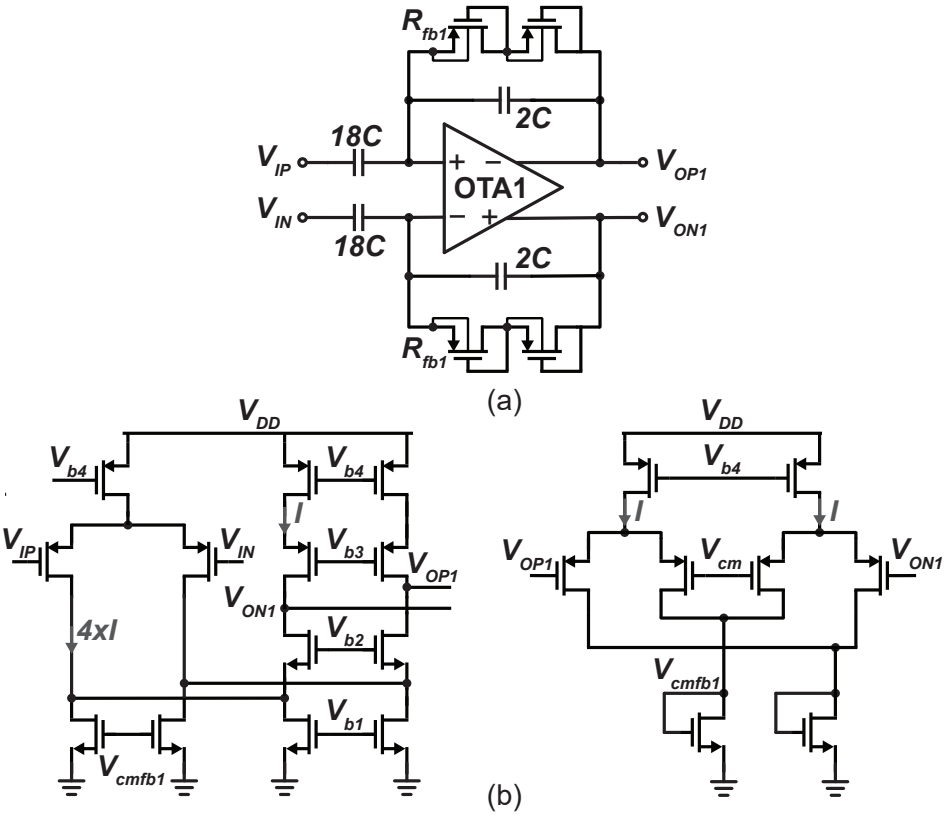


Figure 3.6: Schematics of the (a) low-noise amplifier (LNA) and (b) the folded-cascode (FC) amplifier (OTA1) with its CMFB circuit.

configuration. The closed-loop gain (A_{CL}) of the amplifier is given by:

$$A_{CL} = \frac{\beta}{1 + \frac{\beta}{A_0}}, \tag{3.1}$$

where β is the feedback loop gain defined as C_{in}/C_{fb}. The open-loop gain is ideally infinite, and an infinite A_0 in (3.1) makes the closed-loop gain exactly equal to the feedback loop gain. However, A_0 is finite in reality and leads to closed-loop gain error:

$$Gain\,Error\,(\%) = 100\frac{\beta}{A_0}. \tag{3.2}$$

A folded-cascode (FC) architecture providing high open-loop gain with a single stage is used to implement OTA1 since the first gain stage does not require high output swing. Fig. 3.6(b) shows the schematic of the FC OTA with its common-mode feedback (CMFB) circuit. In order to achieve a noise-efficient operation, the input-pair utilizes large PMOS devices (180 µm / 0.18 µm) biased in weak inversion. Moreover, the currents in the folded branches and CMFB circuit's branches are a factor of four lower than the main current to improve the overall noise efficiency. A CMFB circuit adjusts the output CM voltage of OTA1. As the first gain

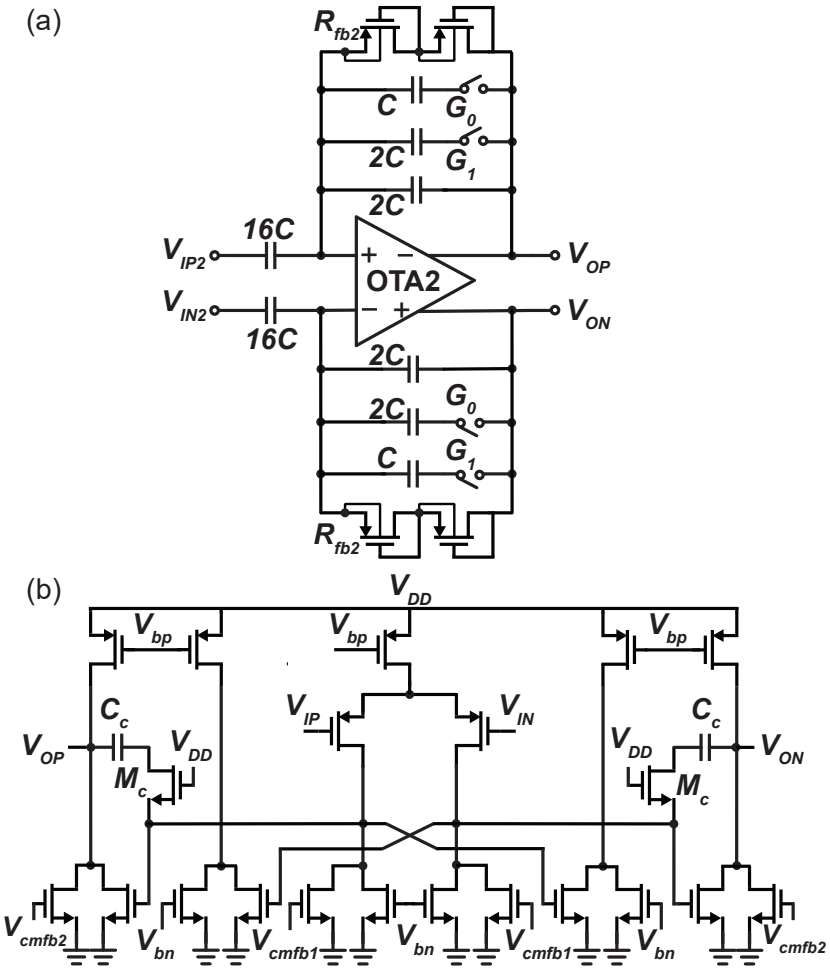


Figure 3.7: Schematics of the (a) variable gain amplifier (VGA) and (b) two-stage Miller amplifier with a class AB output stage (OTA2).

stage does not require high output swing and has very high output resistance, the CMFB topology employing two differential pairs [71] is selected to set the output CM voltage to 0.6 V. Post-layout simulation results show that OTA1 achieves an open-loop gain of 70 dB and a gain-bandwidth product (GBW) of 110 MHz, while drawing 118 µA from 1.2 V. Corner and Monte Carlo simulations verify that OTA1 and its CMFB circuit are stable in any conditions.

3.4.2 Second Stage: Variable Gain Amplifier (VGA)

A VGA is used in the second stage to maximize the dynamic range of the following SAR ADC. Fig. 3.7 (a) shows the schematic of the VGA. Two configuration bits ($G_{1:0}$) set the feedback capacitance to four different values from $2C$ to $5C$, resulting in the following gain settings: 3.2, 4, 5.3, and 8 V/V. Similar to the LNA, the VGA uses a unity capacitance (C) of 56 fF for high gain linearity and sets the input biases of the amplifier with high-value pseudo-resistors (R_{fb2}).

The low-noise requirement of OTA2 is not as strict as that of the LNA since its input-referred noise is divided by the gain of the LNA. Therefore, OTA2 should not dominate the power consumption of the amplification stage. Moreover, OTA2 requires high open-loop gain and large output swing to maximize the signal at the input of the ADC. To achieve this, it is implemented using a two-stage Miller OTA with a class AB output stage.

In order to ensure stability in any mismatch and process variation conditions, the circuit uses the Miller compensation made by the capacitor C_c and M_c, which performs as a resistor. The output stage is an AB scheme that also increases the effective transconductance of the stage by using about half the current of a corresponding class A scheme [83]. This solution improves the power efficiency of the amplification stage. OTA2 uses two separate CMFB circuits for setting the CM voltages of its first and second stages. The first stage uses an amplifier with two differential pairs [71] similar to OTA1, and the second stage faces the large swing of the differential output with a resistive divider and an amplifier [72]. The CM settings of both stages are set to 0.6 V to ensure a maximum output swing at a 1.2 V supply. Post-layout simulation results show that OTA2 has an open-loop gain of 82 dB and a GBW of 32 MHz, while drawing 92 μA from a 1.2 V supply.

3.5 SAR ADC

A 10-bit 1 kS/s SAR ADC is used to digitize the amplified signals. As shown in Fig. 3.3, the SAR ADC consists of two capacitive DAC arrays, sample and hold switches, a low-power dynamic comparator, and synchronous SAR control logic. The fully-differential architecture suppresses the supply noise and achieves a good common-mode noise rejection.

3.5.1 Capacitor Array DAC (CDAC)

A capacitive DAC (CDAC) is usually the most power and area-consuming block of a SAR ADC. In a conventional full binary-weighted CDAC, the number of unit capacitors, C_u, and the area increase exponentially with the number of resolution bits, N. The total capacitance, C_T, in an N-bit conventional full binary-weighted CDAC is $2^N C_u$ [84, 85]. On the other hand, a split CDAC with an attenuation capacitor separates the CDAC into M-bit most significant bit (MSB) and L-bit least significant bit (LSB) arrays. Splitting binary-weighted arrays significantly reduces the number of C_u since it requires $2^M + 2^L$ unit capacitors [86, 87]. For example, a 10-bit full binary weighted CDAC requires 1024 C_u, while splitting the 10-bit CDAC into two 5-bit sub-CDACs requires only 64 C_u. Although the split-capacitor structure reduces the total number of capacitors, it is more sensitive to capacitor mismatch and parasitic capacitance, and requires larger unit capacitors to meet the linearity requirements [85, 87, 88].

The power consumption of capacitor switching and the CDAC area are directly proportional to the size of the unit capacitor. The smallest feasible value for C_u can be determined by one of followings: kT/C noise limit, capacitor matching, parasitic capacitances, and design rules

[85, 89]. The thermal noise has to be lower than the quantization error that sets the SAR ADC's resolution, which can be expressed as:

$$\frac{kT}{C_T} < \frac{V_{LSB}^2}{12} \quad \Rightarrow \quad C_T > 12kT\frac{2^{2N}}{V_{FS}^2}, \tag{3.3}$$

where V_{LSB} is the quantization step and V_{FS} is the full-scale voltage range of the conversion. For 10-bit resolution in a 1.2 V full-scale range, the total DAC capacitance should be larger than 35.9 fF. The fully-differential CDAC structure relaxes the thermal noise constraint further since it doubles the full-scale voltage range. For medium resolutions such as 10-bit, capacitor mismatch and parasitic capacitances are dominant over thermal noise since they can significantly degrade the linearity of the CDAC.

The worst-case standard deviation (σ) of the differential non-linearity (DNL) and the integral non-linearity (INL) determines the value of C_u. The unit capacitors in a CDAC are commonly implemented using Metal-Insulator-Metal (MIM) or Metal-Oxide-Metal (MOM) capacitors. In this design, MIM capacitors make the CDAC since they have a higher capacitance density per area. DNL is usually the most dominant error in a CDAC since its worst-case value is larger than the worst-case INL value. It has been reported that the DNL and INL of the splitting capacitor structure degrade due to its higher sensitivity to capacitor matching and parasitic capacitances [85, 87, 88, 90]. Although the conventional binary-weighted CDAC can achieve high linearity with small unit capacitors, additional considerations must be taken into account. Design rules also set the minimum value of a MIM capacitor. In the used technology, the minimum MIM capacitance is 35.6 fF. A conventional binary-weighted CDAC with a C_u = 35.6 fF would occupy a large area and would be an overdesign because it could achieve sufficient linearity even with lower C_u. A split CDAC with higher C_u but lower C_T can achieve a comparable DNL and INL. Moreover, reducing C_T also improves the energy efficiency of the full system since the IA requires lower power to drive lower capacitance.

The switching operation of the CDAC consumes significant amount of energy, and the value of the C_u is limited by capacitor matching and parasitic effects. To reduce the power consumption further, several switching methods have been proposed [90, 91, 92, 93, 94]. The conventional switching scheme is based on a trial-and-search procedure. Before a conversion cycle, all control bits are preset and they are kept or inverted depending on the comparator's decision. When a control bit needs to be inverted due to a wrong attempt, the switching sequence wastes lots of energy [91]. To achieve a more energy-efficient switching scheme, the V_{cm}-based switching technique [90], which halves the total DAC capacitance, is employed. It respectively grants more than 80% and 30% energy savings compared to the conventional and monotonic switching schemes. This method determines the MSB by connecting the differential arrays to V_{cm} and removes the MSB capacitor to save energy and area. Therefore, the V_{cm}-based switching determines the MSB mismatch independently, and the worst-case DNL and INL occur at $1/4V_{FS}$ and $3/4V_{FS}$, respectively, whereas those of a conventional switching approach happen at $1/2V_{FS}$ due to MSB code transition. As a result, this scheme

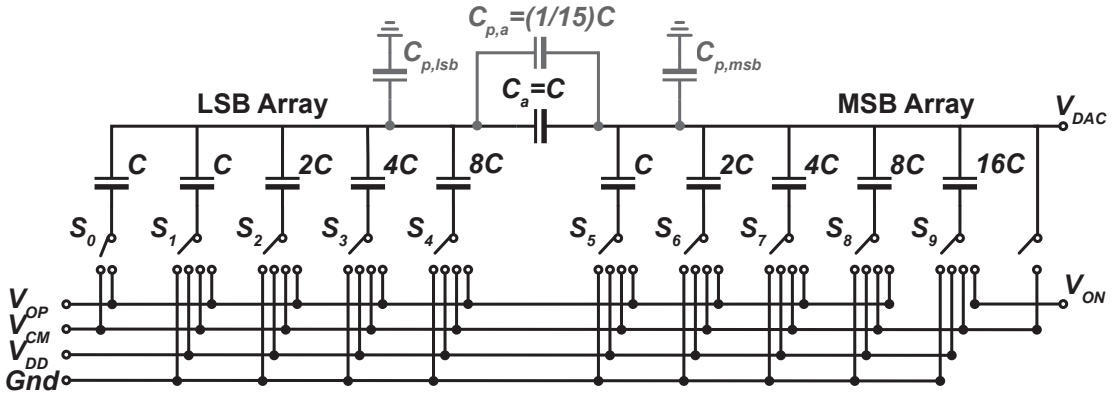


Figure 3.8: Schematic of the split CDAC employing V_{cm}-based switching technique.

also relaxes the capacitor matching request by a factor of $\sqrt{2}$ [90].

The SAR ADC in this work employs differential CDACs using the split capacitor structure with an attenuation capacitor C_a along with the V_{cm}-based switching method to improve power and area efficiency. Fig. 3.8 shows the schematic of the CDAC. The fully-differential architecture suppresses the supply noise and obtains a good CM noise rejection. The V_{cm}-based switching removes the MSB and 5-4 split CDAC is implemented to achieve 10-bit resolution. The main drawback of a splitting capacitor array is its sensitivity to capacitor matching and parasitics. A random mismatch on one of the LSB capacitors or the attenuation capacitor changes effective weights for all the bits [85]. In addition, the parasitic capacitance in the MSB array $C_{p,msb}$ leads to a gain error similar to conventional full binary-weighted CDAC, however, the parasitic capacitance in the LSB array $C_{p,lsb}$ changes the effective weight of the LSB bits and degrades the linearity performance further [88]. A larger number of bits in the LSB array results in worse linearity performance due to stringent matching and parasitic constraints.

The DNL error [90] determines the minimum possible value of the unit capacitor, and

$$\sigma_{DNL,MAX} < \frac{1}{2}LSB \quad \Rightarrow \quad \sqrt{2}(\frac{\sigma_u}{C_u})2^{(N-1)/2} < \frac{1}{2}, \tag{3.4}$$

where σ_u/C_u is the standard deviation of unit capacitor mismatch. A 3σ design in the selected process requires $C_u > 17.2$ fF. However, split CDACs are sensitive to $C_{p,lsb}$ that further degrades the DNL. It has been reported that a top-plate parasitic capacitance of more than 2% limits the maximum achievable ENOB to 9.5 in 5-4 split DACs [87, 88]. Therefore, the design uses a relatively larger C_u to keep the $C_{p,lsb}$ lower than 2% of the LSB total capacitance ($16C_u$) by making the parasitic of interconnection metal lines negligible. The unit capacitance in this work was set to be 76.8 fF. The attenuation capacitor, C_a, in a 5-4 split CDAC has to be $(16/15)C$. However, this value is not suitable for capacitor matching since it is not an integer multiple of C_u. Therefore, this design uses a unit capacitor for C_a and adjusts the layout of the top-to-bottom parasitic capacitance ($C_{p,a}$) in a way to achieve an effective C_a of $(16/15)C \approx$ 81.9 fF.

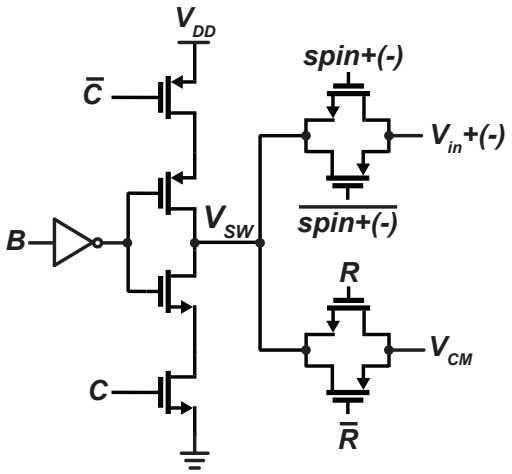


Figure 3.9: Schematic of the sample-and-hold switches.

In addition to capacitor sizing, a careful layout is applied to avoid linearity degradation. The parasitic capacitance in the LSB array is limited to 2% and a careful layout routing sets the $C_{p,a}$ to exactly $(1/15)C_u$. In conventional CDACs, a full common-centroid layout where the LSB capacitors are placed in the middle of the layout is applied to improve the capacitor matching. However, this approach results in a complex routing scheme and increases the parasitic capacitance of interconnection lines [84]. In this design, the LSB capacitors are placed close to bottom-plate switches to simplify the routing, thus reducing the parasitic capacitances. Post-layout simulations with simplified routing show an improvement in the DAC linearity since the parasitics of interconnection lines are significantly reduced.

3.5.2 Sample-and-Hold Switches

Fig. 3.9 shows the sample-and-hold switches, which selectively connect four different voltages to the bottom plate of DAC capacitors (V_{SW}). Compared to the conventional switching scheme, V_{cm}-based switching requires N additional switches to initially reset all the DAC capacitors to the CM voltage [90].

A sampling switch employs a transmission gate to enable full-range input sampling and eliminates the need for switch bootstrapping [91]. Since the sampling operation occurs only during $spin+$ or $spin-$ in 781.25 ns, the settling time has to be sufficiently short to keep the settling error of the sampled voltage lower than 0.5 LSB. In contrast to the top-plate sampling [91], the sampling switches drive much lower capacitance and a sufficiently-low switch on-resistance (R_{ON}) not to degrade the linearity of the ADC is easily achieved. When the sampling phase is completed, a transmission-gate switch connects the bottom plate of the capacitor to V_{CM}. Then, the conversion cycle starts, and single PMOS and NMOS switches are employed to charge or discharge the DAC capacitors to V_{DD} or ground, respectively.

Since the SAR ADC uses the supply voltage as reference, the switches are controlled with a

maximum overdrive and achieve high conductance and linearity. The width of PMOS devices is twice that of NMOS to have equal R_{ON}. Switches are designed in binary-weighted sizes along with binary-weighted capacitors scaling to have a highly-linear switching scheme. The architecture of all bottom-plate switches except S_0 is identical. The switch S_0 is only used for sampling and CM resetting, thus the charge and discharge transistors are always off by respectively connecting their gates to V_{DD} and ground. In addition, a transmission gate switch resets the MSB array of the CDAC during $spin+$ and $spin-$. It employs considerably large transistors to linearly charge the top-plate of the capacitors to V_{CM} in 1.5625 µs.

3.5.3 Dynamic Latch Comparator

The SAR ADC employs a StrongARM [95, 96] latch dynamic comparator since it consumes zero static power and provides rail-to-rail output. The StrongARM latch generates invalid outputs at half of the clock period, so an RS latch stores the valid output for the entire clock cycle [96]. Fig. 3.10 shows the schematic of the StrongARM latch followed by the RS latch.

The static offset of the comparator does not affect the linearity of the ADC. It only slightly reduces the ADC's input range, thus negligibly degrading the signal-to-noise (SNR) ratio [84]. The main parameters affecting the ADC's performance are comparator noise and kick-back charge. The input-referred rms noise ($V_{n,in}$) of the comparator must be lower than the quantization error,

$$V_{n,in} < \frac{V_{LSB}}{\sqrt{12}} \quad \Rightarrow \quad V_{n,in} < \frac{V_{FS}}{2^N\sqrt{12}}, \tag{3.5}$$

where V_{LSB} is the quantization step and V_{FS} is the full-scale voltage range. The SAR ADC in this work uses supply voltage as a reference and is supplied by 1.2 V. The differential mode doubles the signal range, and V_{FS} =2.4 V. For a 10-bit fully-differential SAR ADC, the comparator noise has to be smaller than 677 μV_{rms}.

The input differential pair is the main contributor to noise and originates more than 80% of the input-referred noise. The noise of the comparator can be reduced by increasing the capacitance on the nodes P and Q [96]. Therefore, a larger input pair can be used to increase the values of C_P and C_Q. Employing a larger input pair also reduces the latch's random offset; however, it increases the power consumption and the kickback charge since the kickback current couples to the input through the gate-to-drain capacitances of differential-pair transistors.

Relatively large PMOS transistors (W = 1.5 µm, L = 180 nm) are used in the input pair to ensure a 3σ noise lower than the quantization error. Transient noise simulations are performed to estimate the input noise variation. In contrast to simulations of small-signal analog circuits, a comparator does not provide output noise and gain. Therefore, methodical transient noise simulations proceed as follows. Differential input steps are applied to the comparator that is clocked 1000 times for each step. The number of ones and zeros at the comparator output for each input step gives a Gaussian probability distribution [96]. In the post-layout simulation, the ones and zeros occur with equal probabilities when the differential input around the

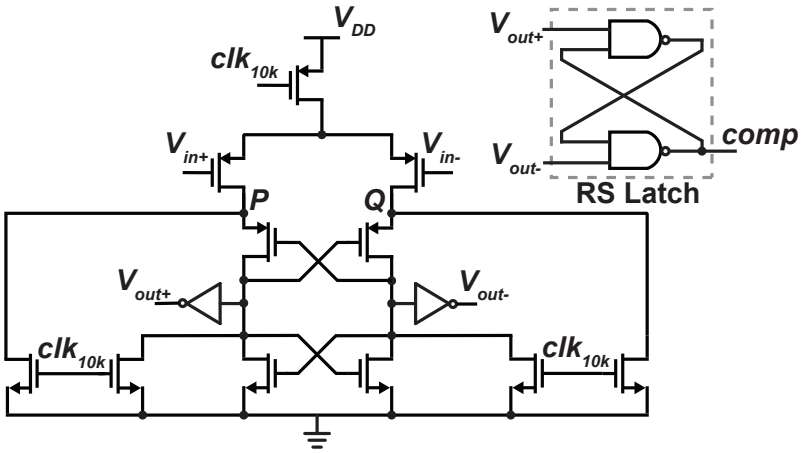


Figure 3.10: Schematic of the StrongARM latch dynamic comparator.

CM voltage is equal to the offset of the comparator. After determining the offset value, the differential input is increased and decreased with very small voltage steps. In the cumulative distribution function, the percentage of ones at 84% gives $+\sigma$ whereas its percentage at 16% gives $-\sigma$. As a result, $\sigma_{n,in}$ = 145 µV, and the comparator achieves a $3\sigma_{n,in}$ lower than the quantization error.

The kickback charge induced on the top plate of the CDAC can cause the comparator decision to shift in the current or next cycle. As the size of the input pair is increased, more kickback current flows into the comparator through the gate-to-drain capacitors of the PMOS input devices [96]. Post-layout simulation results indicate that the kickback noise is lower than the quantization error because the total DAC capacitance is high enough to suppress its effect.

3.5.4 SAR Control Logic

A low-power SAR logic is used to generate the control signals for sampling and conversion operations. An asynchronous clocking scheme [97] is commonly used for high-speed operations to avoid a high-frequency system clock. In this work, the spinning control logic shown in Fig. 3.4 generates the clock and spinning control signals from a 1.28 MHz clock. As shown in Fig. 3.11, this ADC utilizes a low-power synchronous SAR control logic consisting of 10-bit sets of shift registers $SR_{9:0}$ [98], bit registers $BR_{9:0}$ [90], and NOR gates. The shift and bit registers use a transmission-gate D-flip-flop architecture. These registers and NOR gates are implemented by full custom dynamic logic to further decrease power consumption. The SAR logic employs minimum-length transistors, and the width of the NMOS and PMOS devices is set to 250 nm and 500 nm, respectively.

Fig. 3.12 describes the SAR logic operation on its timing diagram. The system uses a 10 kHz clock, and one conversion cycle lasts for 10 clock periods. The spinning control logic generates clk_{10k}, $spin+$, $spin-$, and $start$ signals, which are the inputs of the SAR logic. A conversion

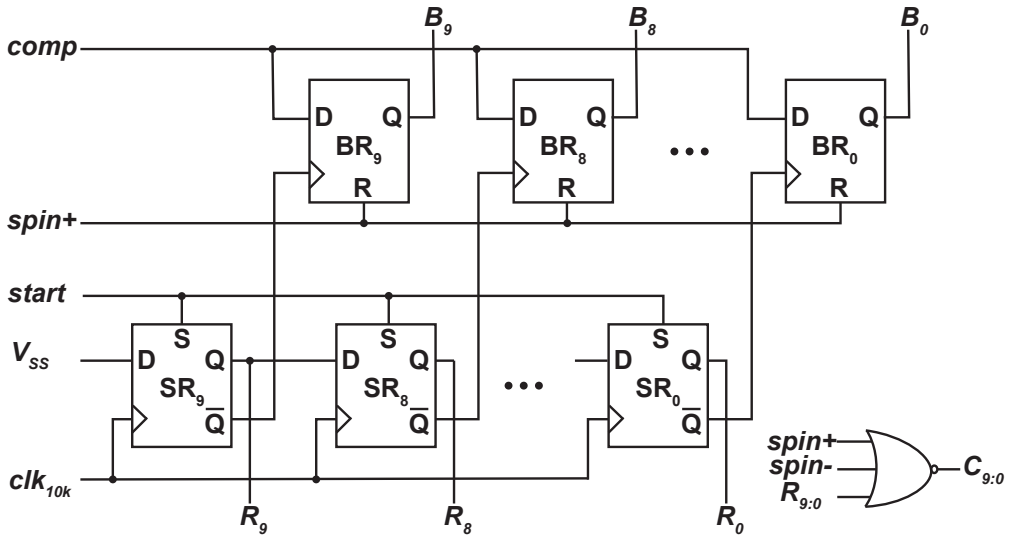


Figure 3.11: Block diagram of the SAR control logic.

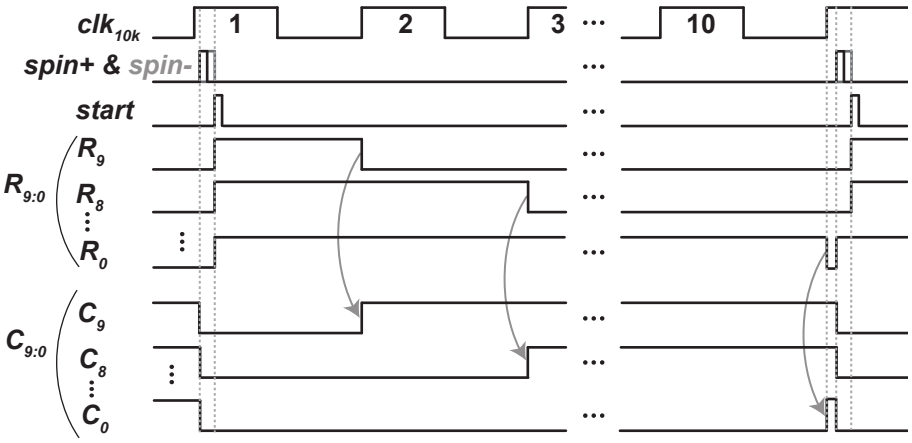


Figure 3.12: Timing diagram of the SAR control logic.

cycle starts at the rising edge of the $spin+$ signal, and all conversion bits ($C_{9:0}$) are set to low to isolate the bottom plates of DAC capacitors from V_{DD} and ground. Then, the input signal is sampled to the capacitors during $spin+$ or $spin-$. When the sampling operation is completed, the start signal becomes high to reset all the reset bits ($R_{9:0}$) to V_{DD}, and the conversion starts at the rising edge of the second clock period. R_9 becomes low to disconnect the bottom plate of the MSB capacitor from V_{CM}, and C_9 goes high to connect it to V_{DD} or ground, depending on the decision of the comparator, B_9. The same operation repeats for all the bits. The LSB estimation happens during the same clock period as the sampling since it requires only 1.5625 µs, and one conversion cycle is completed in 10 clock periods.

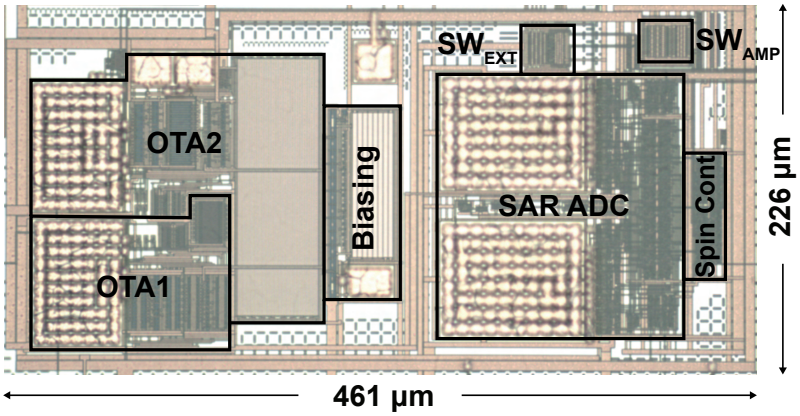


Figure 3.13: Die micrograph of the BDC ASIC fabricated in a 180-nm CMOS process.

3.6 Measurement Results

The BDC application-specific IC (ASIC) was designed and fabricated in a 180-nm standard CMOS technology. Fig. 3.13 shows the die micrograph of the ASIC, which has an active area of 0.1 mm^2. Experimental results verify the performance of the BDC readout IC and the entire pressure sensing system. The following sections report these results.

3.6.1 Electrical Measurements

First, the CCIA and SAR ADC in the implemented bridge-to-digital interface are characterized seperately. Fig. 3.14(a) shows the closed-loop frequency response of the CCIA for different gain configurations. The gain can be adjusted in the range of 29.2 dB (29 V/V) to 37.1 dB (72 V/V) by trimming the 2-bit controlled feedback capacitors (C_{fb2}) for tuning the input range of the CCIA from ±6.6 mV to ±16.5 mV at 1.2 V supply voltage. Fig. 3.14(b) shows that the CCIA's noise spectrum is lower than 18 nV/$\sqrt{\text{Hz}}$ in the bandwidth from 100 kHz to 1 MHz. The excitation switches of the bridge sensor up-modulate the bridge output at a frequency range within the selected bandwidth.

Fig. 3.15 shows the total harmonic distortion (THD) of the CCIA. The variable gain operation enables high linearity for high-amplitude input signals. The THD of the amplifier is 0.08% when an 18 mV peak-to-peak (mV_{pp}) differential input at 100 kHz is applied with maximum gain. For higher amplitude input signals, the gain of the amplifier is reduced, and the THD is 0.14% when a 32 mV_{pp} differential input is applied with minimum gain. However, the THD of the CCIA decreases at higher input frequencies due to its limited bandwidth. The worst-case THD in the selected bandwidth is 0.36% when a 32 mV_{pp} at 1 MHz is applied. The common-mode rejection ratio (CMRR) of the amplifier is 77 dB. The CCIA draws 217 µA static current from a 1.2 V supply, but thanks to the duty-cycling, the average current consumption is 0.51 µA.

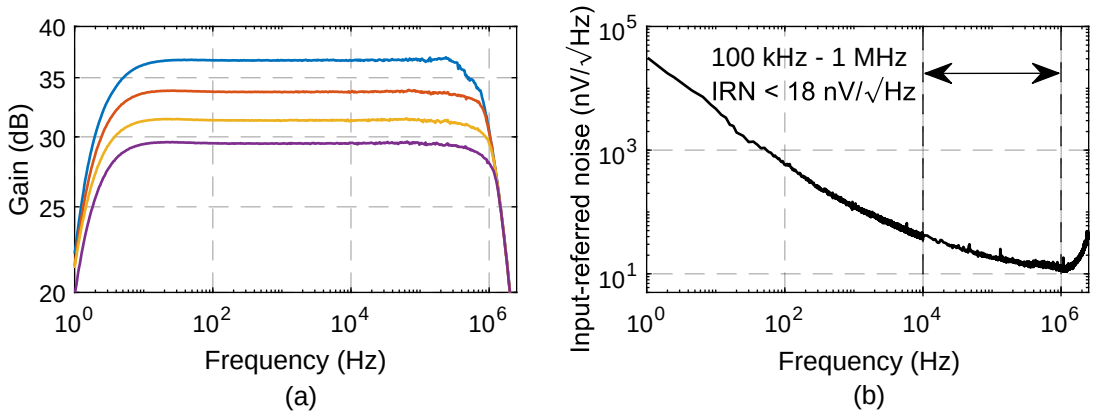


Figure 3.14: CCIA's measured (a) frequency response for different gain configurations and (b) input-referred noise (IRN) spectrum.

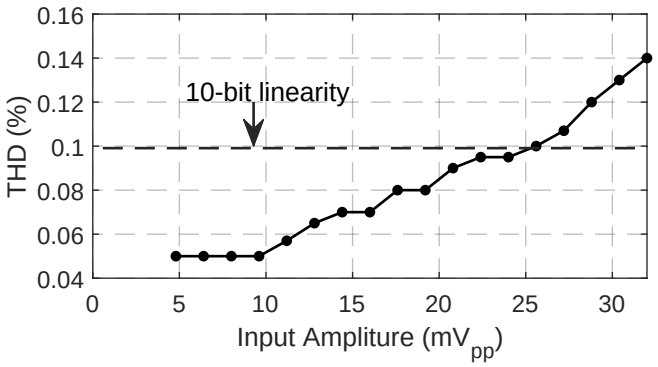


Figure 3.15: THD as a function of the input amplitude.

The SAR ADC was tested at a sampling rate of 1 kS/s and 1.2 V supply voltage. The measured fast Fourier transform (FFT) spectrums are shown in Fig 3.16. At 199.9 Hz input frequency, the measured signal-to-noise and distortion ratio (SNDR) and spurious-free dynamic range (SFDR) are 57 dB and 66.5 dB, respectively. The resultant ENOB is 9.2. At 479.9 Hz input, the measured SNDR and SFDR respectively are 55.3 dB and 61.7 dB, showing a negligible drop in performance over the entire bandwidth. Fig. 3.17 illustrates DNL and INL of the SAR ADC. At 1 kS/s sampling rate, the DNL and INL are +0.3/-0.36 LSB and +1.8/-1.3 LSB, respectively.

The test circuit uses multiple supply voltage connections to allow a detailed measurement of the power consumption in the comparator, capacitive DAC, and SAR logic. The experimental verification shows that the comparator, capacitive DAC, and SAR logic consume 0.5, 5.8, and 12.7 nW at 1.2 V, respectively. Overall, the SAR ADC consumes 19 nW at 1 kS/s sampling rate and achieves a figure-of-merit (FoM = Power/$2^{\mathrm{ENOB}} \times f_s$) of 32.3 fJ/conversion.

The proof of offset-independent output code and negligible residual offset results from measurements with two commercial IAs having different input offsets. Fig. 3.18(a) shows the first amplifier's (THS4551 [99]) output signals with a peak-to-peak output voltage of 511 mV.

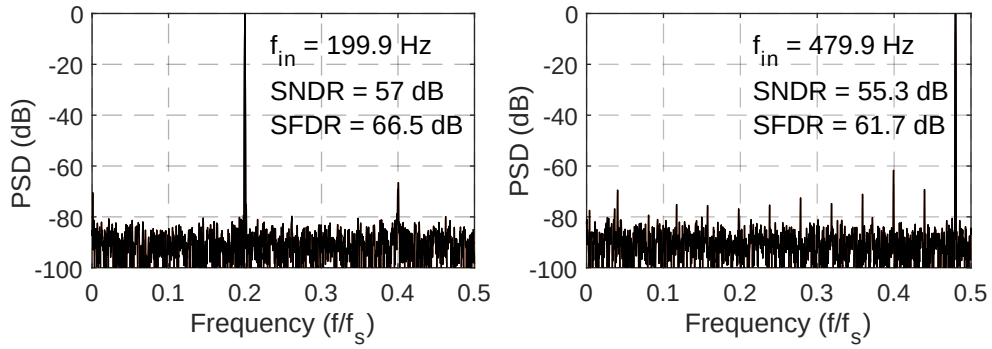


Figure 3.16: Measured FFT spectrum at 1 kS/s.

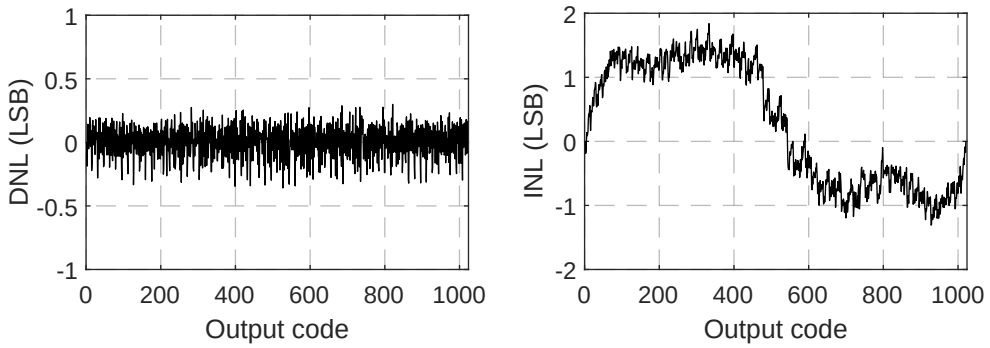


Figure 3.17: Measured DNL and INL.

The output offset is calculated as 596.5 mV – 607.3 mV = –10.8 mV. Fig. 3.18(b) shows the second amplifier's (THS4121 [100]) output signals with the same peak-to-peak output voltage of 511 mV, leading to an output offset of 621.6mV – 599.8 mV = +21.8 mV. In both cases, the SAR ADC ($D_{9:0}$) gives the input's exact value, demonstrating the offset cancellation and showing that the possible residual offset does not affect the circuit's performance.

Fig. 3.19 shows the measured output spectrum of the complete bridge-to-digital readout. At 199.9 Hz input frequency, the BDC achieves an SNDR of 52.4 dB, and the resultant ENOB is 8.4. The LSB for the minimum input is 39.1 µV, while the input-referred noise over the 100 kHz to 1 MHz range is about 18 µV, less than half LSB for the minimum input. Fig. 3.20 shows the measured SNDR values at different input amplitudes. The variable gain operation improves the SNDR for small amplitudes, and the BDC achieves a dynamic range of 55.6 dB. The total current consumption of the ASIC is 9.48 µA from a 1.2 V supply. The current reference circuit consumes 8.4 µA since it is not duty-cycled, and the spinning control logic consumes 560 nA because it includes a clock divider circuit from 1.28 MHz to 1 kHz. If the current consumptions of the reference circuit and spinning control logic are not considered, the BDC ASIC draws 0.53 µA current from a 1.2 V supply and consumes 0.63 nJ energy in 1 ms conversion time.

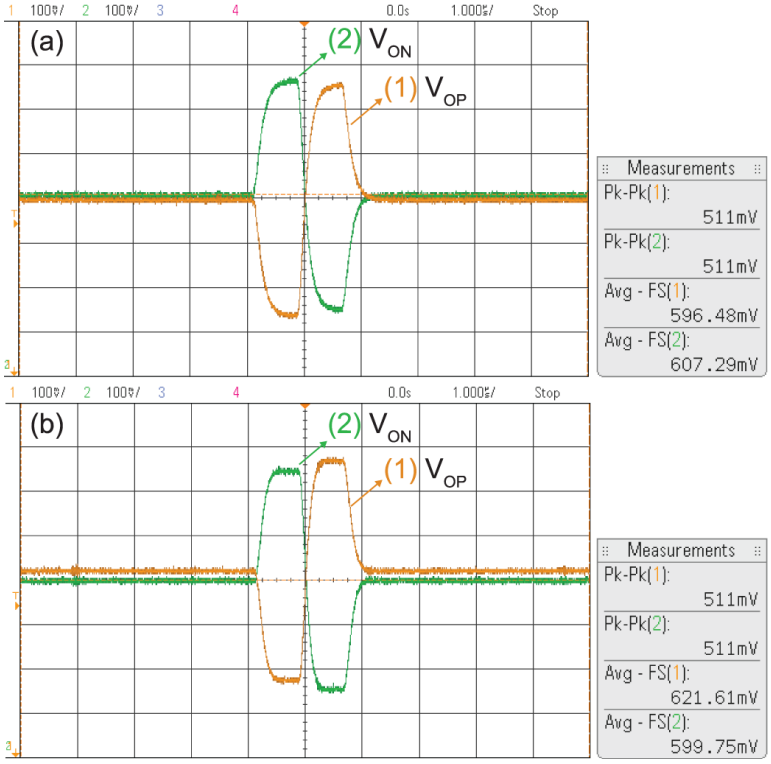


Figure 3.18: Output voltages of the (a) first and (b) second commercial amplifier.

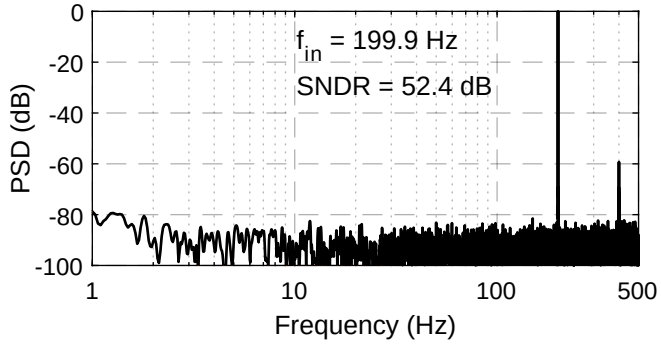


Figure 3.19: Measured output spectrum of the BDC.

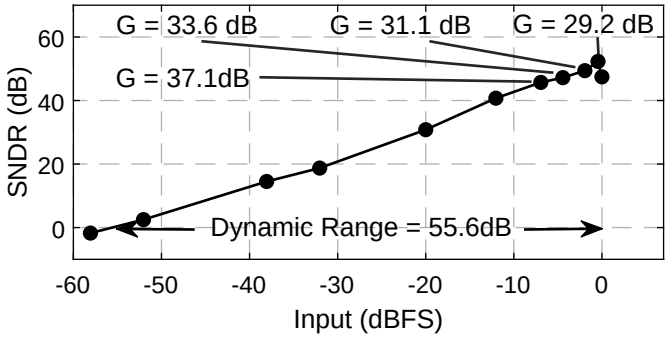


Figure 3.20: SNDR vs. input amplitude of the BDC at f_{in} = 199.9 Hz.

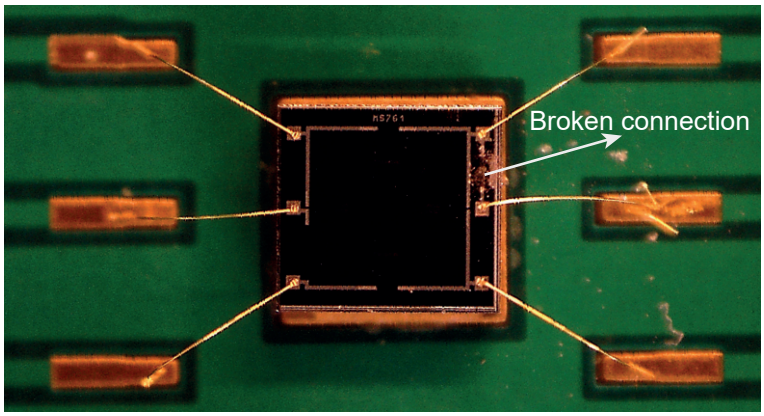


Figure 3.21: Photo of the wire-bonded MS761 sensor with a broken connection eliminating reverse biasing and current leakage issues.

3.6.2 System Measurements

The bridge-to-digital readout ASIC with two different pressure sensors verify the functionality of the BDC. The demo uses small size pressure sensors to meet the miniature requirements of the system for potential body implantation.

The initial use of an absolute pressure sensor (MS761) [101] revealed that the reverse biasing of the bridge sensor leads to a high leakage current. The sensing elements in the bridge sensors are diffused resistances, and the substrate can short the positive supply of the bridge in some MEMS pressure sensors. In such sensors, the voltage applied to the top excitation must always be higher than the bottom excitation voltage. The spinning topology does not work because of the excitation pad's connection to the substrate of the MEMS. In MS761, there is an additional pad for the epitaxial layer, but it is connected to the pad of the positive excitation voltage. To address the leakage problem, the connection between these two pads was broken, and the epitaxial layer are connected to 1.2 V, while the excitation voltage of the bridge spins. Fig. 3.21 shows the photo of the wire-bonded MS761 pressure sensor with a broken connection between the excitation pad and the epitaxial layer pad. This solution eliminates the current leakage issue by avoiding reverse biasing.

A further functionality test of the BDC used a differential pressure sensor. The difficulty in measuring the differential pressure with a sensor die (SM30D) [82] forced us to use its packaged version (SM5G) [102] with an operating pressure range of 0 to 5 PSI (0 to 258.6 mmHg). The substrate of SM5G also connects the top excitation voltage, and there is no additional pad for substrate connection for separating the substrate and excitation voltage. To maintain an acceptable leakage current, the measures with the SM5G sensor use a maximum current on the bridge limited to 300 µA by the DC power supply. However, it is expected that the implanted system will separate the substrate and the excitation voltage of the MEMS sensor.

Fig. 3.22 shows the experimental setup used for the system pressure measurements. A pressure

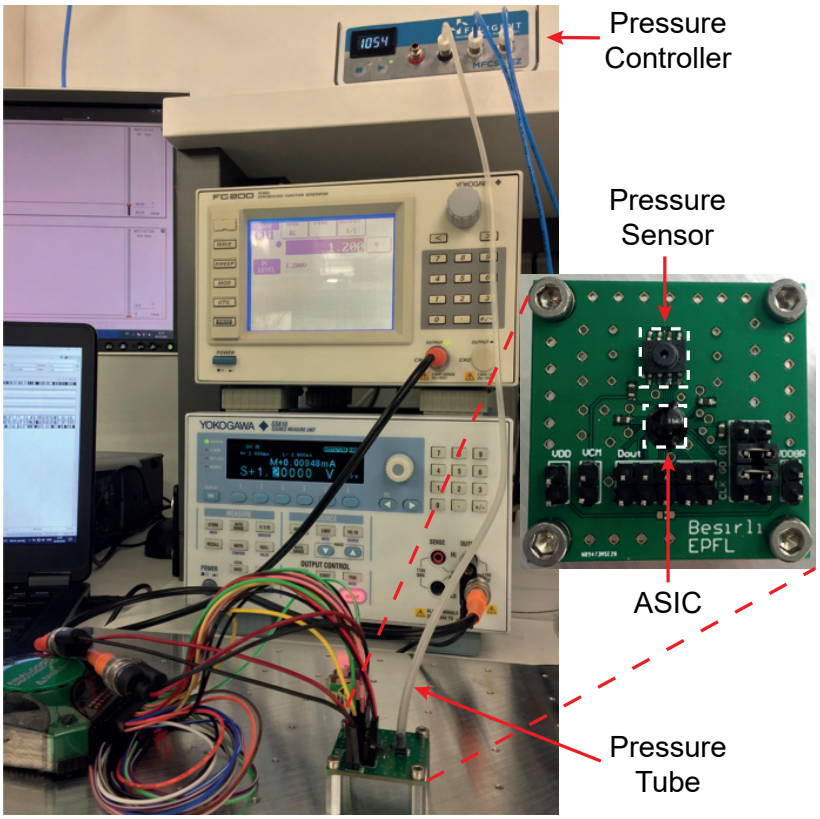


Figure 3.22: Experimental setup for pressure measurements of the BDC.

control (Fluigent MFCS-EZ) generates stable pressure steps. The local pressure network in the laboratory provides pressurized nitrogen for creating positive pressure and tunes the input pressure value via a pneumatic regulator. A vacuum pump connected to the pressure controller generates negative pressure. Conventional instruments bias the ASIC at 1.2 V, provide an input clock at 1.28 MHz, accurately measure the current consumption, and read out the 10-bit digital output.

To characterize the BDC with selected pressure sensors, pressure steps ranging from –135 to +135 mmHg are applied by the pressure controller. The decimal output code of the BDC with MS761 changes from 753 to 814, resulting in a pressure resolution of 4.4 mmHg. The reason for such a low pressure resolution is that the sensor output does not fit the input range of the BDC since the operating pressure range of absolute pressure sensors starts from zero pressure with respect to absolute vacuum (-760 mmHg).

In order to effectively utilize the input range of the BDC, a differential pressure sensor (SM5G) with an operating pressure range of 5 PSI (258.6mmHg) is employed. The output code of the BDC is measured with respect to the ambient pressure. As shown in Fig. 3.23, the output of the BDC with SM5G differential pressure sensor linearly increases from 270 to 884, corresponding to a resolution of 0.44 mmHg with a 1 ms conversion time. Table 3.1 summarises the overall

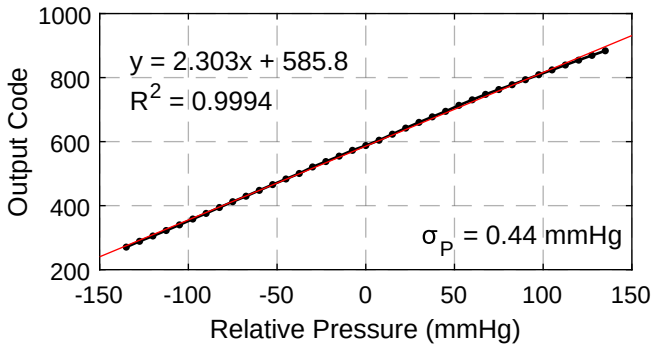


Figure 3.23: Measured decimated output of the BDC with swept pressure from –135 mmHg to +135 mmHg with respect to the ambient pressure.

system performance of the BDC. Fig. 3.24 shows the histogram of the output code for 1024 samples when the relative pressure is zero. It demonstrates an accuracy of 3 LSB, which is equal to 1.32 mmHg. The pressure sensor having 5 kΩ bridge resistances draws 390 nA current and consumes 0.47 nJ excitation energy per conversion.

Table 3.2 summarises the overall system performance of the BDC and compares this work with the state of the art. The total BDC consumed energy is 1.1 nJ per conversion for an ENOB of 8.4. The figure-of-merit (FoM = (Conv. Energy)/2^{ENOB}) is 3.3 pJ/conversion, which represents state-of-the-art performance in terms of energy efficiency.

3.7 Conclusion

This chapter presented the design, fabrication, and testing of an energy-efficient bridge-to-digital converter specifically developed for implantable pressure monitoring systems. The design exploits the duty cycling of the bridge sensor for cancelling the IA's 1/f noise and offset at the same time. The 1/f noise and offset of the IA are inherently suppressed by designing a spinning method simultaneously applied to the bridge sensor and capacitive DAC of the SAR ADC. This method avoids the need for digital filters to cancel spurs, which in conventional chopper amplifiers derive from offset and 1/f noise modulation. The BDC interface, fabricated in a standard 180-nm CMOS technology, achieves 8.4 ENOB at a 1 kS/s sampling rate. The highly duty-cycled CCIA enables the BDC readout to only draw 0.53 µA average current from the 1.2 V supply. Testing of the BDC readout employed both absolute and differential piezoresistive pressure sensors. The BDC with the differential pressure sensor achieves a resolution of 0.44 mmHg in a pressure range of –135 to +135 mmHg. The figure-of-merit of the pressure sensing system is 3.3 pJ/conversion for a total conversion energy of 1.1 nJ, which are state-of-the-art performances. These results make the system suitable for deeply implanted remote hemodynamic monitoring devices.

Table 3.1: Performance summary of the BDC's sub-blocks.

Technology (nm)	180
Supply Voltage (V)	1.2
Capacitively-Coupled IA	
Gain (V/V)	29, 36, 48, 72
Bandwidth (MHz)	1
Input Range (mV)	±6.6 to ±16.5
Input-referred noise (nV/$\sqrt{\text{Hz}}$)	18[a]
Average Power Consumption (nW)	636
SAR ADC	
Sampling Rate (kS/s)	1
SNDR and SFDR (dB)	57, 66.5
DNL and INL (LSB)	+0.3/-0.36, +1.8/-1.3
Power Consumption (nW)	19
Walden FoM (fJ/conversion)	32.3
Full System BDC with Bridge Sensor	
Pressure Range (mmHg)	270
Resolution (mmHg)	0.44
ENOB	8.4
Conversion Energy (nJ/conversion)	1.1[b]

[a]In a bandwidth from 100 kHz to 1 MHz, [b]Current reference circuit and spinning control logic were not considered.

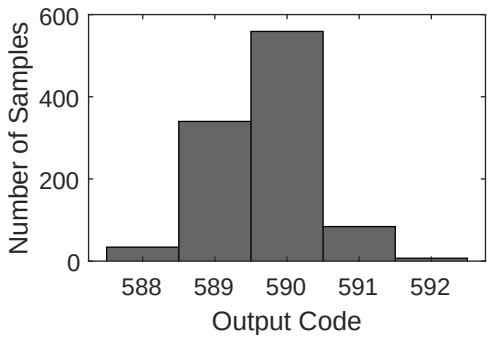


Figure 3.24: Histogram of the decimated output at zero pressure input for 1024 samples.

Table 3.2: BDC's performance summary and comparison with the state of the art.

	IEEE Sens. J. 2014[47]	TBCAS 2015[48]	VLSI 2017[80]	ISSCC 2018[49]	JSSC 2019[50]	IEEE Sens. J. 2020[51]	**This work**
Technology (nm)	90	350	180	180	180	350	**180**
ASIC Supply Voltage (V)	1	3.3	1.8	1.2, 3.6	1.8	1.8	**1.2**
ASIC Supply Current (µA)	19.5[a]	60.6[a]	33.9[a]	0.38@3.6V 0.06@1.2V[a]	1200	328.6	**0.53**[a]
Bridge Voltage (V)	1	3.3	1.8	3.6	5	1.8	**1.2**
Bridge Resistance (kΩ)	12	8.25 - 16.5[b]	1	6	3.7	5	**5**
Bridge Current (µA)	83.3	60.6 - 121.2	102.8	0.13	1351	1.4	**0.39**
Conversion (Conv.) Time (ms)	0.096	0.8	1	1	0.5	0.27	**1**
Conv. Energy without Bridge (nJ/conversion)	1.87	160	61	1.4	1080	159.7	**0.63**
Conv. Energy with Bridge (nJ/conv.)	5	320 - 480	246	1.9	4458	160.4	**1.1**
ENOB	7.03	7.2	9.7	7.9[b]	15.4[b]	9.13	**8.4**
FoM[c] (pJ/conv.)	38.3	2176 - 3265	296	8.0	103.1	286.3	**3.3**

[a]Only sensor interface current (Power management, clock and bias generators were excluded), [b]Estimated from given data, [c]FoM = (Conv. Energy with Bridge)/2^{ENOB}.

4 Implantable Inductive Sensor for Measuring Artery Cross-Sectional Area

This chapter presents a novel method for measuring the cross-sectional area (CSA) of an artery, particularly the pulmonary artery (PA), to be used for the calculation of cardiac output (CO). The method is based on the inductance change of an anchoring loop mounted on a miniaturized system implanted in a section of the artery. The CSA measurement system comprises an inductive readout integrated circuit (IC) and a conductive anchoring loop that changes its inductance according to the deformation of the artery and can be correlated to the diameter and CSA of the artery section. Direct and periodic measurement of the CSA can improve the accuracy of CO monitoring, which is a crucial indicator of heart function to monitor heart failure (HF) patients. An oscillator-based inductive readout IC was designed and fabricated in a standard 180-nm CMOS process, and the anchoring loop was implemented using a 24 cm nitinol wire with a diameter of 0.5 mm. Measurement results show that the inductive readout IC achieves 0.42 nH inductance resolution in a range from 181 nH to 681 nH while consuming 51.2 μA to 39.7 μA, respectively, from a 1.2 V supply. In addition, the correlation between the artery diameter and loop inductance is demonstrated by placing the anchoring loop in cylinder tubes with diameters from 20 mm to 30 mm and the artery diameter measurement achieves a resolution of 0.24 mm, which is a factor of four higher than the lateral resolution of echocardiography. Some parts of this chapter were published in [103].

This chapter is organized as follows: Section 4.1 presents an overview of CO measurement systems. Section 4.2 explains the working principle of an oscillator-based inductive readout circuit for artery CSA measurements, whereas the implementation details are presented in Section 4.3. Section 4.4 summarizes the experimental results and Section 4.5 provides the conclusion.

4.1 Overview of Cardiac Output (CO) Measurement

In order to adapt treatments based on how HF patients react to the prescribed drug, it is important to directly and continuously (24/7) monitor the heart function, especially the cardiac output (CO), which is one of the best indicators of heart function. Cardiac output is

the volume of blood that the heart pumps in a time interval of one minute. When measured by echocardiography, it is defined as the product of stroke volume (SV) and heart rate (HR), where SV is velocity time integral (VTI) multiplied by the cross-sectional area (CSA) of the artery [25]:

$$CO_{[\frac{ml}{min}]} = VTI_{[\frac{cm}{beat}]} \times CSA_{[cm^2]} \times HR_{[\frac{beats}{min}]}. \tag{4.1}$$

The changes in cardiac function associated with HF result in a decrease of CO, and most of the symptoms of HF are related to the reduction of CO. There are several methods to measure or estimate CO [25, 104, 35], however, it is not possible to accurately and continuously (24/7) monitor CO with existing monitoring systems on the market. Cardiac output monitoring devices are either not adapted for non-clinical environments or cannot achieve a high accuracy, thus reducing the quality of diagnosis or treatment. The current state-of-the-art implantable hemodynamic monitoring device is the CardioMEMS^{TM} HF System, which is mounted in a section of the PA by using anchoring loops [29]. Recently, the CardioMEMS^{TM} was used to estimate the CO by using a software algorithm calculating CO based on analysis of pressure waveforms [35]. However, this device relies only on PA pressure to assess cardiovascular status, giving a limited understanding of the HF mechanism. Another device to monitor CO is the ultrasonic cardiac output monitor (USCOM), which is a continuous-wave Doppler monitoring system. Blood flow velocity is measured by the Doppler effect, but the CSA of the artery is only estimated based on a patient's age and weight [25]. These systems do not directly measure the CSA, they estimate or precalculate the CSA by some algorithms. However, to measure the CO accurately, the flow velocity and CSA must be measured simultaneously, as the diameter of the artery can significantly change in many cases, for example, during exercise. Since the CSA is only estimated and not directly measured in these systems, the estimation of CO is not accurate. Existing non-invasive techniques such as echocardiography are not adapted for continuous monitoring of heart functions during patients' everyday life. In addition, the lateral resolution of echocardiography is typically around 1 mm [55]. However, CSA measurement may require higher resolution to improve the accuracy of continuous CO monitoring.

4.2 Oscillator-Based Inductive Readout System

This thesis proposes a novel method for the direct and continuous (24/7) measurement of the cross-sectional area of an artery, particularly the PA, by exploiting the inductive characteristic of a conductive anchoring loop. In CardioMEMS^{TM} [29], the anchoring loop is used only for mounting the implant in the PA. As Fig. 4.1 shows, this thesis aims to use a conductive anchoring loop for both the placement of the implant and the CSA measurement of the artery.

The conductive loop is configured to engage the walls of the section of an artery in which the implantable system is intended to be implanted, causing elastic deformation of the conductive loop. The amount of deformation affects the inductance of the loop, which can thus be correlated to the diameter of the artery. Therefore, two ends of the inductive loop can be connected to an inductive sensor readout in the implant in order to determine the induc-

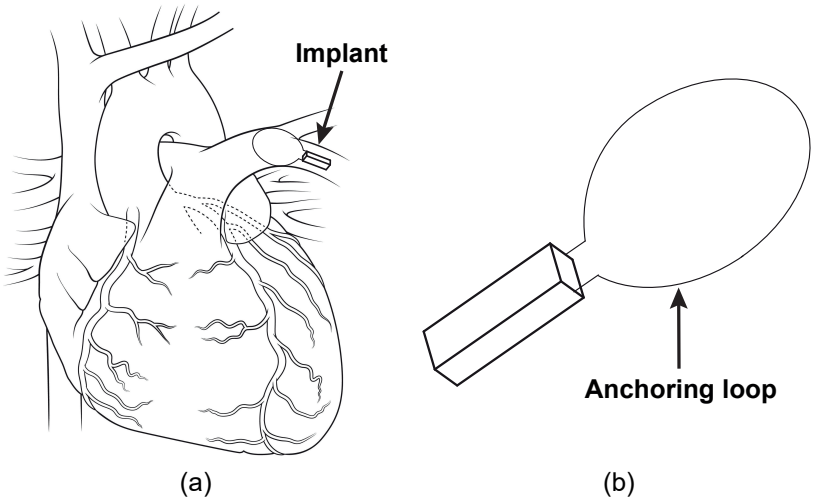


Figure 4.1: (a) Conceptual view of a hemodynamic monitoring implant mounted in a pulmonary artery branch of a patient's heart. (b) Conceptual view of the implant with an anchoring loop for the placement and CSA measurement in the artery.

tance change with the artery diameter. The cross-sectional area can be determined from the diameter measurement of the artery assuming a substantially cylindrical artery section shape. The inductive sensor may comprise a single conductive loop or two conductive loops for measuring the diameter in orthogonal planes. The orthogonal inductance measurements can also provide a more accurate measurement of the CSA, especially taking into account non-circular profiles of the artery section. Additionally, the orthogonal loops offer mechanical stability for the implant's anchoring in the artery section.

An oscillator-based inductive readout IC is designed and implemented to measure the inductance of the anchoring loop. The proposed inductive readout IC consists of a cross-coupled symmetrical voltage-controlled oscillator (VCO) and a counter to read out the inductance value in the time domain. VCOs are widely used in low-power transmitters for wireless data transfer [105, 106, 107, 108]. Such transmitters employ an off-chip loop antenna, which is connected to the differential output pins of the oscillator to transmit the data [106, 107, 108]. To measure the inductance value of a conductive anchoring loop, the loop is connected to the differential output of the oscillator, similar to the connection of a loop antenna. This novel oscillator-based inductive readout enables measuring the inductance of the anchoring loop for diameter measurements.

Fig. 4.2 shows the block diagram of the inductive readout IC with its connections to the external anchoring loop. The anchoring coil and the readout IC are mounted and interconnected on a printed circuit board (PCB). The inductance of the anchoring coil (L) and the parasitic capacitance of bonding pads and PCB traces (C_p) determine the value of the oscillator's resonance frequency (f_0). Since the capacitance of the bonding pads and PCB traces is constant, the resonance frequency is correlated to the change of the loop inductance. The

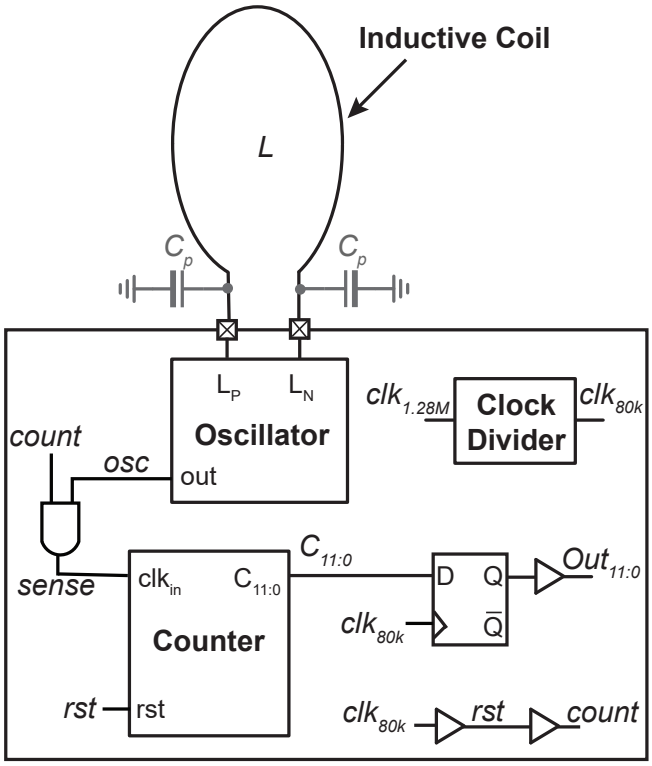


Figure 4.2: Block diagram of the inductive readout IC with its connections to the inductive anchoring coil.

resonance frequency of the oscillator is defined as

$$f_0 = \frac{1}{2\pi\sqrt{LC_p/2}}, \tag{4.2}$$

and is inversely proportional to $\sqrt{L}$ since C_p is constant.

The inductive readout is a counter-based circuit that operates in the time domain. It comprises a free-running oscillator, whose resonant frequency is correlated with the shift in L. A 12-bit counter is incremented to count the pulses of the oscillator. The timing diagram reported in Fig. 4.3 describes the working principle of the inductive readout circuit. The circuit employs a clock input with a frequency of 1.28 MHz. A D flip-flop (DFF) based clock divider divides the clock frequency by 16 to generate a clock signal at 80 kHz (clk_{80k}), and clk_{80k} is buffered with very short delays to generate rst and $count$ signals. The oscillator is free-running and generates osc signal with a frequency determined by C_p and L. At the rising edge of rst signal, the counter is reset and then starts to be incremented for 6.25 µs when $count$ is high. Then, the last output value of the counter ($C_{11:0}$) is stored by DFFs at the rising edge of the next clk_{80k} before the counter is reset for the next measurement cycle. The stored output $Out_{11:0}$ is the inverted version of $C_{11:0}$, in order to make the output increase with a larger loop inductance.

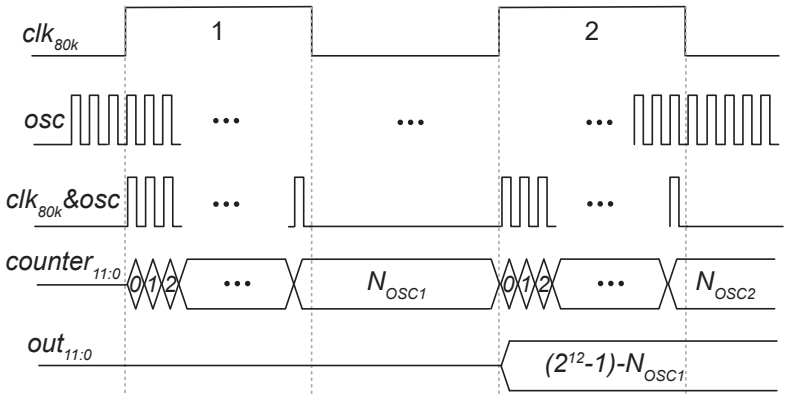


Figure 4.3: Timing diagram of the inductive readout circuit.

4.3 Implementation Details

The implantable unit can be implanted using a catheter tool, whereby upon removal of the catheter tool, the elastically squeezed anchoring loop expands and engages the artery walls to hold the implantable system in place. The material used for the loops may include a conductive polymer or a metal, such as nitinol, elgiloy, stainless steel, cobalt chrome alloysm, or any other suitable conductive materials with elastic properties sufficient to allow elastic compression for the range of diameters from the largest artery section at about 30 mm down to the catheter insertion tool diameter at about 10 mm. In this work, the inductive anchoring loop is realized by a nitinol wire selected for its biocompatibility, conductive characteristic, and sufficient elastic properties. The diameter of the nitinol wire forming the loop is selected to be 0.5 mm to minimize blood flow blockage. The length of the anchoring loop should be about 12 cm in the implantable device, however, the length of the nitinol wire is selected to be 24 cm in the prototype to increase the inductance shift of the loop.

Fig. 4.4 shows the cross-coupled voltage-controlled oscillator, where NMOS and PMOS cross-coupled pairs biased in weak inversion are used to maximize the negative transconductance for the given bias current. The inductance change of the anchoring loop made of the selected nitinol wire in a cylindrical artery section is simulated in Ansys mechanics and electronics simulation software. The inductance of the loop increases when the artery diameter is enlarged from 20 mm to 30 mm. The simulated inductance values at 20 mm and 30 mm diameter are about 200 nH and 212 nH, respectively. The post-layout simulations show that the pad capacitance of the IC is about 140 fF, and the parasitic capacitance of the PCB traces is estimated to be between 750 fF and 1 pF. Thus, C_p is estimated to be 1 pF.

The input clock is at 1.28 MHz, and the VCO resonance frequency decreases approximately from 503.3 MHz to 488.8 MHz when the inductance increases from 200 nH to 212 nH. To increase the resolution of the inductance measurement, the frequency difference between the clock and oscillation frequencies must be increased. For instance, if the $count$ signal were at 1.28 MHz and high only for 390.625 ns, the counter output would increase from 191 to 196-197,

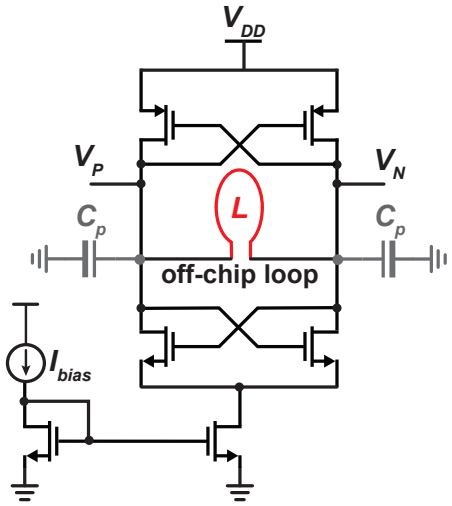


Figure 4.4: Schematic of the cross-coupled voltage controlled oscillator.

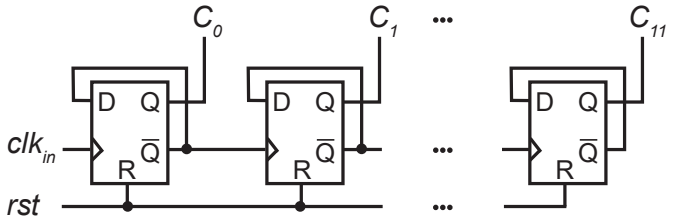


Figure 4.5: Schematic of the 12-bit asynchronous up counter.

resulting in a very low resolution. In order to achieve a resolution of 0.1 mm in a 10 mm range, the output code change should be 100. Therefore, the input clock at 1.28 MHz is divided by 16 to increase the frequency difference with the resonance frequency for a more precise comparison. The counter operates at 80 kHz, and $count$ is high for 6.25 µs. The simulation results show that the output code increases from 3055 to 3145, allowing a resolution of about 0.11 mm. A 12-bit counter is implemented to be able to cover more than 3145 clock pulses. Fig. 4.5 depicts the implemented 12-bit asynchronous up counter consisting of 12 DFFs.

4.4 Experimental Results

The readout IC was designed and fabricated in a 180-nm CMOS process. Fig. 4.6(a) shows the die micrograph, whose core area is 0.026 mm^2. Two different PCBs were implemented to perform measurements with commercial SMD inductors and a nitinol-based anchoring loop.

The first characterization measures the inductive readout circuit with commercial ceramic-core chip inductors, with a range of 181 nH to 681 nH. Since the parasitic capacitance of bonding pads and PCB traces determine the resonance frequency, the SMD inductors were placed very close to the IC to keep the parasitic capacitance below 1 pF. Fig. 4.7(a) and (b) show the change of the output code with respect to the inductance L and $\sqrt{L}$, respectively.

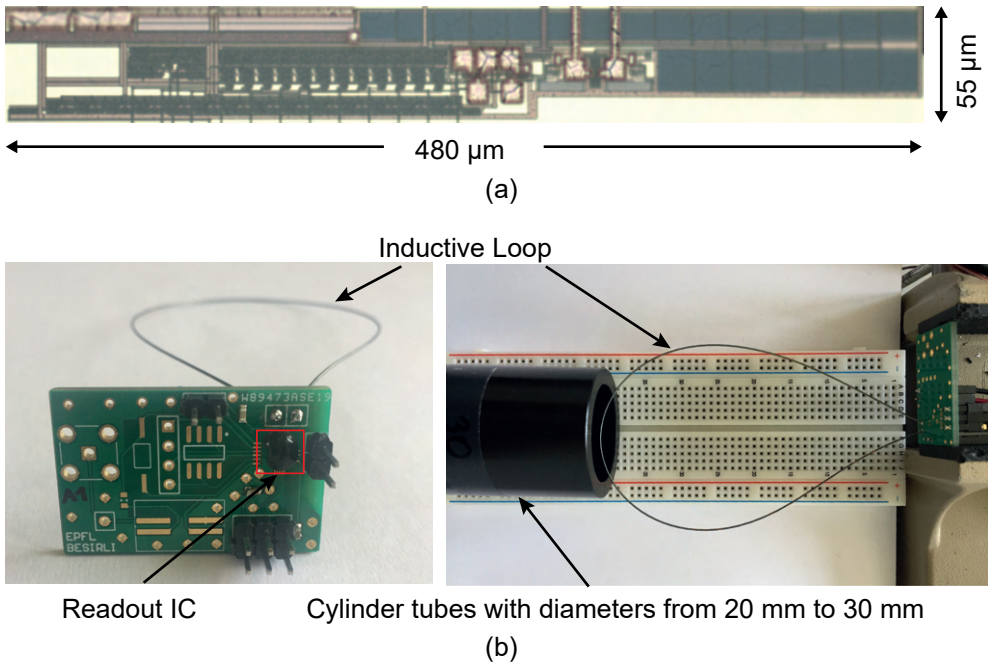


Figure 4.6: (a) Die micrograph of the inductive readout IC. (b) Test PCB with a nitinol anchoring loop and the readout IC, and the experimental setup.

The output code increases almost linearly with $\sqrt{L}$ and achieves a resolution of 0.42 nH in a 500 nH inductance range. The inductive readout IC has a supply voltage of 1.2 V, draws 39.7 µA current when L = 681 nH and 51.1 µA when L = 181 nH.

After that, the inductive readout IC and the anchoring coil are mounted and interconnected on the second PCB, as shown in Fig. 4.6(b). A 24 cm nitinol wire with a diameter of 0.5 mm is connected to the PCB to mimic the conductive anchoring loop for implantable systems. The two through-hole vias for the nitinol wire connections on the PCB are placed very close to the IC pads to minimize the parasitic capacitance. As Fig. 4.6(b) shows, the anchoring loop is placed in cylinder tubes with inner diameters ranging from 20 mm to 30 mm to measure the inductance shift due to the elastic deformation. Fig. 4.8(a) and (b) show the change of the output code with respect to the diameter D and $\sqrt{D}$, respectively. The output code linearly increases with the square root of the tube diameter and achieves a resolution of 0.24 mm in a 10 mm diameter range.

Table 4.1 summarizes the performance of the inductive readout to measure the diameter of the pulmonary artery. The inductance resolution of the system is 0.42 nH in a 500 nH range. The diameter resolution of the system is 0.24 mm, which is about four times better than the typical lateral resolution of echocardiography.

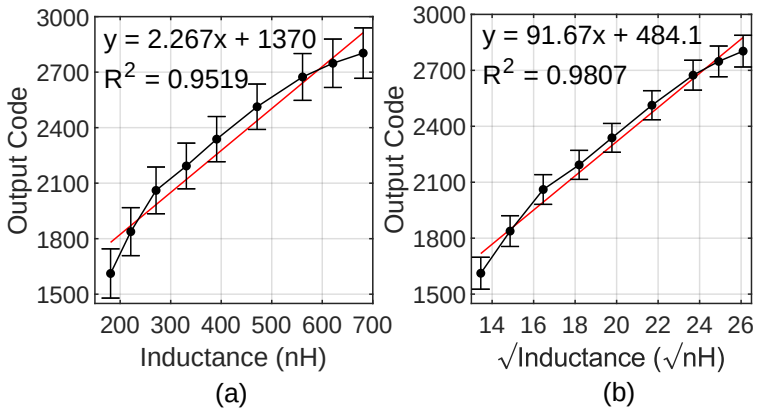


Figure 4.7: Measured decimated output of the inductive readout with respect to (a) the inductance (L), and (b) $\sqrt{L}$.

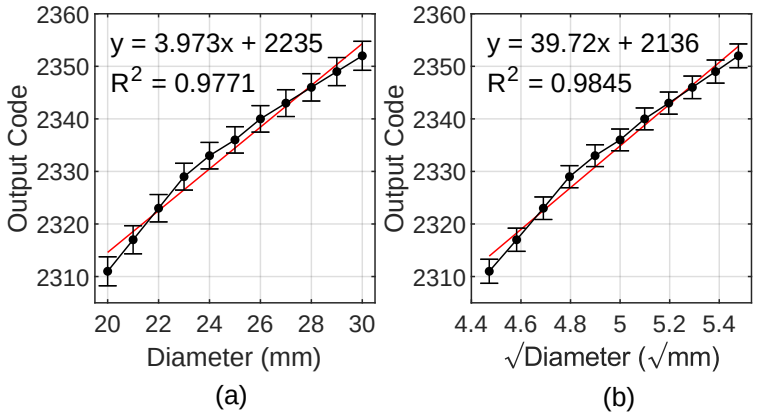


Figure 4.8: Measured decimated output of the inductive readout with the nitinol anchoring loop with respect to the cylindrical tube's (a) diameter D, and (b) $\sqrt{D}$.

4.5 Conclusion

This chapter introduced a novel system for the direct and continuous (24/7) monitoring of the CSA of an artery, particularly the PA, to achieve accurate measurements of cardiac output for effective HF monitoring. The system exploits the inductive characteristic of an anchoring loop that mounts the implant in a branch of the PA. The deformation of the loop changes its inductance, which is correlated with the diameter and CSA of the artery section. A VCO-based inductive readout IC was implemented in a 180-nm process, and the anchoring loop was realized by 24 cm nitinol wire with a diameter of 0.5 mm. The CSA measurement system achieves a resolution of 0.42 nH in a 500 nH range and consumes 39.7 µA to 51.2 µA from a 1.2 V supply. The inductance change of the anchoring loop was tested in cylinder tubes with diameters ranging from 20 mm to 30 mm. The loop's inductance increases as the cylinder's diameter is enlarged, and the readout circuit achieves a resolution of 0.24 mm in a 10 mm diameter range, which is four times higher than the lateral resolution of echocardiography.

Table 4.1: Performance summary of the inductive readout for artery CSA measurement.

Technology (nm)	180
Supply Voltage (V)	1.2
Current Consumption (μA)	39.7[a] - 51.2[b]
Inductance Range (nH)	181 to 681
Inductance Resolution (nH)	0.42
Artery Diameter Range (mm)	20 to 30
Diameter Resolution (mm)	0.24

[a]when L = 681 nH, [b]when L = 181 nH.

In future work, the readout's resolution can be improved to be better than 0.1 mm to achieve more accurate CSA, and thus CO monitoring. Additionally, two orthogonal loops can be employed to improve the CSA measurement, especially in non-circular artery sections.

5 Wireless Ultrasonic Power and Data Transfer

This chapter introduces a wireless ultrasound (US) power and data platform for efficient powering and robust communication of deeply implanted medical devices. In order to reduce the overall dimensions, the implantable system is designed to use a single piezoelectric transducer for both power harvesting and data communication. The operation of the system is as follows: An external piezoelectric transducer beams US power to the implantable piezoelectric transducer, the implant is powered up, samples the sensor data, returns this data via modulating reflected US waves, and the external transducer recovers the returned US data. The wireless powering and communication circuits were designed by Dr. Kerim Türe of the EPFL Radio Frequency Integrated Circuits Group and fabricated in a standard 180-nm process. I conducted electrical measurements and ultrasound experiments to characterize the performance of the US link at significant depths by using a tissue phantom with a thickness of 8.5 cm. The measured link efficiency of the energy harvesting chain is 1.8%, and for an available electrical power of >60 μW, as the average power consumption of the readout circuits, the incident acoustic intensity is less than 0.5% of the FDA diagnostic limit. This demonstrates the feasibility of providing a higher power budget to the implant. While receiving the transmitted power, the implantable transducer uses amplitude shift keying (ASK) modulation to simultaneously return the data to the external transducer through US backscattering. The data rate is set to 40 kbps, and the measured modulation index of the received signal by the external transducer is 26%, providing a robust and reliable communication link.

This chapter is organized as follows: Section 5.1 describes wireless power transfer (WPT) techniques for implantable medical devices, whereas Section 5.2 explains WPT and data communication using ultrasound. Section 5.3 presents the employed external and implantable piezoelectric transducers and discusses the selection of the US operating frequency based on FDA regulations. The power management circuits for power recovery and their measurement results are presented in Section 5.4. The wireless US backscatter communication and the selection of the data rate are discussed in Section 5.5. In Section 5.6, the US link for wireless powering and communication is characterized by using an 8.5 cm tissue phantom, and the measurement results are discussed. Finally, Section 5.7 concludes the chapter.

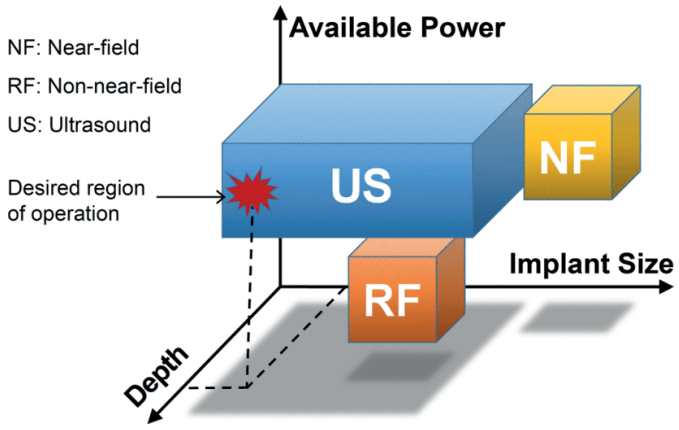


Figure 5.1: Conceptual diagram showing applicable regimes of different WPT methods [44].

5.1 Wireless Power Transfer (WPT) Techniques for Implants

Wireless power transfer and miniature design greatly reduce the invasiveness and discomfort associated with traditional implantable medical devices (IMDs) that use wires or batteries. Wired IMDs are uncomfortable, prone to infection, and not suitable for long-term and remote monitoring of patients. On the other hand, batteries are bulky and their limited lifetime requires surgical intervention for replacement. WPT is the most suitable method to power highly miniaturized IMDs for remote patient monitoring systems. In addition to WPT, IMDs also benefit from a wireless bi-directional communication link.

In the literature, several WPT methods were presented as near-field (NF) magnetic coupling by inductive link [109, 110], NF electric coupling by capacitive link [111, 112], mid-field (MF) and far-field (FF) electromagnetic (EM) radiation by antennas (radio-frequency (RF) transmission) [113, 114], and ultrasound (US) transmission by piezoelectric transducers [115, 116, 44, 45]. The criteria for selecting the optimal method are mainly the WPT range, implant size, and the power budget needed by the implant.

Fig. 5.1 provides a conceptual view of applicable regimes of different WPT methods. NF coupling is efficient to transfer high power over short range (small depth), and requires two bulky inductors for magnetic coupling or capacitors for electric coupling [112]. Mid and far-field RF transmission is limited in terms of power and range due to mismatch between the wavelength and aperture of mm-sized antennas, as well as high attenuation in the tissue at the high-frequency band. As a result, NF coupling and RF power transfer are inefficient for large depth/volume figure of merit [45]. As Fig. 5.1 demonstrates, US is the most efficient way to transfer power to miniature implants (mm-sized) at great depths (>8 cm).

In this thesis, ultrasound is selected for both power delivery and data transmission due to its advantages for deeply implanted miniature devices. Firstly, US has smaller wavelengths in tissue (~1.5 mm at 1 MHz), enabling efficient focusing to millimeter spots at great depths (>8 cm) and high acoustic-electrical conversion efficiency with mm-sized receivers [45]. Secondly, US

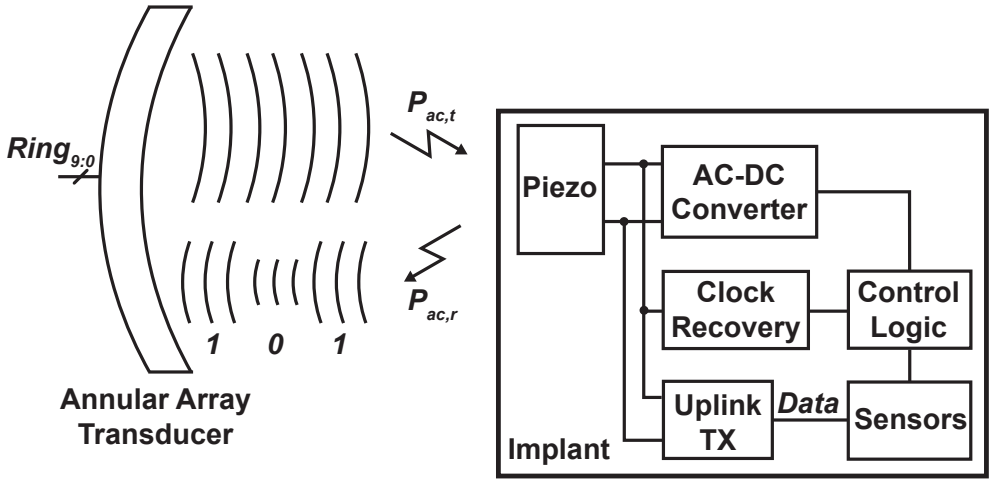


Figure 5.2: Block diagram of the US link for simultaneous power and data transfer.

signals experience lower tissue attenuation (0.3-1 dB·cm^{-1}·MHz^{-1}) [53]. Lastly, FDA allows an intensity of 7.2 mW/mm^2 for diagnostic ultrasound applications [52], while the safe RF exposure limit in the body is only 10-100 uW/mm^2 [117]. As a result, ultrasound is favorable for transferring power to miniature, deeply-implanted medical devices.

Moreover, US waves can be used for wireless data transfer. Since the data rates required in typical implant applications are low (~kS/s), a carrier frequency above about 1 MHz is feasible for a pure US data link. This work uses a single implantable piezoelectric transducer (piezo) for both power recovery and data transmission.

5.2 WPT and Communication Using Ultrasound

Ultrasound link is the most efficient way to power small-volume implants at great depths, and achieves the state of the art in depth/volume figure of merit [45]. In addition, a purely US bi-directional data link is feasible at low data rates. Therefore, a single piezoelectric transducer can be used as a transceiver for both power harvesting and data communication.

Fig. 5.2 shows the block diagram of the US link for simultaneous power and data transfer. An external piezoelectric transducer (e.g. annular array transducer) converts electrical power into mechanical (acoustic) power and transmits the acoustic power toward the implant. Hence, a second transducer (piezo), which is in the implant, converts the acoustic power into electrical power to energize the implanted device. Then, the implanted device is able to send the data relative to the sensor activity back to the external transducer by backscattering.

The acoustic power harvested in the form of AC power by the piezo requires to be converted to DC by power harvesting circuits in the implant. The power harvesting chain consisting of a rectifier followed by voltage regulators acts as an AC-to-DC converter and provides clean and reliable DC supplies to the sensor nodes. The clock of the implantable system is also recovered

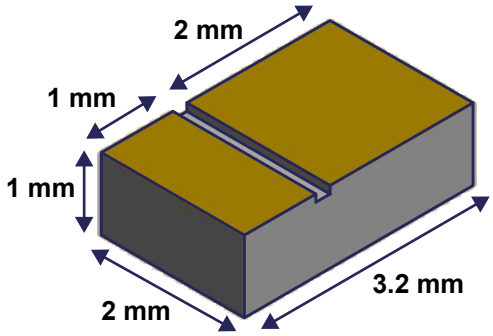


Figure 5.3: Implantable piezoelectric transducer with dimensions of 3.2 mm × 2 mm × 1 mm.

from the AC power harvested by the piezo. While receiving the transmitted power, the piezo simultaneously returns the data to the external transducer through US backscattering. The load modulator, which is connected between two inputs of the rectifier, changes the load impedance and the amplitude of the reflected signal depending on the value of the data. Thus, an amplitude shift keying (ASK) modulation scheme is obtained for uplink data transmission. As a result, the power and uplink data transmission can be simultaneously performed by using a single piezo.

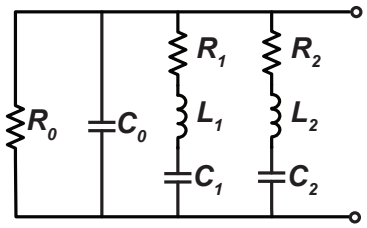
5.3 Piezoelectric Transducers

An ultrasound transducer converts mechanical (acoustic) energy into electrical energy based on piezoelectric effect by using piezoelectric materials such as Lead-Zirconate-Titanate (PZT). Conversely, electrical energy can also be converted into mechanical energy. In this work, an implantable transducer and an external transducer are used to establish the US link between the implant and the external environment.

5.3.1 Implantable Transducer (Piezo)

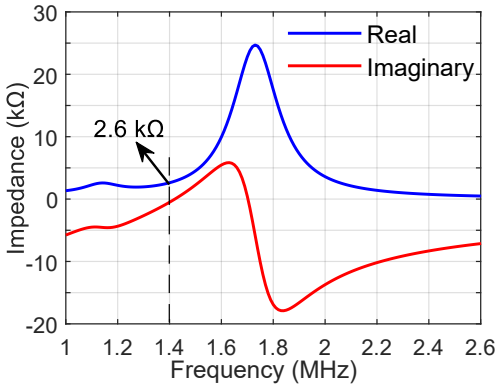
The ultrasonic and electrical characteristics of a piezoelectric transducer, such as the frequency, impedance, and effective aperture, are primarily determined by its piezoelectric material, thickness, and cross-sectional area. In addition to its material and dimensions, the impedance and available power of a piezoelectric transducer also depend on acoustic loadings from the package [44].

The implantable transducer in this work was custom designed and fabricated by IMASONIC. Its dimensions are limited to 3.2 mm × 2 mm × 1 mm due to the very small volume budget in the implant. The operating frequency is mainly controlled by the thickness of the transducer, and increasing the thickness of the piezoelectric material decreases the operating frequency of the transducer [118]. Due to strict volume limitations, the piezo's thickness is set to 1 mm. The simulated operating frequency (f_0) is around 1.4 MHz when the acoustic loadings from the



	i=0	i=1	i=2
R_i (kΩ)	179	16.5	2.8
L_i (mH)		15.7	2.4
C_i (pF)	11	1.3	5.4

(a)



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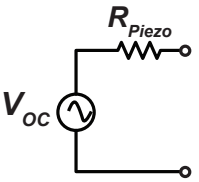


(c)

Figure 5.4: (a) Equivalent circuit model and (b) the simulated impedance of the piezo including the effect of acoustic loadings from 150-µm thick glass. (c) Equivalent circuit model of the piezo at short-circuit resonance frequency.

package are included. Fig. 5.3 shows the designed and fabricated piezo with its dimensions. The total area on the surface is 3.2 mm x 2 mm and the active transducer area is 2 mm x 2 mm.

The selection of the operating frequency at 1.4 MHz is also suitable for FDA safety limits. One of the safety parameters, the mechanical index, is an estimation of the degree of bio-effects, such as cavitation. The mechanical index is inversely proportional to $\sqrt{f_0}$ and must not exceed 1.9 for diagnostic ultrasound [52]. Therefore, low operating frequencies have to be avoided, and f_0 should be at least about 1 MHz to keep the mechanical index lower than 1.9 at different acoustic pressures [119]. An operating frequency of 1.4 MHz is very safe in terms of mechanical index; however, increasing the operating frequency results in a higher attenuation factor in the medium.

The impedance and available power of a piezo are also dependent on acoustic loadings from the package. To ensure biocompatibility, the implantable system will be glass-packaged with a thickness of 150-µm. Therefore, IMASONIC designed the piezo by considering the effect of the glass package. They simulated that the glass package shifts the optimum operating frequency to lower frequencies.

IMASONIC provided the equivalent circuit model of the transducer. The rectifier in the energy recovery circuit was designed and optimized for the given model. Fig. 5.4(a) and (b) respectively present the equivalent circuit model and the simulated impedance of the piezo by including the effect of acoustic loadings from the 150-µm glass package. A piezoelectric transducer has a short-circuit frequency at which its impedance can be purely real. Fig. 5.4(b) shows that the short circuit resonance of the designed piezo is about 1.4 MHz and the short-circuit impedance is about 2.6 kΩ. Fig. 5.4(c) demonstrates the equivalent circuit model of the transducer at short-circuit resonance frequency where R_{Piezo} is 2.6 kΩ. When the

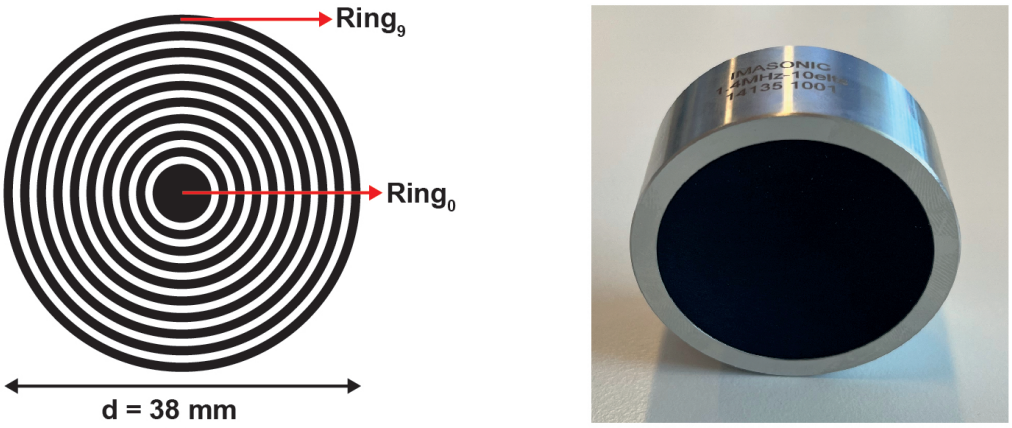


Figure 5.5: (a) Schematic and (b) photo of the external transducer which is an annular array transducer consisting of 10 rings.

impedance of the transducer alone (without the glass package) is measured, the short-circuit resonance is about 1.6 MHz because the glass package shifts the short-circuit impedance to lower frequencies by about 200 kHz.

Another FDA safety regulation is that the maximum acoustic intensity must be lower than 7.2 mW/mm^2 for diagnostic ultrasound [52]. The active surface area of the piezo is 4 mm^2. The available electrical power, P_{AV}, for an incident acoustic intensity, I_0, is defined as [44]

$$P_{AV} = \eta \times I_0 \times Area, \tag{5.1}$$

where η is the acoustic-to-electrical conversion efficiency. The conversion efficiency of these transducers is typically higher than 50%. For an available electrical power of about 60 µW, as the average power consumption of the readout circuits, the acoustic intensity required for implant operation is 30 µW/mm^2, which is less than 0.5% of the FDA diagnostic limit. This allows the acoustic intensity to be increased to reach even the mW power range while still meeting the FDA safety regulations.

5.3.2 External Transducer

The external transducer is an annular array transducer consisting of 10 rings, custom designed and fabricated by IMASONIC. The outer rings are used to transmit energy, while the inner rings are utilized to retrieve data from the implanted device. Fig. 5.5 shows (a) the schematic and (b) the photo of the external transducer. All the rings have equal surface areas of 95 mm^2.

Beamforming is a process of adjusting the delays in electrical signals applied to individual elements of an array to focus the acoustic beam at a given depth and location. This annular array transducer can focus the beam at depths between 5 cm and 12 cm by adjusting the

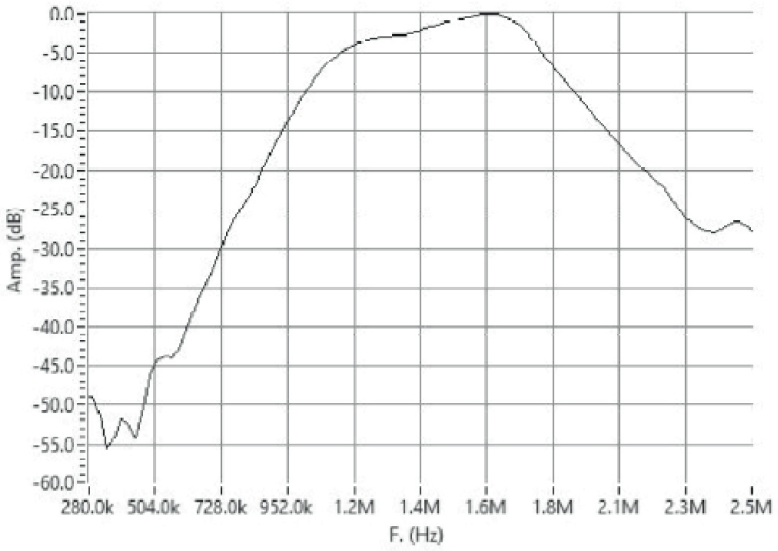


Figure 5.6: Measured frequency spectrum of the external transducer, provided by IMASONIC.

phases of sinusoidal signals applied to different rings. Fig. 5.6 shows the measured frequency spectrum of the external transducer when it is focused at 12 cm. The central frequency is 1.46 MHz and the bandwidth (-6 dB) is 740 kHz.

5.4 Ultrasonic Power Transfer

The US energy harvested in the form of AC power by the implanted transducer needs be converted to DC energy by power recovery circuits in the ASIC. Fig. 5.7 illustrates the building blocks of the implantable system. The power recovery circuits consist of a rectifier to convert the received AC signal to an unregulated DC signal, two voltage regulators such as low drop-out (LDO) regulators (LDO_1 and LDO_2) to regulate the output of the rectifier and to provide clean DC supply voltages, and a third LDO regulator (LDO_{CM}) to provide a common-mode (CM) voltage to the sensor readout blocks. In addition, a diode-based protection circuit is employed to keep the input voltage of the rectifier always lower than 3 V_{pp}.

For a maximum energy transfer, the input impedance of the power recovery chain should match the impedance of the piezo. The input resistance (R_{in}) of a typical AC-DC power recovery circuit is given by:

$$R_{in} = \frac{V_{in}^2}{2P_{in,avg}} = \frac{V_{in}^2 \times \eta_{AC-DC}}{2P_{out,dc}}, \tag{5.2}$$

where V_{in} is the voltage at the input of the rectifier, $P_{in,avg}$ is the average input power of the IC, η_{AC-DC} is the AC to DC conversion efficiency, and $P_{out,dc}$ is the DC load power at the output of the LDO regulator. For V_{in} between 2.1 - 2.6 V_{pp}, $P_{out,dc}$ between 50 µW - 550 µW, and

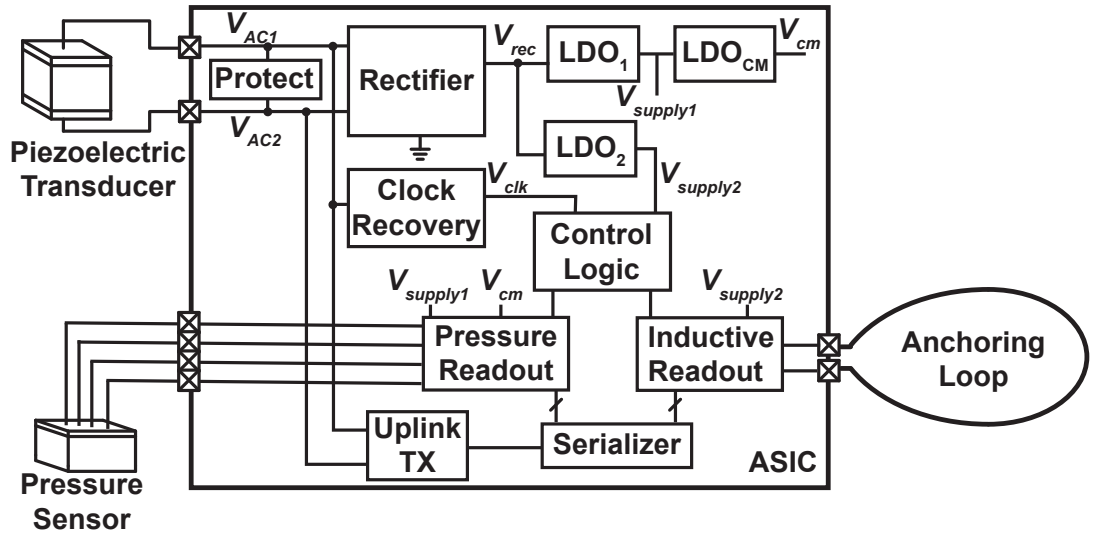


Figure 5.7: Building blocks of the implantable device.

η_{AC-DC} between 40 - 70 %, R_{in} ranges from 2.8 kΩ and 27 kΩ. This assumes that the efficiency is highest at high output power and lowest at low output power. The input impedance also includes the parasitic shunt capacitance of MOS capacitors connected to AC inputs. However, the parasitic shunt capacitance can be ignored at the frequency of interest (1.4 MHz) and for typical values of R_{in}. Therefore, the AC-DC converter is designed to have an R_{in} in a similar range with the piezo's resistance of ~kΩ, which enables achieving a good power conversion efficiency (PCE) without using an input matching network. An input matching network would require a bulky off-chip inductor at the frequency of interest.

5.4.1 Rectifier

A rectifier converts the received AC signal to an unregulated DC signal. Different structures of integrated rectifiers have been reported for IMDs [44, 120, 121, 122, 123]. In general, a full-wave rectifier can provide a larger output voltage than a half-wave rectifier, resulting in a larger voltage conversion efficiency [122]. Fig. 5.8(a) shows the well-known full-wave diode-bridge rectifier. A diode has a forward voltage drop, which must be minimized to increase the PCE. A Schottky diode provides low voltage drop and is widely used in discrete circuits. However, Schottky diodes are not available in many CMOS processes since they require additional process steps and create extra manufacturing costs [123]. Alternatively, integrated rectifiers use diode-connected transistors, but two threshold voltage (V_{TH}) drops limit their ability to achieve high PCE. To improve PCE, active-diode rectifiers have been reported, since active diodes have low on-resistance in comparison to the diode-bridge structure. However, they suffer from reverse leakage current, causing degradation in PCE.

In this thesis, a full-wave comparator-based active rectifier is employed. Fig. 5.8(b) shows the schematic of the full-wave active rectifier, which includes a pair of gate cross-coupled NMOS

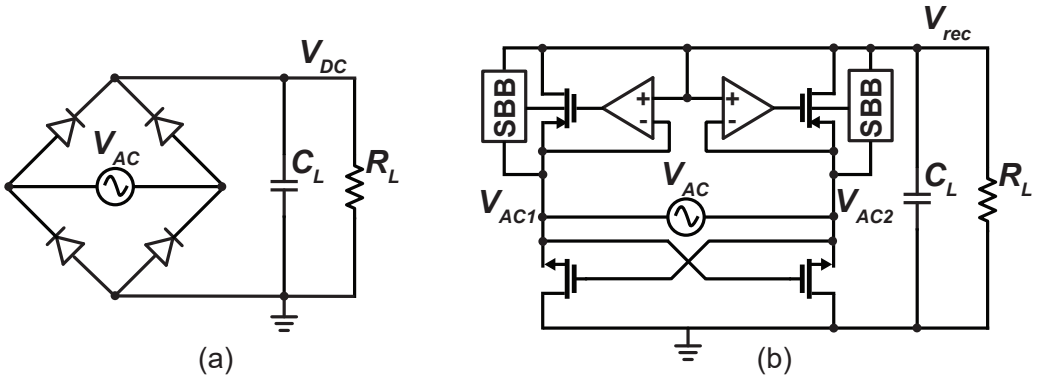


Figure 5.8: Schematics of a (a) full-wave diode-bridge rectifier and (b) full-wave comparator-based active rectifier.

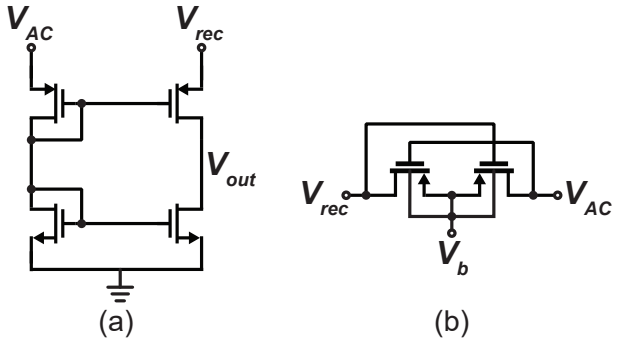


Figure 5.9: Schematics of a (a) conventional common-gate-type comparator and (b) dynamic body bias circuit.

and active PMOS diodes used as switches [123]. This design allows for a low dropout voltage across the transistors, resulting in a high PCE. The gates of the PMOS switches are driven by self-dynamically-powered high-speed comparators that do not require fixed voltage supplies [123]. Fig. 5.9(a) shows the schematic of the conventional common-gate-type comparator used in the rectifier and designed for fast transition and low power to maximize the rectifier's PCE. The dynamic body biasing circuit eliminates the body effect of the PMOS power transistor and is presented in Fig. 5.9(b).

The active full-wave rectifier was designed and implemented in a standard CMOS 180-nm technology. Although the sensor readout circuits are biased at 1.2 V, the input and output voltages of the rectifier can exceed 1.98 V (the maximum voltage for 1.8-V core transistors) due to the voltage drops of the rectifier and regulator. Therefore, the rectifier is implemented by 3.3-V IO transistors. A diode-based protection circuit is employed to ensure that the input voltage of the rectifier is always lower than 3 V_{pp}. To reduce the ripples on the rectified voltage, an on-chip load capacitance is used. Due to the limited area budget, the selected load capacitance is 300 pF. Fig. 5.10 shows the die micrograph of the complete application-specific integrated circuit (ASIC), and the rectifier has a core area of approximately 0.2 mm^2.

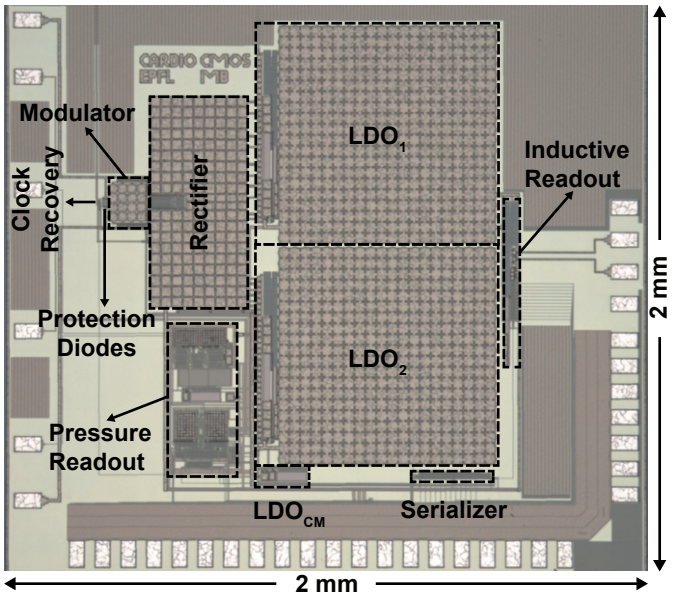


Figure 5.10: Die micrograph of the ASIC in 180-nm CMOS.

The rectifier is characterized for low and high output load powers. To mimic the average power consumption of the pressure and inductance readouts, a 68 kΩ load resistance is employed, resulting in low load power levels of about 40-80 µW. To mimic the power consumption of the readouts when the pressure sensor and the instrumentation amplifier (IA) are active for about 1.56 µs in 1 ms conversion time, a 4.7 kΩ load resistance is employed, resulting in high load power levels of about 0.5-1 mW. Fig. 5.11(a) shows the rectifier output voltage (V_{rec}) versus the input voltage (V_{in}) for different output loads, and Fig. 5.11(b) shows V_{in}-V_{rec} versus V_{in} for 68 kΩ load resistance. V_{rec} must be higher than 1.6 V to ensure that the input voltage of the regulator is higher than 1.6 V to generate a clean supply voltage at 1.2 V. Thus, the rectifier's input voltage has to be higher than 2.1 V_{pp}. As shown in Fig. 5.11(b), the rectifier has the highest voltage conversion efficiency when V_{in} is between 2.1 V_{pp} and 2.6 V_{pp}. In addition, when V_{in} is increased to be higher than 3 V_{pp}, there is no increase in V_{rec} since the protection circuit becomes active and keeps the input of the rectifier always lower than 3 V_{pp}. For optimum rectifier operation, V_{in} should be between 2.1 V_{pp} and 2.6 V_{pp}.

The rectifier's PCE is measured at V_{rec} = 1.85 V for 50 µW and 750 µW output loads, and is equal to 79% and 88%, respectively. For low load powers, the rectifier has lower PCE since the losses in the comparator and power transistors are comparable with the output power. As the output power increases, the power delivered to the load becomes dominant and the PCE improves.

5.4.2 Voltage Regulator

The circuits in the implantable system are designed to work with constant DC supply voltages. The rectifier's output provides an unregulated DC voltage with a ripple. To eliminate this ripple

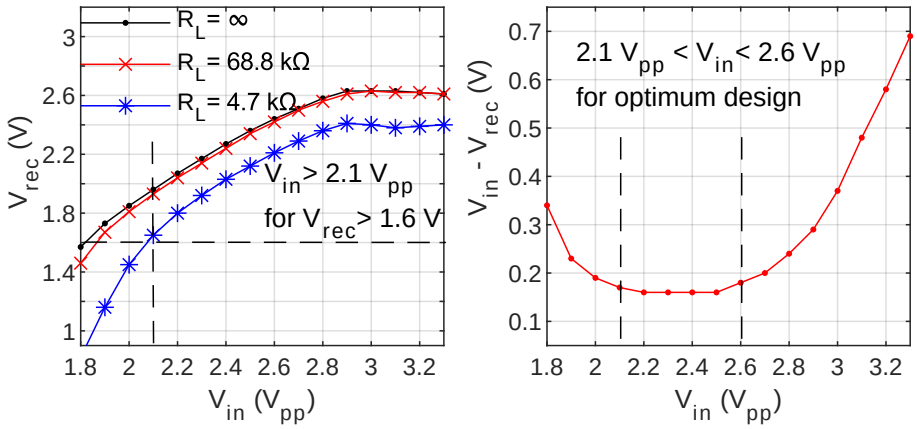


Figure 5.11: (a) Rectifier output voltage (V_{rec}) versus input voltage (V_{in}) for different output loads, and (b) V_{in}-V_{rec} versus V_{in} for 68 kΩ load resistance.

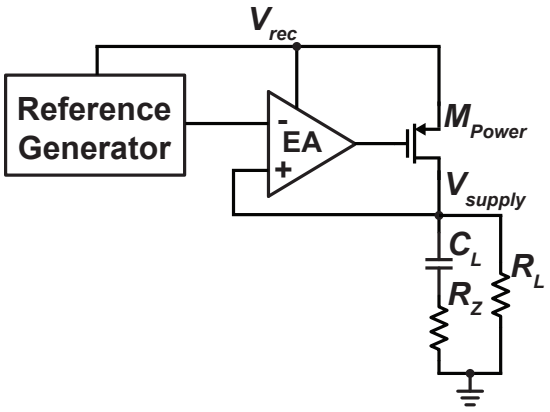


Figure 5.12: Schematic of the LDO regulator.

and provide a clean and reliable DC voltage independent of the input voltage and load power, a voltage regulator is employed. To minimize the loss in the regulation system and have an efficient energy transfer link, low drop-out regulators are utilized.

Fig. 5.12 shows the schematic of the designed fully-integrated LDO regulator to provide a 1.2 V regulated output DC voltage. The LDO regulator comprises an error amplifier (EA), a reference generator, and a PMOS power transistor, all of which are connected to the rectifier's output. The EA controls the gate voltage of the power transistor so that the output voltage matches the generated reference voltage, resulting in a constant, ripple-free DC voltage. In this application, a PMOS power transistor is used since it provides low voltage drop and high power efficiency without adding complexity to the circuit [124].

The power supply rejection (PSR) and the response time of the regulation are respectively determined by the gain and bandwidth of the error amplifier. The unity-gain bandwidth of the EA should be large enough to eliminate ripples at the energy transfer frequency [125]. Fig. 5.13(a) shows the schematic of the single-stage differential amplifier used as an EA. The

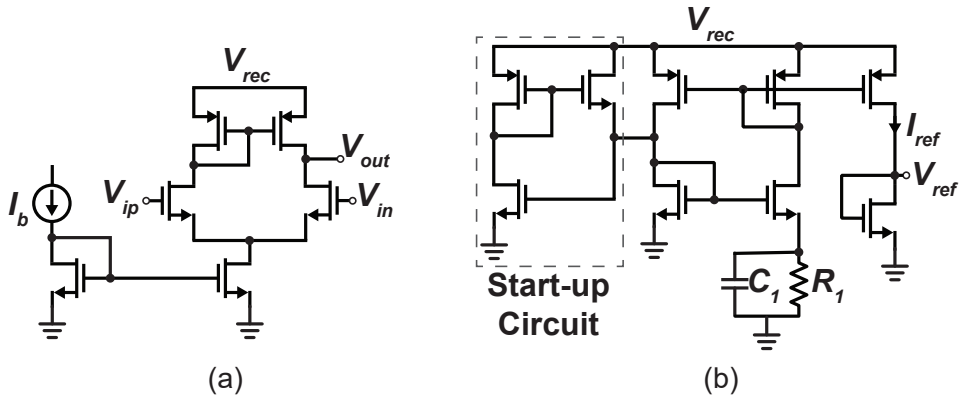


Figure 5.13: Schematic of (a) the single-stage differential amplifier used in the EA, and (b) the Beta-multiplier current reference used as the reference generator.

LDO regulator requires a reference voltage at the input of the EA to compare the regulated supply voltage. As the LDO regulator is supplied by the unregulated output of the rectifier, the reference voltage should be independent of the supply voltage. Fig.5.13(b) shows the schematic of the Beta-multiplier current reference with its start-up circuit to generate a supply-independent reference voltage of 1.2 V.

Due to the miniature volume requirements of cardiac implants, a bulky off-chip capacitor cannot be used. For fully-integrated LDO regulators, large load capacitors are not available; thus, both transient response and PSR degrade significantly. In addition, a large load capacitor moves one dominant pole to lower frequencies and improves the loop stability [125, 126]. To meet the area constraint in the ASIC and keep the load capacitance as high as possible, a 716 pF on-chip output capacitor is employed. To improve the phase margin of the LDO regulator, zero compensation is applied by adding a resistor in series to the load capacitor.

The LDO regulator is designed to ensure that the minimum regulated voltage does not drop below 1.16 V in any mismatch and process variation conditions. Monte Carlo simulations for 200 samples show that the mean supply voltage is 1.23 V with a standard deviation of 22 mV. Post-layout AC simulations are performed to measure the PSR ratio (PSRR) at different input voltages. When V_{in} = 1.6 V, the PSRR around DC is 39.6 dB, whereas it is equal to 43.8 dB at 2.56 MHz, which is the frequency of the rectifier's ripple. When V_{in} = 2 V, the PSRR around DC is 54.2 dB, whereas it is equal to 44.6 dB at 2.56 MHz. To maintain the PSRR around DC at more than 47 dB, the input voltage of the regulator should be higher than 1.7 V.

The LDO regulator was designed and fabricated in a 180-nm standard CMOS process. It was implemented by 3.3-V IO transistors since its input may exceed 1.98 V. Due to the limited area budget, the selected load capacitance is 716 pF. Fig. 5.10 shows that the LDO regulator is the most area-consuming block of the ASIC, occupying 0.5 mm^2 chip area.

The LDO regulator is characterized for low and high output load powers, similar to the rectifier. To mimic the readouts' average power consumption of approximately 50 µW, a 27 kΩ load

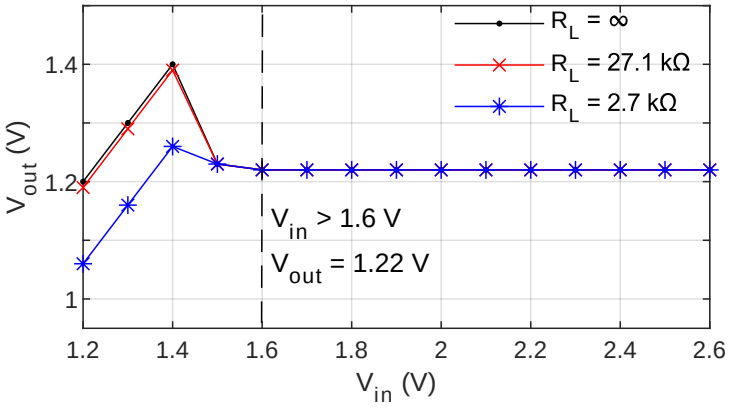


Figure 5.14: Measured output voltage of the LDO regulator versus its input voltage for different output loads.

resistance is used. For the readouts' peak power consumption of about 550 µW, a 2.7 kΩ resistive load is employed. The dropout voltage of the LDO regulator is set to 400 mV in the design. Fig. 5.14 shows the LDO regulator's output voltage (V_{out}) versus its input voltage (V_{in}) at different loads. It demonstrates that V_{in} must be higher than 1.6 V to generate a clean and reliable supply voltage at 1.22 V, which is independent of V_{in} and the load power. The measured quiescent current of the LDO regulator is 18.5 µA. The measured PCEs for output load powers of 55 µW and 550 µW at V_{in} = 1.6 V are 58.2% and 77.8%, respectively.

5.4.3 Voltage Regulator to Generate Common-Mode Voltage

The SAR ADC in the pressure sensor readout uses V_{cm}-based switching technique. The fully-differential SAR ADC requires a stable common-mode (CM) voltage at 0.6 V. A voltage divider is insufficient since the CM voltage must drive the capacitive DAC array. Therefore, a second LDO regulator is designed for charging and discharging the sampling capacitors to 0.6 V.

Fig. 5.15 shows the schematic of the designed LDO regulator (LDO_{CM}) supplied by the regulated output of the first LDO regulator. The reference voltage of the LDO_{CM} is generated by a voltage divider so that the mismatch and process variation shift the CM voltage less than 500 µV in worst-case corners. The proposed LDO_{CM} was designed and fabricated in a 180-nm standard CMOS process, and it was implemented by 1.8-V core transistors. As its supply is already regulated by the first LDO regulator, the load capacitance is selected to be only 1 pF. Fig. 5.10 shows the ASIC with LDO_{CM}, which has a core area of 51 × 151 µm^2.

LDO_{CM} is characterized using a 7.5 pF capacitive load to mimic the capacitive DAC of the SAR ADC. In extreme cases, charging from 0 V to 0.6 V and discharging from 1.2 V to 0.6 V, the settling time is less than 400 ns, which is sufficiently fast for this application. The measured quiescent current of LDO_{CM} is 16.7 µA, and the PCE is less than 30% since the load current is very low.

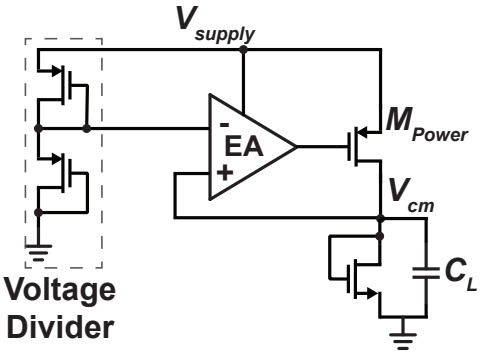


Figure 5.15: Schematic of the LDO regulator generating CM voltage.

5.4.4 System Level Measurements of the Power Recovery Circuits

Initially, system-level measurements of the power recovery circuits are performed without the US transducer, using a waveform generator to provide a sinusoidal input signal to the rectifier. The supply voltage, V_{supply}, generated by the first LDO regulator, is connected to the bridge-to-digital converter (BDC) consisting of a pressure sensor and its readout circuits. The CM voltage, V_{cm}, generated by LDO_{CM}, provides the CM voltage to the IA and SAR ADC in the pressure readout circuits. The clock of the system is generated by a clock recovery circuit, which will be explained in Section 5.5.

Fig. 5.16 shows V_{rec}, V_{supply}, and V_{cm} when a 2.1 V_{pp} sinusoidal signal at 1.28 MHz is applied to the input of the rectifier. The sampling rate of the BDC is 1 kS/s, and the pressure sensor and the IA are active for about 1.56 µs in a 1 ms conversion time. At this 1.56 µs time interval, the BDC draws a higher current at about 600 µA. During a conversion cycle, V_{rec} is about 1.9 V with ~30 mV fluctuations due to noise and ripple. When the pressure sensor and the IA are active, V_{rec} drops to 1.4 for about 1.56 µs. The LDO regulator regulates the output of the rectifier and generates a supply voltage of 1.224 V with fluctuations less than 1 mV. The activation of the pressure sensor and the IA leads to a 9 mV drop in the supply voltage for about 1 µs. The LDO regulator generating the CM voltage, V_{cm}, is supplied by the first LDO regulator and generates a CM voltage at half of V_{supply}. V_{cm} is 608 mV and has fluctuations of about 1 mV. The 9 mV voltage drop in V_{supply} causes a 4.5 mV voltage drop in V_{cm}.

Next, the amplitude of the applied signal is increased from 2.1 V_{pp} to 2.6 V_{pp}. As shown in Fig. 5.17, fluctuations in the powering signals do not change significantly since the output load is the same. However, the voltage drop of the supply decreases from 9 mV to 6 mV since V_{rec} is always higher than 2.1 V. This result shows that a higher input voltage increases the energy consumption without providing a significant improvement.

In the previous measurements, the LDO regulator was biasing only the BDC and LDO_{CM}. Then, the output of the LDO regulator is also connected to the inductive readout circuit measuring the artery diameter. In this configuration, the same LDO regulator provides a supply voltage to the BDC, inductive readout, and LDO_{CM}. It is expected that the inductive readout circuit

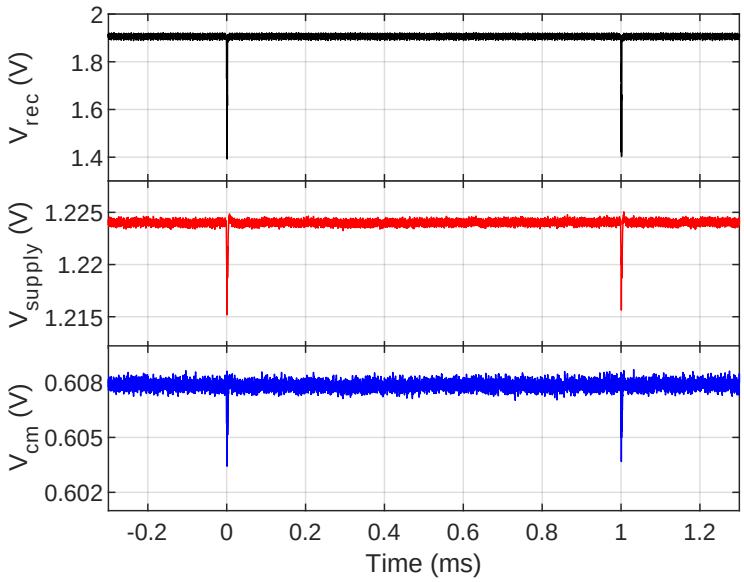


Figure 5.16: Measured powering signals supplying the BDC when V_{in} = 2.1 V_{pp}.

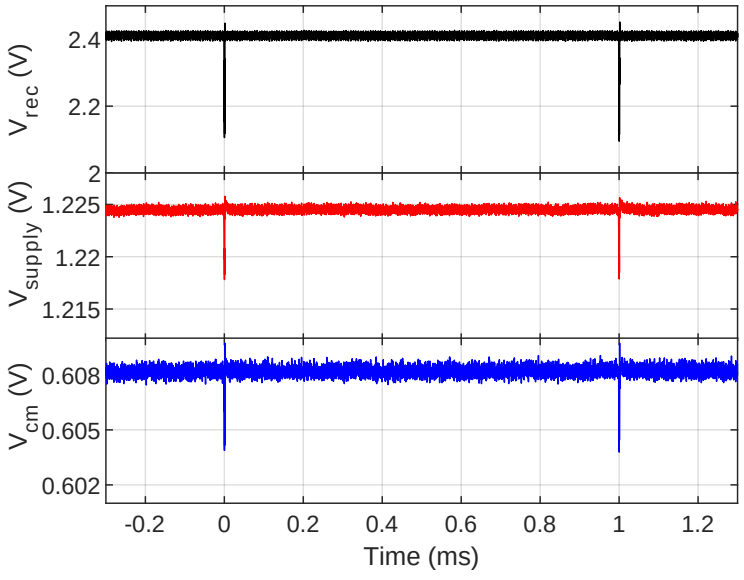


Figure 5.17: Measured powering signals supplying the BDC when V_{in} = 2.6 V_{pp}.

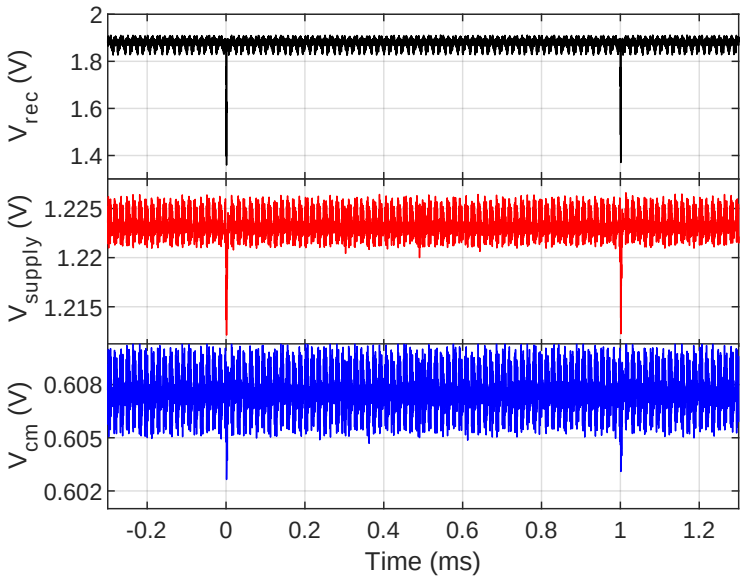


Figure 5.18: Measured powering signals supplying the BDC and the inductive readout when V_{in} = 2.1 V_{pp}.

adds high-frequency ripples and noise to the supply since the inductive readout includes an oscillator operating at about 500 MHz. Fig. 5.18 shows that the fluctuations on V_{rec} become about 80 mV due to the noisy operation of the inductive readout. Similar to the previous measurements, V_{supply} = 1.223 mV and V_{cm} = 608 mV, however, fluctuations in V_{supply} and V_{cm} increase to 5 mV.

The noisy operation of the oscillator in the inductive readout significantly affects the fluctuations in the supply voltage. Therefore, two separate LDO regulators should be used to generate supply voltages at 1.2 V. As shown in Fig. 5.7, the first LDO regulator (LDO_1) provides a supply voltage to the BDC and the LDO regulator generating CM voltage (LDO_{CM}). The second LDO regulator (LDO_2) provides a supply voltage to the inductive readout circuit and noisy digital blocks like the clock divider.

5.5 Wireless Communication

Although the use of RF for power transfer in miniature and deeply implanted devices is limited due to high link loss, it can still be used for data uplink, since the power levels required for communication are much lower than that of power transfer [44]. RF data uplink offers the advantage of a high data rate, but it requires a separate antenna for data uplink, and higher link losses at high frequencies significantly reduce the uplink signal-to-noise ratio (SNR) at great depths. Since the pressure and artery diameter sensing application requires great implantation depths (>8 cm) but only a relatively low data rate (40 kbps), ultrasound is chosen for data uplink. To meet the stringent volume constraint of the implant, a single piezo is

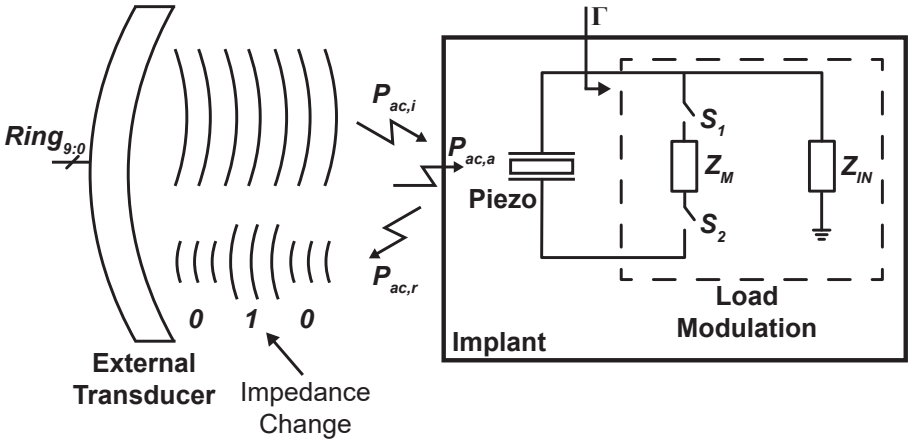


Figure 5.19: Uplink communication through ultrasonic backscattering.

used for both power transfer and backscatter data uplink, with the goal of simultaneously transferring acoustic power while achieving an uplink data rate of 40 kbps through the use of amplitude-shift keying (ASK) modulation.

5.5.1 Ultrasonic Backscatter Communication

In RFID, passive sensor tags transmit data by modulating the incoming RF energy and re-radiating the modulated energy back to the reader. This modulation can be achieved by varying the load impedance, which changes the coefficient of reflectivity [127]. The modulation technique of RFID systems can be adopted for US communication. By modulating the input impedance of the ASIC, the reflection coefficient (Γ) at the interface between the piezo and ASIC is shifted, and the backscatter communication is established between the implant and the external transducer.

Fig. 5.19 represents the uplink communication through ultrasonic backscattering. The external transducer generates acoustic power P_{AC}, which is transmitted toward the piezo. The load of the piezo is the input impedance of the rectifier (Z_{in}), and it matches the piezo's impedance for a high energy transfer. The load modulator is connected between two inputs of the rectifier and changes the piezo's load impedance depending on the value of the data.

The implant modulates the incident acoustic power ($P_{ac,i}$) by shifting the piezo's load. The incident power can be divided into absorbed ($P_{ac,a}$) and reflected ($P_{ac,r}$) acoustic power. The amplitude of the reflected acoustic power is given by

$$P_{ac,r} = P_{ac,i} \times \Gamma, \tag{5.3}$$

where Γ is the reflection coefficient. A reliable communication link can be achieved with an ASK modulation scheme by maximizing the difference between $P_{ac,a}$ and $P_{ac,r}$. When

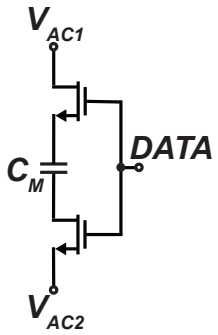


Figure 5.20: Schematic of the modulator circuit.

the piezo's impedance and Z_{in} are perfectly matched, Γ is minimum (close to 0), and all the incident power is absorbed. In the literature, the reflection coefficient is maximized by applying a short circuit to the piezo so that all the incident power is reflected back to the external transducer to improve the communication link [45, 128]. However, the piezo does not harvest energy when the load is shorted to the ground. Although these designs use the same piezoelectric transducer for both energy harvesting and uplink data communication, the communication is achieved at the price of completely stopping energy harvest during the back data transfer.

This work aims to achieve an uplink data transfer using ASK modulation while simultaneously transferring power. In a previous study, Ozeri $et\ al.$ [116] showed that it is possible to achieve an uplink data transfer from an implanted transducer during energy harvesting with less than a 10% reduction in average harvested power by creating a small acoustic mismatch, which increases Γ from 0 to 0.1. Similarly, a small acoustic mismatch is applied by changing the load impedance, which is sufficient to produce detectable uplink data transmission during energy harvesting with less than a 10% reduction in average harvested power.

Fig. 5.20 shows the employed modulator circuit consisting of a capacitor, C_M, and two NMOS switches (S_1 and S_2). When DATA is "0", the NMOS switches are off, and the load of the piezo is Z_{in}, which is well matched to the piezo's impedance. Therefore, the amplitude of the reflected signal is low. When DATA is "1", the NMOS switches become on and connect Z_M between two inputs of the rectifier. It creates an electrical mismatch of <20%, which is low enough for simultaneous power transfer. The modulator was designed and implemented using 3.3-V IO transistors in a standard 180-nm CMOS technology. Fig. 5.10 shows the ASIC with the modulator, which has a core area of 116 µm × 155 µm.

The pressure readout creates a 10-bit output code per conversion, while the inductive readout generates a 12-bit output code. These parallel data have to be serialized before being applied to the modulator. Each data package requires preambles to distinguish the pressure and inductive data, and each transmission cycle. In order to cover the 22-bit sensor output and some additional bits for preambles, the data rate is set to 40 kbps, which is low enough for a 1.28 MHz carrier frequency. The applied communication protocol is as follows: Each 40-bit

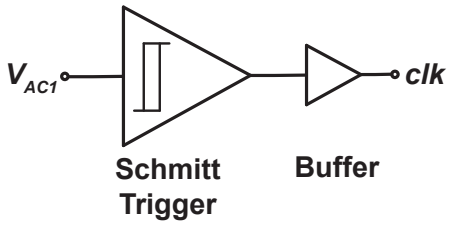


Figure 5.21: Schematic of the clock recovery circuit.

data package starts with a “10” preamble followed by a 10-bit pressure output code. After that, there is a preamble “0010” followed by a 12-bit inductive output code to distinguish the pressure and inductive data. The remaining 12-bit data are set to “0” to enable maximum energy transfer. The serial output is buffered to control the switches of the modulator.

5.5.2 Clock Recovery

The sensor readout circuits require a clock signal, which can be generated by an oscillator or recovered from the received AC voltage for wireless powering. For the simplicity of the system, the clock signal is recovered from acoustic waves received by the piezo. Fig. 5.21 shows the schematic of the clock recovery circuit consisting of a Schmitt trigger [129] and a buffer. The Schmitt trigger uses the received AC voltage by the piezo as the input and creates a square wave at the same frequency as the acoustic waves. Then, the generated clock signal is buffered to the control logic. Although the generated clock does not have a 50% duty cycle due to the hysteresis in the Schmitt trigger, the duty cycle is corrected by the D-flip-flops in the clock divider, and it becomes 50%.

5.6 Ultrasound Characterization

In this section, the wireless powering and communication of the single-piezo implantable system are characterized by using a modular setup allowing for measurement of the various internal nodes of the implantable blocks. Wireless functionality is verified by powering up the implantable system through ultrasound and by measuring the modulation index of the US backscatter, which is reflected from the implant during US power-up.

5.6.1 Modular Test Setup

Fig. 5.22 shows the modular test setup that allows for wireless US measurements while providing access to the internal nodes of the implantable system. To mimic the US attenuation in the body, a tissue phantom is employed.

The average US attenuation (α) along the beam axis in the body is about 0.3 dB·cm^{-1}·MHz^{-1}, and it can be much higher at some body parts, such as 1.09 dB·cm^{-1}·MHz^{-1} in muscles [53].

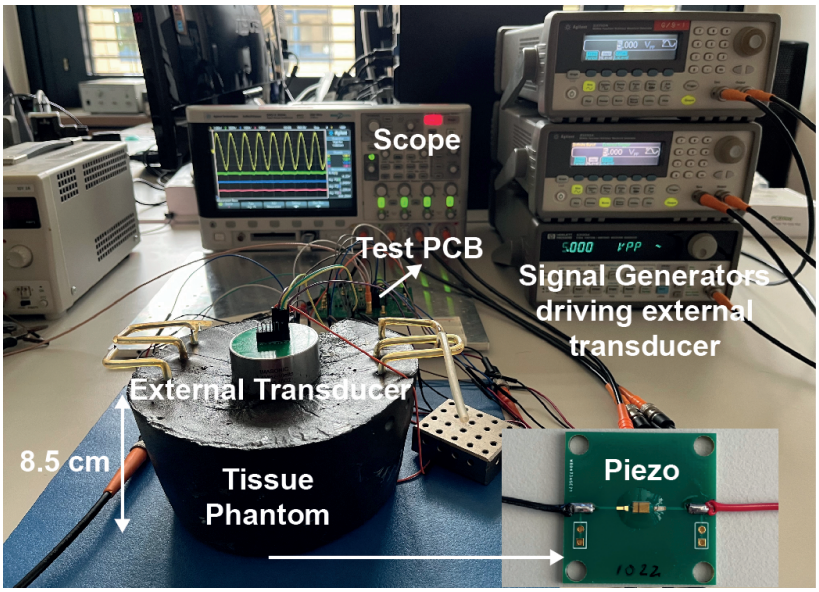


Figure 5.22: Modular test setup for ultrasonic measurements using an 8.5 cm tissue phantom.

Since the attenuation coefficients for human tissues are much higher than the ultrasonic attenuation in water ($\alpha = 0.0022$), a tissue phantom developed by INSERM [119] is employed. The measured attenuation of the phantom material is 0.33 dB·cm^{-1}·MHz^{-1}, which is very close to the average body attenuation. The piezo is wire-bonded on a small PCB and placed at the bottom of the tissue phantom. The external transducer is placed on top of the tissue phantom, and the distance between the two transducers is 8.5 cm. All wireless measurements are conducted through the 8.5 cm tissue phantom.

5.6.2 Experimental Results

Ultrasound Power Transfer

The external transducer, which is an annular array transducer consisting of 10 rings, sends the energy toward the piezo. The sound beam generated by the annular array transducer is focused at a distance of 8.5 cm, with a focal area of 2 × 2 mm^2. To optimize the energy transmission, only three of the rings (Rings$_{3,4,5}$) are employed to transfer power, and all three rings are focused at 8.5 cm depth by applying beamforming, adjusting the delays of the three electrical signals.

The US link efficiency is studied to characterize the power transfer. Fig. 5.23 shows the energy harvesting chain used to measure the link efficiency as a function of the DC power delivered at the rectifier output versus AC power applied to the annular rings of the external transducer. While Rings$_{3,4,5}$ transmit energy, the link efficiency can be expressed as:

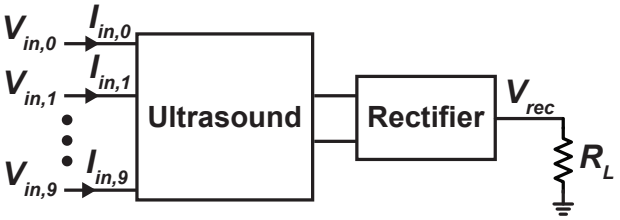


Figure 5.23: Energy harvesting chain for link efficiency characterization.

$$\eta_{link} = \frac{P_{out,rec}}{P_{in,ac}} = \frac{V_{rec}^2}{R_L} \times \frac{1}{\sum_{i=3}^{n=5}(V_{in,i} \times I_{in,i})}, \tag{5.4}$$

where $V_{in,i}$ and $I_{in,i}$ respectively represent the input voltage and input current applied to the rings of the external transducer. The link efficiency includes the conversion efficiencies from electric to ultrasound, from ultrasound to electric, and the rectifier efficiency. In addition, the misalignment between the external transducer and the piezo affects the overall link efficiency. Since the implantable system is not glass-packaged yet, the optimum US frequency for a high link efficiency is expected to be 1.6 MHz. Since the attenuation coefficient of the phantom material is 0.33 dB·cm^{-1}·MHz^{-1}, a 4.5 dB attenuation at 8.5 cm should be considered.

To measure the link efficiency at different load powers, the amplitude and phase of the input voltage applied to Rings$_{3,4,5}$ are adjusted to obtain V_{Rec} = 1.65 V at three different load resistors: 68 kΩ, 8.2 kΩ, and 2.2 kΩ. For the first characterization, $V_{in3,4,5}$ are set to 3.4 V$_{pp}$ to achieve V_{rec} = 1.65 V at R_L = 68 kΩ. Therefore, $P_{out,rec}$ = 40 µW, $P_{in,ac}$ = 10.2 mW, and the link efficiency becomes 0.4%. Next, $V_{in3,4,5}$ are set to 5.2 V$_{pp}$ to obtain V_{rec} = 1.65 V at R_L = 8.2 kΩ. $P_{out,rec}$ = 332 µW, $P_{in,ac}$ = 18.3 mW, and the link efficiency is 1.8%. Lastly, $V_{in3,4,5}$ are set to 10 V$_{pp}$ to have V_{rec} = 1.65 V at R_L = 2.2 kΩ. $P_{out,rec}$ = 1.24 mW, $P_{in,ac}$ = 68 mW, and the link efficiency is 1.8%. As a result, a maximum link efficiency of 1.8% is measured with the phantom tissue having 8.5 cm length, when only three of the rings are transmitting power.

Ultrasound Communication

In order to maintain a maximum link efficiency at an 8.5 cm distance, Rings$_{3,4,5}$ are used to transmit power while Ring$_0$ receives the reflected acoustic waves, providing the uplink data. For US characterization, LDO$_1$ is employed to supply all the blocks in the implant.

As shown in Fig. 5.22, three separate signal generators are used to provide sinusoidal signals to Rings$_{3,4,5}$ of the annular array transducer. For efficient power transfer, $V_{in3,4,5}$ are set to 4.4 V$_{pp}$ and the measured $P_{in,ac}$ is 14 mW. Ring$_0$ is connected to an oscilloscope to monitor the uplink data using ASK modulation. Fig. 5.24 shows the measured voltages at the output of the piezo (V_{TX}), at the output of the rectifier (V_{rec}), at the output of the LDO (V_{supply}), and at Ring$_0$ of the external transducer (V_{RX}). When $V_{in3,4,5}$ = 4.4 V$_{pp}$, the received voltage by the piezo (V_{TX}) is about 2.3 V$_{pp}$, V_{rec} = 2 V, and V_{supply} = 1.23 V. For the pressure measurement,

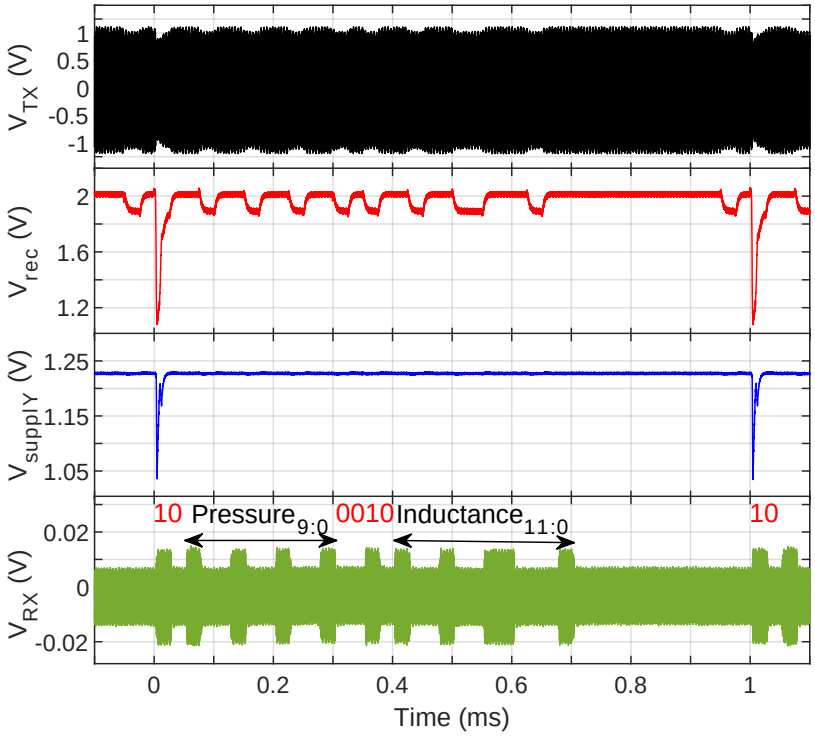


Figure 5.24: Wireless ultrasonic measurement showing powering and communication signals in a measurement cycle.

the sampling rate of the BDC is 1 kS/s, and the pressure sensor and the IA are active for about 1.56 µs in a 1 ms conversion time. Therefore, the ASIC and pressure sensor draw a high current of about 600 µA during 1.56 µs time interval, dropping V_{rec} from 2 V to 1.1 V for a few µs. Thus, V_{supply} decreases from 1.23 V to about 1.04 V.

The pressure and inductive data stored in a cycle are serialized and modulated in the next cycle. To cover pressure and inductive data, and the preambles to distinguish them, the data rate is set to 40 kbps. Each data package starts with a "10" preamble followed by a 10-bit pressure output code. Fig. 5.24 shows that the pressure data is "1001001001". Then, the preamble "0010" distinguishes the pressure and inductive data, and is followed by a 12-bit inductive data. The inductive data is "100100110001". The rest of the bits after inductive data are set to "0". V_{RX} is the backscattered data received by Ring_0. Although the load modulation decreases V_{rec} from 2 V to 1.9 V, V_{supply} does not change, and the load modulation produces detectable uplink data transmission during energy harvesting with only about a 10% reduction of the average harvested power.

Fig. 5.25 shows a zoomed-in version of V_{RX}. Using the definition of the modulation index (MI) in [130], the derived variation in carrier amplitude is equal to:

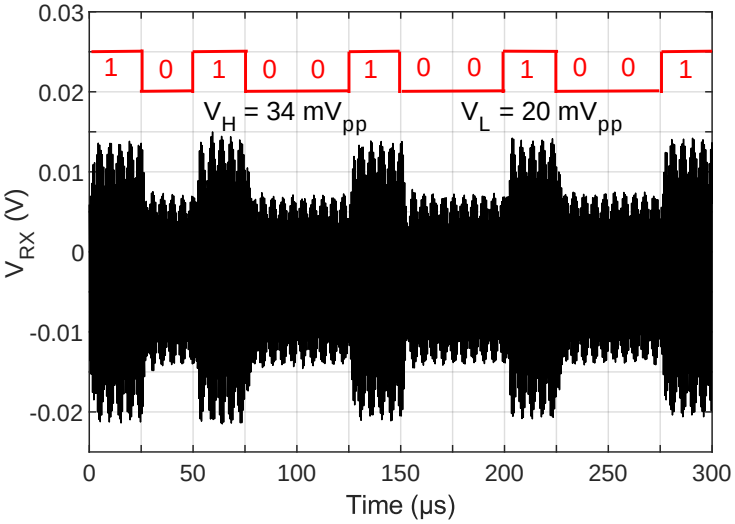


Figure 5.25: US uplink signal received by the external transducer.

$$MI = \frac{V_H - V_L}{V_H + V_L} = 0.26, \tag{5.5}$$

which is high enough to discriminate the received data. Gong *et.al.* [130] demonstrated that even a modulation index below 5.5% is enough to perform a proper demodulation. Therefore, the 26% MI is high enough to perform a proper demodulation.

5.7 Conclusion

This chapter presented the design and characterization of a wireless US power and data transmission platform. The techniques for circuit and system design that enable simultaneous power and data transfer using a single piezoelectric transducer in the implant were demonstrated. The custom-designed implantable and external piezoelectric transducers used to establish a US link were introduced. The main building blocks for energy harvesting, such as the rectifier and voltage regulator, and for uplink data communication, such as the modulator and clock recovery were presented. The ASIC was designed and implemented in a standard 180-nm CMOS process. The performance of the US power and data platform was characterized at 8.5 cm depth by using a tissue phantom with an attenuation coefficient of 0.33 dB·cm^{-1}·MHz^{-1}, which is very close to average body attenuation. The energy harvesting chain achieves a link efficiency of 1.8%. For an available power of 60 µW in the ASIC, the incident acoustic intensity is less than 0.5% of the FDA diagnostic limit, which proves the feasibility of providing even higher DC powers to the implants. In parallel with power transfer, the piezo using ASK modulation returns the data to the external transducer through ultrasound backscattering. The uplink data rate is 40 kbps and the received signal at the external transducer achieves a modulation index of 26%, thus providing a robust communication link.

6 Biocompatible Glass Packaging and Experimental Validations

This chapter introduces the system-level integration of the implantable system with a biocompatible and hermetic glass packaging approach, enabling a long-lasting and low-cost implant. It mainly focuses on the issues encountered during the integration of the glass-packaged system and the corresponding solutions while presenting *in vitro* experimental results of the system in an experimental setup that emulates the arterial blood flow.

This chapter is organized as follows: Section 6.1 summarizes the regulations and standards for implantable devices and explains the selection and advantages of the developed innovative and biocompatible glass packaging approach. The characterization of the glass package encountered some problems, and their solutions are reported in Section 6.2. Section 6.3 presents *in vitro* experimental results and Section 6.4 provides the conclusion.

6.1 Biocompatible Glass Packaging

Medical implants that are placed inside the body must meet certain standards for biocompatibility and safety to prevent harm to the patient. These requirements have been established over time to prevent damage to the human body, which can be caused by the presence of toxic substances in the implant, the body's rejection of the implant as a foreign object, or the implant's malfunction or failure. There are regulations and standards that must be followed before a medical implant can be marketed, including approval by the Food and Drug Administration (FDA) in the United States and obtaining the Conformité Européenne (CE) mark in the European Union. The primary goal of these requirements is to ensure that medical devices are safe for the body and effective in their intended use and to prevent biocompatibility issues that could cause the implant to be removed [131, 132, 133].

The ISO 10993-1 [132, 133] standard is widely accepted as a guideline for evaluating the biocompatibility of medical devices. This standard outlines the required tests to be conducted based on the type of device, the type of tissue it will be in contact with, and the duration of the contact. According to this categorization, the system developed in this thesis is an

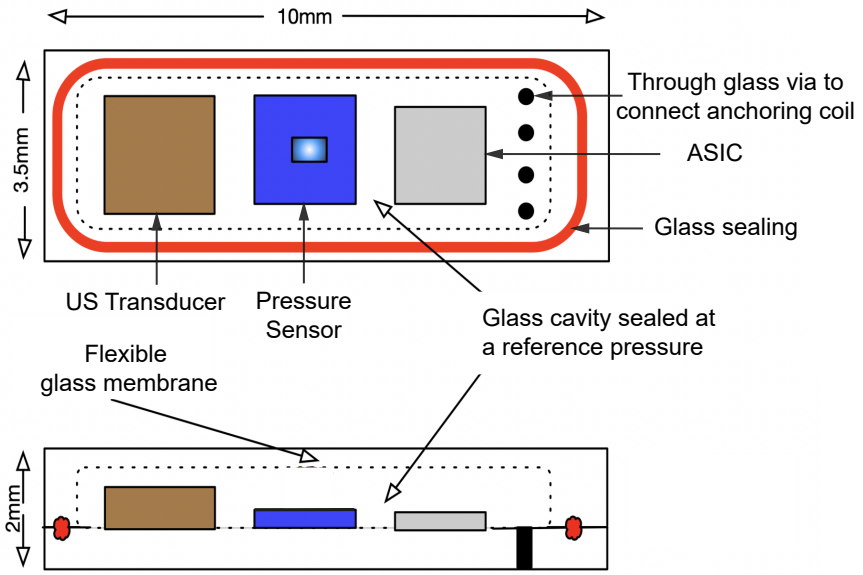


Figure 6.1: Innovative, biocompatible, hermetic, and highly-reliable glass packaging approach.

implantable medical device contacting circulating blood in the cardiovascular system with long-term exposure (> 30 days). Therefore, it should satisfy the tests regarding biological effects such as cytotoxicity, sensitization, irritation, acute and chronice toxicity, implantation effects, and hemocompatibility [132].

The implantable system must be encapsulated in a biocompatible and reliable material to be able to pass future tests successfully. The packaging should perfectly isolate the inner electrical and mechanical components from the human body environment and be hermetically sealed. Different materials, such as metals, glass, polymers, and ceramics are used for packaging medical implants. In the past, metallic or glass hermetic packaging has been utilized for medical implants because of their low water and air permeability, which increases implant lifetime [134]. In addition to being biocompatible and hermetically sealed, other requirements specific to an ultrasonically powered pressure sensor must also be considered. The package must be ultrasonically transparent, allowing efficient energy harvesting, and should transfer pressure from the surrounding environment to the pressure sensor without significant degradation in the sensing performance.

The state-of-the-art implantable hemodynamic monitoring device on the market is the CardioMEMS HF System [29]. It employs a glass package to hermetically seal the system and two nitinol loops to anchor the implant permanently in a branch of the pulmonary artery (PA). Several clinical trials have demonstrated its long-term safety and clinical efficacy [32, 33], so the FDA approved it in 2014. Similar to the CardioMEMS^{TM}, the ultimate goal of this research is to permanently implant this system in a section of the PA. To be compliant with FDA regulations, a glass packaging approach is used to hermetically seal the system and nitinol-based

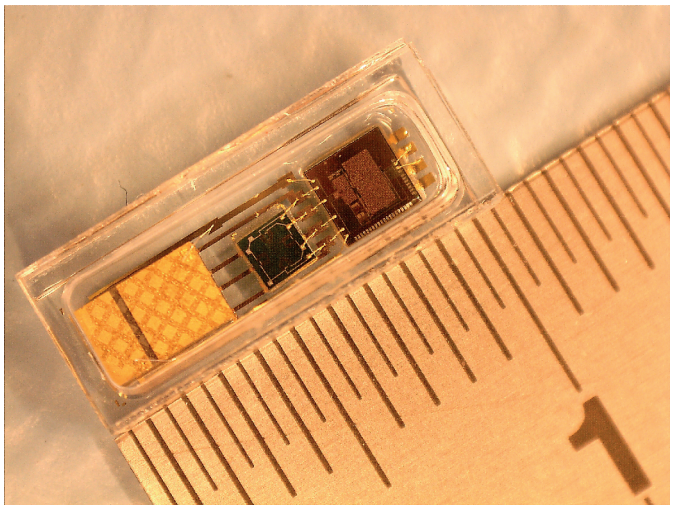


Figure 6.2: Glass-packaged miniature implant without anchoring loops.

anchoring loops are employed for artery diameter measurements. The CardioMEMS^{TM} glass package measures 3.5 mm in width, 2 mm in thickness, and 15 mm in length. To further miniature it, the size of the developed glass-packaged implant is 3.2 mm × 2 mm × 10 mm. The piezoelectric transducer (piezo) for ultrasound (US) energy harvesting and data communication was already designed assuming a 150 µm glass layer on top it. Additionally, such a thin glass membrane is expected to transfer pressure from the surrounding environment to the pressure sensor in the implant.

Fig. 6.1 shows the innovative, biocompatible, hermetic, and highly reliable glass packaging approach for the deep implant, which enables a long-lasting and low-cost implantable device. The company Yalosys developed the glass package using two glass wafers, one with a cavity and another with connectors, which are sealed with a femtosecond (fs) laser. This packaging approach has three main advantages. Firstly, the electric routing is realized on glass with chromium tracks and gold pads, eliminating the need for an additional PCB. The US transducer, pressure sensor, and ASIC are directly wire-bonded to the gold pads on the glass carrier, and the nitinol anchoring loops will be connected to the through glass vias. Secondly, since the thin glass membrane can transmit external pressure to the cavity, it avoids the opening of the glass package to access the pressure sensor membrane, thus significantly increasing reliability and reducing production costs. Lastly, it is MRI-compatible, so patients with the implant do not suffer from any diagnostic limitations. Fig. 6.2 shows the photo of the glass-packaged miniature implant without anchoring loops.

6.2 Glass Package Characterization

To characterize the glass-packaged system, 17 samples were assembled on a carrier glass wafer as shown in Fig. 6.3, and diced by an fs laser. Four of the samples were then hermetically sealed

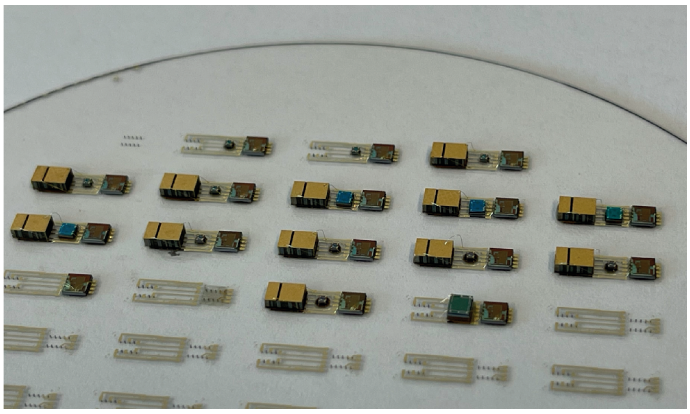


Figure 6.3: Different assembled samples on a carrier glass wafer.

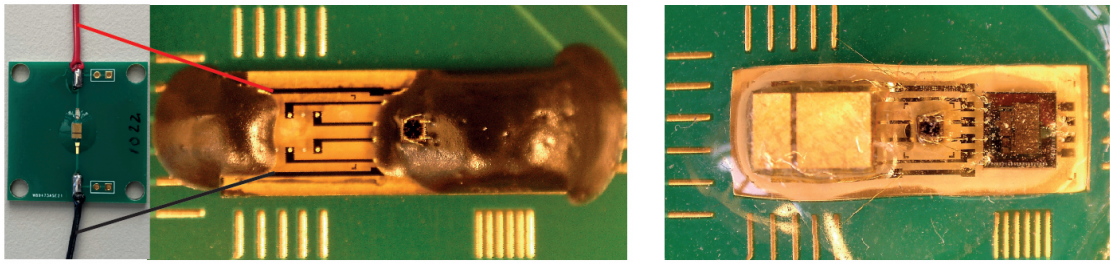
with the second glass wafer containing the cavity. Fig. 6.2 shows one of the hermetically-sealed, fully-packaged glass samples.

Initially, the fully-packaged glass samples are tested by placing them under a tissue phantom to ensure that they received sufficient power. Since there is no wired access to the implant, feedback could only be received through the backscattered communication signal from the piezo. Despite the external transducer being focused on the glass package through an 8.5 cm tissue phantom, the system is unable to power up, and no meaningful backscattered signal is received.

To identify the source of the problem, the glass samples are characterized without their top covers. Firstly, the proper functioning of the chromium tracks, gold pads, and wire bonds is verified. As shown in Fig. 6.4(a), the glass board containing the ASIC and pressure sensor is connected to a PCB, while the piezo is on a separate PCB. The piezo is covered with ultrasonically transparent, bond-wire-protecting epoxy Slygard 184, which has minimal impact on US properties [44]. The piezo is placed under the tissue phantom, and its output is connected to the glass board and an oscilloscope to monitor the received powering signal by the implant. In this case, the implantable system is sufficiently powered and the backscattered signal from the piezo provides the correct pressure value.

After that, the effect of the glass carrier on the harvested energy is characterized. As shown in Fig. 6.4(b), all three components are located on the glass board, and wired connections are made to the output of the piezo to monitor the harvested power. The system is encapsulated in epoxy Slygard 184, and the output of the piezo is connected to an oscilloscope. In this case, the piezo is unable to receive enough acoustic energy, and the ASIC is never powered up. The glass carrier significantly impacts the US characteristics of the system.

Possible reasons behind the energy harvesting problem in the glass carrier were investigated. In the literature, air-backing has been found to be effective in receiving sufficient acoustic energy in a piezo [135, 136]. For efficient energy harvesting, the piezo should not transmit



(a) (b)

Figure 6.4: Glass assembly samples without the top glass cover. (a) The glass board containing the ASIC and pressure sensor, and the piezo are on different PCBs and connected by two wires. (b) All three components are on the glass board, and a wired connection is made to the piezo's output to monitor the harvested power.

acoustic energy to the material on its backside. Therefore, the acoustic impedance of the piezo and its backside must not match. The acoustic impedances of soft tissues such as fat, muscles, and heart, as well as liquids such as water and blood are typically between 1.4 and 1.7 MRayl [53]. The thin glass package used in this thesis was designed to well match the acoustic impedance of the piezo and soft tissues. This is beneficial for the topside of the transducer because it allows efficient transfer of acoustic energy from the soft tissue to the piezo. However, this also means that the acoustic energy cannot be trapped in the piezo since the backside material (glass board) has a well-matched acoustic impedance. As a result, the acoustic energy leaks into the glass board. When the piezo is connected to an FR-4 PCB, it is able to trap sufficient energy because the acoustic impedance of the FR-4 does not match the acoustic impedance of the piezo and soft tissues. The most effective way to efficiently receive acoustic energy is to have an air gap underneath the piezo. The acoustic impedance of air is 0.0004 MRayl [53], so the acoustic energy will be reflected by the air-backing and trapped in the piezo. Therefore, to solve this problem, the glass carrier needs to be modified to have a small air gap underneath the piezo, which can be implemented in the future.

6.3 *In Vitro* Characterization

The glass-packaged system is unable to be powered up adequately, as explained in Section 6.2. Therefore, *in vitro* experiments are conducted using the system on FR-4 PCBs. Fig. 6.5 illustrates the *in vitro* experimental setup emulating the arterial blood flow. A pulsatile blood pump (Harvard apparatus 1423), which is commonly used for hemodynamic studies, pumps distilled water through an artificial artery made of a flexible plastic tube. In the future, the blood and pulmonary artery of a domestic pig will be used for *in vitro* characterization. To mimic the ultrasound attenuation in the body, the 8.5 cm tissue phantom is employed. The first PCB, consisting of the ASIC and the piezo, is placed at the bottom of the tissue phantom. The second PCB with the SM5G pressure sensor is attached to the artificial artery so that the pressure-sensing diaphragm of the sensor is exposed to the pressure inside the artery.

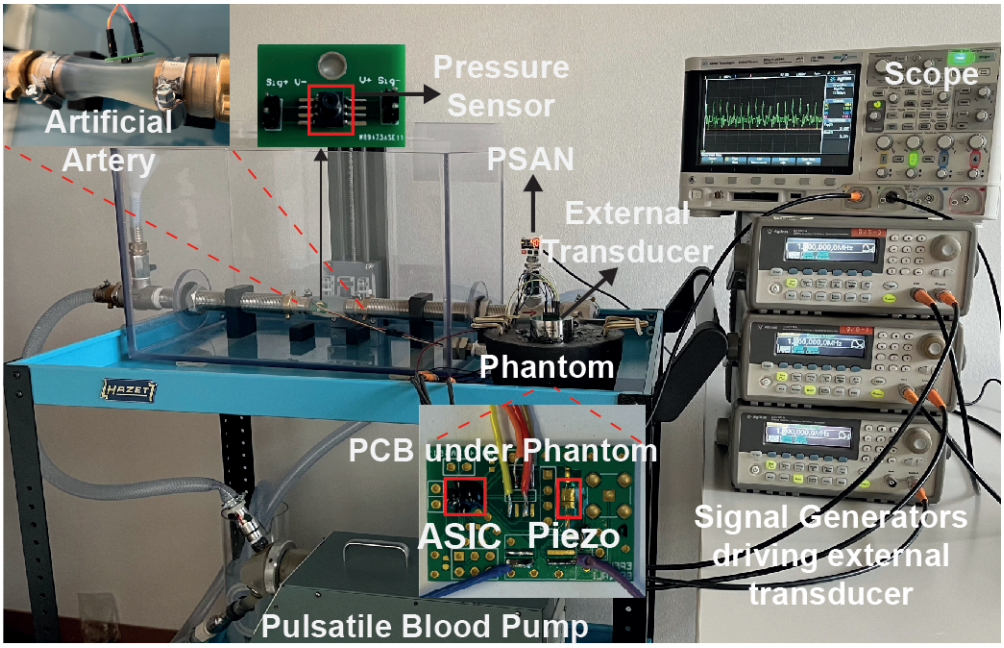


Figure 6.5: *In vitro* experimental setup emulating the arterial blood flow.

As shown in Fig. 6.5, four pads (V_{EXT}, V_{EXB}, $V_{\text{o+}}$ $V_{\text{o-}}$) of the piezoresistive bridge sensor are connected to the ASIC on the first PCB via wires.

In addition, the output of the piezo can be accessed by wires to determine the focal point where the US energy transfer is the most efficient. Three separate waveform generators are used to provide the sinusoidal signals to $\text{Rings}_{3,4,5}$ of the annular array transducer. For efficient power transfer, $V_{in3,4,5}$ are set to 4.4 V_{pp} at 1.6 MHz, and the measured $P_{in,ac}$ is 14 mW. Ring_0 is connected to an oscilloscope to monitor the uplink data using ASK modulation. Fig. 6.6 shows the backscattered signal received by Ring_0. Since the applied signal is at 1.6 MHz, one measurement cycle lasts 0.8 s, and the uplink data rate is 50 kbps. Using the definition of the modulation index in [130], the derived variation in carrier amplitude is equal to

$$MI = \frac{V_H - V_L}{V_H + V_L} \approx \frac{17.8 - 14.1}{17.8 + 14.1} \approx 0.12, \tag{6.1}$$

which is high enough to discriminate the received data.

To evaluate the performance of the remotely-powered pressure monitoring system at systolic and diastolic pressure peaks, pressure measurements are taken for several cardiac cycles. The output phase ratio (systole/diastole) in the pulsatile blood pump is set to 50/50, with a stroke rate of 50 strokes per minute and with a stroke volume of 70 mL per stroke. Fig. 6.7 shows the pressure waveforms measured by the developed remotely-powered implantable system and a commercial wired pressure sensor (PSAN-LC01CV [137]) mechanically attached to the *in vitro* experimental setup. To characterize the BDC at different operating frequencies, the implantable system is remotely powered by US signals at 1.28 MHz and 1.6 MHz. At 1.28 MHz,

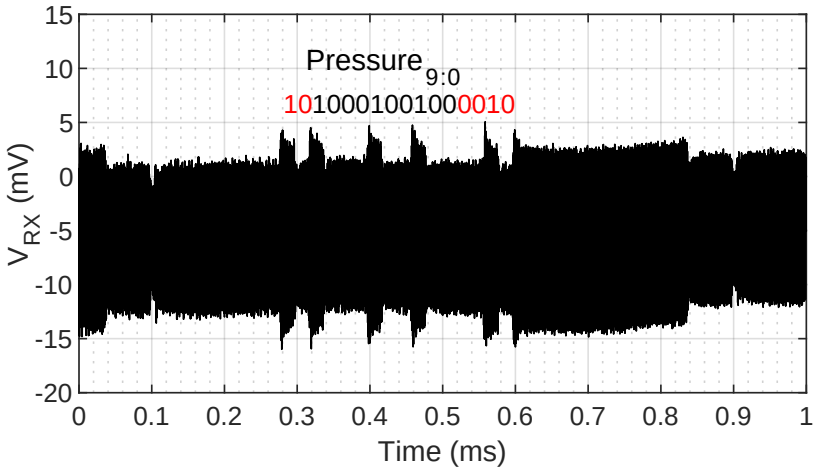


Figure 6.6: US uplink signal showing the pressure value.

the sampling rate of the BDC is 1 kS/s, whereas it is 1.25 kS/s at 1.6 MHz. As shown in Fig. 6.7, the BDC can precisely detect fast peaks of systolic and diastolic pressure changes at both sampling rates. The system performs similarly at both frequencies, with mean pressure values of 8.4 mmHg at 1.28 MHz and 7.6 mmHg at 1.6 MHz. The mean pressure value measured by the PSAN sensor is 7.8 mmHg, which is similar to the mean pressure measured by the implantable system. However, the systolic and diastolic peaks measured by the PSAN are smaller than those measured by the implantable system. This is mainly because the implantable sensor and the PSAN sensor are not exposed to the same pressure waves. The pulsating action of the blood pump causes the artificial artery to expand and contract, resulting in the SM5G sensor attached to the artery experiencing higher pressure peaks. In contrast, the PSAN sensor is attached to a static metallic tube that is not affected by the pulsating action and thus experiences lower pressure peaks. Additionally, the PSAN sensor has a lower sampling rate of 1 measurement every 2.5 ms, compared to the BDC's rate of 1 measurement every 0.8 or 1 ms. This means the PSAN sensor may not be able to detect fast pressure peaks as accurately as the BDC.

6.4 Conclusion

This chapter presented a biocompatible and hermetically-sealed glass packaging method for the implantable system and discussed the challenges encountered in measuring the implant in this type of packaging, as well as potential solutions. The system's performance was characterized in an *in vitro* experimental setup emulating the arterial blood flow. An innovative glass packaging approach that enables highly reliable packaging at low costs was introduced. Although attempts to remotely power the glass-packaged system using ultrasound failed due to acoustic energy leakage into the glass board, the air-backing method can be applied to

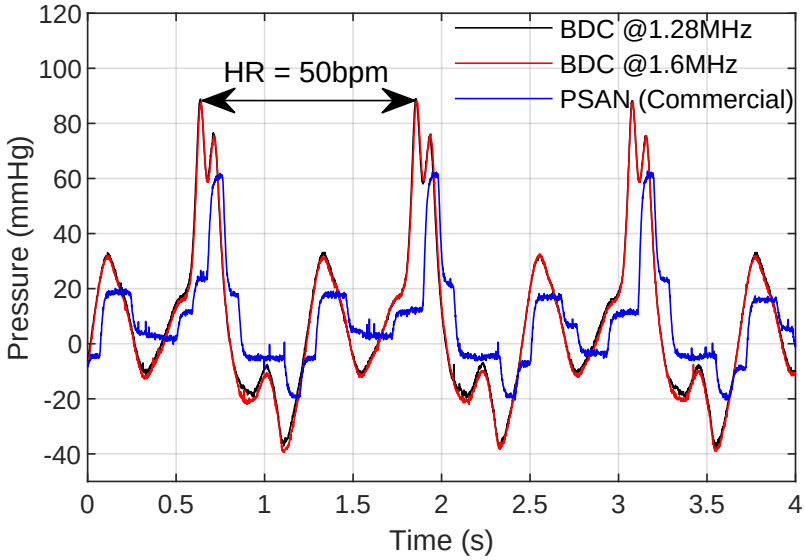


Figure 6.7: Comparison of pressure waveforms measured by the implantable system remotely powered by ultrasound at 1.28 MHz and 1.6 MHz, and the commercial PSAN pressure sensor.

address this issue. The implantable system was tested on FR-4 PCBs, and its performance was verified in the *in vitro* experimental setup. Wireless measurements were taken through an 8.5 cm tissue phantom at operating frequencies of 1.28 MHz and 1.6 MHz, with corresponding uplink data rates of 40 kbps and 50 kbps. The received signal in the external transducer had a modulation index of 12%, providing a robust communication link. In the experimental setup emulating blood flow, the BDC accurately detected fast pressure peaks for systolic and diastolic pressure changes at both operating frequencies. The system performed similarly at both frequencies, with mean pressure values of 8.4 mmHg at 1.28 MHz and 7.6 mmHg at 1.6 MHz. In future work, the glass package can be modified to apply the air-backing method, and the full system can be tested in the *in vitro* experimental setup using the blood and pulmonary artery of a domestic pig.

7 Conclusion

7.1 Summary

In this thesis, an implantable wireless system for remote hemodynamic monitoring was presented. Pulmonary artery (PA) pressure and cardiac output (CO) are two essential parameters to assess HF patients, and current state-of-the-art systems cannot provide both measurements accurately or are not suitable for remote patient monitoring. The main objective of this research is to propose design solutions to enable accurate and continuous monitoring of an HF patient's PA pressure (PAP) and CO by directly and simultaneously measuring PAP and the cross-sectional area (CSA) of the PA with an implantable system. Beyond the state of the art, this thesis introduced an implantable system, which enables direct, simultaneous, and long-term measurement of the PAP and CSA of the artery. Energy and area-efficient design methods were proposed to develop remotely powered miniaturized deep implants.

In Chapter 2, an energy and area-efficient capacitively-coupled chopper instrumentation amplifier (CCCIA) for bridge sensor systems was demonstrated. The CCCIA implemented in 180-nm CMOS has a core area of 0.17 mm^2 and consumes 3.3 μA current from a 1.2 V supply. It has a 3-bit controlled variable gain with a range from 40 V/V to 116 V/V, achieves an input-referred noise density of 88.2 nV/$\sqrt{\text{Hz}}$, an input offset of less than 5 μV, and an output ripple of less than 185 μV. It achieves state-of-the-art performance in terms of small area, and its power consumption, input noise, input offset, and output ripple values are low enough to be used in implantable bridge sensor systems.

In Chapter 3, an energy-efficient, spinning excitation bridge-to-digital converter (BDC) was introduced. The BDC exploits duty cycling to reduce the static power consumption of the bridge sensor and instrumentation amplifier (IA), while cancelling the IA's offset and 1/f noise at the same time. The BDC interface, fabricated in 180-nm CMOS, achieves 8.4 ENOB at a 1 kS/s sampling rate and draws 0.53 μA average current from a 1.2 V supply. The overall pressure sensing system with a differential pressure sensor achieves a resolution of 0.44 mmHg in a pressure range of –135 mmHg to +135 mmHg, and a total conversion energy of 1.1 nJ, which represents state-of-the-art energy efficiency.

In Chapter 4, a novel method was presented for the direct and continuous measurement of an artery's cross-sectional area (CSA) through the exploitation of the inductive characteristic of an implant's anchoring loop. The deformation of the loop shifts the loop inductance, which is correlated to the diameter and CSA of the artery. The oscillator-based readout IC, implemented in 180-nm CMOS, achieves a resolution of 0.42 nH in an inductance range from 181 nH to 681 nH, and respectively consumes 51.2 μA to 39.7 μA from a 1.2 V supply. The diameter measurement, conducted with a 24 cm nitinol wire, achieves a resolution of 0.24 mm in a diameter range from 20 mm to 30 mm, which improves four times the lateral resolution of echocardiography.

In Chapter 5, a wireless ultrasonic power and data transmission platform for miniature deep implants was presented. Simultaneous power and uplink data transfer were achieved by using a single transducer in the implant. Energy harvesting and data communication circuits were implemented in 180-nm CMOS, and the performance of the ultrasound link was characterized at 8.5 cm depth by using a tissue phantom and an external annular array transducer. The ultrasonic powering achieved a link efficiency of 1.8%, and for an available power of 60 μW in the IC, the incident acoustic intensity is less than 0.5% of the FDA limit. The parallel uplink communication using ASK modulation achieved 40 kbps data rate and 26% modulation index.

In Chapter 6, a biocompatible glass packaging approach was presented and its advantages and challenges were discussed. In the remote powering attempts, sufficient energy could not be transferred to the transducer on the glass carrier due to acoustic energy leakage into the glass board. Possible solutions were discussed. Then, the implantable system was tested on FR-4 PCBs by encapsulating it with epoxy, and its performance was verified in an *in vitro* experimental setup emulating the arterial blood flow. The pressure sensing system was able to accurately detect fast pressure peaks for systolic and diastolic pressure changes at both 1.28 MHz and 1.6 MHz ultrasonic powering frequencies, with corresponding uplink data rates of 40 kbps and 50 kbps.

7.2 Future Work

An implantable and remote hemodynamic monitoring system must comply with strict safety and size requirements, which needs innovative circuits and systems design solutions in order to reduce the area and power consumption, to improve the mobility of the monitored patient, to establish reliable wireless powering and communication, and to provide biocompatible packaging for long-term monitoring. While this thesis addressed most of these issues, there are still open opportunities for improvement and additional functionalities that can be added to the system. Some of these opportunities are discussed below:

- This thesis realized a single anchoring loop using a 24 cm nitinol wire for artery CSA measurements. In future work, two orthogonal loops can be employed to improve the CSA measurement, especially in non-circular artery sections. Additionally, the length of

the anchoring loop should be shortened to around 12 cm for safe implantation, and the inductive readout circuit should be modified accordingly to decrease its susceptibility to the parasitics of the package.

- Some problems were encountered in transferring sufficient energy to the glass-packaged system. One of the possible reasons is the acoustic energy leakage from the transducer into the glass board. This issue should be investigated further, and the glass carrier can be modified to have a small air gap underneath the implantable transducer, as an air-backing technique to solve the problem. In addition, the glass package should be further investigated for better pressure transfer from the surrounding environment to the pressure sensor without significant degradation in the sensing performance.

- While this thesis focused on the design of the implantable system, further work is needed on the development of the external base station. For a reliable closed-loop power and data link between the external source and implanted device, the external control unit can scan the body to determine the precise location of the implanted device by employing data uplink feedback and use this information to optimize the alignment between the external base station and the implanted device. Additionally, incorporating adaptable beamforming in the external transducer can adjust the amount of transmitted energy to improve link efficiency.

- By adapting the base station, the external transducer can also be used to measure the blood flow velocity through the Doppler effect, and by integrating these measurements with the measurements of the artery's CSA, direct calculation of the cardiac output becomes possible.

- Further experiments should be performed to investigate the feasibility and safety of the system in a realistic environment. These can include *in vitro* tests using the experimental setup that emulates the blood flow and contains blood and pulmonary artery samples from domestic pigs. In addition, *in vivo* tests that involve the implantation of the device in the pulmonary artery of a pig can also be conducted to assess the long-term exposure of the implantable device developed in this thesis.

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List of Acronyms

AC	Alternating Current
ADC	Analog-to-Digital Converter
ASIC	Application-Specific Integrated Circuit
BDC	Bridge-to-Digital Converter
CCCIA	Capacitively-Coupled Chopper Instrumentation Amplifier
CCIA	Capacitively-Coupled Instrumentation Amplifier
CDAC	Capacitive Digital-to-Analog Converter
CE	Conformité Européenne
CM	Common Mode
CMFB	Common-Mode Feedback
CMOS	Complementary Metal-Oxide Semiconductor
CMRR	Common-Mode Rejection Ratio
CO	Cardiac Output
CSA	Cross-Sectional Area
CVD	Cardiovascular Disease
DAC	Digital-to-Analog Converter
DC	Direct Current
DFF	D Flip-Flop
DNL	Differential Non-Linearity
EA	Error Amplifier
EM	Electromagnetic
ENOB	Effective Number of Bits
FC	Folded Cascode
FDA	Food and Drug Administration
FF	Far-Field
FFT	Fast Fourier Transform
FoM	Figure of Merit
fs	Femtosecond
GBW	Gain-Bandwidth Product
HF	Heart Failure

HFH	Heart Failure Hospitalization
HR	Heart Rate
HV	High Voltage
IA	Instrumentation Amplifier
IC	Integrated Circuit
IMD	Implantable Medical Device
INL	Integral Non-Linearity
IO	Input Output
IRN	Input-Referred Noise
ISO	International Organization for Standardization
kS/s	Kilo Samples per Second
L	Length
LDO	Low Drop-Out
LNA	Low Noise Amplifier
LPF	Low-Pass Filter
LSB	Least Significant Bit
MEMS	Microelectromechanical Systems
MF	Mid-Field
MI	Modulation Index
MIM	Metal-Insulator-Metal
MOM	Metal-Oxide-Metal
MSB	Most Significant Bit
NEF	Noise Efficiency Factor
NF	Near-Field
NMOS	N-Type Metal-Oxide Semiconductor
Opamp	Operational Amplifier
OTA	Operational Transconductance Amplifier
PA	Pulmonary Artery
PAC	Pulmonary Artery Catheter
PAP	Pulmonary Artery Pressure
PCB	Printed Circuit Board
PCE	Power Conversion Efficiency
PH	Pulmonary Hypertension
PSR	Power Supply Rejection
PSRR	Power Supply Rejection Ratio
PZT	Lead Zirconate Titanate
RF	Radio Frequency
RFID	Radio-Frequency Identification
RPM	Remote Patient Monitoring
RRL	Ripple Reduction Loop

SAR	Successive Approximation Register
SC	Switched Capacitor
SFDR	Spurious-Free Dynamic Range
SNDR	Signal-to-Noise and Distortion Ratio
SNR	Signal-to-Noise Ratio
SV	Stroke Volume
THD	Total Harmonic Distortion
US	Ultrasound
USCOM	Ultrasound Cardiac Output Monitor
VCO	Voltage-Controlled Oscillator
VGA	Variable Gain Amplifier
VTI	Velocity Time Integral
W	Width
WHO	World Health Organization
WPT	Wireless Power Transfer

Publications & Patents

Journals

[1] **M. Besirli**, K. Ture, M. Beghetti, F. Maloberti, C. Dehollain, M. Mattavelli, and D. Barrettino, "An Implantable Wireless System for Remote Hemodynamic Monitoring of Heart Failure Patients," *IEEE Transactions on Biomedical Circuits and Systems*, 2023, invited, submitted.

[2] **M. Besirli**, K. Ture, M. Beghetti, C. Dehollain, M. Mattavelli, F. Maloberti, and D. Barrettino, "An Energy-Efficient Bridge-to-Digital Converter for Implantable Pressure Monitoring Systems," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 16, no. 5, pp. 732-741, Oct. 2022.

Conferences

[1] **M. Besirli**, K. Ture, M. Beghetti, C. Dehollain, M. Mattavelli, and D. Barrettino, "An Implantable Inductive Sensor for Direct and Continuous Monitoring of the Pulmonary Artery Cross-Sectional Area," *2022 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, 2022, pp. 31-35.

[2] **M. Besirli**, K. Ture, M. Beghetti, C. Dehollain, M. Mattavelli, and D. Barrettino, "A Capacitively-Coupled Chopper Instrumentation Amplifier for Implantable Bridge Sensor Systems," *2022 20th IEEE Interregional NEWCAS Conference (NEWCAS)*, 2022, pp. 208-212.

[3] **M. Besirli**, K. Ture, D. Barrettino, M. Beghetti, M. Mattavelli, C. Dehollain, and F. Maloberti, and "A 0.4 nJ Excitation Energy Bridge-to-Digital Converter for Implantable Pulmonary Artery Pressure Monitoring," *2021 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, 2021, pp. 1-4.

[4] **M. Besirli**, K. Ture, C. Dehollain, D. Barrettino, and M. Mattavelli, "A CMOS Analog Front-End for Implantable Pulmonary Artery Pressure Monitoring System," *2019 15th Conference on Ph.D Research in Microelectronics and Electronics (PRIME)*, 2019, pp. 261-264.

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[1] D. Barrettino, C. Dehollain, K. Ture, **M. Besirli**, and M. Mattavelli, "Cardiovascular monitoring system," PCT patent application 2022 167 382 A1, Aug. 2022.

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- Thesis title: Integrated Electronics for Deep Implants to Remotely Monitor Hemodynamics
- Designed and developed an implantable wireless system for remote and continuous hemodynamic monitoring of heart failure patients.
- Built innovative ICs for cardiac implants.
- Designed and implemented pressure sensor interfaces with ultra-high energy efficiency.
- Developed a circuit technique to reduce the power consumption of bridge sensors while inherently cancelling the 1/f noise and offset of readout circuits.
- Developed a novel technique to directly measure the diameter and cross-sectional area of an artery based on the inductance change of an implant's anchoring loops.
- Designed and implemented a wireless ultrasonic power and data platform enabling simultaneous power and data transfer using a single piezoelectric transducer in the implant.
- Submitted a patent for a cardiovascular monitoring system.

European Organization for Nuclear Research (CERN), Switzerland 2017 - 2018
Master's thesis student – Electronic Systems for Experiments Group

- Designed a radiation-hard electronic fuse trimmed bandgap voltage reference for the DC-DC converters in LHC Experiments upgrades.
- Characterized implemented integrated circuits in radiation environments.

European Organization for Nuclear Research (CERN), Switzerland 2016
Summer student and bachelor's thesis student – BASE Collaboration

- Designed and implemented a cryogenic ultra-low noise amplifier for antiproton detectors.
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TECHNICAL SKILLS

Patent: One patent application for a cardiovascular monitoring system.
Analog & mixed-signal design: ADCs, amplifiers, current and voltage references, power management, ultrasound powering and communication.
Digital Design: Full custom flows, counters, dynamic logic.
Measurement: PCB design, RF instruments, measurement in pressure and temperature chambers, cryogenic measurements in cryostats, radiation tests in X-ray machines.
EDA tools: Cadence (Virtuoso, Spectre), Mentor Graphics (Calibre, ModelSim), Advanced Design System (ADS), Xilinx, Altium Designer, Eagle, PSpice.
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- LEM Prize at EPFL for the master's thesis.
- Merit scholarship (tuition and housing) for 5 years from Sabanci University for ranking in first 500 out of 1.8 million test-takers in the National University exam.
- Certificate of High Honor for 6 semesters from Sabanci University.
- Top rank in Electronic Engineering program at Sabanci University.