ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

Advanced NEMS Laboratory

Semester Project Report

Fabrication of Suspended Piezoelectrically Transduced Resonators

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for

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Content

I. Introduction

A. Objective

The objective of this semester project is the fabrication of suspended piezoelectrically transduced resonators and to test and compare the quality of the piezoelectric layer using different processes and parameters. A functional fabrication process by lift-off has already been tested before and a different process by ion beam etching was investigated in this project. Some changes in parameters such as temperatures of deposition and material of the seeding layer were investigated too. Another point of the project was to ensure that no fence-like structures are formed during the resonators' fabrication that could short circuit them. These fences arise when the resist sidewalls are coated with conductive material during for example a deposition procedure for a lift-off or a redeposition following a physical etching procedure.

B. Device presentation

The devices we aim at fabricating are piezoelectrically transduced resonators. They are suspended beam (cantilever or clamped-clamped beam) made of a supporter material (SiN) and several other layers on top that forms the piezoelectric device. The piezoelectric stack is composed of a sandwiched piezoelectric material (AlScN) between two electrodes. Applying a voltage between those two electrodes generates an electric field across the piezoelectric material and thank to the piezoelectric effect, the beam can then be actuated. Figure 1 below shows a cross section of a finished device (dimensions not in scale, only explanatory model).

Fig. 1. Typical cross section of one device. In dark blue the Pt, in yellow the Ti, in gray the Si, in light blue the SiN and in green the AlScN. Dimensions are not in scale.

II. Fabrication

Resonators have been fabricated on 12 wafers. The same overall process flow has been followed for all the wafers with some differences between each wafer. This section will explain the principal steps we followed. The original process flow as well as the complete list of differences between the wafers can be observed in the appendix of this document.

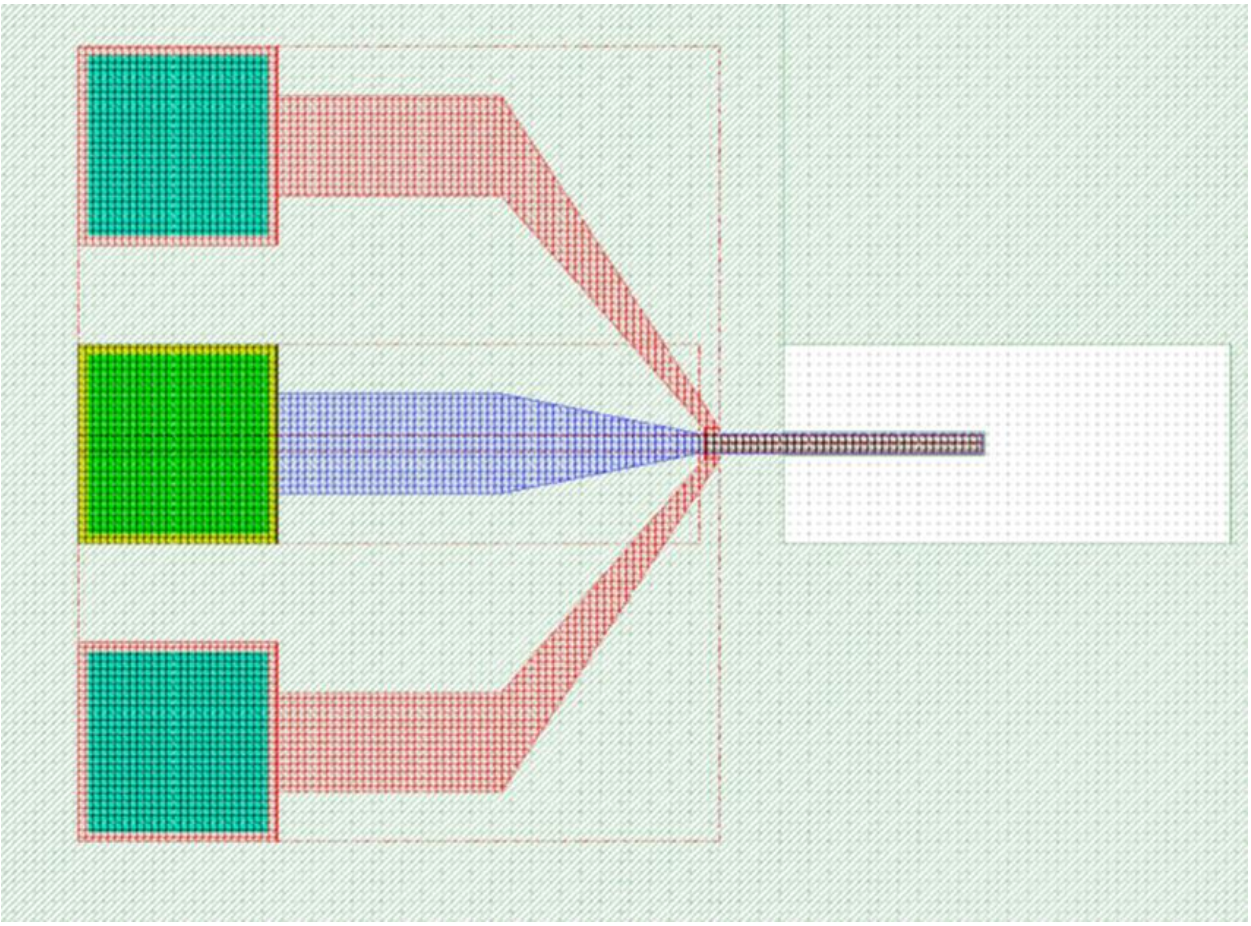

Fig. 2. Example of a 200µm singly-clamped beam device.

A. Initial state of the wafers

All Si wafers started with a layer of 500nm low-stress SiN on both sides. Then a layer of 10nm of Ti or AlN were deposited which serves as an adhesion layer followed by 25 or 50 nm of Pt on 10 wafers. The differences in thicknesses and adhesion layer material were split between the wafers. Some layers were deposited at room temperature (RT) and other at high temperature (HT) as well.

Fig. 3. Cross section of a wafer at its initial state. In dark blue the Pt, in light blue the SiN, in green Ti or AlN (between the light and dark blue) and in gray the Si.

Two wafers were not deposited with the seeding layer and Pt because they were used for the next section lift-off.

B. Bottom electrodes: lithography and lift-off or IBE

Two different methods were used for these steps to compare the already functioning process of lift-off used before to the new ion beam etching procedure. We decided to use a lift-off process on 2 wafers and an ion beam etching process using the Veeco Nexus IBE350 ion beam etcher on the other wafers.

Fig. 4. Cross section before (left) and after (right) lift-off. In dark blue the Pt, in light blue the SiN, in green Ti or AlN, in yellow the photoresist (AZ 1512 HS on LOR 5A) and in gray the Si.

For the lift-off, in order not to form fences we launch twice the development recipe to ensure a sufficient undercut of the LOR 5A and did a quick O_2 Plasma descum before the deposition.

Fig. 5. Cross section before (left) and after (middle and right) ion beam etching. In dark blue the Pt, in light blue the SiN, in green Ti or AlN, in yellow the photoresist (AZ ECI 3007 or AZ 10XT-07) and in gray the Si.

For the IBE, 2 different resists and procedures were tested to see if fences are being formed. The first resist used is a standard 0.6µm thick AZ ECI 3007 and the etching procedure was at medium power at -10° and 30 seconds at -70° to finish ensuring that no redeposition of conductive material was on the sidewalls of the resist. The second resist used is a 0.7µm thick AZ10XT-07 with a reflow procedure (placing it 2min at 125°C on a hotplate after the resist is developed) to flatten the sidewalls, the etching was then only at -10° and medium power too.

C. AlScN and Al Deposition

AlScN 17.5% has been chosen as the piezoelectric material and Al for the top electrodes. Initially the top electrode should have been in Pt, but this was the availabilities of the materials at the time of the project. 200nm of AlScN and 25nm of Al were deposited.

Fig. 6. Cross section after the AlScN and Al deposition. In dark blue the seeding layer + Pt, in light blue the SiN, in green the AlScN, in purple the Al and in gray the Si.

D. Top electrodes: lithography and etching procedure

The etching procedure for the Al for the top electrodes was simply done by developing the AZ 10XT-07 resist.

Indeed, as we only have a 25nm thick layer of Al, the fact that Al is attacked by KOH and that the developer for AZ 10XT resists is AZ 400K, an organic solution based upon KOH, we proceeded to etch the Al just by developing the resist. We just made sure to use a recipe for a thicker layer of resist than the layer we coated to be sure to etch properly the Al. In this case we used the 1.5µm recipe for the development whereas we only coated (and exposed) for 0.7µm.

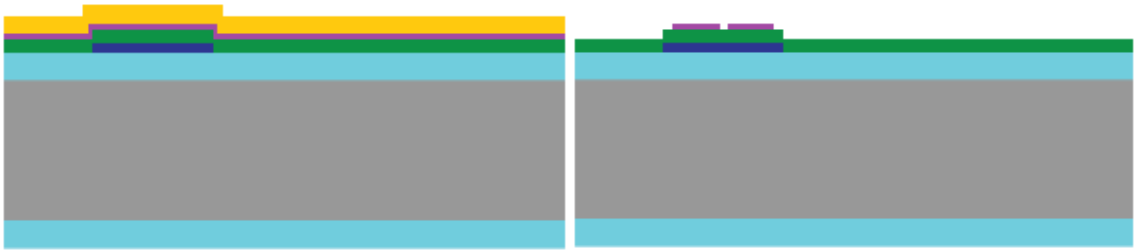

Fig. 7. Cross section before (left) and after (right) resist development. In dark blue the seeding layer + Pt, in light blue the SiN, in green the AlScN, in yellow the photoresist (AZ 10XT-07), in purple the Al and in gray the Si.

After the development, the quality of the AlScN crystal lattice were measured by X-ray diffraction. The rocking curve values stand between 4.1° and 5.3°, the values for each wafer can be observed in the appendix.

E. Bottom pad opening: lithography and IBE

As the AlScN layer has been deposited everywhere on the wafer, the pads of the bottom electrode weren't accessible anymore. An ion beam etching procedure at medium power at -10° and 30 seconds at -70° to finish has been chosen here.

One of the critical aspects of these steps was to be cautious not to over-etch the AlScN and etch away the Pt.

F. Al addition to the electrode pads: lithography and deposition

The previous layer of Al was too thin (only 25nm) as we could see scratches after touching the pads with multimeter probes, so we decided to deposit, only on the pads, a much thicker layer of 300nm by lift-off.

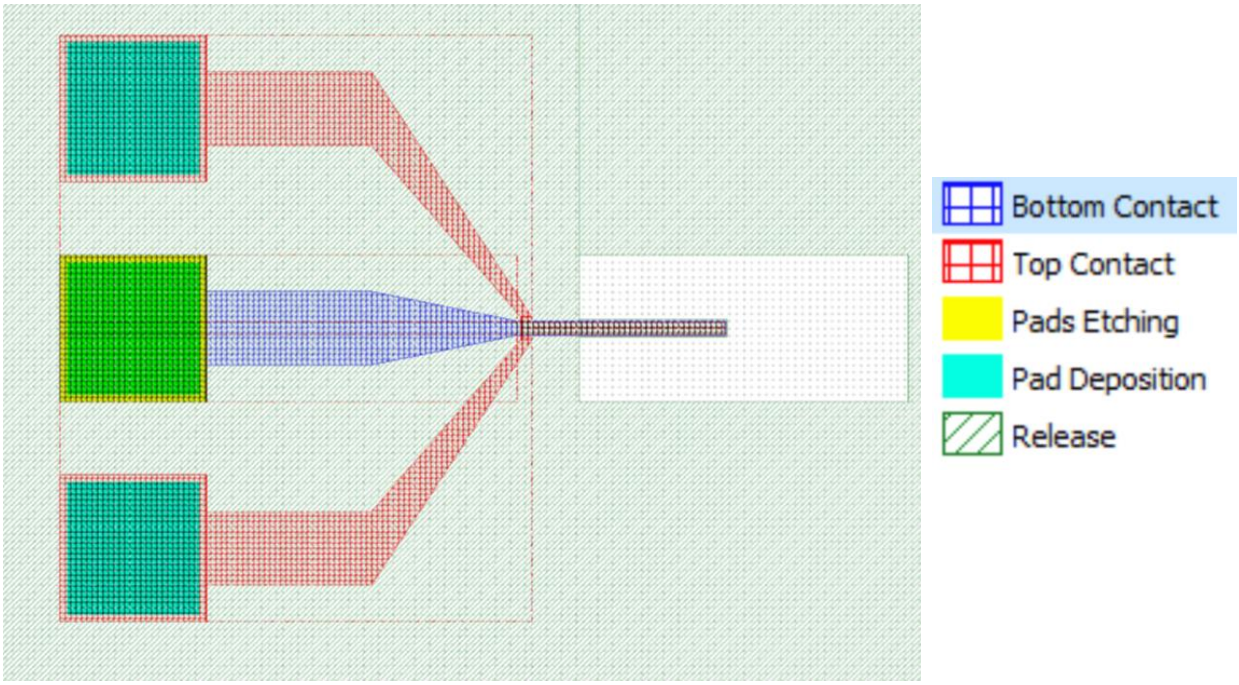

Fig. 8. Schematic of a 200µm singly-clamped beam (left) and the different layers (right). Hatched green is the release while the solid green is the intersection of the pads etching and the pad deposition

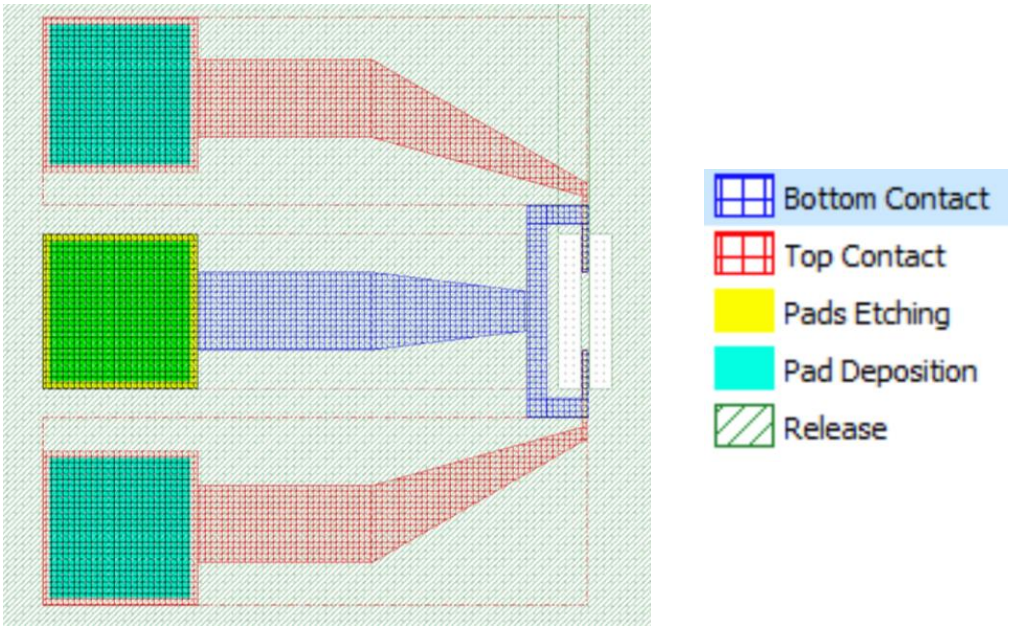

Fig. 9. Schematic of a 200µm double clamped beam (left) and the different layers (right). Hatched green is the release while the solid green is the intersection of the pads etching and the pad deposition

G. Release: lithography and IBE

Finally, the release was started with the lithography and the ion beam etching of the AlScN.

Fig. 10. Cross section before (left) and after (right) ion beam etching. In dark blue the seeding layer + Pt, in light blue the SiN, in green the AlScN, in yellow the resist, in purple the Al and in gray the Si.

The wafers were left at this stage at the end of the semester. The last steps are the etching of the SiN et Si to fully release the resonators.

Some measurements like the d31 piezoelectric coefficient for example will be conducted after the full release of the resonators to further evaluate the piezoelectric quality of the different fabrication processes.

III. Results and discussion

Most of the fabrication went without important drawbacks or failures. Only a second deposition of Al had to be added to the process flow and the ion beam etching for the bottom pad opening of one wafer shows results that were not expected.

A. Bottom electrodes lift-off and ion beam etching inspection

The first processes for the bottom electrode went well without any fences detected no matter the technique used.

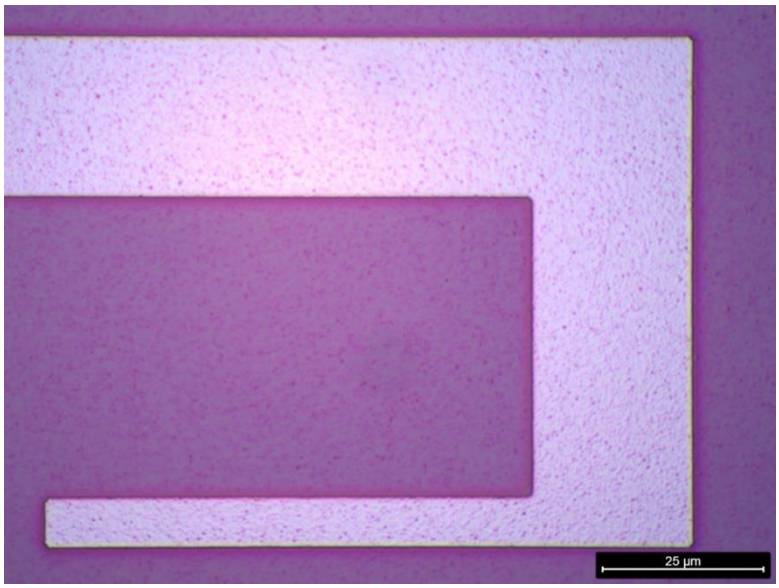

Fig. 11. Wafer 114707. Picture of a structure taken after the first etching procedure (here IBE, without reflow), in dark purple the SiN and in light purple the Pt

For the lift-off, results show no fences on both wafers done with this process. The profile can be seen on the figure below. It is important to notice that we launch twice the development recipe to ensure a sufficient undercut and did a quick O_2 Plasma descum before the deposition.

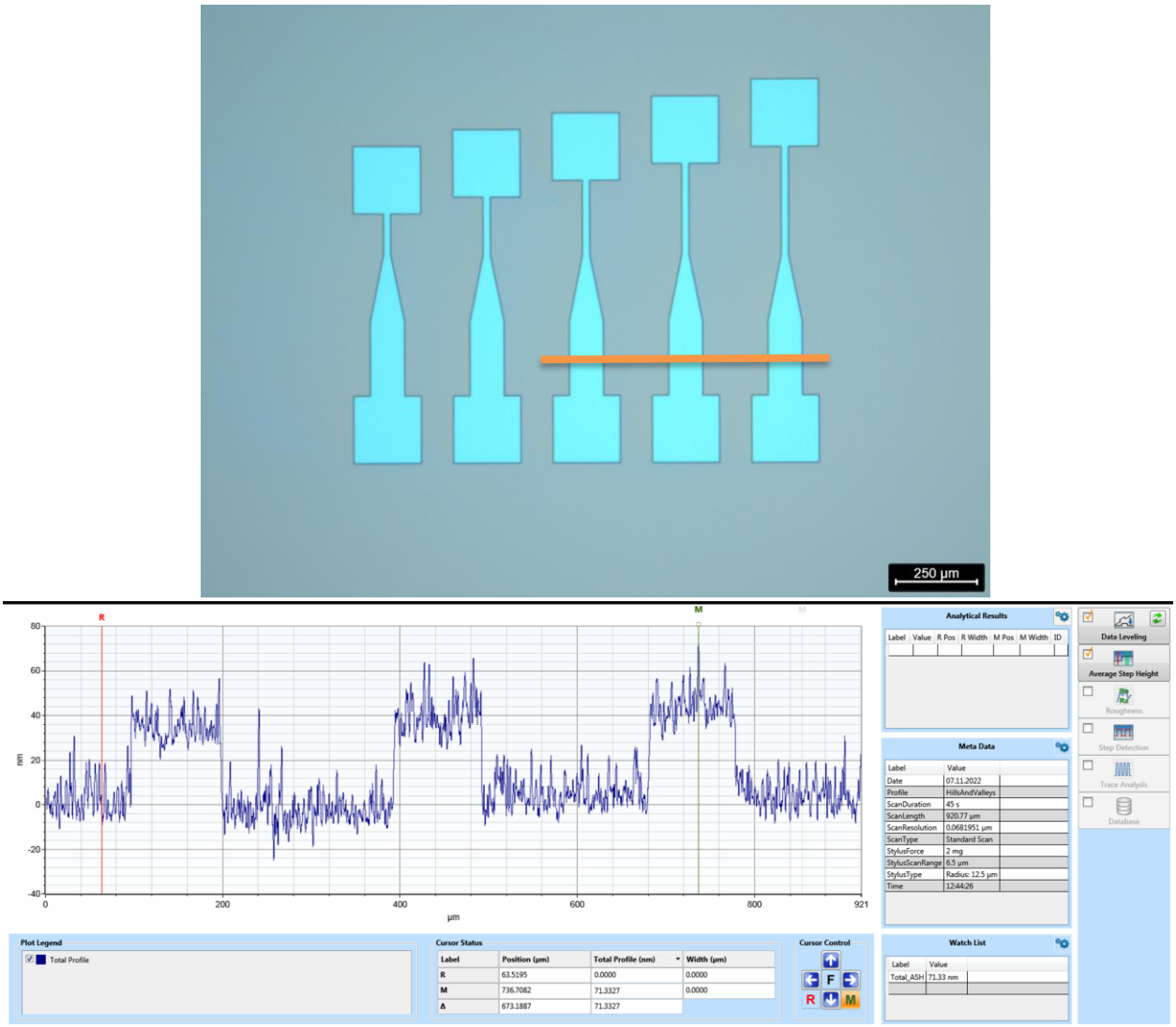

Fig. 12. Wafer 114361. Picture of a structure (top) after lift-off and profile (Bruker Dektak XT) following the orange line showing no fencing

For the ion beam etching, 2 processes were tested too. One with a 0.7µm AZ 10XT-07 photoresist coating plus a reflow at a single -10° exposition on the machine (Veeco Nexus IBE350), and the other with a 0.6µm AZ ECI 3007 coating and at -10° and -70° exposition on the machine.

The reflow step was done to have flatter resist's sidewalls and the -70° step was done to etch potential redeposition of conductive material on the resist's sidewalls. As the time of etching was short (<1min) it was decided to keep the same amount of etching time for -10° and -70°.

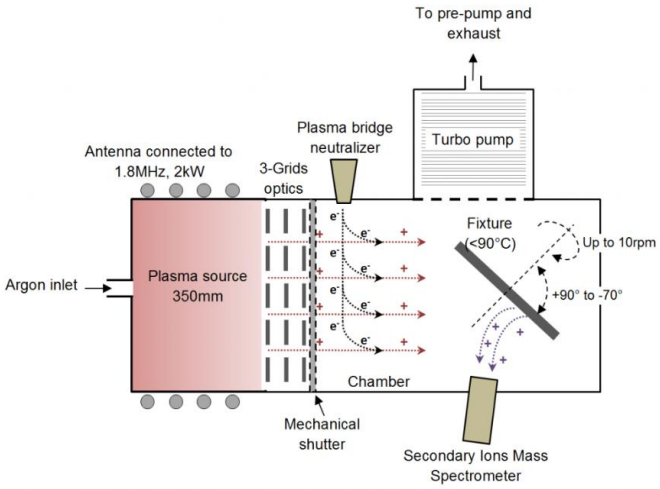

Fig. 13. Description of the IBE350 ion beam etcher (source: CMi)

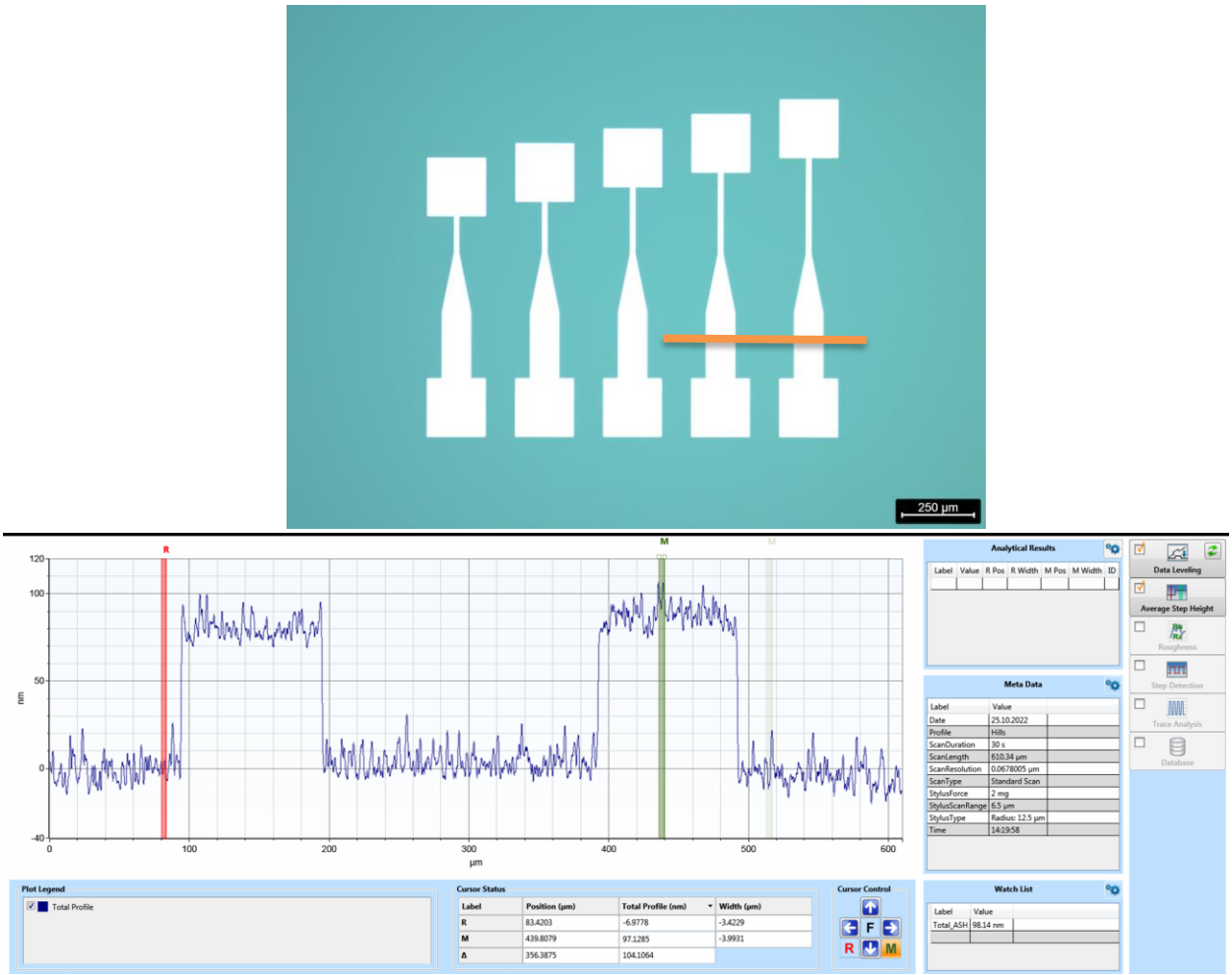

Fig. 14. Wafer 114360. Picture of a structure (top) after IBE with reflow and profile (Bruker Dektak XT) following the orange line showing no fencing

A Scanning Electron Microscope (SEM) was used on 2 wafers in addition to the mechanical profilometer to ensure that no fences were present after the processes.

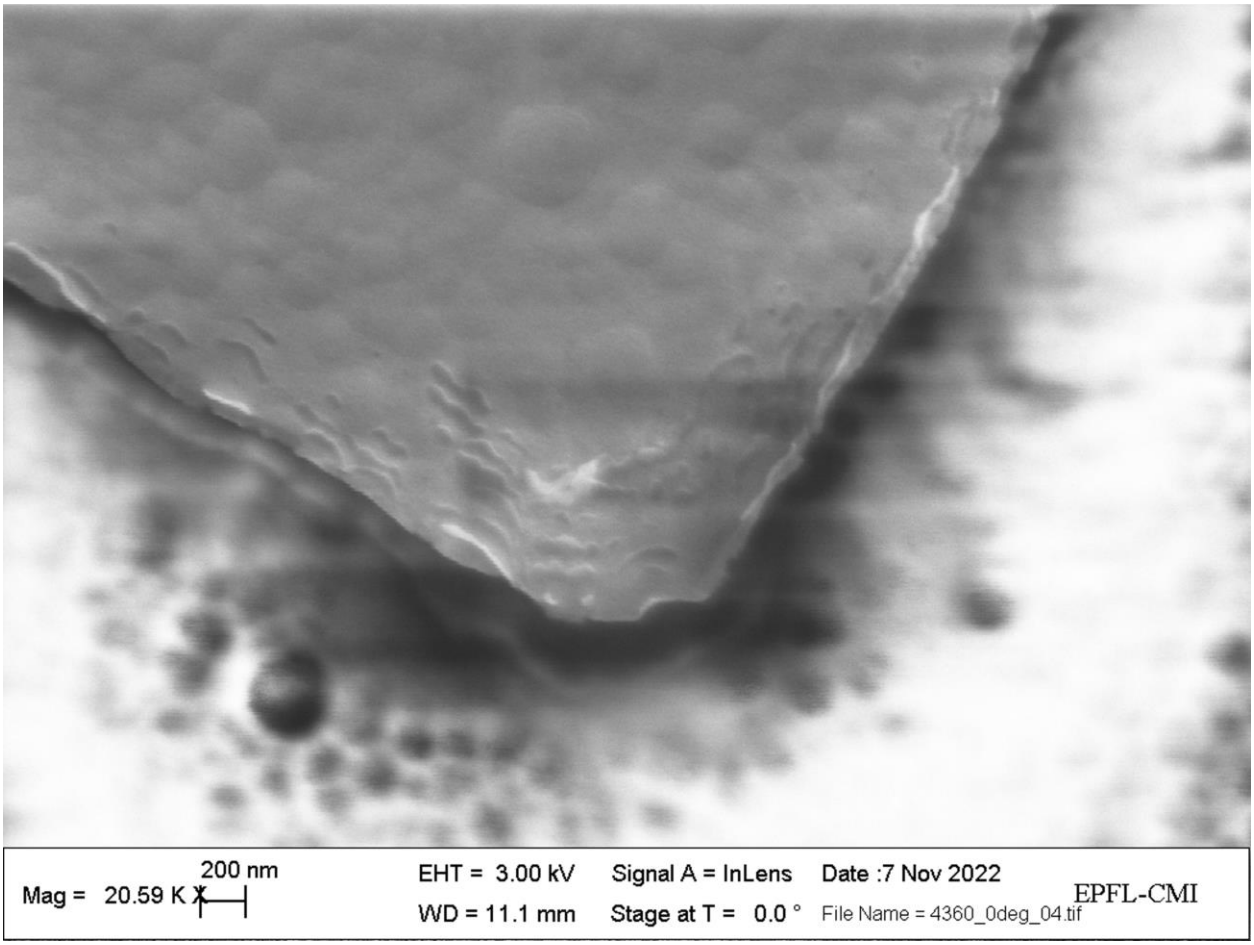

Fig. 15. Wafer 114360. SEM picture (Zeiss LEO 1550 normal incidence) of the sidewalls of a structure after a reflow and the etching procedure

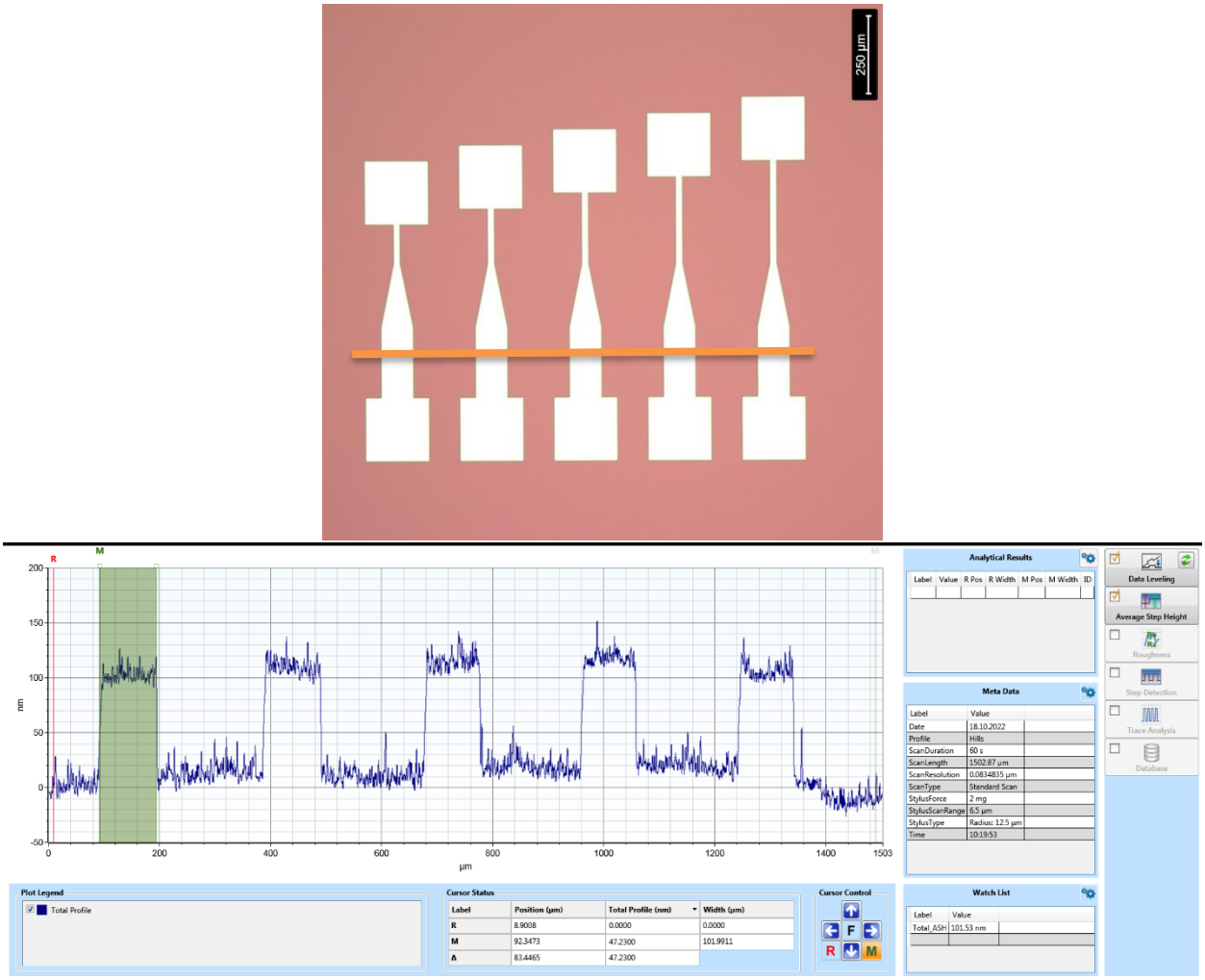

Fig. 16. Wafer 114709. Picture of a structure (top) after IBE (-10° and -70°) and profile (Bruker Dektak XT) following the orange line showing no fencing

It might seem that IBE procedures gave smoother profiles than the lift-off but this is not really the case. Indeed, the vertical scales on the pictures are not identical due to differences in structure thickness, in this case we have 35nm deposited for the 114361 wafer, and 60nm deposited for the 114360 and 114709 wafers. As we weren't worried about over etching with the IBE, one can see that the measured heights for the IBE wafers are larger than the deposition thickness, the structure height on the 114709 wafer is even larger due to the additional -70° step compared to the 114360 wafer. All of this can give this roughness difference impression between the figures.

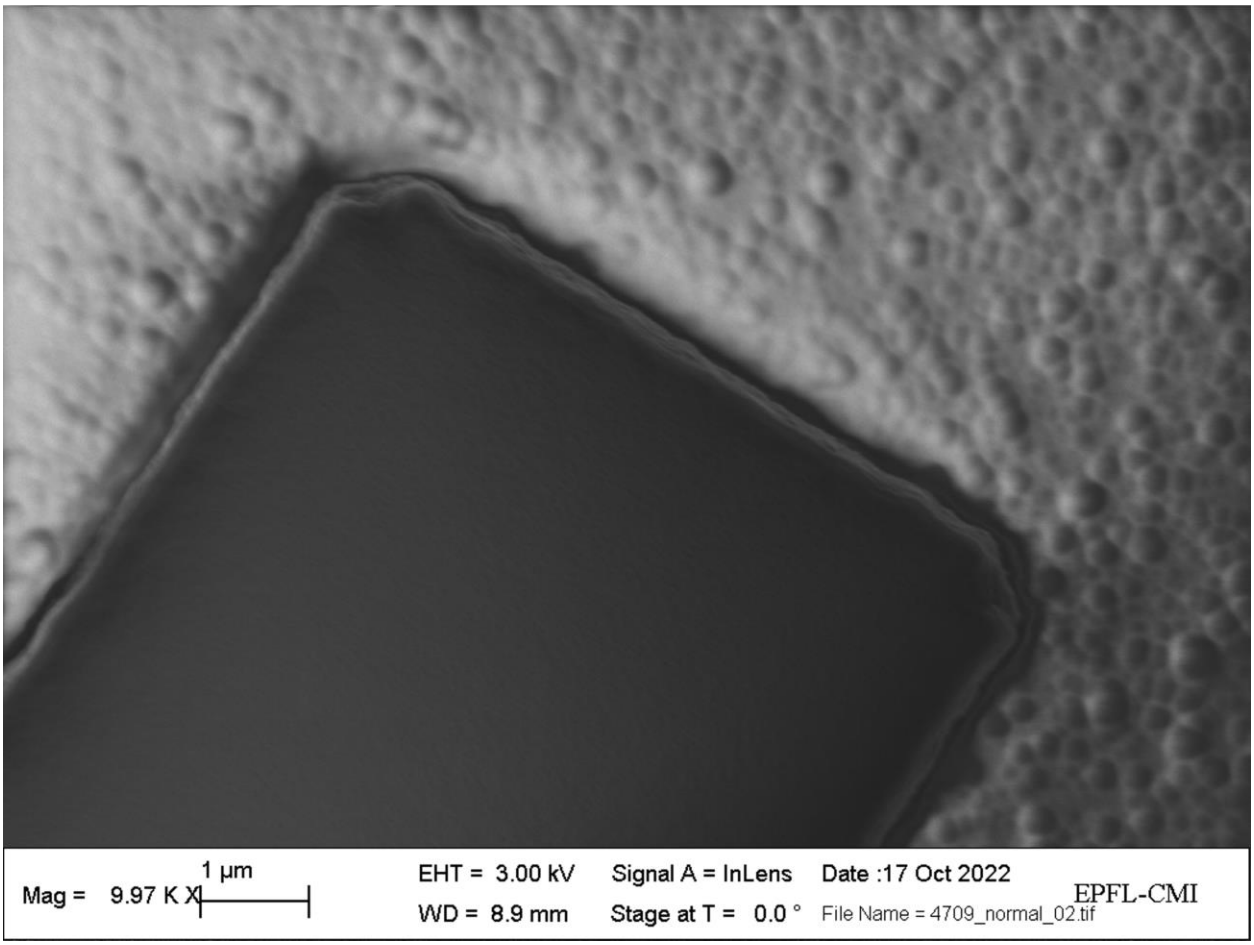

Fig. 17. Wafer 114709. SEM picture (Zeiss LEO 1550 normal incidence) of the sidewalls of a structure after IBE of -10° and -70°. A layer of resist is still on top of the structure.

In the end one can see that we obtain very good results with the three techniques.

B. Top electrodes inspection

The top electrodes after the resist development show good results The alignment of the wafers with the mask went well for most lithography.

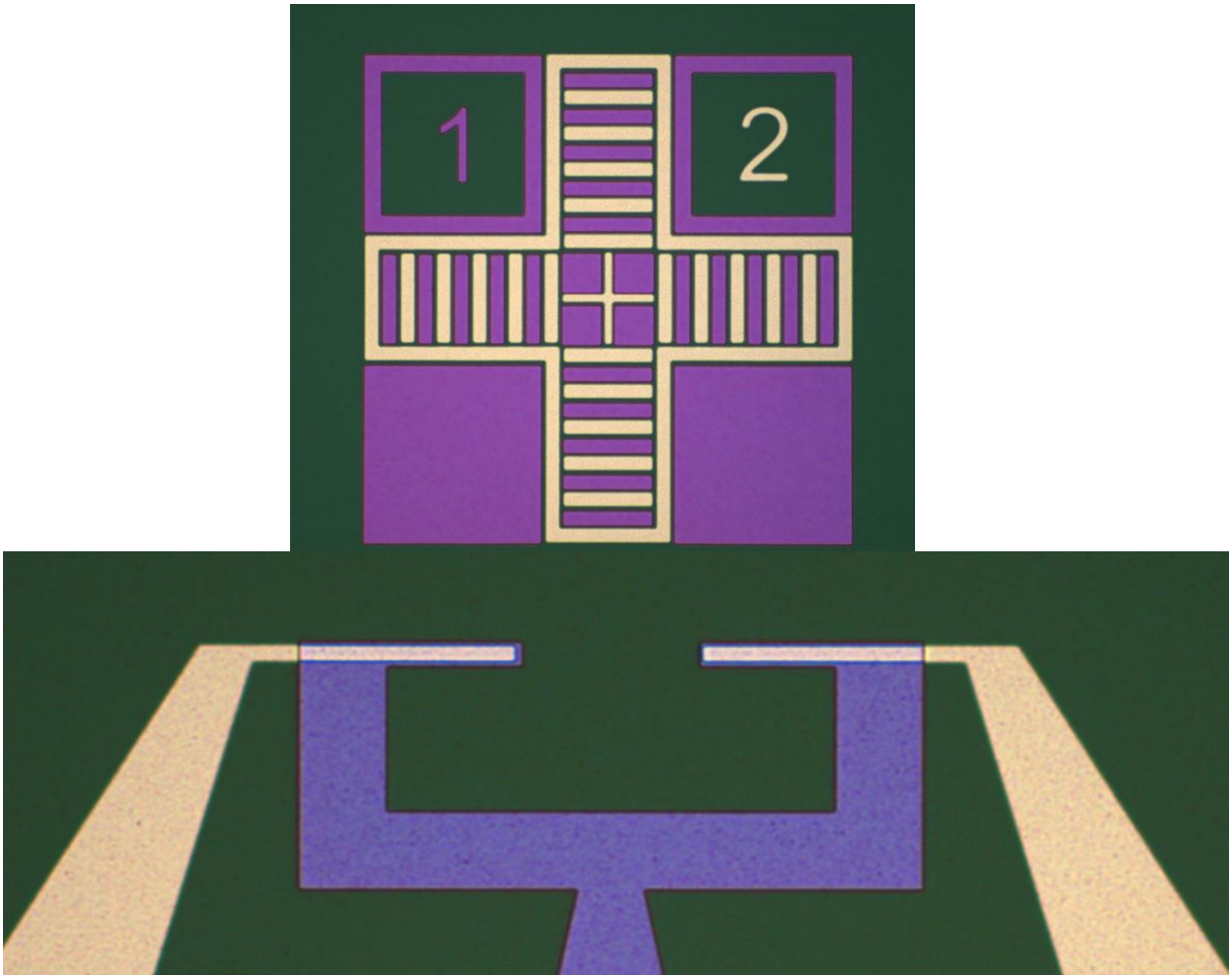

Fig. 18. Wafer 114608. Alignment mark (top) and picture of a structure after the resist development

Unfortunately for 2 wafers, the alignment wasn't perfect, and some structures could have some issues during the testing phase after the release.

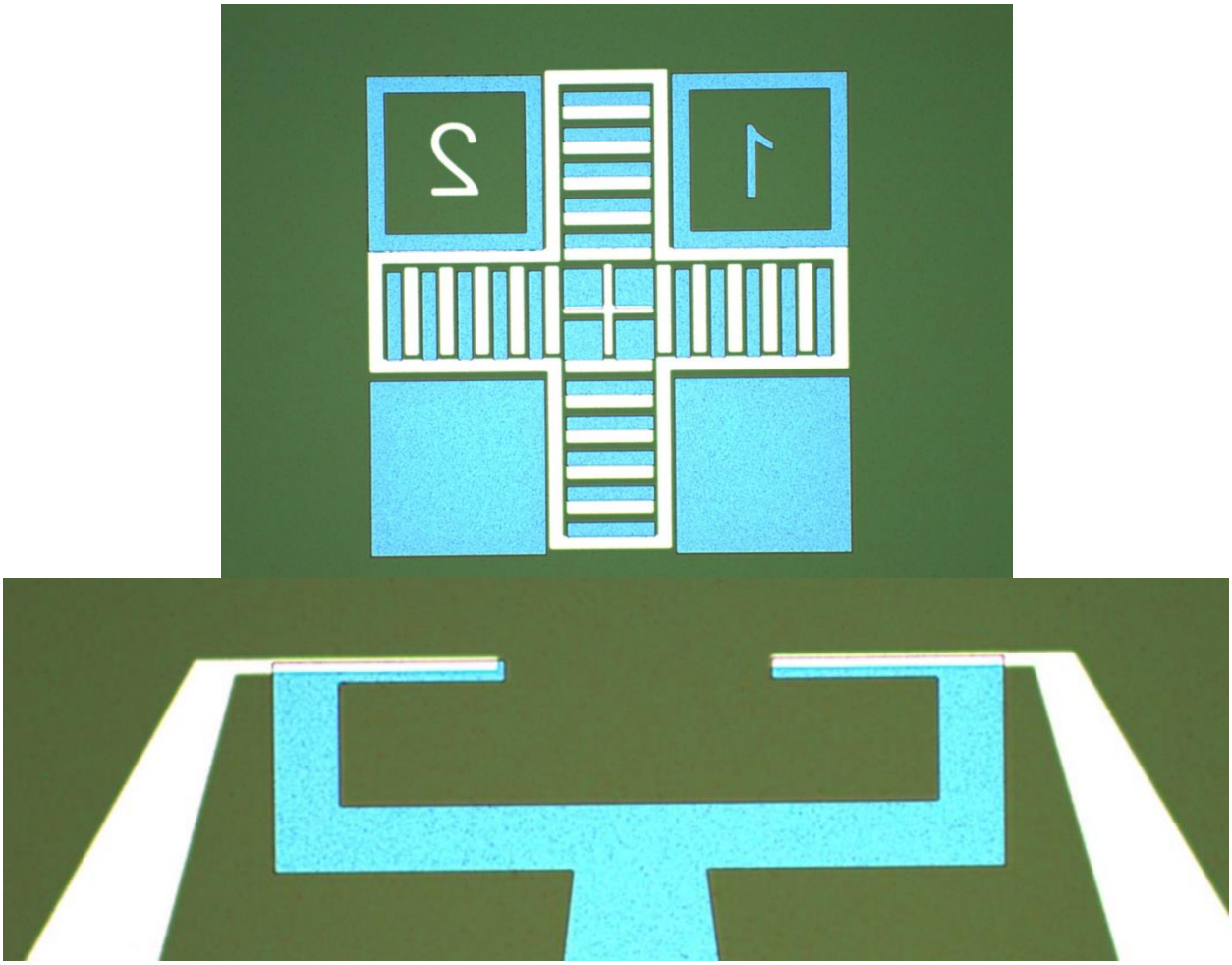

Fig. 20. Wafer 114709. Alignment mark (top) and picture of a structure after the resist development, a misalignment can be observed

Fig. 19. Wafer 114709. Picture of a structure after the resist development. The misalignment is not critical on this structure

As mentioned previously, a too thin layer of Al was initially deposited. Indeed, after touching the pads with multimeter probes some scratches could be seen on the figure below and would affect the electrical contact one can have on the pad. It was then decided to perform a second lithography and a second deposition of 300nm of Al on the pads with a lift-off process. These operations were performed by the TAs.

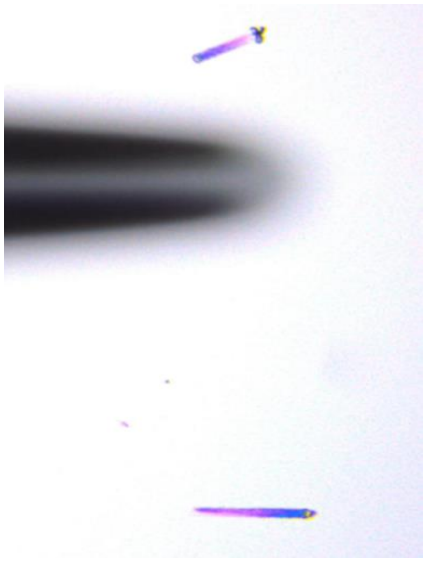

Fig. 21. Picture of the initial layer of Al. Some scratches can be seen after a resistivity test with a mutimeter

C. Bottom pad opening inspection

The lithography and ion beam etching procedures went well for all wafers except one, the wafer 114512.

Indeed, for this wafer, it seems that the IBE didn't etch it evenly around the surface of the wafer. After the same etching time passed as for the other wafers for this procedure, the "H" testing structures on this wafer, designed to quickly see and test the deposition and accessibility of the electrodes, showed much higher resistance than the other wafers and very different values depending on the "H" structure tested. The optical thickness measurement tool (Filmetrics F54) used up until now, never showed a coherent thickness value of AlScN after this etching procedure. As it seemed that it should just be a thin layer of remaining AlScN, it has then been decided to etch a bit more the wafer at low power and to rely on the Secondary Ions Mass Spectrometer of the IBE to indicate us when to stop. We were very cautious not to over-etch the Pt bottom pad of this wafer as it only has a 25nm Pt layer that can be etched very quickly. Unfortunately, the IBE's Mass Spectrometer directly indicated that Pt was etch at the start of the low power procedure. We only did 10 seconds of exposition before stopping the machine. We measured the resistance again with no great improvement and re-tried to measure the thickness of the AlScN remaining with nothing coherent once again. We decided one last time to etch a bit more and did 15 more seconds of exposition. The results still weren't great, but we were too afraid to continue and possibly over-etch the pad and decided to stop here. The final resistance value can be seen on the figure below. This wafer will still follow the next procedures as the other wafers until the release.

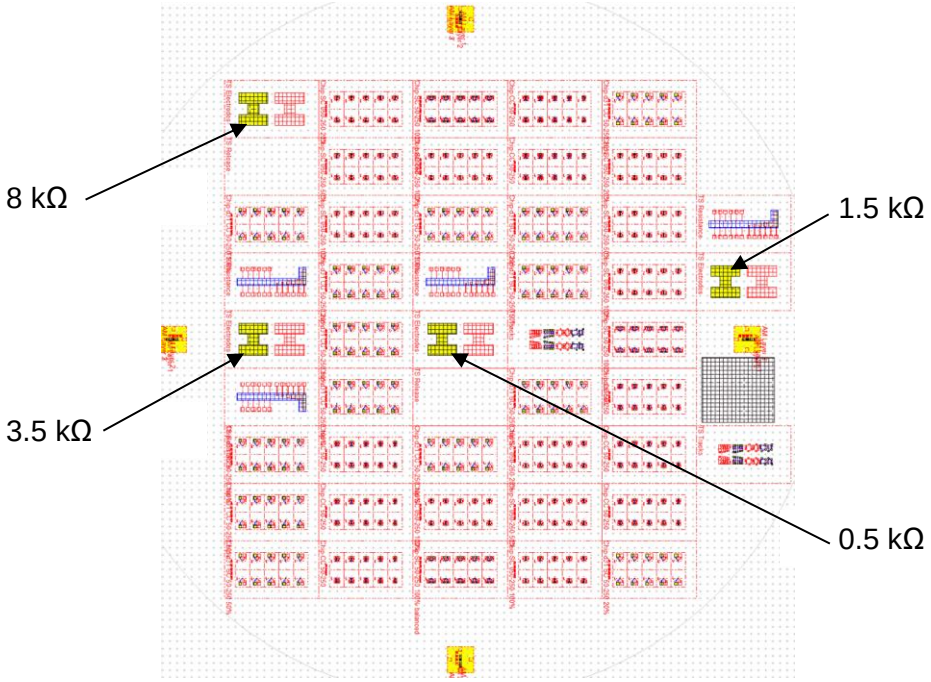

Fig. 22. Wafer 114512. Schematic of « H » testing structures and resistance values after the third time on the IBE.

Conclusion

The objective of this semester project is the fabrication of suspended piezoelectrically transduced resonators, to test and compare the quality of the piezoelectric layer using different processes and parameters and to ensure that no fence-like structures are formed during the resonators' fabrication.

Fabrication of resonators on 12 wafers without any fences has been achieved using various techniques like lift-off or ion beam etching with and without reflow.

However, on one wafer an ion beam etching procedure showed strange results with an uneven etching rate around the surface of the wafer. We then hope that following tests after the complete release of the resonators could still be conducted on this wafer.

Appendix

Wafer	RC	Initial description	PR Photolitho Bottom electrodes	Etching/Lift-off Procedure	Deposition	PR Photolitho Top electrodes
114361	5.166	10nm Ti + 25nm Pt Lift-off	0.4µm LOR + 1.1µm AZ1512	Lift-off	200nm AlScN 17.5% + 25 nm Al	0.7µm 10XT-07
114403	5.336	10nm Ti + 50nm Pt Lift-off				
114360	4.517	10nm Ti + 50nm Pt HT reflow	0.7µm 10XT-07	IBE (only -10°)		
114608	4.378	10nm AlN + 50nm Pt HT reflow				
114707	4.769	10nm Ti + 50nm Pt RT	0.6µm ECI 3007	IBE (-10° and -70°)		
114486	4.147	10nm Ti + 50nm Pt HT				
114709	4.981	10nm Ti + 25nm Pt RT				
114512	4.292	10nm Ti + 25nm Pt HT				
114559	4.687	10nm AlN + 50nm Pt RT				
114577	4.804	10nm AlN + 50nm Pt HT				
114558	4.686	10nm AlN + 25nm Pt RT				
114586	4.580	10nm AlN + 25nm Pt HT				

Fig. 24. Summary of operations done on each wafer (1/2).

Al Etching Procedure	PR Photolitho Bottom electrodes openings	AlScN Etching Procedure	PR 2nd Photolitho Top electrodes	Deposition	PR Photolitho Release	AlScN Etching Procedure
10XT-07 developement (1.5µm recipe)	1.5µm ECI 3007	IBE (-10° and -70°)	4µm ECI 3027	300 nm Al	4µm ECI 3027	IBE (only -10°)

Fig. 23. Summary of operations done on each wafer (2/2).