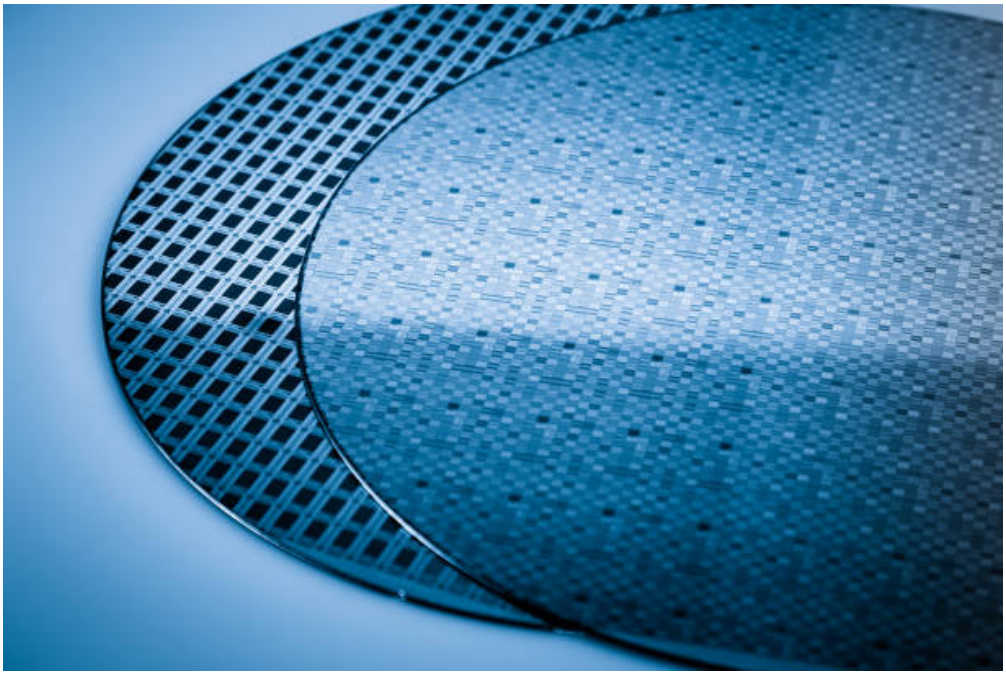
ÉCOLE POLYTECHNIQUE
FÉDÉRALE DE LAUSANNE

ME-401 : Semester Project in Mechanical Engineering

Annealing and Etching Processes for Hafnium Carbide MEMS



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Acknowledgements

I would like to thank Professor Villanueva for giving me the opportunity to work in this project and for his guidance throughout the semester. I am very grateful for the lessons and help given by the doctoral students of the ANEMS lab, especially Marco who was there in the critical moments to lend an expert hand in the clean room. Finally, I would like to acknowledge the great support by the CMi engineers and staff without witch we would all be doomed.

Abstract

HfC has been very under-investigated due to its rarity and synthesising difficulty. Its potential for MEMS and NEMS applications has been recognized and is the object of an ongoing feasibility study for production since 2022. We continue on this impulse by testing annealing protocols in the range between 200°C and 600°C to reduce deposition residual stress, and determining etch rates for Ion Beam Etching in the incident angle range between 0° and 70°. Protocols to determine etching verticality are also tested and analysed.

1 State of the Art

Hafnium Carbide use for MEMS is still a rather unexplored territory with little research in production and metrology models. F. Bauer started this project a semester earlier investigating the physical properties of thin films and etching methods [2]. While good selectivity was achieved, it was hypothesized that the damage suffered during release was due to high pre-stress in the film. Successful annealing experiments presented by Lewis and L.J. Porter in their paper on plastic deformation of Hafnium Carbide powders in 1970 [6] confirmed that an additional step should be considered. We also found inspiration in the research done by A. Bruder on Hafnium Oxide Crystallization to craft the experimental annealing protocol [3]. Additionally, the work by W. Thongruang on the synthesis of HfC thin films is a comprehensive study published in 1997 which served us as an excellent reference of the material properties [8].
Very little research is available on HfC etching. Fortunately, F. Bauer's research clearly showed that Ion Beam Etching and XeF_2 release were both effective methods in this context.

2 Annealing

As previously mentioned, an annealing step was evaluated to reduce the stress in the HfC film which was identified as being the source of damage during subsequent release. The idea was to find a temperature which would reduce surface stress as much as possible while keeping electrical resistivity within 5% of its original value. Prof. Villanueva estimated that the stresses in the HfC layer should be no more than 500 MPa in order to have succesful lithography.

The 11 wafers initially produced during the first deposition round yielded compressive stresses ranging between -10GPa to -4 GPa. The stress in function of the deposition parameters of the first batch are all displayed in Figure 1.

2.1 Annealing Process

Initially, we ramp-heated to increasingly high temperatures from 23°C in increments of 100K very similarly to what was previously done in A. Bruder's work on Hafnium Oxide [3]. The oven is then held at maximum temperature for 15 minutes and left closed during cooling. To prevent any possible oxidation, the entire process happened in Nitrogen atmosphere and wafers entered in contact with air only below 100°C.

The strategy was to measure electrical resistivity and stress between each increment to later determine the optimal temperature through linear regression. The Table 2 shows all the annealing steps taken on each wafer. The corresponding process flow is in section D.1.

2.2 Results and Analysis

We noticed a very subtle decrease in compressive stress with each annealing step taken 2a. The stress variation appears to be independent from temperature at this range with the average reduction per annealing being around 160MPa. The conductive properties of the material do not vary at all which is surprising considering the general tendency of metal carbides of group IV to decrease in that aspect with temperature [7].

Unfortunately, due to the extremely high magnitude of the pre-stresses, the idea of annealing the first $Si - SiO_2 - HfC$ wafer batch was quickly abandoned until better deposition results were achieved due to insufficient reduction of the stress. The wafer 120596 ended up shedding its HfC film during annealing at $T_{max} = 600$°C most probably related to thermal expansion mismatch between layers.

If this direction were to have been continued, further investigation of the microstructure of HfC using x-ray diffraction would be worthwhile to find if a recrystallization temperature exists. If so, how the transition affects the stress and if it could have been the reason for the film to disappear. It would also help explain why the resistivity remains unaffected by heat treatment.

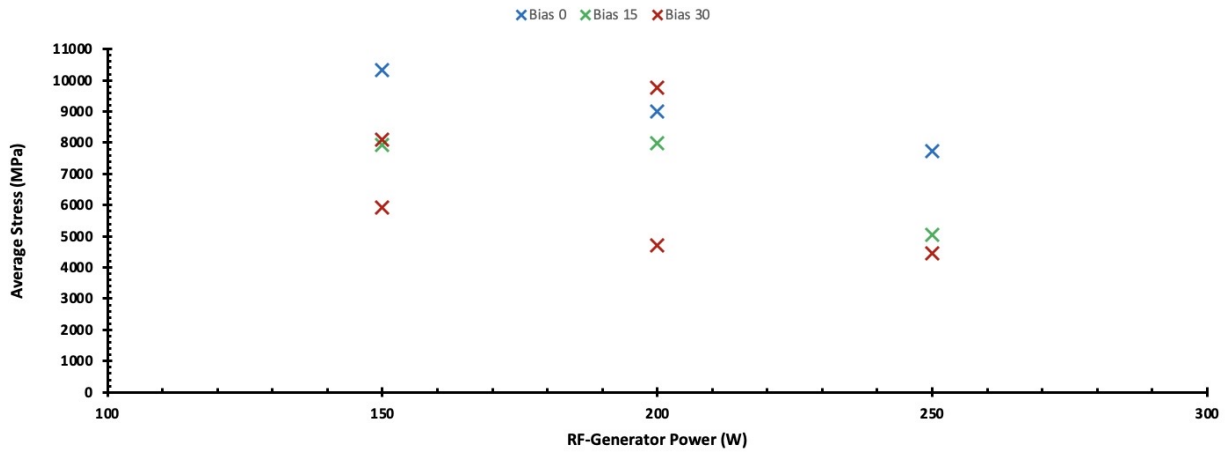
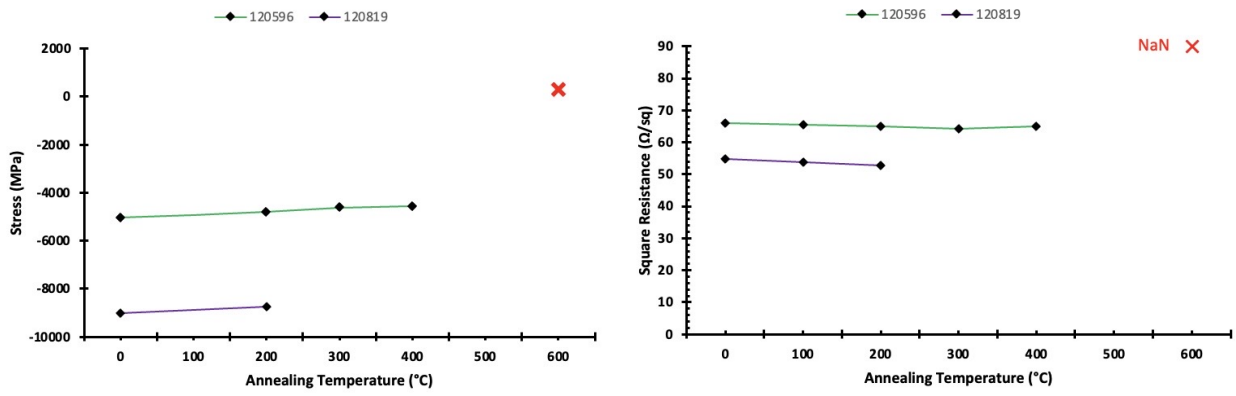


Figure 1: The first batch of HfC deposition counted 11 wafers. The depositions were done at 0.005mbar, on 525 μm Si substrate covered by a thin 500nm SiO_2 film for insulation. The depositions were investigated by my collegue J. Barini. For more information on deposition parameteres and optimization, please refer to his work.



(a) (b)

Figure 2: **(a)** The stress evolution in the HfC film for 2 different wafers. The average stress reduction per annealing step was 160 MPa which is almost negligible when compared to the astounding residual stresses measured on the first batch of 11 wafers (ranging from -10GPa to -4GPa). The red marker represents the annealing step at which the HfC layer shed itself off in the oven. [5] **(b)** The quasi-inexistent evolution of the average square resistivity in the HfC film. The infinite resistivity measurement after the $T_{max} = 600$°C step is due to the machine scanning raw Silicon Oxide (insulator).

3 Ion Beam Etching

Ion Beam Etching was deemed a promising etching method after the initial results on etch rates obtained by F. Bauer [2]. This investigation goes further by investigating etch rates and etching verticality as function of incident angle. We assumed the influence of deposition recipe was minor but was still non-exhaustively evaluated through sanity checks at -10° (no contradiction).

3.1 Etch Rate Process

The etch rate protocol was the source of much debate due to the mixed results obtained in deposition. We had in mind to measure square resistivity variations before and after etching but the first batches were akin to an electrical insulator rendering this strategy impossible. We shortly investigated lithography coupled with mechanical profilometry to no avail (Process Flow in subsection D.3). Only once the third round of depositions yielded low layer resistivity, were we able to proceed.

We ion beam etched cleaved wafers ($\approx$ 2cm wide squares) with known square resistances to remove thicknesses around 100nm and measured them again. The etch times were inspired by an empirical etch rate determined using the IBE's integrated spectrometer. We lent little attention to past location of the wafer dies for the first two measurements but decided to only prepare samples from the center for the last try. More detail on this is provided in subsection 3.3. The corresponding process flow is detailed in subsection D.2.

3.2 Etching Verticality Process

We followed two recipes to produce two identical wafers due to valve malfunctions on the IBE (long-term unavailability of the machine was possible and we had to accelerate the process). The initial plan was to proceed by doing Lithography and IBE a quadrant of the wafer at a time and cleaving it at the very end. This allowed for high power IBE (Table 4) which can only be done on whole wafers because chips attached to carriers are not in direct contact with the cooling flow causing heat-related damage in the resist layer. Additionally, this way of fabrication allowed for easier manipulation but was overall slow due to the high number of steps on thoroughly booked machines. The process flow is detailed in section D.4 and was later used when time was no longer of the essence.

The second, quicker process was to cleave the wafer after patterning all four quadrants and sticking them on carriers before etching them at low power (Table 3). This process flow is detailed in section D.5. Additionally, the photolithography pattern used on each quadrant was advised by M. Liffredo and displayed in Figures 8a 8b.

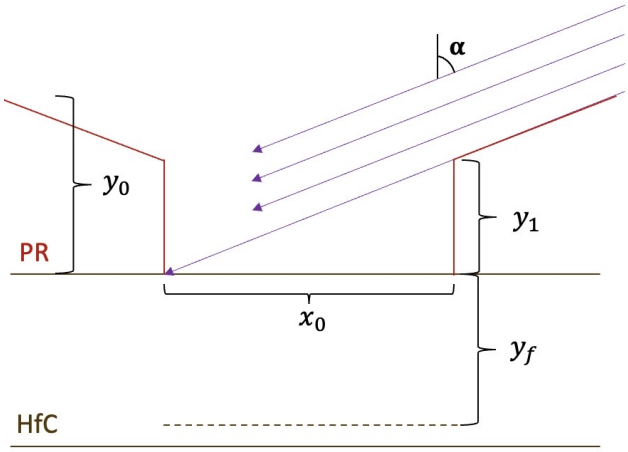


Figure 3: IBE geometry on grooves at an incidient angle α, an initial PR thickness y_0 and a final etching depth y_f. This particular instance shows the PR height y_1 at which HfC starts being etched. The computations in section B.5 showed that $y_1 = y_0$ (HfC was etched from the start).

The computation for etching times relies on the geometries of the grooves (Figure 3). It

takes into account the time to reach HfC at an angle by burning the resist edges and the necessary time to etch away 450nm of HfC (Section B.5). In general, the development can be summarized by the following expressions :

$$t_1(\alpha) = \frac{y_0 - x_0 tan(90 - \alpha)}{\dot{y}_{PR}} \quad (1)$$

$$t_{max} = \frac{y_{PR}}{\dot{y}_{PR}} \qquad t_f = \frac{y_f}{\dot{y}_{HfC}}(\alpha)$$

3.3 Results and Analysis

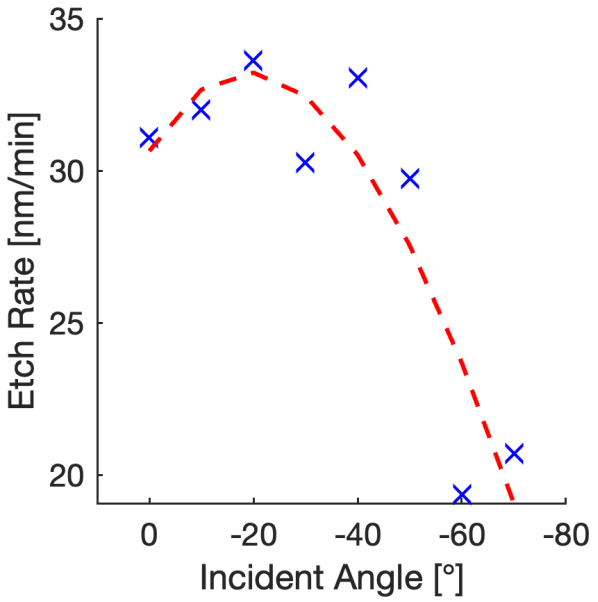


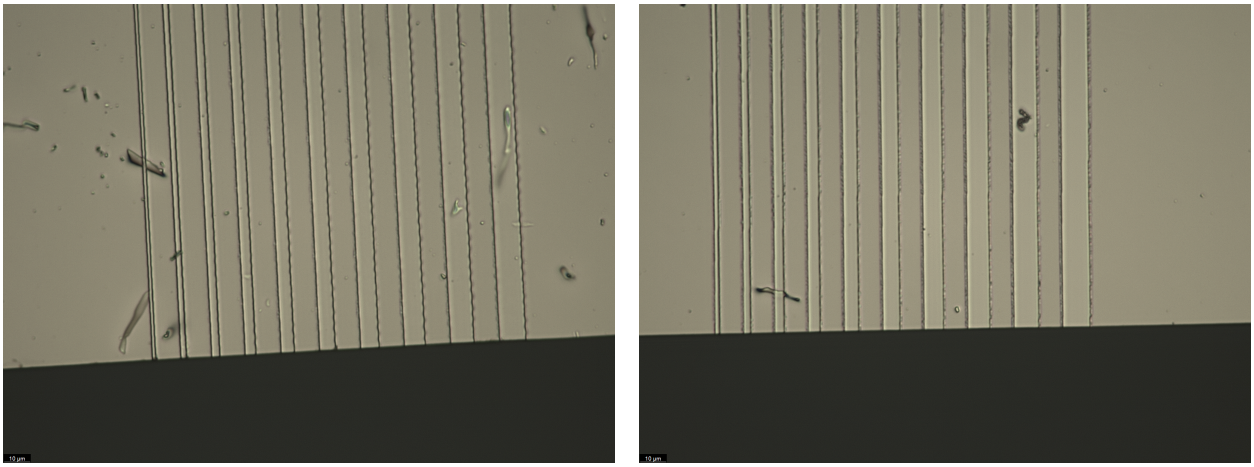
Figure 4: Etch rate as a function of the ion beam's incident angle. The data displayed is the average of all etch rate studies done on inner cleavings (patterns on Figures 7a 7b) displayed on Figures 11a 11b, 11c. The green curve is the cubic fitting (y = -2.37e-5x^3 -8.02e-3x^2 -0.280 x + 30.6, R^2 = 0.822) and predicts a maximum etch rate of 33.2 nm/min at -19.1°.

The first two etch rate runs were obtained from the same wafer and can be seen in Figures 11a 11b. The first is acceptable in the -10° to -30° range (R^2 = 0.7780) and the second, on top of very uninsightful, does not even allow the quadratic interpolation to be of the right curvature (R^2 = 0.1275). After investigation, it was concluded that the reason for the poor performances was that the uniformity of the wafer was greatly overestimated, especially at the edges. Figures 10a 10b display far larger average square resistances (888 Ω/sq) and standard deviation (185 Ω/sq) on the outer layer (defined practically to be the zone between the edge and a 2cm disk representing the inner layer with respect to the chip sizes taken) compared to the inner layer (468 Ω/sq and 28.8 Ω/sq respectively). These measurements can be attributed to the deposited HfC amount decreasing the further the point is from the center.

We therefore do not recommend assuming uniformity for this recipe and instead encourage using the cleaving pattern shown in Figure 7b which was used to determine the 3rd set of data displayed in Figure 11c. It fits nicely whilst being the expected curvature and overall shape. Figure 4 was constructed by averaging every inner measurement across both wafers. A least-squares cubic interpolation done on Matlab was chosen to fit the data based on the investigation by B.Abraham-Shrauner and N.Jagannathan [1] on ion beam etching profiles. It yields a maximum etch rate of 33.2 nm/min at -19.1°.

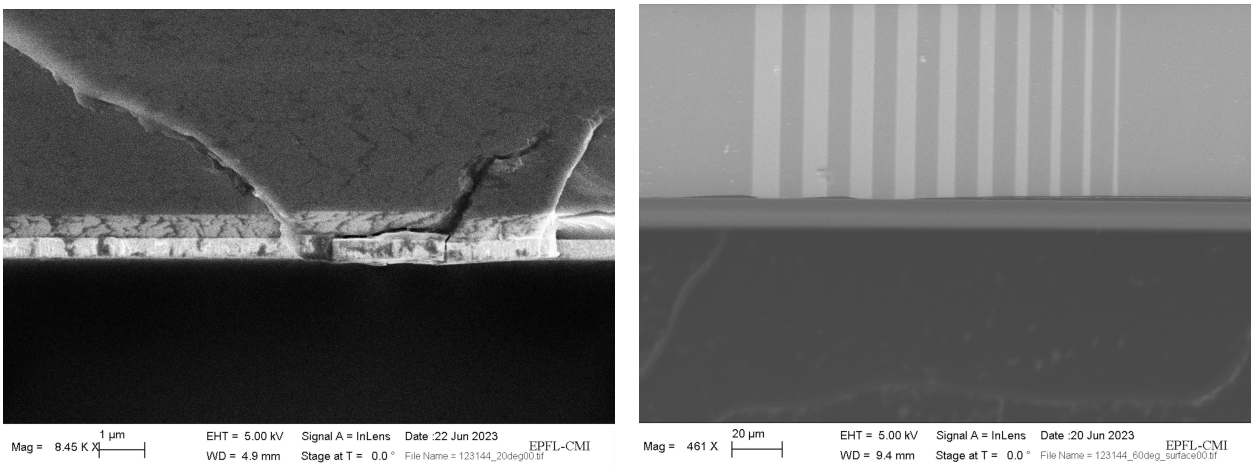
Interestingly, Hafnium Carbide shares the scale and approximate behaviour of titanium when etch with pure Argon Ions [4]. We also corroborate the scale of the results obtained by F. Bauer for an angle of incidence of -10°. Nonetheless, when comparing the two samples used as well as F. Bauer's for -10° with respect to the average in Figure 4 yields a standard deviation of 5.37 which could point in the direction of deposition recipe having a non-negligible impact on etch rate.

Unfortuantely, the etching verticality study did not match any of the expectations. The cross-section SEM images were unsuccessful at observing any patterns whatsoever (Figure 6a) even though they were visible on the chip faces (Figures 6b). Optical measurements were made to understand the problem and grossly determine if the grooves had any depth.



(a) (b)

Figure 5: **(a)** Optical microscopy of patterns cleared of PR after IBE at 10° of incidence. The PR was dosed at 125 mJ/cm^2. The grooves are barely etched pointing to a residual resist layer before IBE. **(b)** The 20° of incidence sample seemingly showing deeper patterns due to the thicker transitions between groove and layer. In this case the PR was dosed at 320 mJ/cm^2 during lithography.



(a) (b)

Figure 6: **(a)** SEM cross-section image of the chip etched at 20° of incidence at the location of the grooves (lithography dose was $320mJ/cm^2$. The two layers (SiO_2 and HfC) are clearly visible and show no signs of etching. **(b)** Tilted (30°) SEM image of the chip etched at 60° of incidence. Even though this sample's PR was exposed at $125mJ/cm^2$ and that no evidence of patterns could be found by exploring the cross section, the grooves are visible.

We see that there is a clear difference in the groove depth between the chip dosed at $125mJ/cm^s$ during lithography and the one dosed at $320mJ/cm^s$ in Figure 5. This indicates that the PR might not have been exposed all the way through even if the recommended parameters by the CMi process team were followed (laser wavelength : 405nm, dose : $125mJ/cm^2$, defocus : -1). The remaining PR delayed the HfC from being etched which reduced the groove depth. Unfortunately, optical profilometry showed that even the sample dosed at $320mJ/cm^2$ had not been etched all the way either (Figure 12) with the $8\mu m$ thick groove being 170nm deep instead of 450nm. Even though this result is to be taken lightly because optical profilometry on nearly transparent layers (SiO_2) can be imprecise, we still believe it is interesting enough to investigate lithography particularities of this setup to avoid these problems in the future.

4 Conclusion

The conducted annealing procedures on the first deposition batch did not affect the stresses and conductivity significantly enough to be continued. We were successful at determining the relationship between etch rate and incident angle even though severe conductivity gradients were observed throughout the wafer. The fabrication of samples to study the verticality of etching was failed most probably due to underexposed resist during the lithography step. The natural sequel to this research should be to explore the coating and lithography parameters to develop a better protocol for HfC. Additionally, it would be useful to confirm that the influence of deposition recipe on the etch rate is indeed negligible by testing more IBE parameters against on a wider range of HfC layers.

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[8] Wiriya Thongruang. "Synthesis and characterization of hafnium carbide thin films". In: 1996.

A Sample Data Base

Wafer N°	Composition	Process
120596	Si (525um), SiO_2 (500nm), HfC (50nm)	D.1, destroyed
120819	Si (525um), SiO_2 (500nm), HfC (50nm)	D.1, destroyed
121751	Si (525um), SiO_2 (500nm), HfC (540nm)	D.2, stored
123196	Si (525um), SiO_2 (500nm), HfC (540nm)	D.2, stored
120842	Si (525um), SiO_2 (500nm), HfC (37.5nm)	D.3, destroyed
123368	Si (525um), SiO_2 (500nm), HfC (500nm)	D.5. stored
123144	Si (525um), SiO_2 (500nm), HfC (500nm)	D.4, stored

Table 1: Wafer Data base

B Method Complements

B.1 Annealing Temperatures and corresponding wafers

Wafer ID	T_{max}	Status
120596	200°C	OK
120596	300°C	OK
120596	400°C	OK
120596	500°C	OK
120596	600°C	HfC disappeared
120819	200°C	OK

Table 2: Annealing steps at $T_0 = 23$°C (initial temperature), $S_{ramp} = 20$K/min (ramp heating rate), $t_{max} = 15$min (time at max temperature)

B.2 Etch Rate IBE Parameters

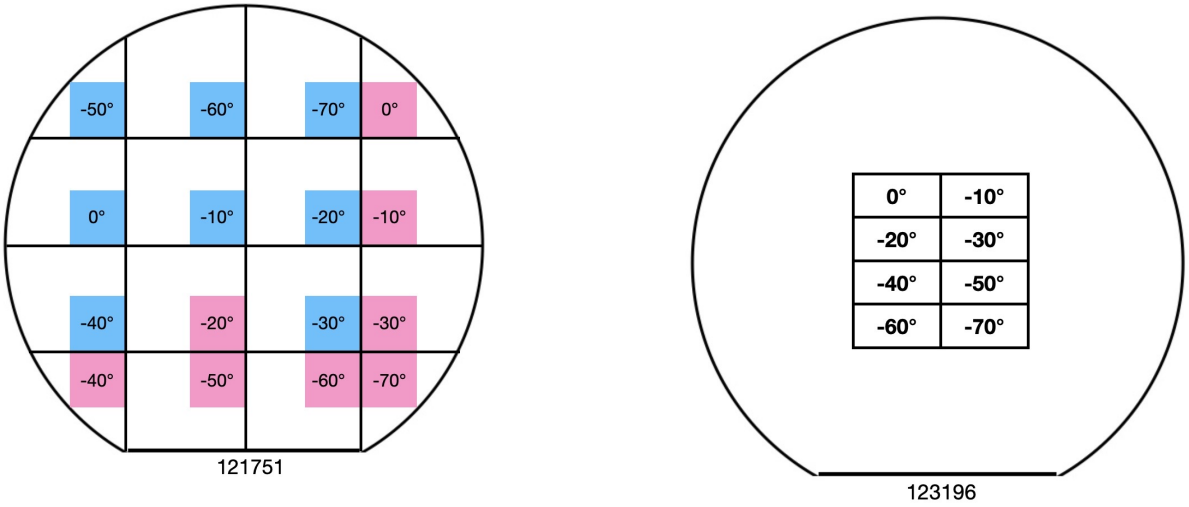
Beam Voltage	Beam Current
300V	500mA
Suppressor Voltage	Incident RF Power
400V	500W
FlowCool Flowrate	K Factor
25	1

Table 3: The IBE parameters used to determine etch rates on 500nm thick HfC layers on the *Veeco Nexus IBE350*. This particular set of parameters is equivalent to the "Low-IBE" program.

Beam Voltage	Beam Current
700V	1100mA
Suppressor Voltage	Incident RF Power
400V	1100W
FlowCool Flowrate	K Factor
25	0.5

Table 4: The IBE parameters used on 500nm thick HfC layers on the *Veeco Nexus IBE350*. This particular set of parameters is equivalent to the "High-IBE" program.

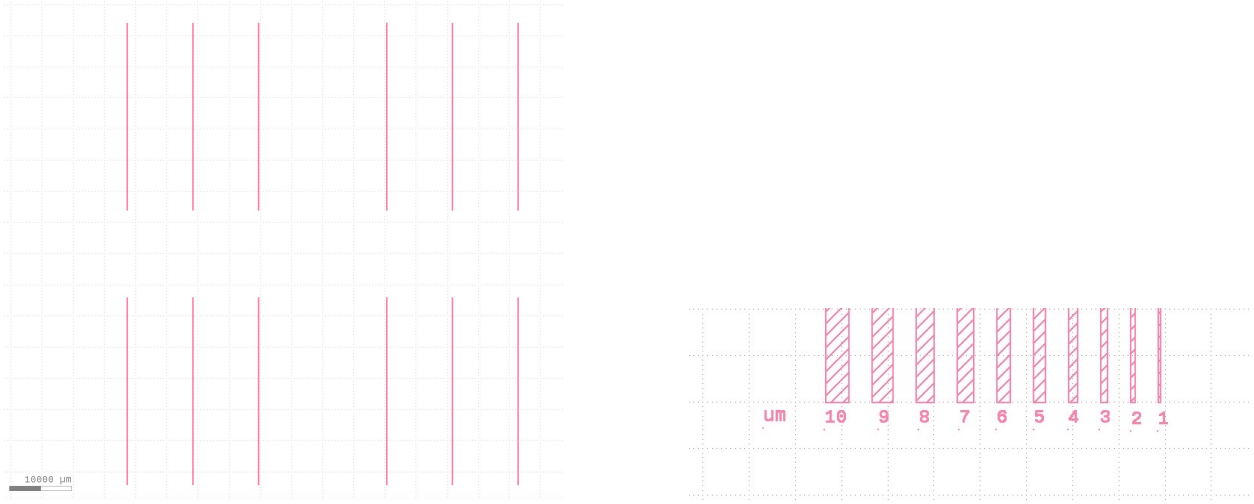
B.3 Etch Rate Cleaving Enumeration



(a) (b)

Figure 7: **(a)** Cleaving pattern of wafer N°121751 used to determine etch rate as a function of IBE incident angle (0° to -70°). Blue : Figure 11a. Pink : Figure 11b. **(b)** Cleaving pattern of wafer N°123196 used to determine etch rate corresponding results are on Figure 11c.

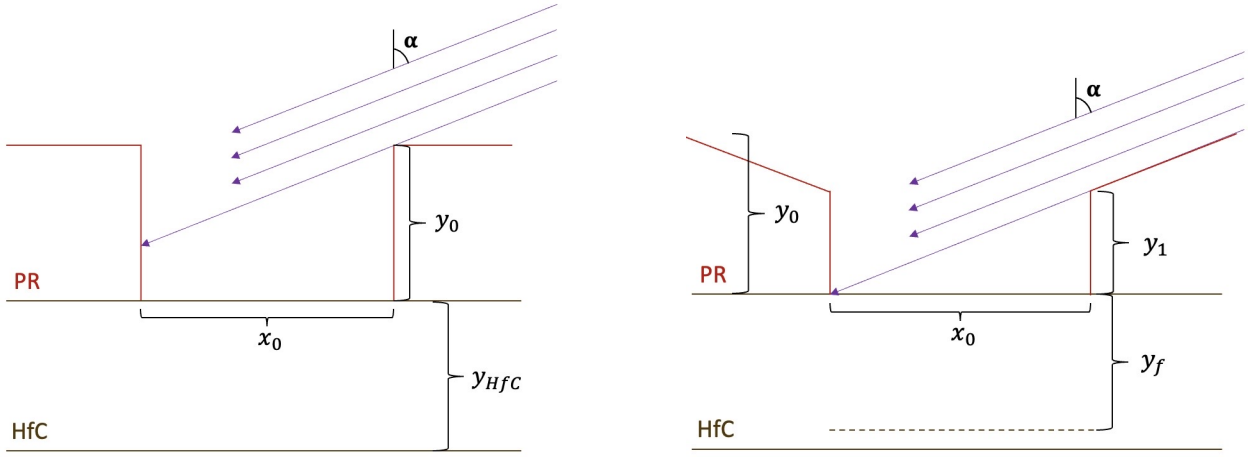
B.4 Photolithography Patterns - MLA150



(a) (b)

Figure 8: **(a)** The entire pattern engraved either sequentially by quarters (Process Flow D.4) or on the entire wafer (Process Flow D.5). Each quarter has 3 sets (red lines) of grooves for redundancy. (**(b)** Up close, every set is made of 10 30mm long grooves varying in width from 10μm to 1μm by a step of 1μm and separated by 10 μm from each other.

B.5 Etch Times for IBE Verticality Study



(a) (b)

Figure 9: **(a)** Modelling of a groove used to compute the etch times for each IBE incidence. This particular instant t_0 represents the initial state of a groove in which HfC may be hindered from the Argon beams by the PR. **(b)** Hypothetical instant t_1 at which argon ions get to the HfC layer for the first time after some PR was etched away. If PR does not hinder Argon ions from touching the layer from the start $t_1 = t_0$.

The first computation is to check for any hindrance or, in other words, to compute the time t_1 that it takes to start etching HfC after removing enough PR. We want to make sure we do not etch through the entire HfC layer hence the limit case is that of the 10μm thick groove because it will be the first to start shedding HfC. The goal is to remove 450nm so as to leave 50nm in store. Hence the parameters as shown in Figures 9a 9b are fixed at $x_0 = 10\mu m$, $y_0 = 1\mu m$, $y_{HfC} = 500nm$, $y_f = 450nm$, $\dot{y}_{PR}(Low\_IBE) = 9.12nm/min$, $\dot{y}_{PR}(High\_IBE) = 48nm/min$ and $\alpha = [10°, 20°, 45°, 60°]$. The etch rates on HfC were predetermined and displayed in Figure 4 (for high beam etch rates, the relation is $\dot{y}_{Low\_IBE} = 0.19 * \dot{y}_{High\_IBE}$).

$$y_1(\alpha) = x_0 tan(90 - \alpha) \qquad y_0 - y_1(\alpha) = \dot{y}_{PR} t_1(\alpha) \quad \rightarrow \quad t_1(\alpha) = \frac{y_0 - x_0 tan(90 - \alpha)}{\dot{y}_{PR}} \tag{2}$$

IBE incidence α [°]	10	20	45	60
$t_1(\alpha)$ - Low_IBE [min:s]	-6108:52	-2902:34	-986:50	-523:25
$t_1(\alpha)$ - High_IBE [min:s]	-1160:41	-551:34	-187:30	-99:27

Table 5: Times to reach the HfC by removing PR. In this case they are all negative hence the HfC is exposed to IBE from the start ($t_1 = t_0$)

Secondly, we must verify the maximum time the sample can spend in the IBE before all the PR layer is removed. This is simply checked by computing :

$$t_{max,Low\_IBE} = \frac{y_{PR}}{\dot{y}_{PR-Low\_IBE}} = 109min39s \qquad t_{max,High\_IBE} = \frac{y_{PR}}{\dot{y}_{PR-High\_IBE}} = 20min49s$$

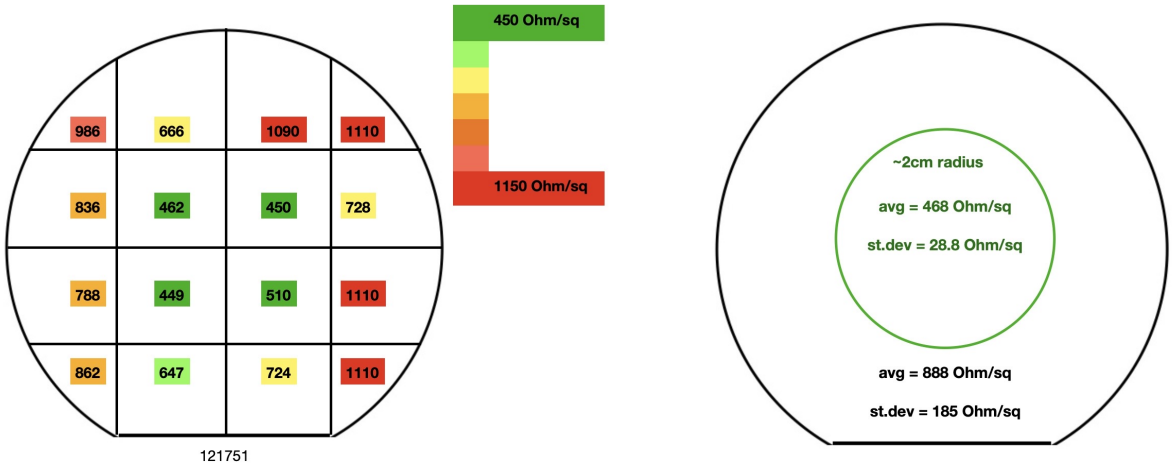
Since all the values of t_1 are negative, the HfC is hit from the start ($t_1 = t_0$) which implies that the etch time to reach 450nm depth is nothing but : $t_f = \frac{y_f}{\dot{y}_{HfC}(\alpha)}$.

IBE incidence α [°]	10	20	45	60
$t_f(\alpha)$ - Low_IBE [min:s]	14:04	13:23	14:20	23:19
$t_f(\alpha)$ - High_IBE [min:s]	2:41	2:32	2:43	4:26

Table 6: Times to etch away 450nm HfC. Since no PR is need to reach it, t_f only depends on the etch rate of HfC.

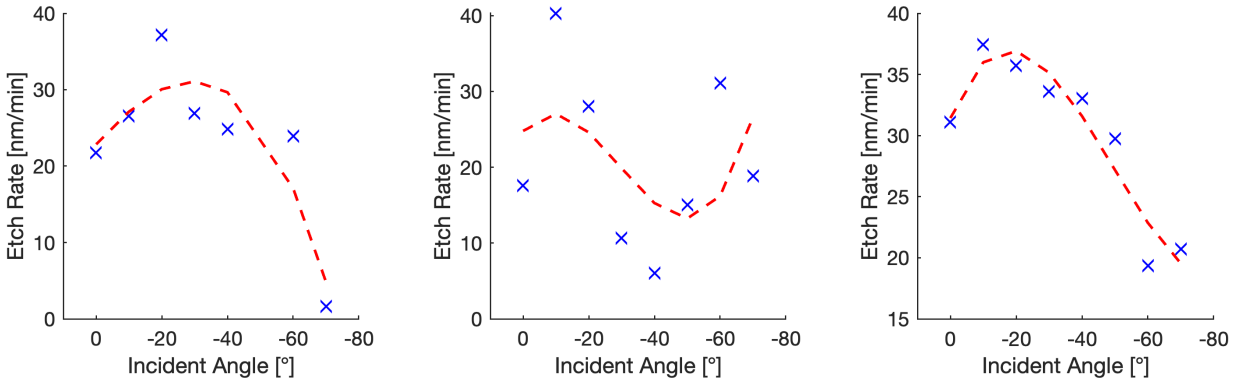
None of these times exceed their respective t_{max} hence the etch times are valid. All considered, we deemed more important to keep a bit of HfC reserve instead of trying to get deep etches in the smaller grooves.

C Result Complements



(a) (b)

Figure 10: **(a)** Reconstruction of square resistance measurement with the respective 4 point measurement average done on each chip. **(b)** Separation of the wafer in an inner and outer zone. The 2cm radius was determined in practice due to the weak results in the outer rim. The most important factor is the difference variance which directly impacts the ability of an operator to make pertinent measurements. This effect can be seen by comparing the information give my crosses (inner) and dots (outer) in Figures 11a and 11b.



(a) (b) (c)

Figure 11: Etch rate with respect to the IBE incident angle. The measures taken within the area of a 2cm center disk are in parentheses and the respective cubic interpolations are in brackets.
(a) (-10°, -20°, -30°), [y = -9.49e-5 x^3 - 3.81e-3 x^2 - 0.475 x + 22.9], $R^2 = 0.784$
(b) (-20°), [y = -4.04e-4 x^3 - 3.57e-2 x^2 - 0.542 x + 24.8], $R^2 = 0.235$
(c) (0°,-10°, -20°, -30°, -40°, -50°, -60°, -70°), [y = -1.55e-4 x^3 - 2.28e-2 x^2 - 0.669 x + 31.4], $R^2 = 0.909$

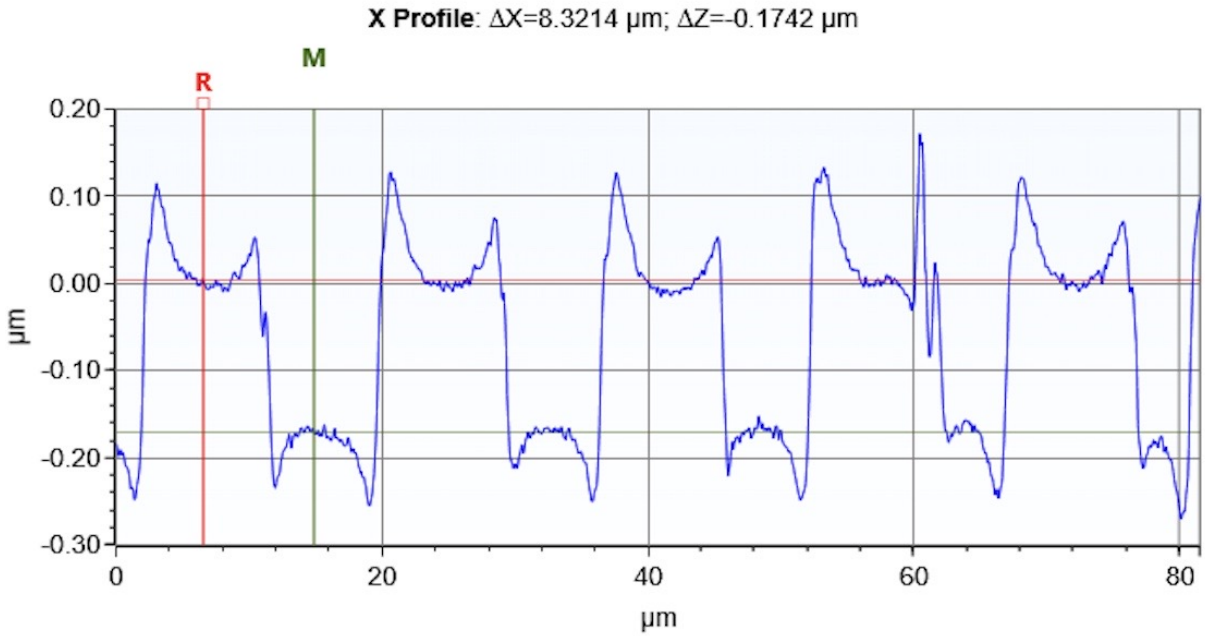


Figure 12: Optical Profilometry of the grooves patterned on the sample at a 320 mJ/cm^2 dose during lithography (followed by IBE at 20° of incidence). This measurement allowed us to draw observations after the SEM cross section imaging was unsuccessful. The grooves are approximately $0.17\mu m$ deep against the expected 450nm (computations similar to the ones showed in section B.5 showed that the center of the measured $8\mu m$ thick groove was etched from the start). This indicates that the IBE was hindered, most likely by a residual PR layer on the pattern.

D Process Flows

The following process flows were approved by the CMi technical service at EPFL

D.1 3rd of March 2023

Lab : Advanced NEMS
Operator Name : **Nicolas Avellan, Joao Barini**
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CMi EPFL Center of MicroNanoTechnology

☒ Semestral Project ☐ Master Project ☐ Thesis ☐ Other

Project Name: Characterisation of HfC thin films deposition

Description of the fabrication project

The goal is to optimize the deposition and annealing techniques of Hafnium Carbide. We aim at creating a deposition protocol for multiple thicknesses as well as an annealing protocol to reduce the observed brittlness of HfC. We analyse and improve electrical conductivity of the samples to complete the analysis.

Technologies used *!! remove non-used !!*
Sputtering, Annealing, Ellipsometry, Optical metrology

Ebeam litho data - Photolitho masks - Laser direct write data			
Mask #	**Critical Dimension**	**Critical Alignment**	**Remarks**

Substrate Type
Silicon wafer (100mm <100>, 525 um thickness), HfC layer (200-2000um)

Interconnections and packaging of final device

Thinning/grinding/polishing of the samples is required at some stage of the process.
☒ No ☐ Yes => confirm involved materials with CMi staff

Dicing of the samples is required at some stage of the process.
☒ No ☐ Yes => confirm dicing layout with CMi staff

Wire-bonding of dies, with glob-top protection, is required at the end of the process.
☒ No ☐ Yes => confirm pads design (size, pitch) and involved materials with CMi staff

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Step-by-step process outline

Step	Process description	Cross-section after process
1.	***Wafer stress measurement*** Tool: Z15 Toho FLX	
2.	***HfC deposition*** Tool: Z11 Alliance-Concept DP650 Thickness : 100nm – 1um (to evaluate with CMi staff)	
3.	*Optical measurement* Tool: Z4 Woodlam RC2	
4.	*Film Stress Measurement* Machine: Z15 Toho FLX	
5.	*Sheet resistance Measurement* Machine: Z4 Filmetrics R50	
6.	*Annealing* Machine: Z11 Neytech Qex Slope : 20K/min T_max : 600°C Time spent at T_max : 15min Atmosphere : Nitrogen	
7.	*Plane Stress Measurement* Machine: Z15 Toho Technology FLX	
8.	*Optical measurement* Tool: Z4 Woodlam RC2	
9.	*Sheet resistance Measurement* Machine: Z4 Filmetrics R50	

D.2 10th of May 2023

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☒ Semestral Project ☐ Master Project ☐ Thesis ☐ Other

Project Name: Characterisation of HfC thin films deposition

Description of the fabrication project

The goal is to optimize the deposition and annealing techniques of Hafnium Carbide. We want to determine the ion beam etch rate of the HfC layer for multiple angles and recipes. The etch rate is determined with both the mass spectrometer of the IBE and R50 filmetrics to check.

Technologies used *!! remove non-used !!*			
Ion Beam Etching, Metrology			
Ebeam litho data - Photolitho masks - Laser direct write data			
Mask #	**Critical Dimension**	**Critical Alignment**	**Remarks**
1	**>1mm**	**>1mm**	**Mask to allow for only one quarter of the wafer to be used per test.**
Substrate Type			
Silicon wafer (100mm <100>, 525 um thickness), SiO_2 layer (500nm) ,HfC layer (50-500nm)			

Interconnections and packaging of final device

Thinning/grinding/polishing of the samples is required at some stage of the process.

☒ No ☐ Yes => confirm involved materials with CMi staff

Dicing of the samples is required at some stage of the process.

☐ No ☒ Yes => confirm dicing layout with CMi staff

Wire-bonding of dies, with glob-top protection, is required at the end of the process.

☒ No ☐ Yes => confirm pads design (size, pitch) and involved materials with CMi staff

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Step-by-step process outline

Step	Process description	Cross-section after process
1.	***Resistivity Measurement*** Machine : Z4 Filmetrics R50	
2.	Mounting of Chip to 100mm Carrier Wafer using Quick Stick Machine: Z6 – RC8 THP-Manual Coater	
3.	***Ion Beam Etching*** Tool: Z11 Veeco Nexus IBE350	
4.	***Resistivity Measurement*** Machine : Z4 Filmetrics R50	
5.	***Geometric Profiling*** Machine : Bruker Dektak XT	

D.3 18th of May 2023

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☒ Semestral Project ☐ Master Project ☐ Thesis ☐ Other

Project Name: Characterisation of HfC thin films deposition

Description of the fabrication project

The goal is to optimize the deposition and annealing techniques of Hafnium Carbide. We want to determine the ion beam etch rate of the HfC layer for multiple angles and recipes. The etch rate is determined with both the mass spectrometer of the IBE and R50 filmetrics to check.

Technologies used *!! remove non-used !!*			
Ion Beam Etching, Mechanical Metrology, Photolithography, Sputtering			
Ebeam litho data - Photolitho masks - Laser direct write data			
Mask #	**Critical Dimension**	**Critical Alignment**	**Remarks**
1	**>1mm**	**>1mm**	**Mask to allow for only one quarter of the wafer to be used per test.**
Substrate Type			
Silicon wafer (100mm <100>, 525 um thickness), SiO_2 layer (500nm) ,HfC layer (50-500nm)			

Interconnections and packaging of final device

Thinning/grinding/polishing of the samples is required at some stage of the process.

☒ No ☐ Yes => confirm involved materials with CMi staff

Dicing of the samples is required at some stage of the process.

☒ No ☐ Yes => confirm dicing layout with CMi staff

Wire-bonding of dies, with glob-top protection, is required at the end of the process.

☒ No ☐ Yes => confirm pads design (size, pitch) and involved materials with CMi staff

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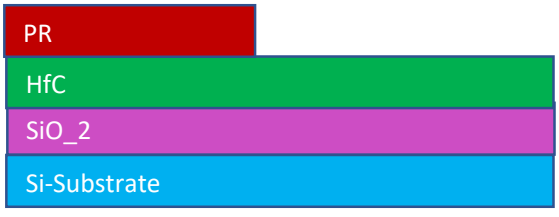
Step-by-step process outline

Step	Process description	Cross-section after process
1.	***Measurement of HfC Film Thickness***	
2.	***Photolitography Coating*** *Machine: ACS200* *Resist: ECI3027* *Target Thickness: 2 microns*	
3.	***Photolitography Exposure*** *Machine: Süss MicroTec MA6 03* *Mask: #1*	
4.	***Photolit Development*** *Machine: ACS200* *Developer: MF CD 26*	
5.	***Measurement of PR film thickness*** *Machine : F20-UV*	

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6.	***Ion Beam Ething*** *Machine : Veeco Nexus IBE 350* *Power : Low*	
7.	***Measurement of HfC and PR film thickness*** *Instrument : F20-UV*	
8.	***Photolithography Stripp Off*** *O2 plasma 1min in Tepla + 1165 remover in UFT wet bench Z2*	
9.	***Measurement of HfC layer thickness*** *Instrument : Bruker Dektak XT*	

D.4 1st of June 2023

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☒ Semestral Project ☐ Master Project ☐ Thesis ☐ Other

Project Name: Characterisation of HfC thin films deposition

Description of the fabrication project

The goal is to find the verticality obtained using IBE on the HfC layers. The study is done on a single wafer which will be etched differently on 4 quadrants to determine the etched groove geometry for -10°, -20°, -45° and -60°.

Technologies used *!! remove non-used !!*			
Sputtering, Photolithography, Wet Etching, Ion Beam Etching, Oxygen Plasma Etching			
Ebeam litho data - Photolitho masks - Laser direct write data			
Mask #	**Critical Dimension**	**Critical Alignment**	**Remarks**
1	**>1mm**	**>1mm**	**Mask to allow for only one quarter of the wafer to be used per test.**
Substrate Type			
Silicon wafer (100mm <100>, 525 um thickness), SiO_2 layer (500nm) ,HfC layer (50-500nm)			

Interconnections and packaging of final device

Thinning/grinding/polishing of the samples is required at some stage of the process.

☒ No ☐ Yes => confirm involved materials with CMi staff

Dicing of the samples is required at some stage of the process.

☐ No ☒ Yes => confirm dicing layout with CMi staff

Wire-bonding of dies, with glob-top protection, is required at the end of the process.

☒ No ☐ Yes => confirm pads design (size, pitch) and involved materials with CMi staff

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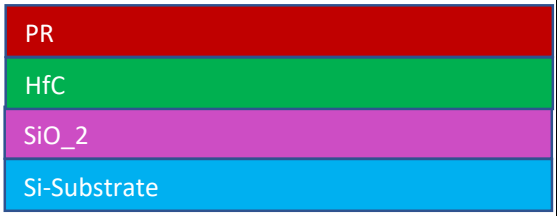
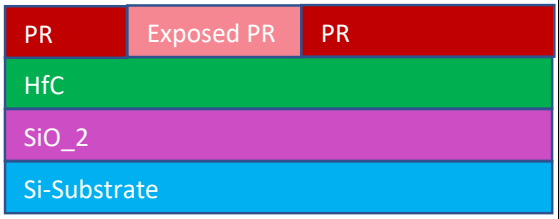
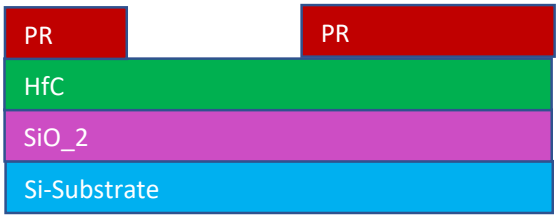
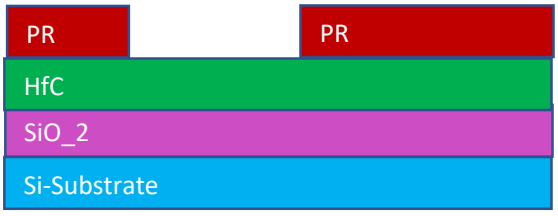
Step-by-step process outline

Step	Process description	Cross-section after process
1.	***Measurement of the IBE Verticality on an HfC film***	
2.	***Photolitography Coating*** *Machine: ACS200* *Resist: ECI3007* *Target Thickness: 1 micron* *Program : C4_H_3007_1u_EC*	
3.	***Photolitography Exposure*** *Machine: MLA150* *Only on 1 quadrant of the wafer.*	
4.	***Photolit Development*** *Machine: ACS200* *Developer: MF CD 26* *Program : D4_PEB_3007-1u_B*	
5.	***Measurement of PR film thickness*** *Machine : F20-UV*	

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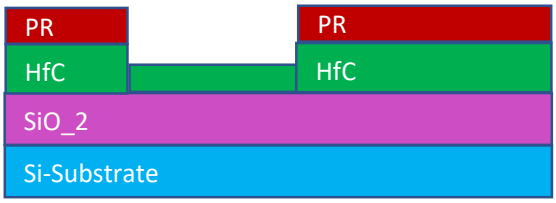
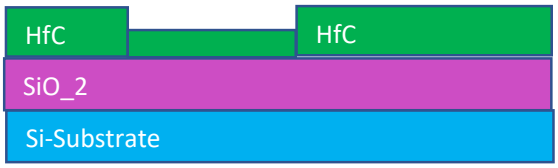
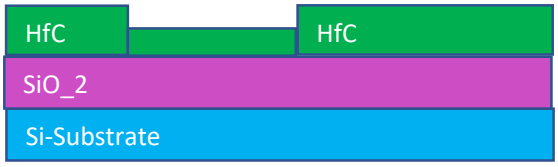
6.	***Ion Beam Ething*** *Machine : Veeco Nexus IBE 350* *Power : Low, 3min*	
7.	***PR Sstrip Off*** *Machine 1 : Tepla 300* *O2 plasma 1min* *Machine 2 : Wet bench* *Remover 1156*	
8.	***Repeat steps 2-7 for all 4 quadrants with different IBE angles.*** ***Cleave the 4 quadrants at the end.***	
9.	***Cross-section inspection*** *Machine : SEM Leo*	

D.5 5th of June 2023

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☒ Semestral Project ☐ Master Project ☐ Thesis ☐ Other

Project Name: Characterisation of HfC thin films deposition

Description of the fabrication project

The goal is to find the verticality obtained using IBE on the HfC layers. The study is done on a single wafer which will be etched differently on 4 quadrants to determine the etched groove geometry for -10°, -20°, -45° and -60°.

Technologies used *!! remove non-used !!*			
Sputtering, Photolithography, Wet Etching, Ion Beam Etching, Oxygen Plasma Etching			
Ebeam litho data - Photolitho masks - Laser direct write data			
Mask #	**Critical Dimension**	**Critical Alignment**	**Remarks**
1	**>1mm**	**>1mm**	**Mask to allow for only one quarter of the wafer to be used per test.**
Substrate Type			
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Interconnections and packaging of final device

Thinning/grinding/polishing of the samples is required at some stage of the process.

☒ No ☐ Yes => confirm involved materials with CMi staff

Dicing of the samples is required at some stage of the process.

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Wire-bonding of dies, with glob-top protection, is required at the end of the process.

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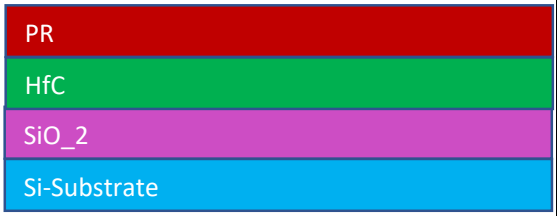
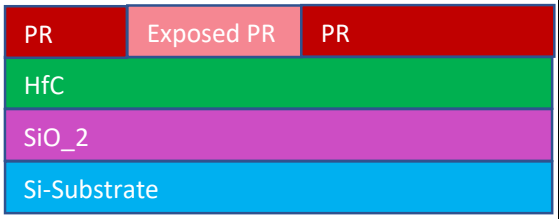
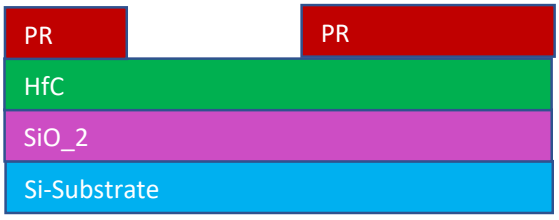
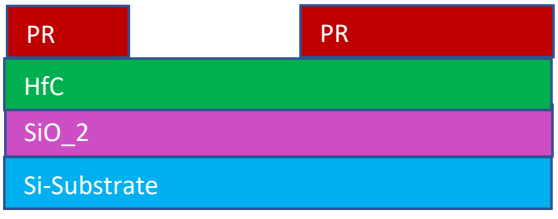
Step-by-step process outline

Step	Process description	Cross-section after process
1.	***Measurement of the IBE Verticality on an HfC film***	
2.	***Photolitography Coating*** *Machine: ACS200* *Resist: ECI3007* *Target Thickness: 1 micron* *Program : C4_H_3007_1u_EC*	
3.	***Photolitography Exposure*** *Machine: MLA150* *On all 4 quadrants*	
4.	***Photolit Development*** *Machine: ACS200* *Developer: MF CD 26* *Program : D4_PEB_3007-1u_B*	
5.	***Measurement of PR film thickness*** *Machine : F20-UV*	

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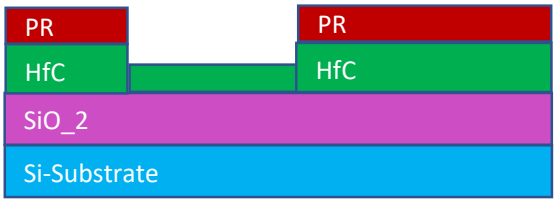
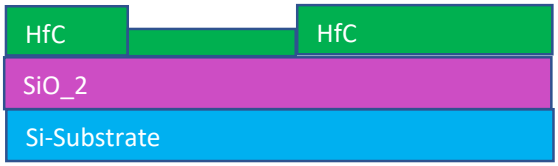
6.	***Cleave the 4 quadrants.***	
7.	***Ion Beam Ething*** *Machine : Veeco Nexus IBE 350*	
8.	***PR Strip Off*** *Machine 1 : Tepla 300* *O2 plasma 1min* *Machine 2 : Wet bench* *Remover 1156*	
9.	***Cross-section inspection*** *Machine : SEM Leo*