Compound Logic Gates for Pipeline Depth Minimization in Single Flux Quantum Integrated Systems

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ABSTRACT

Superconductive electronics is a promising candidate for supplementing or replacing existing CMOS VLSI systems. Rapid single-flux quantum (RSFQ) is one of the most advanced superconductive technologies operating at tens of gigahertz while reducing the operating power by up to three orders of magnitude as compared to conventional semiconductor systems. Achieving VLSI complexity of RSFQ integrated systems, however remains an elusive task due to fundamental differences between RSFQ and CMOS technologies. Most RSFQ logic gates, such as NOT and XOR are sequential in nature. Compared to CMOS, the number of logical pipeline stages is prohibitively large, greatly complicating the design of complex systems. Furthermore, additional circuitry, such as splitters and path balancing flip-flops, constitute a major overhead. In this paper, the novel gate compounding technique is presented to maximize the functionality achievable within a single clock cycle. The logic gates are decomposed into primitives that can be efficiently combined to evaluate complex expressions in a single clock cycle. Structures generated by gate compounding are not sensitive to signal arrival time, simplifying the system design process. The expressive power of SFQ logic is increased, allowing any two-input truth table to be implemented within a single clock cycle. A 4-bit carry lookahead adder (CLA) is implemented using compound gates, demonstrating smaller area, pipeline depth, and clock tree size.

CCS CONCEPTS

• **Hardware** → *Combinational circuits*; *Sequential circuits*; **Emerging architectures**; *Standard cell libraries*; **Technology-mapping**; **Circuit optimization**.

KEYWORDS

circuit optimization, technology mapping, emerging technologies, cryogenic technologies, superconductivity, single flux quantum, logic synthesis

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1 INTRODUCTION

Superconductive electronics is one of the most promising beyond-CMOS technologies, with Rapid Single-Flux Quantum (RSFQ) [15] being one of the most prominent superconductive technologies. RSFQ systems consistently achieve operating frequencies on the order of tens of gigahertz [11], with particular structures operating at hundreds of gigahertz [3]. Furthermore, the operating power of the RSFQ systems is two to three orders of magnitude smaller than CMOS, even considering the refrigeration power [7].

Achieving the aforementioned advantages at scale however remains a challenging task. In CMOS, transistors encode information by voltage levels. In contrast, in RSFQ, Josephson Junctions (JJ) encode information using single flux quantum (SFQ) pulses [2]. The absence or presence of a SFQ pulse encode, respectively, a logical 0 or 1. The flow of pulses within a logic network requires synchronization. While a few structures, such as splitter and OR, can operate asynchronously, most logic gates in the original RSFQ cell library, such as AND, NOT and XOR, require clock signal [15]. This feature requires the data to be pipelined at the gate level.

Two features further complicate the development of large-scale RSFQ systems. Due to the quantized nature of SFQ pulses, most RSFQ logic gates have a limited fanout of one. A special gate called splitter is necessary to duplicate a signal [2, 14], as illustrated in Fig. 1. The need for splitters is particularly significant in clock distribution networks. Delivering a clock signal to n clocked gates requires a binary tree of at least $(n-1)$ splitters [1]. In addition, path balancing is required to ensure the correct order of data propagation within the network, as indicated by two path balancing D-flip-flops (DFF) in Fig. 1. The number of path balancing DFFs and splitters can be prohibitively large, degrading the area and yield of an integrated system. Despite the advances in technology mapping [13, 17], the overhead of path balancing and clock distribution remains large, motivating the investigation of alternative RSFQ architectures.

A large body of literature targets the reduction in number of clocked elements by maximizing the functionality realized within a

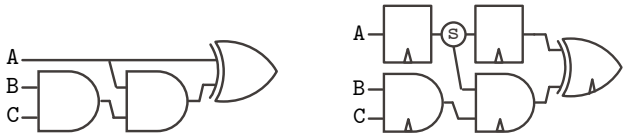

Figure 1: a) An example of a CMOS circuit. b) Equivalent RSFQ circuit with a splitter and two path balancing DFFs.

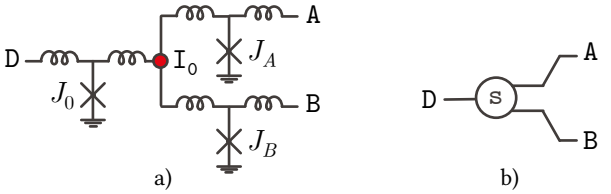

Figure 2: a) Splitter gate. The red dot I_0 denotes the bias current. b) Symbol for splitter used in this paper.

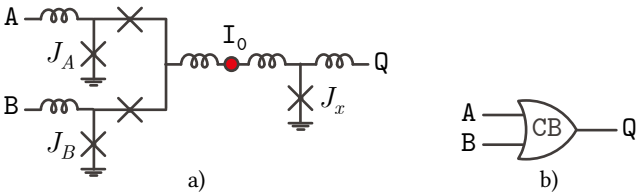

Figure 3: a) Merger (confluence buffer) gate and b) equivalent symbol.

single clock cycle. Dynamic SFQ (DSFQ) is a relatively new branch of RSFQ technology where the gates reset to the initial state after the specified period of time [18]. The design of DSFQ circuits is therefore similar to CMOS circuits where large combinational blocks can be synchronized using relatively few synchronous elements [14]. The major advantage of DSFQ technology is smaller area as compared to the conventional RSFQ circuits. Furthermore, with fewer clocked elements, the clock network complexity and path balancing are greatly simplified. A similar approach based on clockless logic gates is proposed in [11]. Based on nondestructive readout (NDRO) flip-flop, clockless NIMPLY and AND functions are efficiently realized. By combining the clocked and clockless gates, the pipeline depth is significantly reduced. A carry-lookahead adder [8] and a 32-bit arithmetic logic unit [10] operating at speeds above 10 GHz have been successfully demonstrated.

The major challenge imposed by both of these methods is the complex timing constraints. In DSFQ, the interaction between the input skew tolerance, clock frequency, and bias margins [14] complicates the circuit design. The NDRO-based clockless gates are sensitive to the order of input arrival, necessitating careful timing analysis [9]. To alleviate this issue, the novel gate compounding technique is proposed in this paper. By analyzing the synchronization mechanisms within the RSFQ gates, the functionality achievable within a single clock cycle is greatly enriched. Significant reduction in pipeline depth and number of clocked elements can be achieved, not only reducing the latency and area of a functional circuit, but also reducing the size of the clock distribution network. The logic gates obtained using the proposed technique are not sensitive to the order of input arrival, reducing the complexity of the system design process. The rest of the paper is organized as follows. Components of the RSFQ technology are reviewed in Section 2. The gate compounding technique is described in Section 3. Practical features of the proposed technique are reviewed in Section 4. Validation of the technique using a case study is provided in Section 5, followed by conclusions in Section 6.

2 REVISITING THE RSFQ LOGIC GATES

The proposed gate compounding technique exploits the differences among data synchronization mechanisms in the RSFQ technology. Based on the data synchronization mechanism, RSFQ logic gates can be divided into three categories. In this section, the RSFQ logic gates are reviewed based on these categories.

2.1 Asynchronous input, asynchronous output (AA)

The AA components process the input information immediately upon arrival. The result of the processing is released after a fixed delay, without a synchronizing signal. For gate compounding, the most important gates in this category are splitter and merger.

The **splitter** gate is depicted in Fig. 2. The input junction J_0 generates a SFQ pulse that is distributed to two output junctions, J_1 and J_2 biased close to critical current. Upon arrival of the input pulse, J_1 and J_2 both produce a SFQ pulse, thereby copying the input signal.

Merger, often referred to as **confluence buffer** (CB), directs signals from multiple (typically two) input branches into one output branch, as shown in Fig. 3. A pulse arriving from either of the input branches switches the junction J_x, triggering the release of SFQ pulse towards the output. A CB therefore effectively performs a logical OR function. The merger produces two output pulses, if the pulses are temporally separated, or a single pulse, if the signals arrive simultaneously.

2.2 Asynchronous input, synchronous output (AS)

The components of AS category accept and process the input information immediately upon arrival. The release of the data is however delayed until the arrival of the clock signal. The primary components of this type include D-flip-flop, inverter, and exclusive-or.

The simplest RSFQ component of this type is **D-flip-flop** (DFF), depicted in Fig. 4a. The storage loop J_1-J_2 has two stable states, enabling storage of digital information. The inductors and JJs are tuned to initially direct the bias current into J_0, as shown by the solid blue line, corresponding to storage of logical 0. A SFQ pulse at input D briefly increases the current flowing through J_0 beyond the critical current. J_0 temporarily exhibits high effective inductance, causing the bias current to redirect toward J_1, thereby reversing the loop current to clockwise (shown by the red dashed line), corresponding to the logical 1.

A SFQ pulse at CLK terminal is reads the state of the storage loop. If the loop current is directed counterclockwise, the clock pulse switches the junction J_2, producing no pulse at the output Q, reading the state 0. Conversely, if the loop current is directed clockwise, the clock pulse switches the junction J_1, producing the SFQ pulse at Q, reading the state 1. Switching J_1 redirects the bias current towards J_0, resetting the storage loops to the initial state 0. The DFF is therefore often called a destructive readout (DRO) gate [5], since the information is removed from the storage loop by clock signal.

Inverter is a relatively expensive component in RSFQ, as shown in Fig. 4b. The bias current within the main loop J_0-L_0-J_1-L_1 initially flows counterclockwise, as denoted by the solid blue line. J_1 is therefore biased farther from critical current, causing the incoming clock pulse to switch J_2, releasing the pulse to output Q. The input pulse A switches J_0 and reverses the current within the loop to

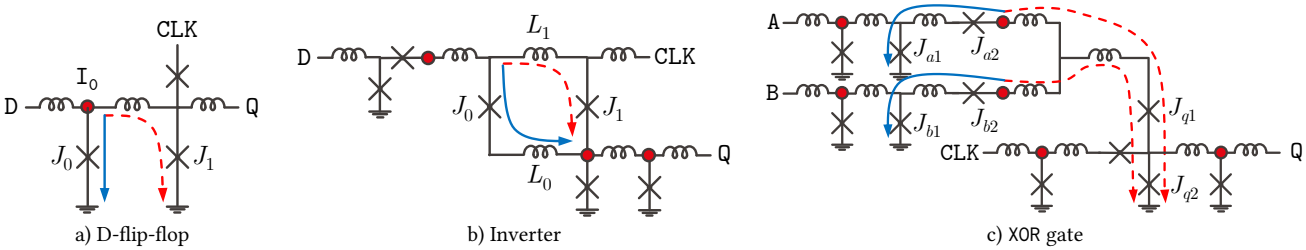

Figure 4: Asynchronous input, synchronous output (AS) components. The solid blue and dashed red lines denote the storage loops in, respectively, logical `0` and `1` state.

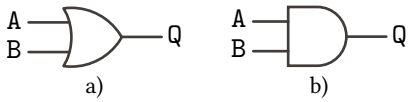

Figure 5: Synchronous input, asynchronous output (SA) gates derived from confluence buffer (see Fig. 3a).

clockwise, as denoted by the dashed red line. A clock pulse therefore switches J_1, resetting the main to the initial state, while producing no output.

The **exclusive-or (XOR)** gate, illustrated in Fig. 4c, hosts two quantizing storage loops. A single input pulse arriving to branch A (B) gate reverses the persistent current within the loop J_{a1}-J_{a2}-J_{q1}-J_{q2} (J_{b1}-J_{b2}-J_{q1}-J_{q2}). A data pulse arriving at the opposite branch B (A) before the clock signal increases the persistent current beyond the critical current of junction J_{q1} removing the flux from the loop and resetting both loops to the initial state. The clock pulse reads the state of the loop via the comparator J_{clk}-J_{q2}.

2.3 Synchronous input, asynchronous output (SA)

To function correctly, the SA components require the inputs to arrive simultaneously, while releasing the result immediately after processing. Assuming simultaneously arriving inputs, a CB depicted in Fig. 3 can be tuned to produce at most a single output pulse, producing an **OR** gate [16]. Furthermore, by increasing the size and reducing the bias current flowing through J_x, the current necessary for switching J_x can be increased. Under these conditions, the SFQ pulses need to arrive at both inputs simultaneously to increase current through J_x beyond the critical value, producing an **AND** gate. In this paper, standard symbols are used to depict the SA gates, as shown in Fig. 5.

3 GATE COMPOUNDING TECHNIQUE

The three categories of components described in the previous section impose specific restrictions on the flow of data within a RSFQ circuit. Most importantly, the SA components can only be placed directly after the AS elements, since the SA components can ensure simultaneous release of the SFQ pulses. To comply with these restrictions, **gate compounding** technique is proposed in this paper. A generic RSFQ logic gate can be produced by following the generic gate structure illustrated in Fig. 6. Inputs to a compound gate are initially processed by AA gates. The signals then flow towards the AS gates where the result of a logical operation is stored until the

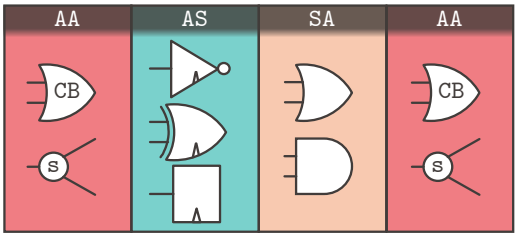

Figure 6: Generic compound gate structure.

arrival of the clock signal. The clock signal triggers the simultaneous release of the data towards the SA gates. Finally, the AA gates complete the function.

There are two major advantages of the proposed structure. The first advantage is robustness. Since the initial processing is handled by the AA or AS gates, arbitrary order of input arrival is supported, relaxing the timing constraints of the circuit. The second advantage is expressive power. The proposed gate compounding technique significantly expands the set of functions realizable within a single clock cycle. To illustrate the effectiveness of gate compounding, consider the NIMPLY ($Q = A\bar{B}$) function. Two clock cycles and one path balancing DFF are needed to realize this function using the conventional cells, as illustrated in Fig. 7a. Note however that the synchronization is already performed by the inverter and DFF. The two DFFs within the AND gate are therefore redundant and can be removed, as illustrated in Figs. 7b-c. To verify the correct functionality of this structure, the AND gate from RSFQlib [19] is modified by replacing one of the clocked branches with an inverter. The function is completed in a single clock cycle with no path balancing DFFs. Correct behavior is verified in the simulation, as illustrated in Fig. 7.

The original RSFQ library allows 13 of 16 two-input functions to be realized within a single cycle [14]. The proposed technique

Table 1: Two-input logic functions realizable within a single clock cycle.

Function	#JJ	Min. T_{clk}, ps	Max. f_{clk}, GHz	Bias margin, %	
NOT	9	8	125.0	-16	27
AND	11	19	52.6	-34	16
OR	8	12	83.3	-42	16
XOR	11	33	30.3	-34	10
NOR	14	18	55.6	-16	27
NAND	23	19	52.6	-16	22
IMPLY	17	22	45.5	-25	26
NIMPLY	14	19	52.6	-27	16
XNOR	38	42	23.8	-16	14

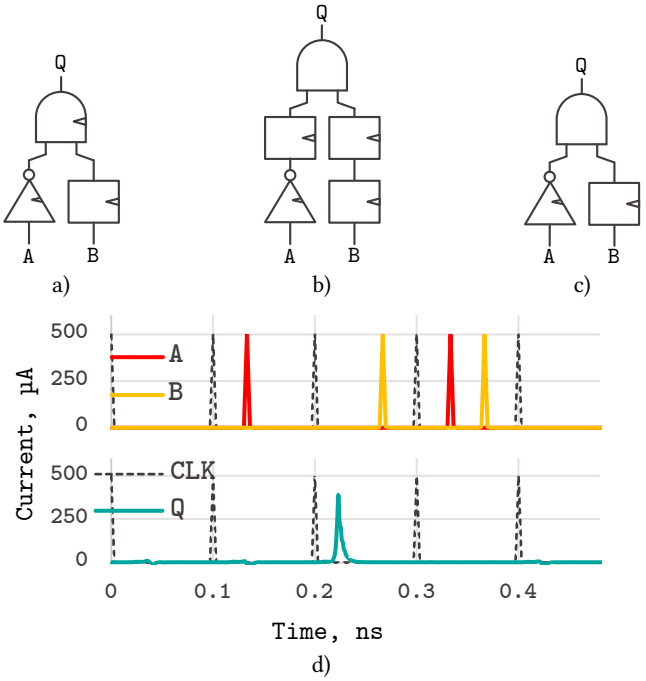

Figure 7: NIMPLY function ($Q = A\bar{B}$) optimized by gate compounding. a) Conventional realization requiring two clock cycles and one path balancing DFF. b) Equivalent representation decoupling DFFs and tuned merger within an AND gate. c) NIMPLY gate optimized by removing redundant DFFs. d) Simulation showing correct functionality of the gate.

enables a single cycle NIMPLY and XNOR gates. All of the 16 two-input truth tables can be implemented within a single clock cycle using compound RSFQ gates. The characteristics of the two-input logic functions are described in Table 1. The proposed NIMPLY gates exhibit DC bias margins comparable to the gates presented in Sunmagnetics MITLL SFQ5ee library [19]. The maximum operating frequency is over 50GHz, comparable to conventional AND and OR gates. By representing XNOR as

$$\overline{a \oplus b} = \overline{(a+b)} + ab, \tag{1}$$

the function can be realized in a single clock cycle. The resulting structure however exhibits relatively large area and relatively small operating frequency and bias margins, indicating the need for judicious use of gate compounding.

4 PRACTICAL CONSIDERATIONS

Recall that, if the two pulses entering a CB are sufficiently spaced in time, the CB produces two SFQ pulses at the output. The second pulse has no effect if the subsequent gate is a DFF or an inverter [2]. If however the CB is followed by XOR incorrect result may be produced. Consider the circuit shown in Fig. 8. The storage loop within the XOR gate is correctly switched and reset with pulses A and C. The pulse B arriving during the same clock cycle, however, sets the storage loop to state 1, producing incorrect result. To avoid this data hazard, the XOR gate can be placed after a CB only if the CB is guaranteed to produce at most one SFQ pulse, i.e., the inputs to a CB are never simultaneously equal to 1. This condition can be

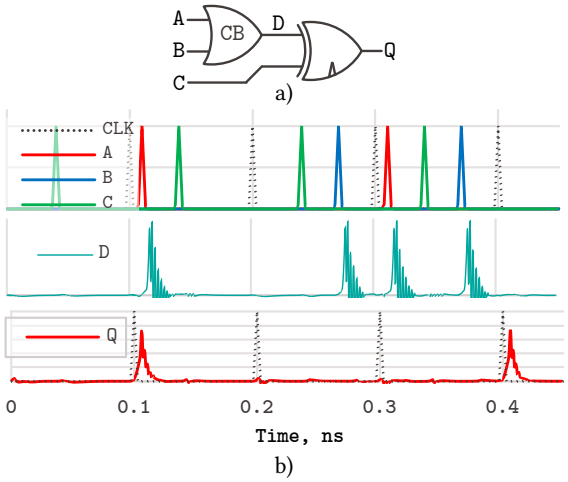

Figure 8: Incorrect realization of $(A + B) \oplus C$ function using CB and XOR gate. a) Schematic connecting CB to the input of XOR gate. b) During the last clock cycle, the main loop within an XOR gate is set to 1 by A, reset by C, and subsequently set to 1 by pulse B, incorrectly producing output pulse.

detected during the logic synthesis. In [12], for example, the inputs of the CB are connected to an AND gate. If the output of the AND gate is always zero, the CB cannot produce more than one pulse and can, therefore, be used as an input to the XOR gate.

5 CASE STUDY

To evaluate the proposed methodology, 4-bit carry lookahead adder is constructed using compound gates. The logic cells are implemented using ColdFlux cell library [19]. Two primary modules used in this structure are depicted in Fig. 9. The initial processing module accepts the bits a_i and b_i of the summands and performs logical AND and XOR. These signals are next processed using the main generate-propagate (GP) module depicted in Fig. 9b. The module accepts two pairs of signals p_i, g_i, p_j, and g_j to produce two outputs,

$$G = (g_i + p_i)(g_i + g_j), \tag{2}$$

$$P = p_i p_j. \tag{3}$$

In three of the modules, the output P is unused. The corresponding circuitry is therefore removed from the module. The modules are connected as shown in Fig. 9c to determine the carry for each bit. The sum bits are determined in the final stage as $s_0 = p_0$ and $s_4 = c_4$, and $s_i = p_i \oplus c_i$, $i = 1, 2, 3$.

The addition operation is completed in four clock cycles. Observe that every functional block requires only a single clock cycle by using compound gate structure. The major advantage of the proposed technology is simplicity. Unlike DSFQ [18] or NDRO-based clockless gates [11], the compound gates do not depend on the relative arrival time of the signals. Satisfying standard timing constraints, such as setup and hold time is therefore sufficient to ensure correct functionality. Counter flow clocking [6] approach is used to eliminate the risk of double clocking, while the risk of setup time violation is eliminated by adjusting the clock period. A total of 658 JJs are required to create the adder circuit. The correct

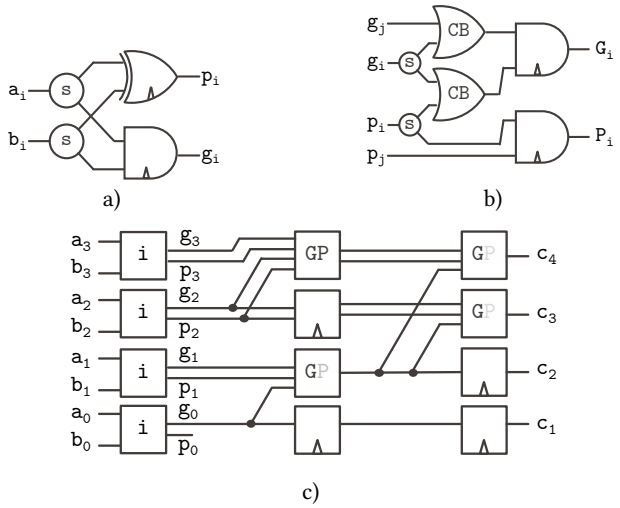

Figure 9: Carry lookahead adder structure. a) Initial processing block `i`, producing signals g_i and p_i. b) Main processing block `GP`. c) Adder topology. Grey `P` denotes the blocks where input p_i and output `P` are unused.

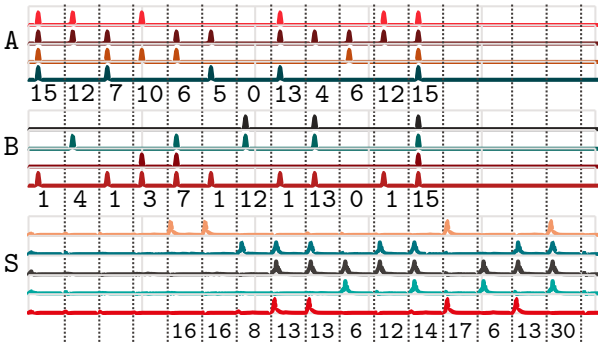

Figure 10: Simulation of CLA using compound gates at 16.4 GHz. Correct sum is determined in four cycles.

functionality of the circuit is evaluated using JoSIM [4] and the output for selected inputs is shown in Fig. 10. The maximum operating frequency of the adder is 16.4 GHz, yielding latency of 244 ps.

Due to different technology libraries, direct comparison of physical parameters, such as operating frequency or latency, is not representative. It is however possible to compare the number of JJs and the clock depth of the adder circuits. In [20], using conventional RSFQ logic cells, 4-bit CLA requires eight clock cycles. In [8], the conventional CLA requires 928 JJs and six clock cycles. With 658 JJs, the gate compounding technique therefore significantly improves the pipeline depth as compared to the regular RSFQ technology.

6 CONCLUSIONS AND FUTURE WORK

The large pipeline depth of the conventional RSFQ circuits is a major obstacle for the development of VLSI-complexity superconductive circuits. Path balancing DFFs and large splitter trees for clock signal distribution degrade the area and yield of the RSFQ integrated systems. Alternative solutions, such as clockless NDRO-based gates and DSFQ require careful timing analysis due to sensitivity to input arrival time. The gate compounding technique proposed in this paper efficiently combines multiple RSFQ elements into a single gate. The proposed methodology enriches the logic functionality realizable within a single clock cycle. The compound gates are not sensitive to relative input arrival time, greatly simplifying the timing analysis and logic synthesis. Novel two-input gates obtained using gate compounding, such as `NIMPLY`, exhibit bias margins and maximum frequency comparable to conventional two-input gates, such as `XOR`. The 4-bit carry lookahead adder realized using the proposed method operates at frequency of up to 16.4 GHz and exhibits superior delay and area as compared to an adder realized using the conventional logic cells.

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