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First developments towards producing inductive magnetic sensors using state-of-the-art photolithography techniques

Duccio Testa,[a,*] **Marcus Cemes,**[b] **Ambrine Douhane**[b] **and Florian Tanguy**[b]

[a] *Swiss Plasma Center (SPC), Ecole Polytechnique Fédérale de Lausanne (EPFL), CH-1015, Lausanne, Switzerland*
[b] *SPC & Center of MicroNano Technologies (CMi), EPFL, CH-1015, Lausanne, Switzerland*

E-mail: duccio.testa@epfl.ch

Abstract: Inductive magnetic sensors are needed for tokamak operation to provide the low-frequency (LF) measurements leading to the equilibrium reconstruction and to monitor the higher frequency (HF) instabilities; the HF magnetic sensors are often also used as a back-up to the LF ones. For the HF inductive magnetic sensors (fluctuation measurements), we need to minimize the self-inductance (L_{SELF}) provided that the effective area (NA_{EFF}) remains sufficiently large, typically requiring $L_{SELF} < 100\,\mu H$ and $NA_{EFF} \sim 0.01\,m^2$. For the LF inductive magnetic sensors (equilibrium reconstruction), the only physics-based design criteria are that of maximizing $NA_{EFF} > 0.10\,m^2$, essentially independently of the resulting L_{SELF}. Due to these rather different measurement specifications, it is quite the common case that different sets of LF and HF inductive magnetic sensors are used, which significantly complicates the R&D activities and the ensuing manufacturing processes.

Starting in 2007, our group at the Swiss Plasma Centre at the Ecole Polytechnique Fédérale de Lausanne (EPFL) has originally developed the Low-Temperature Co-fired Ceramic (LTCC) technology for producing inductive magnetic sensors, this technology being exceptionally suitable for operating temperatures up to ~1'000C in very harsh environmental conditions. The similarly named High-Temperature (HTCC) technology uses the same processes but different materials, and it is then suitable for operating temperatures up to ~1'600C. ITER will have about ~250 such LTCC sensors, of EPFL design and prototyped at the EPFL, but manufactured by a commercial entity to technical specifications lower than those achieved at the EPFL in terms of track width, track separation and overall manufacturing yields.

*Corresponding author.

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While state-of-the-art in 2007, the LTCC and HTCC technologies are now at least 20 years old and new processes have been developed for commercial applications, essentially based on different photolithography (PL) techniques. Recent, and already industrialized, advances in microfabrication using PL techniques offer the possibility to create more compact and optimized designs starting from current industrial standards, therefore extremely facilitating the very costly *lab-to-fab* step of production, namely all the activities that lead from the ideas in the lab to the actual (industrialized) fabrication. Our goal is to continue to push the frontier of magnetic sensors, bring a commercially viable design that can be used in tomorrow's scientific projects, such as nuclear fusion and astronomy/astrophysics (for instance, in the new generations of miniaturized satellites).

The main advantage of the PL techniques is that a much smaller track width ($dd1$) can be achieved, down from the routine $dd1 = 100$ µm of the EPFL LTCC sensors (for ITER: $dd1 = 400$ µm) to dd1< 10 µm. A smaller dd1 allows to pack more planar winding loops (m) enclosing a larger area over a smaller geometrical surface. Therefore, PL coils can have a lower self-inductance $L_{\mathrm{SELF}} \propto \mathrm{m}^2$ while having the same effective area $NA_{\mathrm{EFF}} \propto \mathrm{m}$ compared to coils manufactured by other more common technologies. Therefore, with PL techniques a similar design could be used for both HF and LF applications, the difference simply being the number of stacked-up layers (n) used to make-up the entire sensor.

In this paper we will present the first developments towards the production of inductive magnetic sensors using PL techniques. Whilst providing the possibility of designing better performing and more compact sensors, the introduction of PL techniques in the manufacturing processes for inductive magnetic sensors has uncovered new limitations and obstacles, such as the required vertical track thickness that is poorly suited for the existing deposition techniques, the need for stacking up multiple wafers and the connection between the sensor and the in-vessel cabling.

Keywords: Plasma diagnostics - probes; Si microstrip and pad detectors

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1 Introduction.

A major conceptual difficulty in the design of inductive magnetic sensors is the differentiation between equilibrium (low-frequency (LF), integrated) and fluctuation (high-frequency (HF), NOT integrated) measurements. While for the former an effective area $NA_{\mathrm{EFF}} > 0.10\,\mathrm{m}^2$ is typically needed, with the self-inductance L_{SELF} essentially un-important, for the latter L_{SELF} must be minimized to below $\sim 100\,\mu\mathrm{H}$ (depending on the length of the acquisition line and the acquisition electronics) but still with a sufficiently high $NA_{\mathrm{EFF}} > 0.01\,\mathrm{m}^2$. Then, different sets of LF and HF inductive magnetic sensors are used, which significantly complicates the R&D activities and the ensuing manufacturing processes.

Starting in 2007, our group at the Swiss Plasma Centre (SPC) at the Ecole Polytechnique Fédérale de Lausanne (EPFL) has originally developed and re-engineered the Low-Temperature Co-fired Ceramic (LTCC) technology [1] for producing inductive magnetic sensors adapted to the very harsh environmental conditions of the in-vessel side of a magnetically confined thermonuclear fusion device. The LTCC processing and results obtained with these inductive magnetic sensors are presented in refs. [2–9]. Figure 1 shows a 3D design of an LTCC magnetic sensor: multiple planar turns (m) are screen-printed on a ceramic substrate and then multiple layers (n) are electrically connected in series using vertical tracks (the vias). LTCC sensors of the EPFL design have been installed in FTU, WEST and TCV, and indeed one the many variants we prototyped was then finally chosen for industrialized manufacturing and installation in ITER.

The LTCC developments by our group at the EPFL had two main aims:

1) reduce the volume occupation of the inductive magnetic sensor, so that not only it becomes easier to fit it in the limited amount of space between the first wall and the tiles (or blanket) modules, but also all irradiation damages linked to volumetric effects are significantly reduced;

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2) by significantly reducing the size of the printed wire and the separation between the printed wires (respectively called track width (dd1) and separation (ss1) in the LTTC nomenclature, routinely achieving $dd1 = 100\,\mu m$ and $ss1 = 50\,\mu m$ for the EPFL prototypes) with respect to that of the ordinary Mirnov sensor (typically the wire diameter is 1 mm to 2 mm), it was hoped that the same baseline module could be used for producing LF and HF inductive magnetic sensors, the difference simply then being the number of stacked-up modules (n) connected in series to produce the two different sensors.

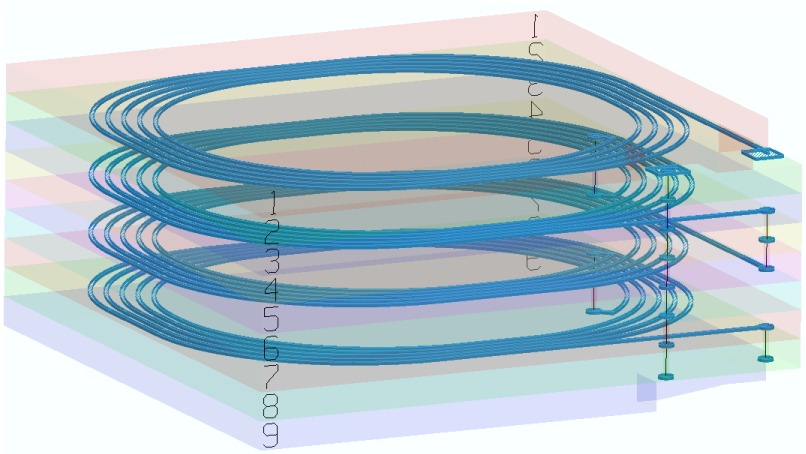

Figure 1. Overall 3D winding pattern of an LTCC/HTCC inductive magnetic sensor. The overall concept design is the same for a photolithography sensor, what changes is the materials used for the wafer and the metallic ink and the specifications (width, separation, thickness) of the tracks.

While the first aim was easily attained, so that the same NA_{EFF} could be achieved with a volume occupation for an LTCC sensor significantly below 1/10 of that needed for the equivalent Mirnov sensor (in turns giving a much lower L_{SELF} for the LTCC than that for the Mirnov sensor due to the smaller number of turns required to obtain the same NA_{EFF}), the second goal proved impossible to achieve due to the limited planar size of the sensor, typically 30 mm × 30 mm, and the minimal track width that could be processed, which is linked to the size of the droplet used for screen-printing such tracks.

As can be easily seen in figure 2 (reproduced from [2]), when many turns (all with the same $dd1 = 100\,\mu m = ss1$) are needed to obtain the desired NA_{EFF}, the inner-most turns on the same plane (= m) contribute significantly less to the effective area NA_{EFF} $(m \times n)$, while still adding to the self-inductance of the sensor $L_{SELF} \sim (m \times n)^2$. In this example, a sensor was built for each planar design always using $n = 4$ layers, and varying $m = [1, 5, 10, 20]$. The measurements for the effective area and self-inductance of these sensors are presented in table 1.

When comparing the different designs, we can easily remark that the ratio of the effective areas normalized by the number of planar turns rapidly decreases with m, namely the inner turns contribute much less to increasing NA_{EFF}. Similarly, the ratio of the self-inductances normalized by the square of the number of planar turns decreases with an increasing m as the inner turns capture less magnetic flux. However, overall L_{SELF} still increases significantly so that sensors having a sufficiently large NA_{EFF} suitable for the equilibrium (low-frequency) measurements, have a too large L_{SELF} to be also usable for the instabilities (high-frequency) measurements.

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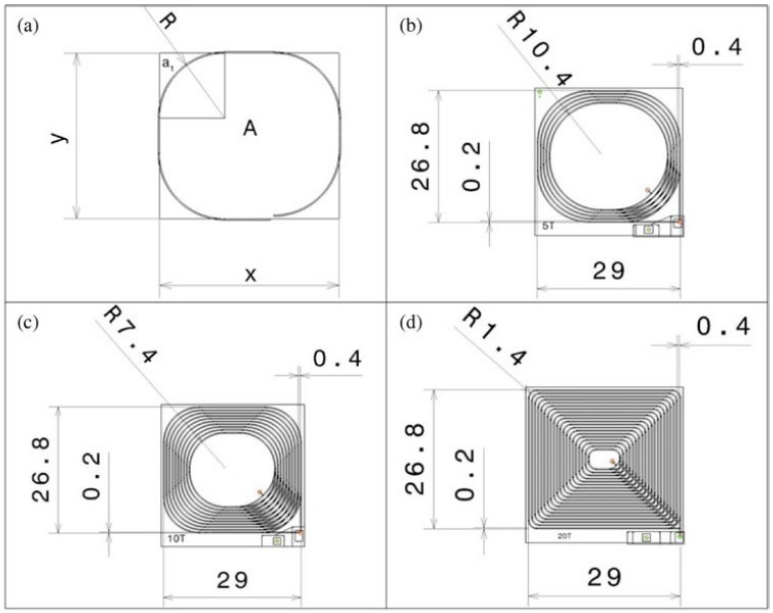

Figure 2. Four different prototypes of LTCC sensors designed at the EPFL, respectively with m=[1,5,10,20] planar turns on each layer, all with planar size 30 mm × 30 mm, $dd1 = 100\,\mu m$ and $ss1 = 50\,\mu m$. Note that the inner turns contribute progressively much less to the increasing $NA_{\rm EFF}$, while still contributing to the increasing $L_{\rm SELF}$.

Table 1. Measurement of the effective area and self-inductance for the four designs illustrated in figure 2 with $m = [1, 5, 10, 20]$ planar turns and always n=4 layers. All sensors are realized on a planar geometrical size 30×30 mm with the same $dd1 = 100\,\mu m = ss1$.

design type	m=1 (figure 2a)	m=5 (figure 2b)	m=10 (figure 2c)	m=20 (figure 2d)
$NA_{\rm EFF}$ [m^2]	0.0035	0.0135	0.0228	0.0317
$(NA_{\rm EFF}(m)/m)/NA_{\rm EFF}$ (m=1)	1.0000	0.7714	0.6514	0.4529
$L_{\rm SELF}$ [µH]	1.4235	31.7947	72.9578	140.4127
$(L_{\rm SELF}(m)/m^2)/L_{\rm SELF}$ (m=1)	1.0000	0.8934	0.5125	0.2466

The smaller track width and track separation that can be obtained with current state-of-the-art photolithography (PL) techniques allow to pack more planar turns capturing magnetic flux over a larger area keeping the same geometrical surface (S) of the substrate wafer. For a smaller $(dd1 + ss1)$, we can then achieve the same overall $NA_{\rm EFF} \propto S \times (n \times m_{\rm OPT})^{\alpha}$, but with a much smaller $L_{\rm SELF} \propto S \times (n \times m_{\rm OPT})^{2\beta}$ because the optimized value of the number of planar turns $m_{\rm OPT}$ would be smaller than the m which would be needed for a larger $(dd1 + ss1)$. Note that here both $\{\alpha, \beta\} < 1$ since some magnetic flux is lost through the turns as the windings are not fully packed in 3D. Therefore, *in principle* the same wafer design can be used for LF and HF inductive magnetic sensors, the former simply having more wafers stacked-up in series [10]. Labelling the surface enclosed by each turn as S_k, with $S_1 \leq S$ being the surface of the outermost turn, we have that $S_k/S_1 \rightarrow o(1)$ as $(dd1 + ss1)$ increases, while $S_k/S_1 = O(1)$ if $(dd1 + ss1)(H + W)/S_1 = o(1)$,

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where $\{H, W\}$ are the outer dimensions of the wafer. Formally, this can be stated as follows (L_1 being the perimeter of the outermost turn, and assuming here for simplicity $S_1 = S = H \times W$):

$$\frac{S_k}{S_1} = 1 - \frac{2(k-1)(dd1 + ss1)(H+W)}{HW} = 1 - (k-1)\frac{L_1(dd1 + ss1)}{S_1} \tag{1.1}$$

We can now explicitly consider this relation for $H = W = 40$ mm and three actual test cases:

a) the ITER LTCC sensors as produced by the selected commercial manufacturer, which has $dd1 = 400$ µm and $ss1 = 200$ µm;

b) the prototype of the ITER LTCC sensors as produced in-house at the EPFL, which has $dd1 = 100$ µm and $ss1 = 50$ µm, namely a much smaller track width and track separation;

c) one of our first prototypes for a PL sensor, with the typical PL specs $dd1 = 10$ µm and $ss1 = 5$ µm.

Table 2 show the values obtained from eq. (1.1) for these three test examples, always considering one single layer ($n = 1$) and multiple planar turns $m = [5, 20, m_{\mathrm{MAX}} \leq 100]$, where m_{MAX} is the maximum number of turns that one single layer can accommodate (capped to = 100 for the PL design). We straightforwardly note that the much smaller increase in effective area for an increasing number of planar turns of larger track width and separation implies that a lot more turns are needed on a single layer to make up the large $NA_{\mathrm{EFF}} > 0.10\,\mathrm{m}^2$ required for equilibrium sensors. Therefore, an optimal value $\mathrm{m}_{\mathrm{OPT}}$ cannot be found that allows to satisfy concurrently a sufficiently high $NA_{\mathrm{EFF}} \sim 0.01\,\mathrm{m}^2$ and a sufficiently small $L_{\mathrm{SELF}} < 10$ µH per layer even with the best LTCC design specifications realized @EPFL. These results then demonstrate that being able to produce inductive magnetic sensors using PL specs will allow to develop one single modular unit with a very low L_{SELF} and a sufficiently high NA_{EFF} suitable for the HF measurements, and then *multiply* this unit using an electrical connection in series (the vias as in the LTCC design) to obtain the sensor with the much higher NA_{EFF} suitable for the LF measurements.

Table 2. Analytical estimation of the effective area for three different designs for an inductive magnetic sensor, based on the ITER LTCC sensors and the first PL prototypes. Here S_1 is the nominal area of the outermost turn $S_1 = H \times W = 1.60 \times 10^{-3}$ [m^2].

design type	LTCC-ITER commercial	LTCC-ITER by EPFL	PL sensor by EPFL
max. number of m per layer	22	100	>200
S_2/S_1 (per layer)	0.9409	0.9851	0.9985
NA_{EFF} ($m = 5$) [m^2] (per layer)	$4.4270 \times S_1 = 7.0832 \times 10^{-3}$ [m^2]	$4.8517 \times S_1 = 7.7627 \times 10^{-3}$ [m^2]	$4.9850 \times S_1 = 7.9760 \times 10^{-3}$ [m^2]
NA_{EFF} ($m = 20$) [m^2] (per layer)	$10.8230 \times S_1 = 17.3168 \times 10^{-3}$ [m^2]	$17.2889 \times S_1 = 27.6622 \times 10^{-3}$ [m^2]	$19.7164 \times S_1 = 31.5462 \times 10^{-3}$ [m^2]
NA_{EFF} ($m = MAX$) [m^2] (per layer)	$11.1199 \times S_1$ (for $m = 22$)	$44.2197 \times S_1$ (for $m = 100$)	$92.7597 \times S_1$ (for $m = 100$)

This paper is organised as follows. Section 2 presents the main steps for the fabrication of inductive magnetic sensors using PL processes. Section 3 highlights the challenges and workable solutions towards the industrialization of the production processes we are currently performing R&D on. Section 4 shows the calculated electrical characteristics for some test examples of prototypes that we have produced. Section 5 shows the initial measurements of the electrical characteristics of a few different prototypes, highlighting the technical challenges that must be overcome to make accurately such measurements. Finally, section 6 presents the summary and the conclusions of our work.

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2 Fabrication steps for inductive magnetic sensors using PL process.

The design of a PL (inductive) magnetic sensors starts with preparing the *mask* for printing metallic tracks onto an electrically insulating wafer [11]. A chrome (Cr) mask is fabricated using a direct laser writer, using a machine-readable GDS schematic generated by our extensible C++ code, called *CoilDesigner*. The code is run interactively, allowing experimentation of generation parameters and calculation of the main electrical properties of the sensor (NA_{EFF}, L_{SELF}, and the self-resistance R_{SELF}) using simplified analytical formulas.

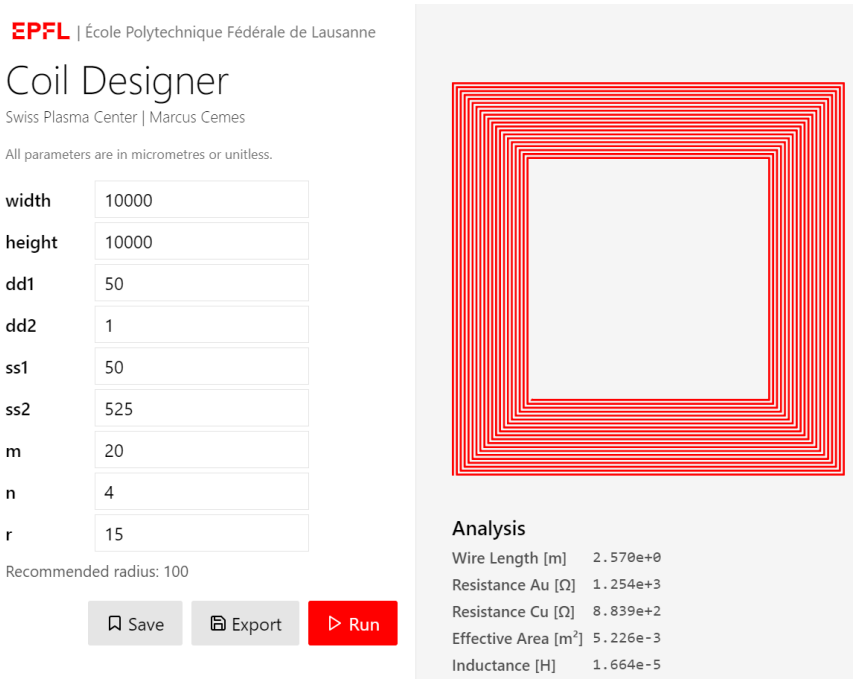

Figure 3. The design of one planar layer produced by our C++ code, already in machine-format for a much easier implementation. For clarity of viewing, here the design parameters are $H = 10\,\mathrm{mm} = W$, $dd1 = 50\,\mu\mathrm{m}$, $ss1 = 50\,\mu\mathrm{m}$, $dd2 = 1\,\mu\mathrm{m}$, $ss2 = 525\,\mu\mathrm{m}$, $m = 20$, $n = 4$, and $r = 15\,\mu\mathrm{m}$. Output values of the resistance for a gold (Au) and copper (Cu) ink are calculated, together with the effective area and the self-inductance.

A screenshot of our *CoilDesigner* program is shown in figure 3 during its run-time. The input parameters for our code are the essential design parameters for the sensor:

- $\{W, H\} \rightarrow$ the outer dimensions (W = width, H = height) of the sensor (units = [µm])
- $\{dd1, ss1, dd2\} \rightarrow$ the track width, separation, and thickness (units = [µm])
- $ss2 \rightarrow$ the wafer thickness (units = [µm]), $ss2 = 525\,\mu\mathrm{m}$ typically
- $m \rightarrow$ the number of planar turns over one wafer
- $n \rightarrow$ the number of stacked-up wafers
- $r \rightarrow$ the curvature radius of the tracks in the corners of the wafer (units = [µm])

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The results for the self-resistance, self-inductance and effective area are obtained analytically as follows, the main geometrical simplification being that the curvature radius of the turns is neglected in all calculations:

$$R_{\mathrm{SELF}} = \rho \frac{2(H+W)}{dd1 \times dd2} \tag{2.1a}$$

$$NA_{\mathrm{EFF}} = nm(HW) - 2n(dd1 + ss1) \times \left[(H+W) \times \sum_{1}^{m} (k-1) - 2(dd1 + ss1) \left(\sum_{1}^{m} (k-1) \right)^2 \right] \tag{2.1b}$$

$$L_{\mathrm{SELF}} = 4\pi\mu_0(1+\chi_R) \frac{nm \times NA_{\mathrm{EFF}}}{\sqrt{(2n \times ss2)^2 + NA_{\mathrm{EFF}}}} \tag{2.1c}$$

Here in eqs. (2.1) $\{\rho, \chi_R\}$ are the resistivity and magnetic permeability of the specific material used as ink, and μ_0 is the vacuum magnetic permeability. When checked against the full Finite Elements (FE) calculations reported in section-4, the analytical results of eqs. (2.1) do not typically differ by the FE results by more than 30% for L_{SELF}, and typically by less than 5% for R_{SELF} and by less than 10% for NA_{EFF}.

Figure 4 shows the design of a mask with multiple designs for PL test prototypes screen-printed on it. Figure 5 then shows the actual Cr mask produced with these multiple designs. Multiple designs can be implemented on one single mask to assess different prototypes, and the same mask can also be reused multiple times if it does not sustain damage during the actual processing of the wafers.

The fabrication of a PL (inductive) magnetic sensor involves different processing steps [11], the usual commercial nomenclature for this ensemble of operations being a *process flow*. The different steps and a simplified description are presented in table 3 below, which is also complemented by the corresponding step-by-step figures. The colour coding for the materials are as follows: **grey** = Si (can be doped, thus conductive, or amorphous, thus already insulating); **light blue** = SiO_2 (the insulating layer): **red** = the (often organic) photoresist; **gold** = the Au metallic ink used for the tracks.

Figure 6 then shows an example of one the first printed wafers, using the mask shown in figure 5. This wafer has various processing defects and this allows to illustrate directly and visually some of the challenges we are facing towards the commercial industrialization (the so-called *lab-to-fab* step) of the processes we are re-engineering or entirely developing anew in the CMi facilities at the EPFL.

While the PL processes are very well industrialized for commercial applications in not-harsh operating conditions, the materials and the chemistry used to produce the printed wafer are somewhat problematic for the harsh environmental conditions to which the in-vessel components of a magnetically confined thermonuclear fusion devices are subjected to. A summary of the main materials used with the PL processes is provided below:

- **substrate**: SiO_2 or un-doped Si with SiO_2 layer deposition, this is currently the most-used industrial standard; while SiO_2 is acceptable for TCV and DTT, it is not yet entirely clear if this material will be acceptable in forthcoming fusion devices such as DEMO-EU;
- **substrate**: synthetic Sapphire is relatively widely used in the PL industry essentially for bio-medical applications, and might be preferred in DEMO-EU as it becomes transparent to microwaves when sufficiently cooled so that a temperature runaway is prevented; *swelling might a problem for such wafers under the DEMO irradiation conditions;*

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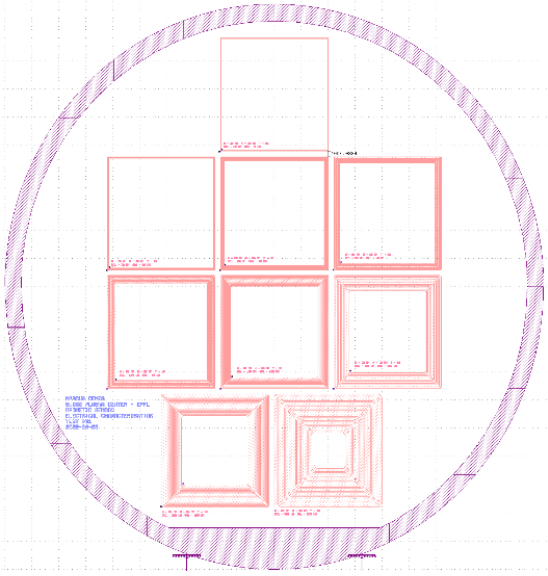

Figure 4. Here nine different designs are produced on one single mask, to then be printed on a single wafer. The number of turns/layer increases from $m = 2$ (top design) to $m = 10$ (bottom right design); the track width varies between $dd1 = 10\,\mu\text{m}$ (top design) to $dd1 = 100\,\mu\text{m}$ (bottom right design), with track separation $ss1 = dd1/2$ always, i.e. varying between $ss1 = 5\,\mu\text{m}$ and $ss1 = 50\,\mu\text{m}$.

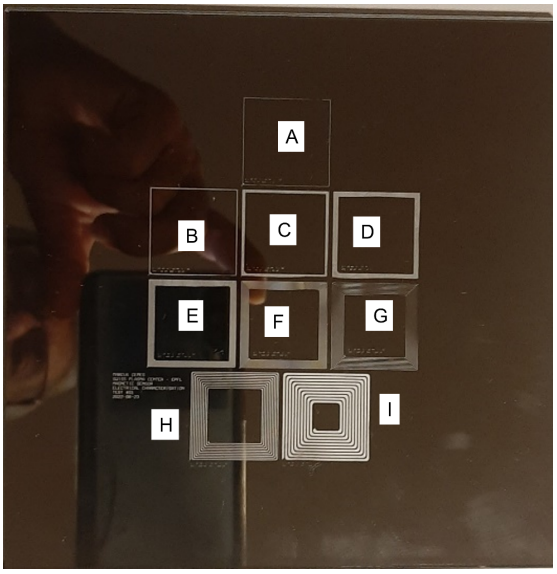

Figure 5. The corresponding mask laser-printed on the Cr substrate used for processing the wafers with Au tracks. Different designs are printed using a variety of combinations of values for $\{m, dd1, ss1\}$, ranging from type-A with $\{m, dd1, ss1\} = \{2, 10\,\mu\text{m}, 5\,\mu\text{m}\}$, i.e. the smallest track width and separation, to type-I with $\{m, dd1, ss1\} = \{10, 100\,\mu\text{m}, 50\,\mu\text{m}\}$, i.e. practically reproducing an LTCC design using PL techniques.

- **substrate**: other glass-type and quartz-type materials, such as those based on Boron-Nitride or Zirconium-Oxide compounds, are possible but are not yet a routinely used industrial standard;
- **conducting tracks**: Au as metallic ink, could also use Ag for high electrical conductivity; *these are high-ambient-temperature inks which are usable if the maximum in-vessel temperature at the position of the sensor cannot be kept below 400deg in steady state operating conditions (which would also include baking and glow-cleaning discharges);*
- **conducting tracks**: for higher electrical conductivity, and for similar high operating temperatures >400deg, Cu is also a routinely used industrial standard, but glidcop, namely the most fusion-relevant variant of Cu used for in-vessel components, is not;
- **conducting tracks**: for higher electrical conductivity and if the operating temperature can be kept well below ~400deg, Al becomes a valid low-ambient-temperature alternative ink as it is routinely commercially available;
- **adhesive ink-to-wafer**: the best adhesion is typically obtained industrially using an intermediate layer of Cr or Ti ~50–100 nm thick; this quantity of high-Z materials may be too big for in-vessel components in thermonuclear fusion devices in case of out-gassing, and therefore

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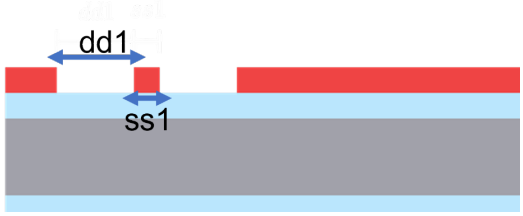
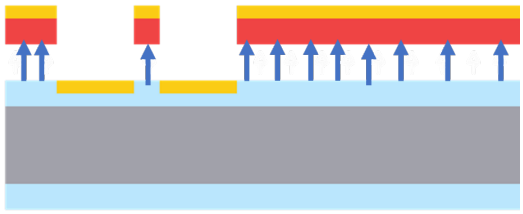
Table 3. The main fabrication steps for (inductive) magnetic sensors produced using PL processes.

	**PHOTORESIST COATING** A commercial (often organic) photoresist is uniformly spread onto an Si wafer (with SiO_2 layers on both sides of it) to a thickness of just a few µms, by spinning at high speed.
	**EXPOSURE & DEVELOPMENT** The photoresist is exposed under UV light using a reusable mask, and then developed to remove unwanted regions and uncover the underlying SiO_2 layer onto which the metallic tracks can then be deposited.
	**ETCHING** The *visible* part of the SiO_2 layer can then be partially removed using anisotropic etching techniques, such as dry etching. Isotropic techniques, such as wet etching, are also possible for certain materials using specific machines.
	**METAL EVAPORATION** A metallic conductor of choice, such as Au, is evaporated in a strong vacuum to ensure a long mean free path, and therefore minimal deposition on the photoresist sidewalls. With this process the track thickness is then limited to 1–2 µm. A negative photoresist is also preferable as the sidewalls lean-in for an easier lift-off.
	**LIFT-OFF** The photoresist is removed by a solvent in an ultrasound bath, taking along with it the unwanted areas of deposited metal. The resulting wafer contains conducting tracks embedded within a dielectric layer, ready for another coil layer to be deposited.

the wafer-to-ink adhesion process and chemistry has been completely re-engineered in-house to be able to only use a 10 nm-thick layer of Cr or Ti. See for instance the incomplete winding patterns on some of the test prototypes shown in figure 6: this manufacturing defect was specifically due to having used a too small Cr adhesion layer, only 5 nm-thick.

Finally, we have addressed the question of the assembly of multiple wafers inside a suitable holder. Four printed Au circuits of size 30×30 mm have been diced from a fully printed SiO_2 wafer board (which contains 12 such circuits), stacked-up and assembled into a stainless-steel (non-ferromagnetic) holder, as shown in figure 7. This holder has three guiding M4 pins to attach a protection cover (also stainless-steel): these pins can then manually or machine-guided into position using a compression system to avoid damaging the wafers. This system can also be thermally controlled to improve

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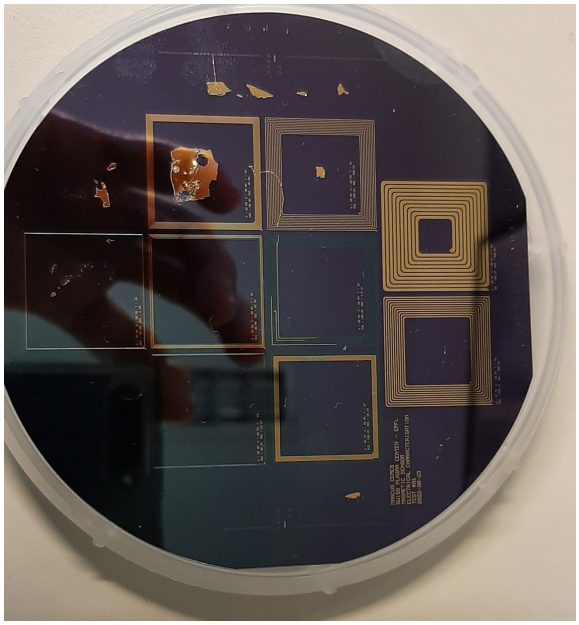

Figure 6. An SiO_2 wafer printed with Au using the multiple winding patterns on the Cr mask shown in figures 4, 5. Note some processing defects, essentially due to a problematic lift-off of the organic photoresist and the ensuing cleaning of this material. These defects have now essentially been corrected by re-engineering in-house the lift-off and cleaning processes, with expected considerable economic and temporal savings during the commercial *lab-to-fab* step of industrialization. For instance, the visible bad adhesion (incomplete winding pattern) of some of the gold tracks on the SiO_2 wafer is due to having used a too small Cr layer, 5 nm thick compared to the usual industrial standard of 50 nm. Now a Cr layer 10 nm thick is used, and the bad adhesion problem has been solved, which has significantly reduced the amount of unwanted high-Z material in the assembly compared to what would have been the case had the current industrial standards not been revisited.

wafer-to-wafer adhesion. This sensor-holder assembly has been designed for installation in DTT but is also compatible with the size requirements for a 3D sensor assembly in DEMO, where 3× such holders will be needed inside the same cavity in the blanket modules. *This assembly is currently used to check the correct vertical alignment between multiple wafers (the wafers are just stacked-up, not yet electrically connected in series) and the fact that no damage occurs when the wafers are inserted and extracted multiple times from the holder. The gap visible at the top of the left frame of figure 7 show the spacing where the connecter to the in-vessel cabling will be mounted.*

3 Challenges and workable solutions for industrializing the production of PL inductive magnetic sensors

As evident from the process flow and the materials/chemistry discussion presented above, we are facing various challenges towards the commercial industrialization of the PL processes we are developing in-house at the CMi facilities at the EPFL. The most important challenge is that the entire sensor assembly must be able to withstand up to 600 C and the associated cyclic stresses caused by thermal dilatation in the very harsh in-vessel environmental conditions of a fusion device: high vacuum, extremely high radiation fluxes, neutron and γs irradiation, . . . just to name the most

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Figure 7. The sensor-assembly prototype, on the left without cover so as to show the circuits, on the right with the cover and the three guiding M4 pins. One of the sides of the holder is open to allow for the mounting of the ICB connector to the in-vessel cabling, which is currently being prototyped.

important ones. Table 4 below provides an illustrative summary of the main challenges we are facing and the viable solutions we are exploring.

We believe that all these challenges can be met, so that the R&D process can be sufficiently accelerated and thus significantly reduce the unavoidable *lab-to-fab* costs related to the commercial industrialization of these processes. The manufacturing risks can therefore be reduced by various innovative solutions that can be prototyped rapidly and at a very low-cost at the CMi facilities at the EPFL.

4 Estimated electrical characteristic of PL inductive magnetic sensors.

To estimate the electrical properties of the PL inductive magnetic sensors, we have further developed the 1D variant of the algorithm used to model the LTCC sensors [2, 9]. This algorithm calculates the nominal electrical characteristics of the sensor given its outer dimensions, the track specifications (width, thickness, separation) and the materials: effective area NA_{EFF}, self-inductance L_{SELF}, self-resistance R_{SELF}, resonant frequency f_{RES}, effective bandwidth γ_{RES}. The analytical calculations are supplemented by a Finite Elements (FE) analysis solving for the magnetic field induced in the sensor by a nominal current in the winding loops. The FE analysis is very time-consuming, requiring a 3D spatial resolution better than $\sim 1/10$ of the winding separation to reach numerical convergency, as illustrated in figure 8.

When convergence is reached in the FE algorithm, the results are typically close to the analytical values within ±30%, and at worst (very small track separation $ss1 \leq 5\,\mu\mathrm{m}$ with $ss1 \sim dd1$, $ss2 \geq 500\,\mu\mathrm{m}$, $m \geq 20$, $n \geq 10$) the difference between the analytical and FE results is still within a factor ~2. We are currently developing a more sophisticated meshing algorithm to improve the numerical performance of the FE algorithm. Looking in details at the results presented in figure 8, the analytical results are compared with the full FE and simplified FE values, the latter obtained if the variation in the surface enclosed by the inner turns is negligible compared to the surface of the outermost turn, namely $(S_k\text{-}S_{k-1}) \ll S_1$. The full and the simplified FE values for L_{SELF} are

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Table 4. An illustrative summary of the main challenges we are facing and the workable solutions we are exploring towards the commercial industrialization of the PL processes we are developing in-house at the CMi facilities at the EPFL for producing inductive magnetic sensors using PL techniques.

CHALLENGES	POSSIBLE SOLUTIONS
substrate-1: SiO_2 or un-doped Si may not be suitable for the fusion environment: thermal radiation, neutrons, γs and microwaves	**substrate-1**: testing less commonly industrialized materials such as synthetic Sapphire (un-doped) is possible @CMi; other glass-type and quartz-type materials also commercially available but cannot currently be assessed @CMi
substrate-2: synthetic Sapphire is suitable for the fusion environments (the remarkably similar synthetic diamond is used for the plasma facing windows of microwave systems), but is more difficult to process and is a well-developed industrial standard only for bio-medical applications	**substrate-2**: microwaves testing using the Falcon & the T-rex facilities at the SPC, neutronic testing using the DD & DT neutrons and γs irradiation facilities at ENEA Frascati (FNG facility [12]) and University of TorVergata (Calliope facility [13]), both in Italy
thickness of conducting tracks: limited to $< 2\,\mu$m using current sputtering and/or evaporation techniques; this gives a rather high sensor' self-resistance $R_{\mathrm{SELF}} \sim 10\,\mathrm{k}\Omega$ for the LF inductive sensors; the main difficulty is the introduction of heat, which can introduce stress in the film from thermal dilatation	**thickness of conducting tracks**: a) if certain environmental constraints could be relaxed, Cu and Al can be used and $ss1 = 5\,\mu$m can be achieved @CMi; b) *inversed* sputtering and/or evaporation by carving tracks into the wafers instead of depositing, can be tested @CMi; c) growing alternate insulating & conductive layers to build-up track thickness, can be tested @CMi; d) electro-plating process can easily produce thicknesses $>10\,\mu$m, cyanide solutions must then be cleaned-up; *the electro-plating process is being explored with a specialized Swiss-based company and is currently being re-established @CMi*
adhesive ink-to-wafer: Cr layer should be reduced and possibly removed completely for compatibility with the fusion environment	**adhesive ink-to-wafer**: Cr layer reduction has been assessed @CMi, then lift-off processes must be re-engineered and optimized: *are μgr of unwanted materials fully encapsulated in the assembly really still such a major problem?*
multiple layers-1: stacking multiple wafers is not a current industrial standard; punching & uniformly filling vias through the wafers is also complex (minimum vias diameter $>100\,\mu$m with ink-jet printing)	**multiple layers-1**: a) punching vias using femtosecond lasers or micro-sabling, *canNOT be done @CMi but only by specialized Swiss-based companies*; b) filling vias using ink-jet printing or micro-metric metal pins, can be done @EPFL
multiple layers-2: *coil stacking* technique whereby multiple layers are grown over the same substrate by alternating conductive and insulating deposition is limited to $\sim 10\,\mu$m	**multiple layers-2**: *coil-stacking* process (in-house CMOS development) is being developed at CMi; main advantage: punching vias will not be needed
assembly of stacked-up wafers: the multi-wafer package must be inserted into a holder as the wafers cannot withstand direct brazing and/or threading of (micro-)bolts for in-vessel installation	**assembly of stacked-up wafers**: a multi-wafer stainless steel holder has been designed & prototyped at the SPC
connection to in-vessel cabling: industrial wire-bonding techniques are not suitable (wire is $<\mu$m thick), direct brazing or cold Electron Beam Welding (EBW) also not suitable (wafer is extremely sensitive to very localized thermal stresses), standard anodic bonding does not work for the required metal-to-glass sintering	**connection to in-vessel cabling**: using proprietary Impulse Current Bonding (ICB) techniques and connectors [14], *design being developed by a specialized Swiss-based company*; cold EBW could be used (a fusion welding process where a beam of high-energy e^- is applied to join two materials)

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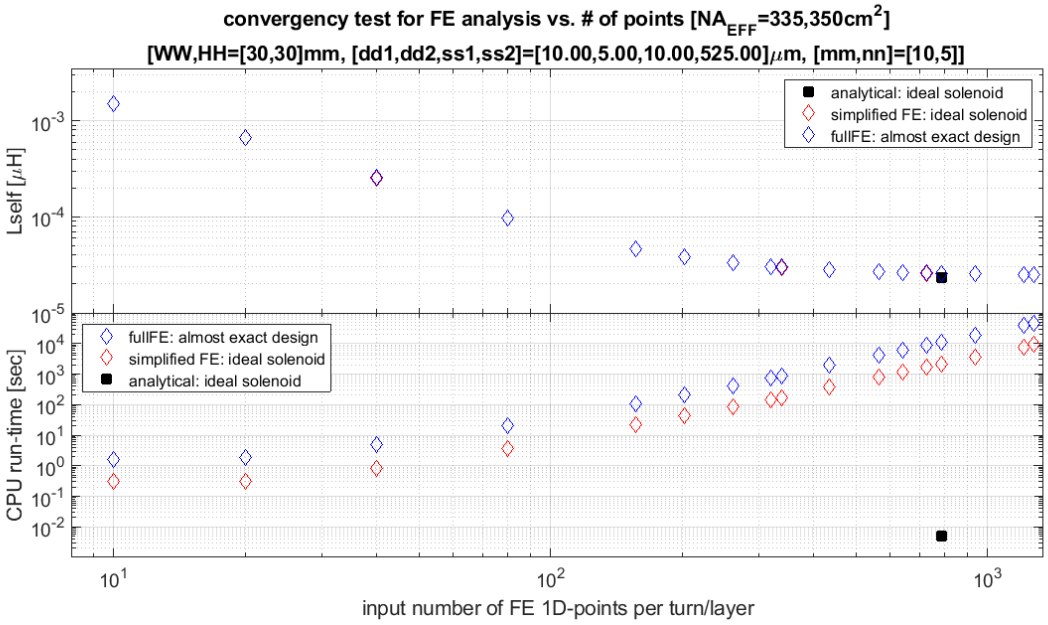

Figure 8. Convergency test for the FE algorithm as function of the input number of FE points. Numerical convergency is obtained when the 3D spatial resolution is typically O(ss1/10), and at numerical convergency, both FE (full and simplified) values are remarkably close to the analytical ones, within 30%. The FE computational time is at least 10^6 times larger, and the full FE analyses are approximately *10% to 30%* more computational expensive than the simplified ones. Two values are provided for $NA_{\rm EFF}$, the first from the FE analyses (the full and simplified ones having essentially the same value within <3%), the second from the analytical calculation, which does not include the curvature radii of the windings: thus the latter value is approximately ~5% larger than the first.

essentially similar for this case of $\{dd1 = 10\,\mu\text{m}, ss1 = 5\,\mu\text{m}, m = 10, n = 5\}$, and the computational time is slightly lower for the simplified FE analyses. At numerical convergency, both FE values are remarkably close to the analytical one, within 30%, but the FE computational time is at least 10^6 times larger. This indicates that a PL inductive sensor, with $dd1 = 10\,\mu\text{m}$ and $ss1 = 5\,\mu\text{m}$, and a moderate value for m, such that indeed $(S_k\text{-}S_{k-1}) \ll S_1$, is very close to a quasi-ideal solenoid, for which the analytical results presented in eqs. (2.1) hold true but for having neglected the curvature radii of all the windings (which is conversely included in the FE analyses). Following the comparison between the FE analyses and the analytical calculations, we are now confident that we can use the (much faster to obtain) analytical results to predict the electrical properties of the PL sensors, and only benchmark these predictions using the (much slower to obtain) FE calculations for a final verification on a few nominal test cases.

Figure 9 and figure 10 then show the calculated frequency-dependent impedance for two test prototypes using the same design specs, aiming for a sufficiently good high frequency response and a sufficiently large $NA_{\rm EFF} \sim 350\,\text{cm}^2$, but produced with different materials for the wafer (SiO_2 vs. synthetic Sapphire) and the metallic ink (Au vs. Pt). For a PL sensor with Au ink on an SiO_2 wafer, the self-inductance is $L_{\rm SELF} \sim 12.5\,\mu\text{H}$, the DC resistance is $R_{\rm SELF} \sim 100\,\Omega$, and the self-resonance is found at $f_{\rm RES} \sim 25\,\text{MHz}$. For a PL sensor with Pt ink on a sapphire wafer, we find $L_{\rm SELF} \sim 25\,\mu\text{H}$, $R_{\rm SELF} \sim 1\,\text{k}\Omega$, and the resonance is at $f_{\rm RES} \sim 5\,\text{MHz}$. These differences are simply due to having

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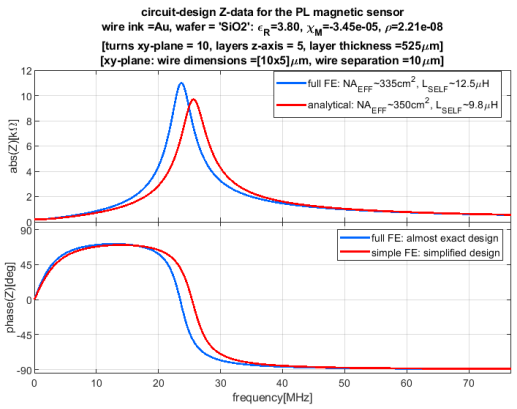

Figure 9. The calculated impedance for a PL sensor with Au ink on an SiO_2 wafer, designing the sensor for HF measurements.

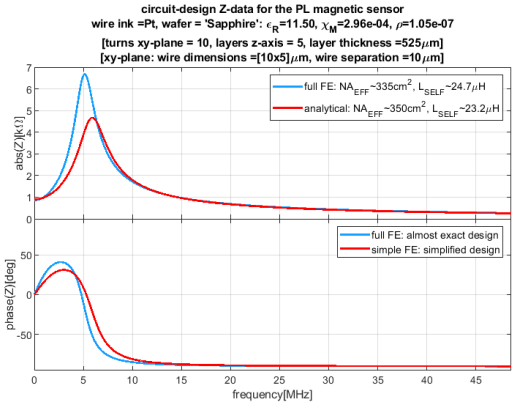

Figure 10. The calculated impedance for a PL sensor with Pt ink on a sapphire wafer, with the same design parameters as in figure 8.

used different materials for the sensor, as the geometry and the full FE calculations are the same.

5 Initial measurements of the electrical characteristics of the PL test prototypes.

The initial electrical characterization of the PL test prototypes took place at the Laboratoire d'Actionneurs Intégrés (Microcity Neuchatel, CH) using the Agilent 4294A Impedance Analyzer. This instrument works by matching the measured impedance to a pre-determined equivalent circuit, selected between different possible options. Theoretically, the sensor has an equivalent circuit with a resistor R_{SELF} in series with an inductor L_{SELF}, linked to a parasitic resistor due to the isolation of the wafer in parallel with a capacitor, as shown in figure 11. The approximate theoretical values of the components, depending on the material for the wafers and the metallic ink, as shown in figure 9 and figure 10, are $R_{\mathrm{SELF}} \sim O(k\Omega)$, $L_{\mathrm{SELF}} \sim O(\mu H)$, $R_{\mathrm{ISOL}} \sim O(\mathrm{M}\Omega)$, $C_{\mathrm{SELF}} \sim O(\mathrm{pF})$.

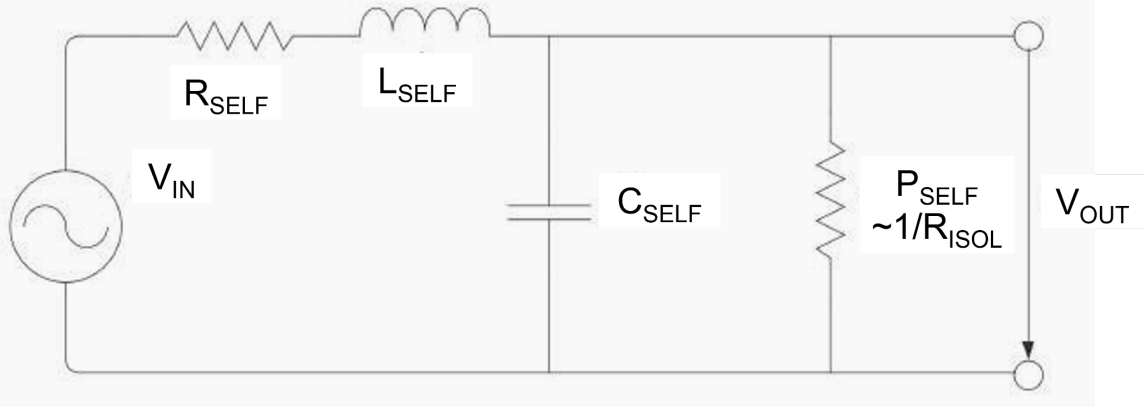

Figure 11. Equivalent circuit model for an inductive magnetic sensor; here $P_{\mathrm{SELF}} \sim 1/(R_{\mathrm{ISOL}} + i\omega L_{\mathrm{ISOL}})$ is the (possibly frequency-dependent) parallel admittance of the circuit, which may also include an inductive component, particularly for a long cabling to GND, in addition to a pure isolation resistance.

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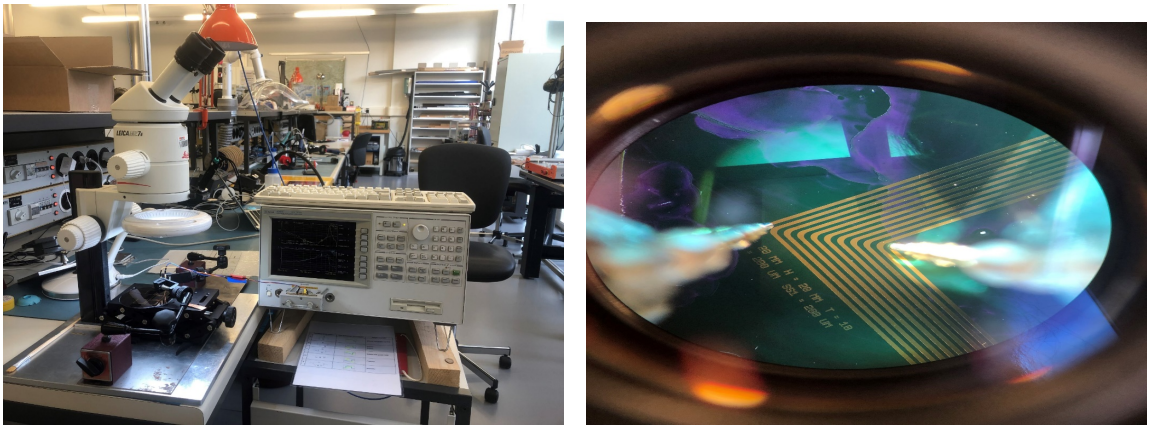

Figure 12. The setup used for the electrical characterization, composed of: (a) two conductive tips (50 µm broad, visible in the zoomed figure on the right), which are then often much broader than the sum of the track width and track separation, (b) two electrical wires for connecting the tips to the analyzer; (c) a ×5 optical microscope for checking the positioning of the tips on the tracks; (d) a lamp for illuminating the setup assembly; (e) a carrier translating in the z direction.

The setup used for the electrical measurement is shown in figure 12. The main elements of the measurement setup are a set of two conductive tips (50 µm broad), which are then often much broader than the sum of the track width and track separation, and two electrical wires for connecting the tips to the analyzer. The test prototype being measured in figure 11 is the type-I in figure 5, with $\{m, dd1, ss1\} = \{10, 100\,\mu\text{m}, 50\mu\text{m}\}$, namely the one with the largest track width and separation, which are just compatible with the size of the tips. With the available instrumentation the tips are manually guided to make the connection with the printed circuit, and it has proven very problematic to correctly achieve such a precise connection without an optically controlled guidance system. In turns, this makes some of the measurements currently unreliable or simply impossible to make, for instance those for the test prototypes with $dd1 = 10\,\mu\text{m}$.

The goal of the measurement is to obtain the complex impedance $Z_{\text{MEAS}}(\omega)$ with its modulus as well as its phase as function of a varying frequency ω. Knowing this information, R_{SELF}, L_{SELF}, C_{SELF} and R_{ISOL}, all as defined earlier, can be found using the machine own software by imposing the circuit model shown in figure 11. Based on the equivalent circuit of figure 11 and by trivial computation [2, 9], $Z(\omega)$ is given by:

$$Z_{\text{MEAS}}(\omega) = \frac{R_{\text{SELF}} + i\omega L_{\text{SELF}}}{1 + (R_{\text{SELF}} + i\omega L_{\text{SELF}})(P_{\text{SELF}} + i\omega C_{\text{SELF}})}. \tag{5.1}$$

These measurements were however only partially successful as the internal software of the impedance analyzer could not find an equivalent circuit matching that shown in figure 11, and thus could not directly give the values of $\{R_{\text{SELF}}, L_{\text{SELF}}, C_{\text{SELF}}$ and $R_{\text{ISOL}}\}$ in all selectable frequency ranges. An example of the measurements is shown in figure 13 in the frequency range between 1 MHz and 100 MHz for a test prototype with Au tracks on a SiO_2 wafer with $dd1 = 20\,\mu\text{m}$, $ss1 = 10\,\mu\text{m}$, $dd2 = 800\,\text{nm}$, $n = 1$, $m = 40$. By manually fitting the data and assuming $R_{\text{ISOL}} = 1\,\text{M}\Omega$, we obtain $R_{\text{SELF}} \sim 1.6k\,\Omega$, $L_{\text{SELF}} \sim 5.6\,\mu\text{H}$ and $C_{\text{SELF}} \sim 1\,\text{pF}$: the values for R_{SELF} and L_{SELF} are indeed consistent with those obtained from the analytical and FE calculations for this prototype.

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The reasons for the failing of the internal software of this instrumentation remain unclear, and this has prompted us to look for a different measurement setup and a different instrumentation to obtain a correct electrical characterization of our test prototypes. A new AC high-precision impedance analyzer will become available at the CMi from May 2023 with optically guided translating tables and very thin probes, which should be suitable for measuring the circuits even with the smaller track widths. In the meantime, we have proceeded with DC resistance measurements using the MPI TS150 Prober Station. This DC analysis only gives a value for R_{SELF}, which is however a good starting point. The measurement is performed by applying a DC voltage U in the range from −500 mV to +500 mV and sensing the induced current I, which is limited to 100 mA. The resulting resistance R_{SELF} is simply found using Ohm's law $R_{\mathrm{SELF}} = U/I$. The measurements obtained for one test prototype are shown in figure 14 and indicate a DC resistance $R_{\mathrm{SELF}} \sim 1.2\,\mathrm{k}\Omega$, which is in line with our estimations.

To solve the problem of the connection between the tracks on the wafers and the measurement instrumentation a new approach is being developed and prototyped, whereby the different test sensors to be electrically characterized will be mounted on a PCB board printed with a suitable circuit towards standard-size output connection pads, much easier to access with standard instrumentation, The connection between the tracks on the wafer and the tracks on the PCB will be made using wire bonding techniques, and needs to be optimized and correctly compensated so that the impedance of the sensors is measured, removing the effect of the PCB circuit.

6 Summary and conclusions

We have started the development towards the first prototypes of inductive magnetic sensors produced using photolithography processes. To significantly reduce the *lab-to-fab* costs, this work was performed at the EPFL at the Centre of MicroNano Technology (CMi), an European leader in the R&D for these PL processes. A most notable feature of this R&D activity is that it is a common project led by the EPFL Swiss Plasma Center and co-financed by different institutions to partially share the costs: the SPC at the EPFL for its TCV tokamak, the Consorzio DTT in Italy for their forthcoming tokamak being built in Frascati, and the Max-Planck-Institut für Plasmaphysik (IPP) in Garching for its ASDEX-U tokamak. DEMO-EU has also recently joined this R&D project for the 2023–2027 activities, *funded through EuroFusion*, in the framework of the Horizon 2027 EU programme.

The aim of this R&D work is to design better performing and more compact sensors, so that the same modular unit can be used for the HF measurements, and then as well for the LF measurements when adequately multiplied through a series connection. To this end, we have decided to use the current state-of-the-art PL technologies so that our fusion-oriented developments will be industrialized by already existing commercial partners with as minimal an effort as possible. By using processes and materials that are not too dissimilar from those currently deployed commercially, our fusion-led developments have also become of interest for other high-tech applications in harsh environmental conditions, even if not so harsh as those of fusion, such as miniaturized magnetic sensors for the next-generation of miniaturized satellites [15]. The development of a multi-layer connection scheme is also potentially useful for advanced biomedical applications, such as RNA multiplication for individualized cancer therapies studies [16].

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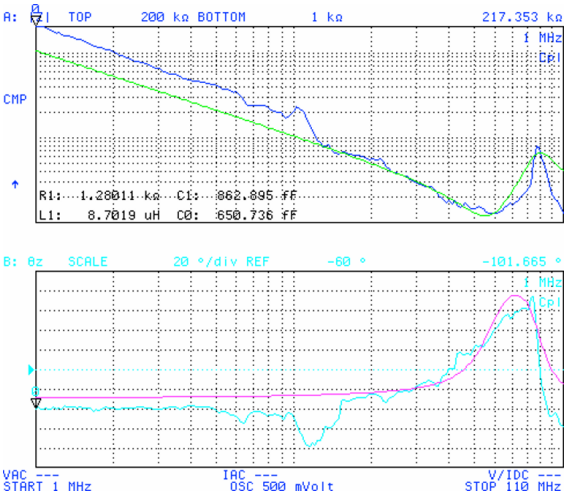

Figure 13. The measured impedance data (modulus on the top frame, argument on the bottom frame) for one test prototype with $dd1 = 20\,\mu\text{m}$, $ss1 = 10\,\mu\text{m}$, $dd2 = 800\,\text{nm}$, $n = 1$, $m = 40$. The internal software of the instrumentation finds an equivalent circuit which is different from the only acceptable one, shown in figure 10, since it has an additional capacitance (C0, while we should have C1). Therefore, the output values for $R_1 = R_{\text{SELF}}$, $L_1 = L_{\text{SELF}}$ and $C_1 = C_{\text{SELF}}$ are not to be trusted and only a manual fitting of the data using eq. (5.1) allows to determine R_{SELF}, L_{SELF} and C_{SELF}.

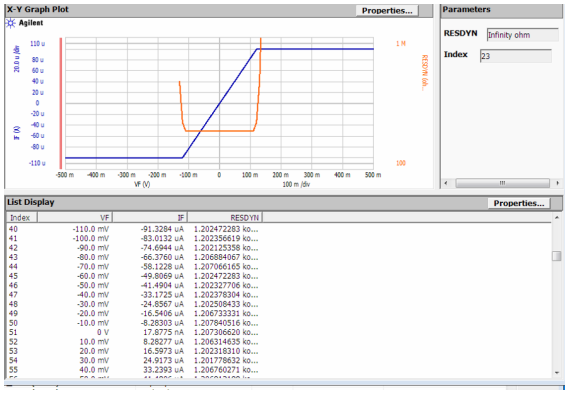

Figure 14. The measured DC resistance R_{SELF} obtained using the MPI TS150 Prober Station at the CMi. A very constant value of $R_{\text{SELF}} = U/I \sim 1.2\,\text{k}\Omega$ is obtained for U in the range between $-100\,\text{mV}$ and $+100\,\text{mV}$. For higher absolute values of the applied voltage U the instrumentation gets into its current limit at 100 mA and thus the R_{SELF} measurements cannot currently be obtained with this instrumentation.

Our most important result so far is that we have been able to produce circuits of different designs on SiO_2 wafers while optimizing and even often re-engineering most of the production processes towards eliminating those materials which are deemed to be unsuitable for the in-vessel conditions of a high-performance fusion device such as TCV, ASDEX-U, DTT (and DEMO). The achievements (highlighted in **bold**), and the current shortcomings (highlighted in *italic underlined*) of our developments that need further R&D work, can be summarized as follows:

1. **bring track width down to ~10µm from the 100µm of our routinely produced LTCC sensors**: essentially done → this increases the measurement performance (higher NA_{EFF} at lower L_{SELF}) while further reducing the sensor's size;

2. **analytical and numerical design rules developed starting from the design rules for the LTCC-1D sensors for ITER and TCV**: essentially done → as an example, with $1 \times (dd1 + ss1) = 600\,\mu\text{m}$ for the LTCC-1D sensors in ITER we can now easily have $\sim 20 \times (dd1 + ss1)$ for the PL sensors in DTT, hence a much lower $n \times m = N_{\text{TURNS}}$, thus for the same $NA_{\text{EFF}} \propto (N_{\text{TURNS}})^{\alpha}$ we achieve a much lower $L_{\text{SELF}} \propto (N_{\text{TURNS}})^{2\beta}$, with $\{\alpha, \beta\} < 1$;

3. **current and voltage capabilities of µm track size** → our calculations shows that eddy current and skin-depth effects do not become problematic, even at high frequencies ~MHz;

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4. *bring track thickness up to ~ 5 µm* → current industrial standard <1 µm gives too high a R_{SELF} in the order of the kΩ; a switch to the electro-plating processes is being prepared as the required equipment is being re-commissioned at the CMi @EPFL after a ~10 years gap to meet our requirements and in view of the possible applications for satellites and biomedical physics; *these processes will also be further developed in collaboration with Swiss-based commercial entities;*

5. *stack-up multiple wafers electrically connected in series* → the current industrial standard is single wafer processing, we thus need to develop and combine different techniques to build up multiple layers over multiple wafers and to obtain an electrical connection: build up multiple layers on the same wafer (*coil stacking*), punching and filling of vias to connected multiple wafers, *to be further developed in collaboration with Swiss-based commercial entities;*

6. *microwave and irradiation testing*: can these small tracks survive, and for how long, and if they do, do they keep the same electrical specs, and for how long? *To be assessed through tests in dedicated facilities;*

7. *electrical connection between the sensor and the in-vessel cabling*: cold Electron Beam Welding (EBW), or similar but proprietary techniques (ICB), *to be further developed in collaboration with Swiss-based commercial entities;*

8. *and additionally: could we combine inductive magnetic sensors with steady-state Hall sensors using the fact that the bottom side of the wafer is covered with an SiO_2 insulating layer onto which many state-of-art ceramic, glass-type or quartz-type materials could be bonded using ICB processes? Hall sensors for DEMO are currently set-up on a TPC platform, Electron-Beam-Laser etching will allow to go down to a wire size ~ µm from the ~mm currently used and thus make the production processed compatible with that of inductive magnetic sensors.*

Finally, it is worth remembering that whilst providing the possibility of designing better performing and more compact sensors, the introduction of PL techniques in the manufacturing process has uncovered new limitations and obstacles, such as the required vertical track thickness that is poorly suited for existing deposition techniques, the need for stacking up multiple wafers and the in-vessel sensor-cabling connection. Naturally, the economic viability for large-scale manufacturing of the design will also be a deciding factor, being dependent on the complexity of the manufacturing process.

Acknowledgments

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References

[1] Y.Imanaka, *Multilayered Low Temperature Cofired Ceramics Technology*, Springer (2005) [DOI:10.1007/b101196].

[2] D. Testa et al., *Prototyping a High-Frequency Inductive Magnetic Sensor Using the Nonconventional, Low-Temperature Co-Fired Ceramic Technology for Use in ITER*, *Fusion Sci. Technol.* **59** (2011) 376.

[3] D. Testa et al., *3D, LTCC-type, High-Frequency Magnetic Sensors for the TCV Tokamak*, in *Proceedings 28th Symposium on Fusion Technology (SOFT 2014 Conference)*, San Sebastian, Spain, 29 September – 3 October 2014.

[4] D. Testa et al., *3D, LTCC-type, high-frequency magnetic sensors for the TCV Tokamak*, *Fusion Eng. Des.* **96-97** (2015) 989.

[5] T. Maeder, C. Jacq and D. Testa, *LTCC and thick-film ceramic magnetic sensors for tokamak nuclear fusion*, in *EuroSensors 2016 Conference*, Budapest, Hungary, 4–7 September 2016.

[6] T. Maeder et al., *LTCC and Thick-film Ceramic Magnetic Sensors for Tokamak Nuclear Fusion*, *Procedia Engineering* **168** (2016) 646.

[7] D. Testa et al., *Manufacturing, Installation, Commissioning and First Results with LTCC-3D High-Frequency Magnetic Sensors on the Tokamak à Configuration Variable*, invited oral, *30th Symposium on Fusion Technology*, Giardini Naxos, Italy, 16–21 September 2018.

[8] D. Testa et al., *LTCC magnetic sensors at EPFL and TCV: Lessons learnt for ITER*, *Fusion Eng. Des.* **146** (2019) 1553.

[9] D. Testa, *Manufacturing, installation, commissioning, and first results with the 3D low-temperature co-fired ceramic high-frequency magnetic sensors on the Tokamak à Configuration Variable*, *Rev. Sci. Instrum.* **91** (2020) 081401.

[10] D. Testa, *Micro & Nano Technologies Ideas for DEMO: magnetic sensors*, in *Micro & Nano Fabrication Annual Review Meeting*, Ecole Polytechnique Fédérale de Lausanne, Lausanne, Switzerland, 3 May 2022.

[11] D. Testa, M. Cemes, A. Douhane and F. Tanguy, *Micro & Nano technologies ideas for DTT: Inductive Magnetic Sensors*, in *6th International Conference on Frontiers in Diagnostic Technologies (ICFDT6)*, Centro Ricerche ENEA Frascati, Frascati, Italy, 19–21 October 2022.

[12] A. Pietropaolo et al., *The Frascati Neutron Generator: a multi-purpose facility for physics and engineering*, *J. Phys. Conf. Ser.* **1021** (2018) 012004.

[13] S. Baccaro et al., *Calliope ^{60}Co gamma irradiation facility for space qualification at ENEA-Casaccia research centre (Rome)*, *Phys. Astron. Int. J.* **3** (2019) 94.

[14] S. Brun, *ICB technology — a novel assembly technology for the micromachining and semiconworld*, in *Chemnitz Seminar 2022*, Chemnitz, Germany, 22 June 2022.

[15] Swiss Space Centre @ EPFL and European Space Agency, private communications during informal meetings held in view of the Swiss Space Community Day 2023, https://espace.epfl.ch/event/space-community-days-switzerland-2023/.

[16] InnoSuisse initiatives, private communication during informal meetings held during the EPFL Engineering Industry Day 2023, see https://memento.epfl.ch/event/epfl-engineering-industry-day/.

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