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Ultra-Low Power Short-Range 60-GHz FMCW Radar Front-End

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Abstract

The millimeter wave (mm-wave) frequency bands have been increasingly attracting interest over the past years because they provide the opportunity to operate using large bandwidths which are not available at lower frequencies. They enable new communication standards supporting high data rates and enhance the performance of sensing applications. Radio detection and ranging (radar) systems benefit from multi-GHz bandwidth achieving a range resolution in the order of a few millimeters. The 60-GHz frequency band is one of the most used mm-wave bands because it is an unlicensed industrial, scientific, and medical (ISM) band from 57 to 66 GHz specifically for short-range devices (SRD). Another important advantage of operating at mm-wave is the miniaturization of passive components as antennas, which eases the possibility of adding several transmitter (TX) and receiver (RX) elements to build a multiple-input multiple-output (MIMO) radar.

Designing a high-resolution radar requires operating over a very wide band which intuitively would introduce more noise power. However, the previous statement does not correspond to the case of a frequency-modulated continuous-wave (FMCW) radar which shows a bandwidth compression at the baseband frequency. This is the main reason why FMCW is preferred over impulse radio ultra-wideband (IR-UWB). IR-UWB occupies a baseband bandwidth as large as its mm-wave bandwidth, thus demanding a high-speed ADC in the order GSps, increasing the total power consumption of the system. FMCW radars have been rapidly developing in recent years driven primarily by the automotive and industrial market, prioritizing high performance over low power consumption. Most of the commercial radar chips are not suitable for portable battery-powered or Internet-of-Things (IoT) applications because they consume several hundreds of mW or few Watts. The motivation of this work is to design a low-power low-cost fully integrated MIMO radar-on-chip (RoC).

This thesis explains the basic principles of FMCW radars and how to take advantage of autocorrelation in a radar system. Furthermore, the research focuses on low-power design at mm-wave for a 60-GHz radar front-end: TX and RX. These are the main blocks which usually dominate the power consumption in a MIMO scheme since several of them would be integrated. The TX and RX have a modular design, they are built as TX-RX slices with individual local oscillator (LO) buffers and transmission lines to facilitate the expansion to more MIMO

elements. The designed front-end was integrated with a PLL to have a complete solution. The proposed low-power mm-wave front-end is validated through two integrations, both fabricated in the GF 22-nm FDSOI process. The first chip includes a BPSK modulator on a 3-stage amplifier TX and a RX based on an active mixer-first architecture. The second chip optimizes the TX power consumption by merging functionalities into a power mixer, while the RX adopts a passive mixer-first architecture to further minimize power consumption. The final fully integrated 4-TX & 4-RX FMCW radar system reports a record low power consumption per virtual channel of 6.3 mW obtained by exploiting coupling mechanisms, band-tuning schemes, and matching network optimization for low output power. In the single channel configuration, the power consumption is 40.2 mW. Each TX-RX slice occupies only 0.4 mm × 1.25 mm and the total chip area is 2.5 mm × 1.25 mm, due to the extensive use of transformers for coupling stages and direct frequency synthesis at 60 GHz. A platform is built based on the proposed FMCW radar to demonstrate its sensing capabilities, it achieves a range resolution of 19 mm. The RoC shows a functional 60-GHz FMCW radar for short-range applications with the lowest power consumption and smallest form factor reported today.

Keywords: remote sensing, radar systems, FMCW radar, integrated RF tranceivers, millimeter-wave (mm-wave) integrated circuits, low-power tranceivers, power amplifiers, mixer-first.

Résumé

Les bandes de fréquence des ondes millimétriques (mm-wave) suscitent de plus en plus d'intérêt ces dernières années car elles offrent la possibilité de fonctionner en utilisant de larges bandes passantes qui ne sont pas disponibles à des fréquences plus basses. Elles permettent de nouvelles normes de communication prenant en charge des débits de données élevés et améliorent les performances des applications de détection. Les systèmes de radio pour la détection et la télémétrie (radar) bénéficient d'une bande passante multi-GHz atteignant une résolution de distance de l'ordre de quelques millimètres. La bande de fréquences 60 GHz est l'une des bandes mm-wave la plus utilisée, car il s'agit d'une bande industrielle, scientifique et médicale (ISM) sans licence de 57 à 66 GHz spécifiquement pour les dispositifs à courte distance (SRD). Un autre avantage important du fonctionnement en mm-wave est la miniaturisation des composants passifs telle que les antennes, ce qui facilite la possibilité d'ajouter plusieurs éléments émetteurs (TX) et récepteurs (RX) pour construire un radar à multiples entrées et multiples sorties (MIMO).

Concevoir un radar à haute résolution nécessite de fonctionner sur une très large bande qui introduirait intuitivement plus de puissance de bruit. Cependant, l'affirmation précédente ne correspond pas au cas d'un radar à onde continue modulée en fréquence (FMCW) qui présente une compression de bande passante à la fréquence de la bande de base. C'est la raison principale pour laquelle le FMCW est préféré à la radio à impulsions ultra large bande (IR-UWB). L'IR-UWB occupe une bande passante en bande de base aussi grande que sa bande passante en mm-wave, exigeant ainsi un ADC à haute vitesse dans l'ordre des GSps, augmentant la consommation d'énergie totale du système. Les radars FMCW se sont rapidement développés ces dernières années, principalement portés par le marché automobile et industriel, privilégiant les hautes performances à la faible consommation d'énergie. La plupart des puces radar commerciales ne conviennent pas aux applications portables alimentées par batterie ou Internet des objets (IoT) car elles consomment plusieurs centaines de mW voir quelques Watts. La motivation de ce travail est de concevoir un radar-on-chip (RoC) MIMO entièrement intégré à faible consommation et à faible coût.

Cette thèse explique les principes de base des radars FMCW et comment bénéficier de l'autocorrélation dans un système radar. De plus, la recherche se concentre sur la conception basse

consommation en mm-wave pour un radar front-end à 60 GHz : TX et RX. Ce sont les blocs principaux qui dominent généralement la consommation d'énergie dans un schéma MIMO puisque plusieurs d'entre eux seraient intégrés. Les TX et RX ont une conception modulaire, ils sont construits sous forme de tranches TX-RX avec des oscillateurs local (LO) individuels et des lignes de transmission pour faciliter l'extension à davantage d'éléments MIMO. Le front-end a été intégré avec une PLL pour avoir une solution complète.
Le mm-wave front-end à faible puissance proposé ici a été validé par deux intégrations, les deux puces ont été fabriquées dans la technologie GF 22-nm FDSOI. La première puce comprend un modulateur BPSK sur un amplificateur à 3 étages TX et un RX basé sur une architecture de mélangeur actif. La deuxième puce optimise la consommation d'énergie du TX en fusionnant les fonctionnalités dans un mélangeur de puissance, tandis que le RX adopte une architecture de mélangeur passif pour minimiser davantage la consommation d'énergie. Le système radar final entièrement intégré 4-TX & 4-RX FMCW enregistre une faible consommation d'énergie record par canal virtuel de 6.3 mW obtenue en exploitant les mécanismes de couplage, les schémas de réglage de bande et l'optimisation du réseau correspondant pour les faibles puissance de sortie. Dans la configuration à canal unique, la consommation électrique est de 40.2 mW. Chaque tranche TX-RX occupe seulement 0.4 mm × 1.25 mm et la surface totale de la puce est de 2.5 mm × 1.25 mm, en raison de l'utilisation intensive de transformateurs pour les étages de couplage et la synthèse directe de fréquence à 60 GHz. Une plateforme est construite sur la base du radar FMCW proposé pour démontrer ses capacités de détection, atteignant une résolution de distance de 19 mm. Le RoC montre un radar 60-GHz FMCW fonctionnel pour les applications à courte distance avec la plus faible consommation d'énergie et le plus petit facteur de forme rapporté aujourd'hui.

Mots-clés : télédétection, systèmes radar, radar FMCW, émetteurs-récepteurs RF intégrés, circuits intégrés à ondes millimétriques (mm-wave), émetteurs-récepteurs de faible puissance, amplificateurs de puissance, mélangeur d'abord.

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1 Introduction

1.1 Brief History of RADARs

Radio detection and ranging (RADAR or radar) systems have been around for over a hundred years and now they are finding their way into our daily life. Nevertheless, the idea itself of detecting objects using electromagnetic waves is almost as old as Maxwell theories. It was in 1886 when Heinrich Hertz proved that radio waves could be reflected by conducting bodies [1]. Then later, in 1903 a German engineer called Christian Hülsmeyer performed experiments in which he was able to detect ships and even obtained a patent the year later [2]. However, his results did not catch the attention of the German navy since the detection was barely better than that of a visual observer given the technology available at that time. Even the renowned Guglielmo Marconi failed to gain support for the idea of using radio waves for detection in the field of navigation [3].

While in Europe radar systems did not seem to cause interest for investing in further research, in the United States (US) its Naval Research Laboratory (NRL) began to realize about its capabilities for target detection in military applications. Continuous-wave (CW) radars were used in the early 1930s for detecting the presence of targets but the technology was not there yet for extracting the position accurately. This limitation was addressed by the development of the pulse radar which began in 1934 and started to show successful results almost two years later, it was initially able to detect a target up to 2.5 miles. The pulse radar was designed to operate at 28 MHz but the size of the antenna was considered prohibitively large for being used on ships. Given that the antenna size is inversely proportional to the operating frequency, the development of pulse radar at higher frequencies was desired by the NRL. It took only a few months to build and later in 1936 an improved 200-MHz pulse radar demonstrated range measurements up to 10-12 miles [1].

In the meantime as tensions intensified in Europe towards the war, the United Kingdom (UK) began to research into radars as an alert system against air attack. Although the UK started later than the US, the research and development went faster due to their fear and proximity to military conflicts. In the early 1935 an Scottish engineer, Sir Robert Watson-Watt, was

questioned about the idea of a death ray based on radio waves but he found it unfeasible at that time because of the amount of power required. Instead, he came up with the idea of using radio waves for detection of aircraft as an alternative to sonars which were used at that time with a range limited to approximately 20 miles. Already by February 1935 Watson-Watt had a working prototype based on communication equipment, by June he had built a pulse radar and demonstrated aircraft detection, and by March 1936 a radar system operating at 25 MHz was able to detect targets up to 90 miles proving to be superior to sonars. This technology led to the deployment of the Chain Home (CH) radar stations along the British coast and they played a key role in the battle of Britain and furthermore in the development of War World II.

Another major breakthrough for radars during the years of war was the cavity magnetron. Its development was a joint effort between the UK and US to improve the transmitted output power at higher frequencies. The US dedicated more effort on the research of microwave radars to benefit from a shorter wavelength for a better angular resolution. However, they lacked a high enough transmitting power source at those frequencies. On the other side of the Atlantic there were two scientists, John Randall and Harry Boot, that had invented a valve that could spit out pulses of microwave radio energy on a wavelength of 10 cm (~3 GHz)[4]. It was the cavity magnetron and it was able to produce about 1 kW output power, around 100 times larger than anything seen before. Unfortunately, due to the war the UK did not have the means to continue supporting the project and they offered the invention to US in exchange for financial and industrial help. By early 1941 it was already adapted for airborne radars and in mass production[4]. The cavity magnetron has been mentioned by many historians as the most important invention during the war and even of the 20th century. Its impact was so broad that even today a small version of the cavity magnetron can be found at home in microwave ovens.

Nowadays, radar systems have expanded to other fields apart from military applications such as meteorology, automotive, and even healthcare. The advances in wireless communication and the invention of the transistor led to the miniaturization of high frequency systems that today we can easily fit in a few centimeter devices. Although the war was a catalyst for technological progress, there are new challenges to facilitate the integration of electronics and improve our quality of life.

1.2 Overview of Radar Systems

Radar systems can significantly vary depending on the application for which they are designed. There are also different types of radars which can extract different types of information from a target depending on the requirements of the application. The basic principle of a radar is to illuminate a target using radiated electromagnetic energy and detect its reflection. Although radars can be very complicated and large systems, a simplified picture of a radar is shown in Fig. 1.1.

The basic blocks in a radar system are the following:

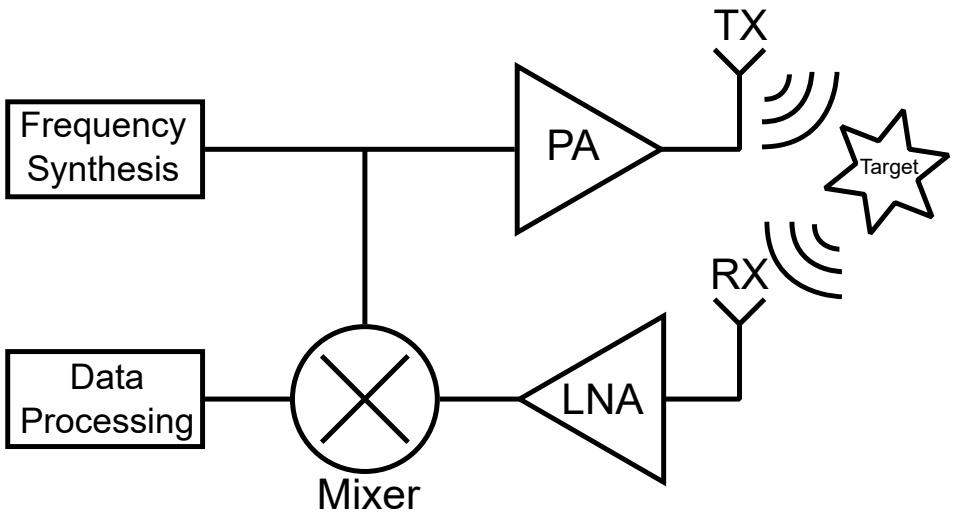


Figure 1.1: Simplified diagram of radar.

- Frequency Synthesis: It generates the radio signal, generally it is required to be set at a precise frequency and low-noise to obtain more accurate measurements. It is often referred to as the local oscillator (LO). Depending on the type of radar it can be modulated if required.

- Transmitter (TX): Commonly referred as power amplifier (PA) because it provides gain to the LO signal. It is not strictly necessary but often needed to interface the frequency synthesis with a transmitting antenna.

- Receiver (RX): A mixer is the fundamental element in a radar receiver because it provides the difference between the LO signal and the received signal. The output of the mixer carries the information of the target such as range, velocity, etc. Optionally, it often also includes a low-noise amplifier (LNA) to provide gain to the received signal before mixing and make it less susceptible to noise from subsequent stages.

- Antenna: Its purpose is either to transform electric current into radiated energy and vice versa. It is possible to have one antenna for TX and another one for RX, but also a single antenna can be used if an extra element called duplexer is used to allow bi-directional communication over a single path. Another important feature of an antenna is its directivity which can concentrate radiated energy within a narrow beamwidth.

- Data Processing: The raw data coming from the mixer can be quite noisy and thus signal conditioning is required. It can be done either in the analog or digital domain. In the case of the latter an analog-to-digital converter (ADC) is needed, but normally filtering and amplification stages are still performed in the analog domain.

There are several types of radars, some of the most important in the context of integrated circuits are:

- Pulse radar: It radiates a series of short rectangular pulses and then it stays silent to receive the reflected signal. The range resolution of the radar is given by the pulse duration, the shorter the pulse the wider the bandwidth, and in turn the better the resolution. The average output power is normally low because the pulse repetition interval is much larger than the pulse duration, it means that most of the time the radar is not transmitting, and one of the main challenges is the design of a high peak output power TX. One of the main advantages is that transmission and reception are not simultaneously hence there are no TX-RX leakage issues.

- Continuous-wave (CW) radar: In contrast to pulse radar, as the name implies, a continuous wave is transmitted and received continuously, thus both occur simultaneously. The average and peak power are usually equal and does not require a high peak output power. Since TX and RX work simultaneously it is often preferred to have independent antennas for each and in some cases TX-RX leakage canceling techniques are implemented. Its main limitation is that it operates based on Doppler frequency shifts to measure the velocity of targets but cannot measure the range at which the target is located. It can also exploit micro-Doppler effects [5] to measure displacement of a target, useful for vital signs monitoring (VSM).

- Frequency-modulated continuous-wave (FMCW) radar: This radar is a modulated version of the previously mentioned CW radar. The continuous wave is modulated in frequency to be able to extract range information (this will be explained in detail later). It can be seen as well as a linear frequency sweep in time, and similarly to pulse radar the wider the bandwidth the better the range resolution.

1.3 mm-Wave and Low-Power Applications

In recent years, radar development has been mainly driven by the automotive industry thanks to its reliable performance. Radar is normally used as a complementary technology to light detection and ranging (LiDAR or lidar) and cameras for applications like collision avoidance. Even though the two other technologies are more precise they are also more sensitive to adverse weather conditions and they are relatively more expensive. Radio waves have less absorption compared to light waves and can work in all conditions including fog, smoke, snow, heavy rain and during night. One of the most important automotive standards relying on radars is the advanced driver-assistance systems (ADAS) which is playing a growing role in applications such as adaptive cruise control (ACC), blind-spot detection (BSD), collision warning, cross traffic alerts, autonomous emergency braking (AEB), but also in-cabin applications going from monitoring systems and child presence detection to seat belt reminders and intruder alerts[6]. This technology is paving the path towards autonomous vehicles (AV) and

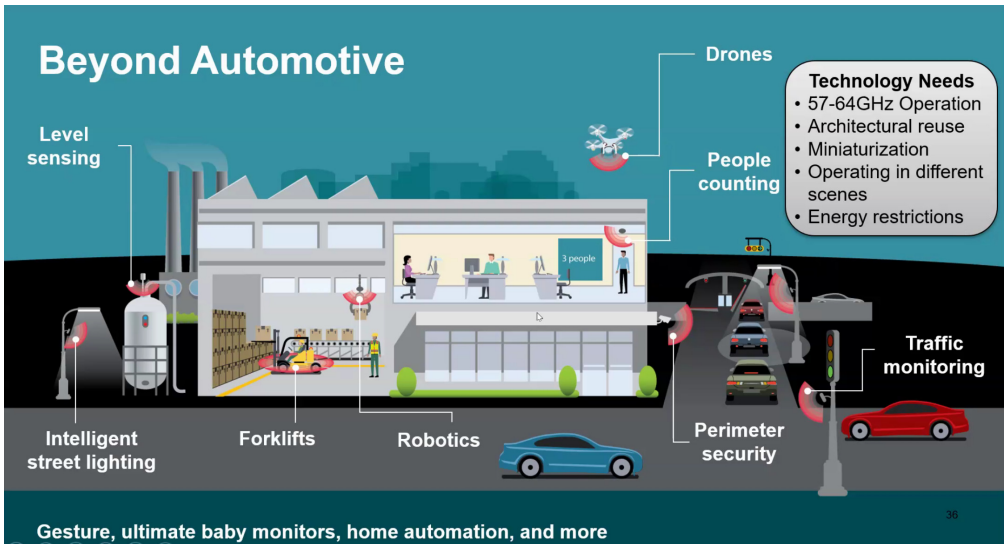
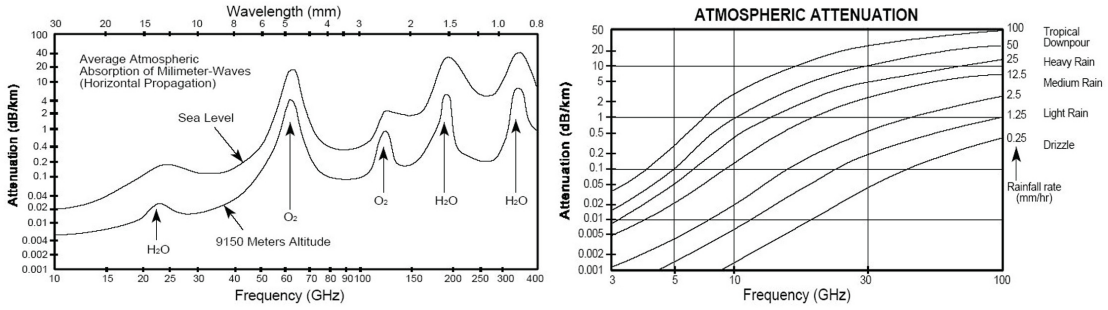


Figure 1.2: Potential markets for radar beyond automotive applications[7].

they require high performance to achieve their goals. Moreover, high performance usually means high power consumption, which can be afforded in the scenario of automotive where the power consumption is not tightly constrained. However, there are other markets for radar where battery-powered and Internet-of-Things (IoT) applications require much lower power consumption than automotive. For example Fig. 1.2 depicts other types of applications for radar beyond automotive.

Besides the various applications named in Fig. 1.2 it is also important to notice the frequency band from 57 to 64 GHz. As mentioned in the previous section, pulse and FMCW radars improve their range resolution with wider bandwidths which are often available at higher frequencies such as millimeter waves (mm-wave). For example, there is a narrow band (NB) unlicensed industrial, scientific and medical (ISM) band from 24.05 to 24.25 GHz, a 200 MHz bandwidth provides a range resolution of 75 cm which is not enough for automotive



(a) (b)

Figure 1.3: Attenuation vs frequency for (a) atmospheric absorption[8], and (b) added absorption due to precipitation[9].

applications. A more interesting band from 77 to 81 GHz provides a range resolution of 3.75 cm, 20x better performance, and it is indeed a band reserved for automotive applications[10]. The reason why the 77 GHz band is allocated for automotive is not only due to the wide bandwidth but also because it favors long range applications due to the low atmospheric attenuation at that frequencies. Instead, the 60 GHz band experiences a sea level atmospheric peak attenuation of 20 dB/km due to oxygen absorption compared to 0.4 dB/km at 77 GHz, as shown in Fig. 1.3a. This attenuation further increases for outdoor applications in case of precipitation, as shown in Fig. 1.3b. Since the 60 GHz band is not suitable for long range sensing, it is allocated for short-range devices (SRD), typically for indoor applications.

Industrial indoor applications such as security systems, automatic doors, smart-lighting control, and other features of a smart building are relying more and more on radars as motion sensors[11]. These types of applications previously used passive infrared (PIR) sensors, however they are very sensitive to temperatures and their reliability can drop significantly. Another important advantage for radar indoor sensing is the protection of privacy in contrast to cameras or any other optical image technologies. The importance of radar for presence and motion detection is reflected in Fig. 1.4, as the forecast for 2025 shows 9 million units radar devices for industrial applications, almost threefold from today.

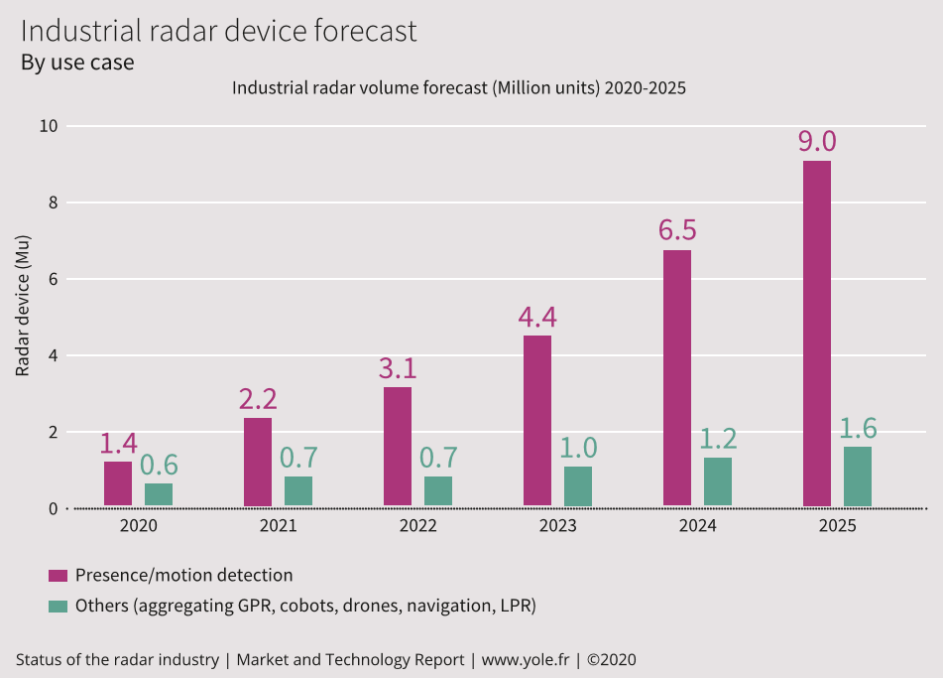


Figure 1.4: Industrial radar device forecast[11].

Another interesting market for presence and motion detection is smart homes. Apart from radars there are other numerous devices that are already placed in many homes to make life more convenient, and this number is increasing with different functionalities to automate more processes at home. The growing number of connected devices brings many advantages

but the price to pay also increases, particularly the cost of energy. Especially today, energy consumption has become a critical problem at large scale and also in our homes. Many electronic devices such as thermostats, smart speakers, digital assistants, TV screens, stay in a standby mode even when they are turned "off" because they remain alert in case they have to react instantaneously to an user[12]. The consumption of one device might be negligible but with the concept of smart homes one can easily have tens of devices consuming unnecessarily when the user is not even at home, and it is much worse when accounting for the millions of smart homes together. Energy wasting can be decreased by using radar sensors to monitor the presence of people and turning really off the electronic devices if they are not needed. One of the main companies working on radar sensors for smart homes is Infineon. They show in Fig. 1.5 an estimated worldwide average energy saving of 55 TWh per year thanks to the use of monitoring radars to optimize power consumption. It is also important to note that the power consumption of the radar itself should be significantly lower than the consumption of the "on" or standby mode electronic device.

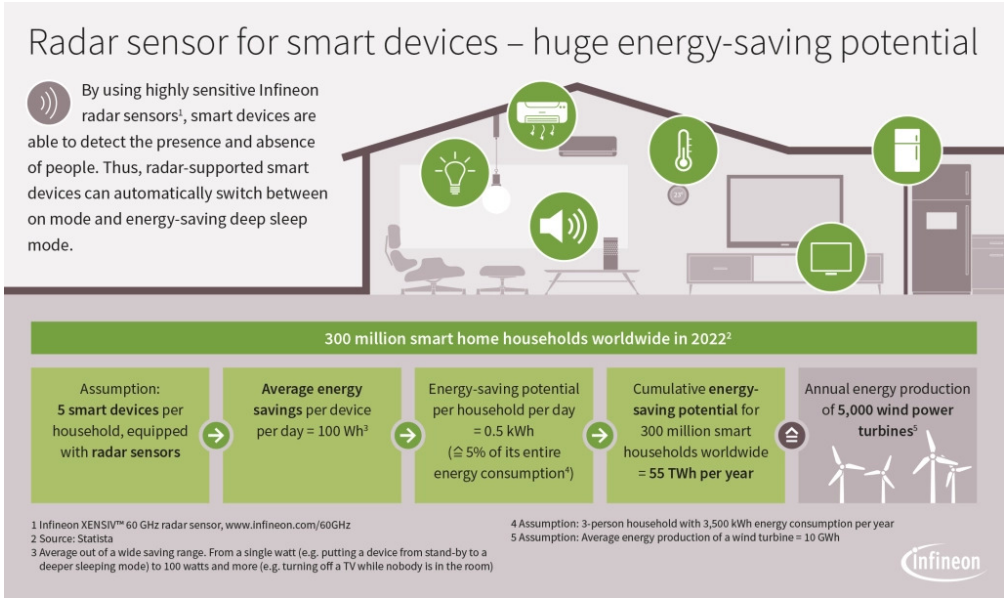


Figure 1.5: Potential energy savings with radar-powered smart devices[12].

1.4 State-of-the-Art on RADARs

This section presents the research in this field carried out through the past years until today and shows some of the architectures observed in academic and commercial radar sensors highlighting their main features.

1.4.1 Literature review

As aforementioned, in the past decades the most popular application for FMCW radar has been automotive mid- and long-range for ACC systems thus requiring a real-time response to activate braking systems an covering ranges from few meters up to 100 m. Among the first fully integrated radar transceivers demonstrating mid-range and long-range sensing are [13] and [14], respectively. Both systems modulate the transmitted signal by means of a phase-locked loop (PLL), using a voltage-controlled oscillator (VCO) at 77 GHz and sweeping a bandwidth up to 700 MHz. They do not demonstrate radar measurements using the total available bandwidth of 4 GHz reserved for automotive radar which goes from 77 to 81 GHz. This evidences the difficulty of modulating along such a wide band while maintaining a good linearity to prevent accuracy degradation of the range measurement. Different techniques have been implemented for linear frequency modulation. In [13] the modulation is performed out of the loop using a direct digital frequency synthesizer (DDFS) which works as the frequency reference for an integer-N PLL. A DDFS provides an accurate linear chirp and since it is a digital block it benefits from technology scaling, however the implementation of a DDFS for sweeping such a large bandwidth suffers from high power consumption and large area. In [14] a fractional-N PLL is implemented together with a sigma-delta (Σ-Δ) modulator which allows fine tuning of the frequency steps. Other solutions for improving linearity have been proposed in [15] and [16], implementing two-point injection and digital pre-distortion, respectively. These two solutions also show the trend towards all-digital PLLs (ADPLL) because digital-assisted circuits are less sensitive to technology and they even benefit from scaling down.

More challenges appear also on the RF front-end concerning the transmitter (TX) and receiver (RX) channels. The closer the operating frequency approaches to the maximum frequency of the transistor the more stability problems designers must face. Any amplification stage at mm-waves is prone to suffer from stability issues because even small parasitic capacitor can act as a low-impedance path creating positive feedback loops and driving the amplifier into self-oscillation. At high frequencies there is also less available gain which makes it more costly in terms of power to amplify a signal. Even something that might seem trivial as LO signal distribution could consume as much power as a power amplifier. There are some works showing good practices for the design of mm-wave amplifiers [17] and how to optimize for wide bandwidth [18].

More recent works as in [19] move to higher frequencies above 100 GHz to be able to increase the sweeping bandwidth and improve range resolution. At these frequencies the transistor starts to reach the maximum frequency of operation, at least in conventional CMOS, and some designers prefer moving to SiGe BiCMOS technologies. Nevertheless, it might not be cost-efficient and it makes more difficult the integration of an efficient digital signal processing (DSP) in the same die. In [20] a work published by IMEC and fabricated in a 28-nm CMOS process shows a 145-GHz FMCW radar with a bandwidth of 10 GHz, including on-chip antennas and demonstrating a measured range resolution of 27 mm.

The 60 GHz unlicensed ISM frequency band is one of the most used mm-wave bands because of its large available spectrum. It ranges from 57 to 66 GHz (only up to 64 GHz in US) corresponding to a theoretical range resolution of 16.67 mm. Another important advantage of operating at mm-wave is the miniaturization of passive components as antennas, which ease the possibility of adding several TX and RX elements to build a multiple-input multiple-output (MIMO) radar and enhance the angular resolution.

1.4.2 Academic and commercial works

This section presents some of the state-of-the-art radars operating in the 60-GHz band.

Nasr et al. [21]

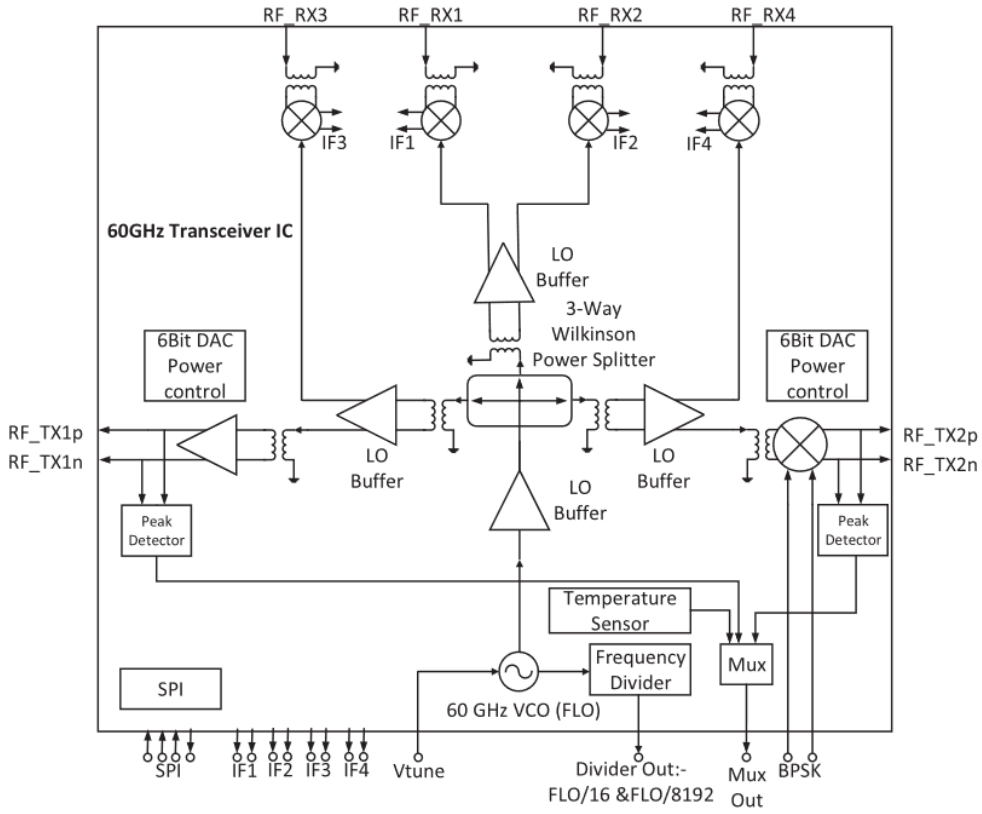


Figure 1.6: Block diagram of proposed 60-GHz 6-channel transceiver chip presented in [21].

This work presented a 57 to 64 GHz FMCW radar with 2 TX and 4 RX paths. It was fabricated in a 350-nm SiGe BiCMOS process from Infineon with a 3.3 V supply. The frequency synthesis or LO consists of an integrated VCO directly at 60 GHz and frequency dividers but the loop of the PLL is closed off-chip. The phase noise measured at 1 MHz frequency offset is −105 dBc/Hz. Provided the 7 GHz frequency chirp the theoretical range resolution is 21.4 mm. The signal is split by a 3-way Wilkinson power splitter to distribute it to the 2 TX and 4 RX paths. Each TX

shows a saturated output power of 4 dBm over the complete frequency range. The RX shows a noise figure (NF) below 10 dB with gain of 19 dB and an input referred 1-dB compression point (IP1dB) of 10 dBm. The main highlight of the chip is the high performance especially on the low phase noise, however it was not a complete solution because of the absence of the full PLL. The technology used offers a low flicker noise and high maximum frequency, but these come at the expense of not using a CMOS compatible technology. The high performance on the RF front-end has also a high cost on the power consumption, when all channels are operating it consumes 0.9 W and the die area is 20.25 mm^2.

Ng et al. [22]

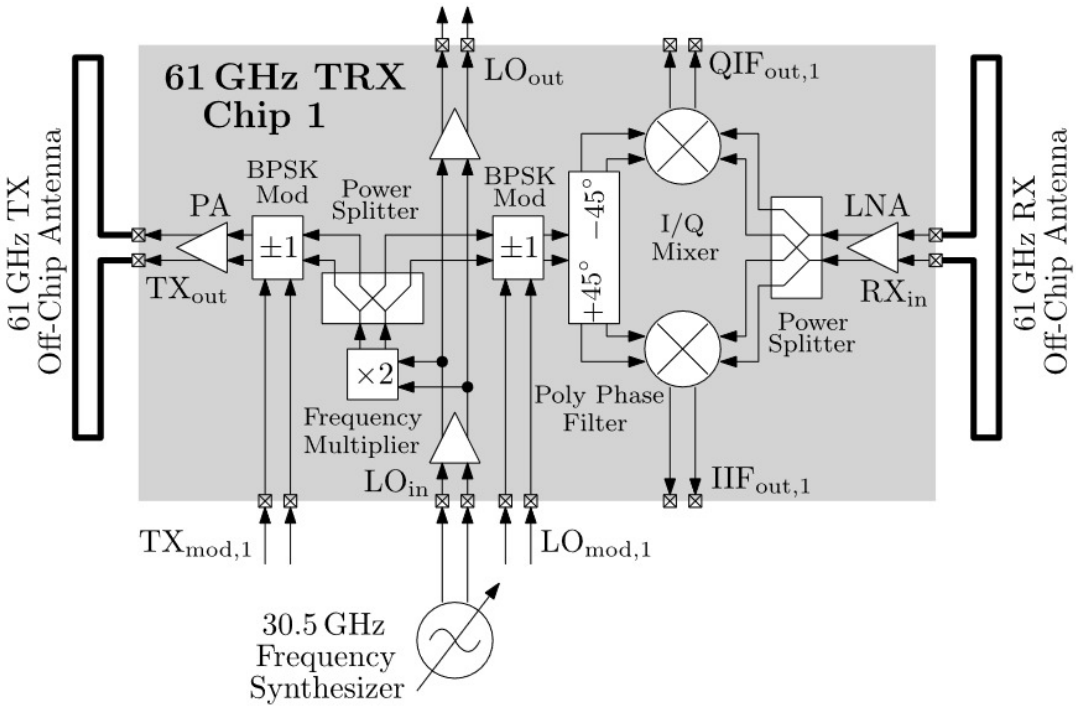


Figure 1.7: Simplified block diagram of a 61-GHz scalable sensor platform presented in [22].

This paper describes a scalable FMCW radar transceiver (TRX) which enables the cascading of multiple TRXs to implement a MIMO radar system. The front-end of the chip was fabricated in a 130-nm SiGe BiCMOS process from IHP. The frequency synthesis is not integrated together but on another die and it generates a signal at half the radar frequency. This signal is input into the front-end chip and after a frequency multiplier by 2 the signal measured ranges from 58.5 to 63.5 GHz. Thanks to the benefits of using a SiGe process the phase noise is also very low, it was measured at 1 MHz frequency offset obtaining −100 dBc/Hz. The swept bandwidth of 5 GHz offers a theoretical range resolution of 30 mm. The TX output power is 11.5 dBm while the RX shows a NF of 9.8 dB and gain of 24 dB. Since it is a similar technology as the previous work the performance is also high but the drawbacks are similar, moreover the idea of a scalable platform distributing the LO signal across multiple chips is very interesting because

opens the possibility for a multi-purpose applications. Although the chip has only 1 TX and 1 RX the power consumption is quite high because of the LO distribution buffers and high TX output power. The total power consumption is 0.59 W and the die area is 3.72 mm^2. The paper shows as well radar measurements with corner cube reflectors at different distances up to 4 m and the theoretical range resolution of 30 mm becomes 60 mm using a Hann window to estimate the range.

Rimmelspacher et al. [23]

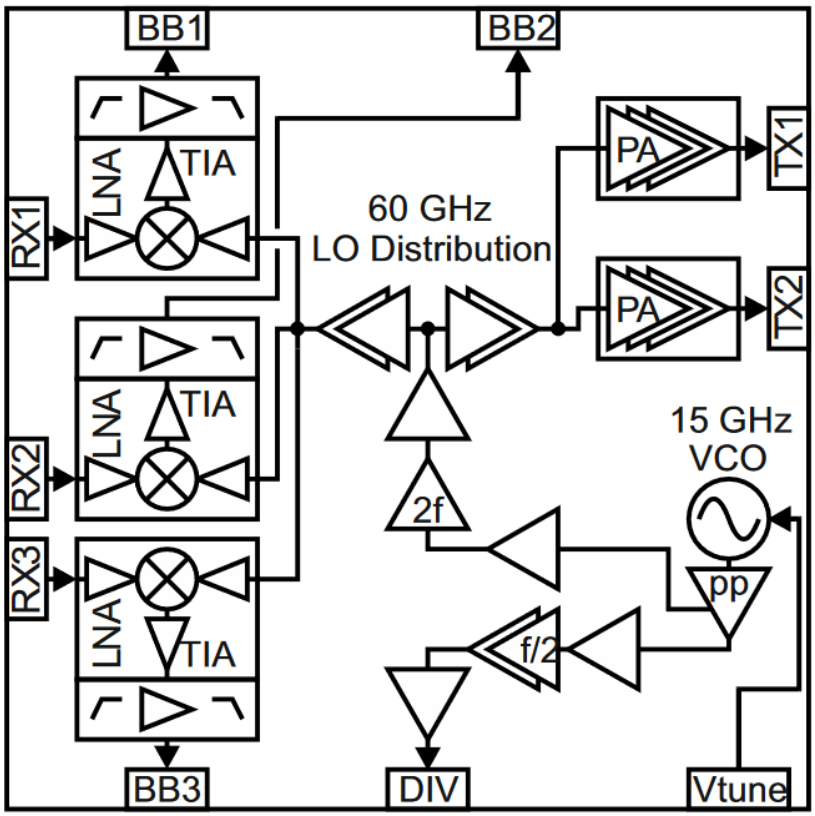


Figure 1.8: Simplified block diagram of a 60-GHz transceiver chip presented in [23].

Similarly to [21], this work is also conducted by Infineon but in a more advanced node as it is 28-nm CMOS bulk technology, making it easier to integrate with DSP on the same die. The FMCW radar sensor provides 2 TX and 3 RX paths with a frequency band ranging from 57 to 64 GHz, meaning a range resolution of 21.4 mm. The frequency synthesis is performed at 15 GHz on chip but the PLL loop is closed off-chip, there are on-chip frequency multipliers by 4. The VCO achieves a phase noise of −99.4 dBc/Hz at 1 MHz frequency offset, it is slightly worse than the SiGe version because this technology is less optimized for RF applications. The saturated TX output power is 10 dBm across the entire bandwidth. The RX achieves a NF of 12 dB, a gain of 77 dB and an IP1dB of −12 dBm. The work claims to be a low-power radar but it is still consuming 0.48 W, however the die area is 7.45 mm^2, almost three times smaller than [21] thanks to the advanced node used.

Lee et al. [24]

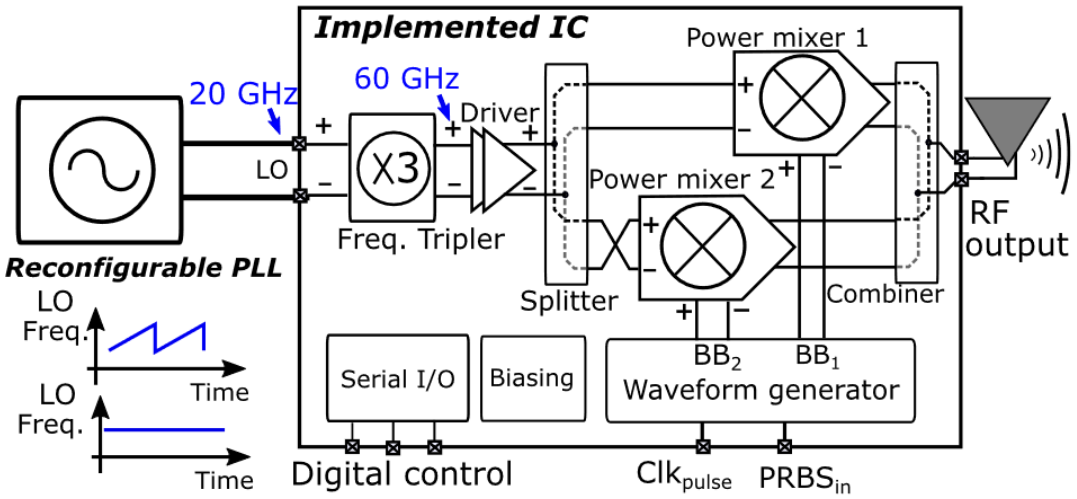


Figure 1.9: A 60-GHz multi-mode transmitter architecture presented in [24].

The chip presented in [24] is a multi-mode 60 GHz radar transmitter developed by IBM and Texas Instruments (TI). Although it does not integrate the RX part this work is interesting because of its versatility to function as a pulse, FMCW, and even a pulse-modulated continuous-wave (PMCW). PMCW is an alternative to FMCW which instead of modulating the frequency it is fixed but a pseudo-random binary sequence (PRBS) modulates the LO signal. The bit rate of the PRBS can be in the order of GSps to obtain a wide bandwidth and be able to achieve a high range resolution. In the case of [24], for each mode has different performance, the FMCW bandwidth is 10 GHz, the PMCW rate is 10 GSps, and the pulse width is as short as 25 ps (equivalent to a bandwidth of 40 GHz). The frequency synthesis is performed off-chip at 20 GHz and multiplied by 3 on-chip, it is also reconfigurable to adapt for each of the radar modes. The TX average and peak output power are 12.8 dBm and 14.7 dBm, respectively. Although the chip shows ultra wideband (UWB) high performance there is no allocated bandwidth below 100 GHz where such wide band can be used, therefore the chip is over-designed and some of its features could be traded-off for a lower power consumption. The chip was fabricated in a 45-nm RFSOI technology, with a power consumption of 0.51 W and the die area is 1.95 mm^2.

Kankuppe et al. [25]

This work presented in [25] is an ultra-low power 1-TX/1-RX 60-GHz FMCW radar developed by IMEC. The highlight of this radar sensor is the reduced power consumption being one order of magnitude lower than the radar mentioned above. It also includes a fully integrated frequency synthesis at 10 GHz, the signal is then multiplied in two different stages, by 3 and then by 2. The measured phase noise is −92.9 dBc/Hz at 1 MHz frequency offset. The TX output power is 8.1 dBm. The RX shows a NF of 10.5 dB, a variable gain with a maximum of 46 dB, and an IP1dB of −33 dBm measured for the highest gain. The effective FMCW swept bandwidth is 7.2 GHz

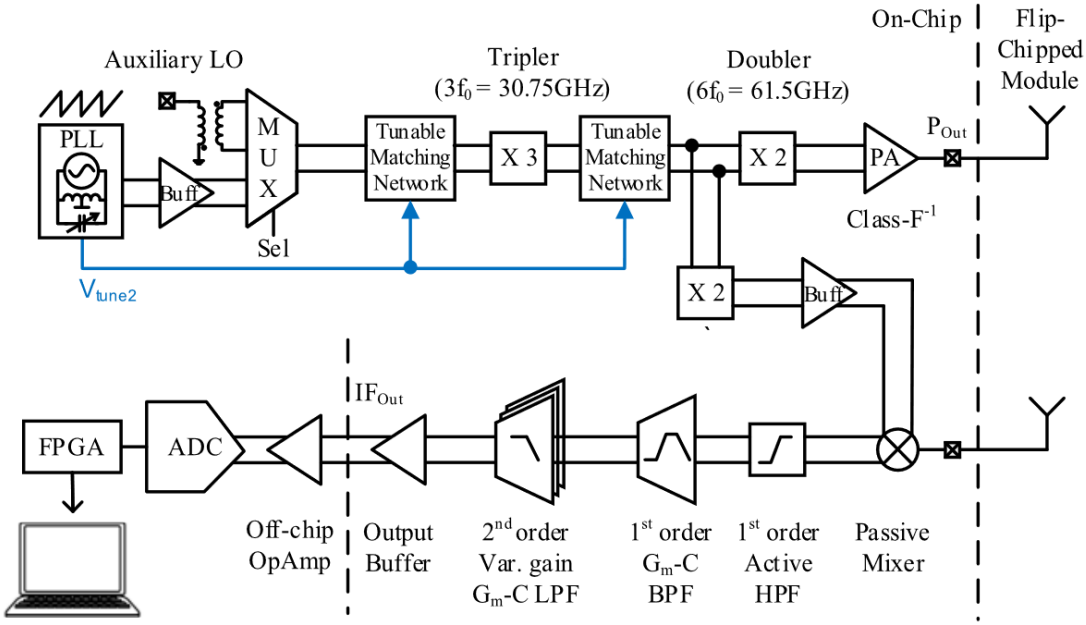


Figure 1.10: 60-GHz FMCW radar architecture presented in [25].

with a theoretical range resolution of 38 mm considering a 1.8 windowing factor (Blackman Harris window). This theoretical value is very close to the measured range resolution of 43 mm. A radar demonstrator was built to verify the radar capabilities in different scenarios: multitarget detection, pedestrian movement detection, and heartbeat detection. The radar consumes only 62 mW and the die area is 4.13 mm^2.

Acconeer: 60-GHz Pulsed Coherent Radar (PCR) [26]

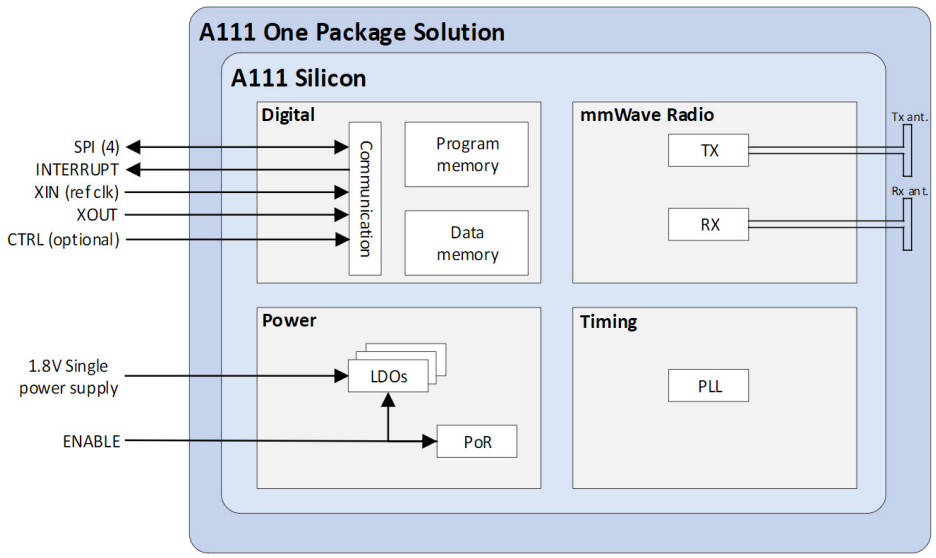


Figure 1.11: Block diagram of Acconeer A111 radar sensor [26].

Acconeer is among the world leader companies in small size, low-cost, and low-power consumption mm-wave radars sensors. In 2022, the company reached a million units shipped to over 60 countries. The current radar they offer is the A111 chip, it is a pulsed coherent radar (PCR) and operates in the 57 to 64 GHz band. The sensor consists of 1 TX and 1 RX, with integrated baseband and RF front-end, including antenna in package (AiP). The maximum TX output power is 10 dBm, however there are no details about the RX performance. The radar is fully integrated in a small package of 29 mm^2 and the average power consumption is 20 mW considering an update rate of 100 Hz. The datasheet of the sensor shows a maximum detection range of 2 m measured for a spherical corner reflector of 5 cm radius. The main applications for this radar sensor are: motion and speed detection, object tracking, VSM such as breathing and heart rate. The company has announced an improved second version, A121 radar sensor, possible to reach up to 20 m with a range resolution of 43 mm.

TI IWRL6432: Single-chip low-power 57 to 64 GHz industrial mmWave radar sensor [27]

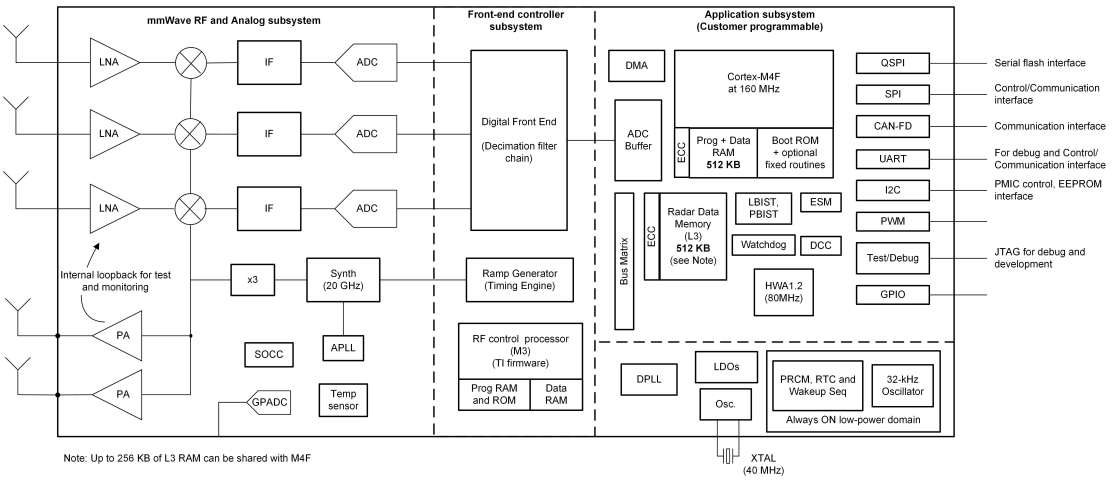


Figure 1.12: Block diagram of TI IWRL6432 radar sensor [27].

Texas Instrument developed a low-power 60-GHz FMCW radar sensor based on their original 77-GHz automotive radar. It is fabricated in a 45-nm RF CMOS process with a bandwidth of 7 GHz equivalent to a theoretical range resolution of 21.4 mm. It does not include the antennas as in the case of Acconeer but it has a better angular resolution with its 2 TX and 3 RX channels. The phase noise is −89 dBc/Hz at 1 MHz frequency offset, the TX output power is 11 dBm, and the NF is 12.5 dB. The overall performance is comparable to academic works aforementioned but the added value is that this chip includes also a complete digital baseband, a microcontroller unit (MCU), a hardware accelerator (HWA) block, plus it is a commercial product functional across different operating conditions. The trade-off for the high-performance radar is again power consumption. There was a significant reduction from the automotive IWR1443 and a previous industrial 60- to 64-GHz IWR6443 versions, both consuming 2.6 W (RF only), to the current 987 mW. Nevertheless, this power consumption is still considerably high for energy-efficient applications.

Infineon BGT60TR13C: XENSIV™ 60-GHz radar sensor for advanced sensing [28]

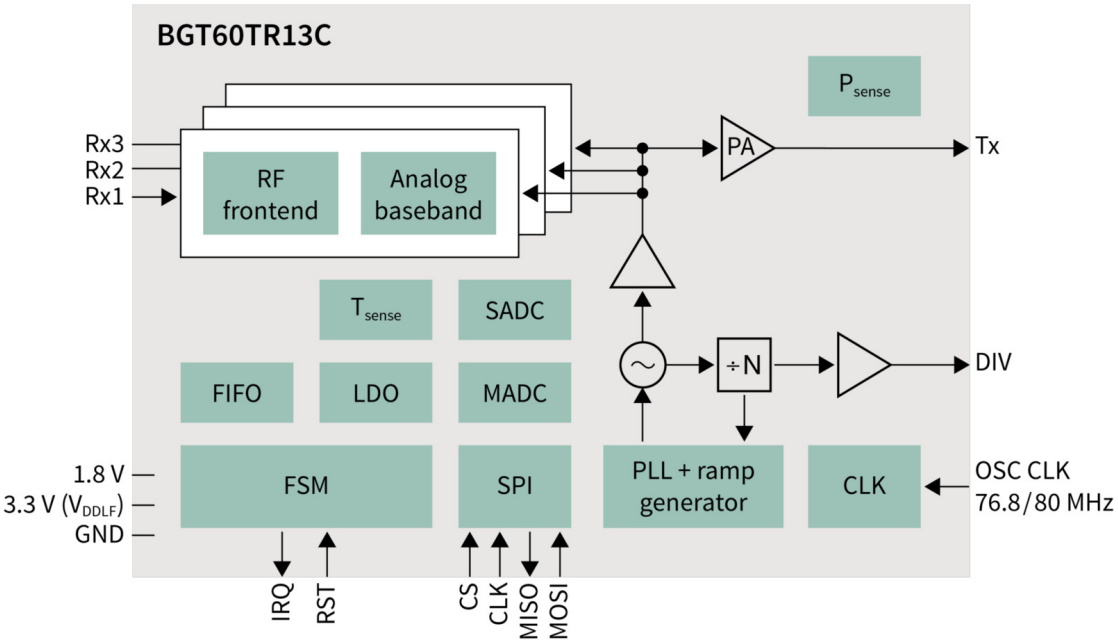


Figure 1.13: Block diagram of Infineon BGT60TR13C radar sensor [28].

In previously mentioned academic works Infineon BiCMOS process was used but in this case the chip is an actual commercial product including a complete integrated frequency synthesis and baseband. The sensor is a FMCW radar operating from 58 to 63.5 GHz, providing a theoretical range resolution of 27.3 mm. The product offers 1 TX and 3 RX channels with AiP. The TX output power is 5 dBm, the chirp slope is 400 MHz/μs, and the maximum detection range of 15 m. The total power consumption for is 350 mW (RF only) and the chip occupies an area of 32.5 mm^2, slightly larger than Acconeer but with more channels. The main applications for this sensor are presence detection, touchless interaction and VSM.

1.5 Thesis Motivation and Organization

The motivation of the work presented here arises from the fact that for years the development of radars have been driven primarily by the automotive and industrial market, prioritizing high performance over low power consumption. There are complete solutions in the market as already mentioned from Acconeer, TI and Infineon providing a fully integrated radar, but those sensors still consume hundreds of mW. There are some low-power projects being developed for portable or IoT applications where they do not require such high performance because the target application is short-range sensing and performance can be traded-off for power. One of the most important low-power short-range radar projects is [29] from Google, in collaboration with Infineon, however it is fabricated in 350-nm SiGe bipolar process based on [21]. This chip was already included in Google's Pixel 4 smartphone for motion sensing but the sensor was removed in the next model Pixel 5, the main reason being the cost[30]. The above academic

Table 1.1: State-of-the-art Radars Summary.

	Academic					Industrial		
Reference	[21]	[22]	[23]	[24]	[25]	[26]	[27]	[28]
Radar type	FMCW	FMCW	FMCW	Pulse FMCW PMCW	FMCW	Pulse	FMCW	FMCW
Technology	350 nm SiGe	130 nm SiGe	28 nm CMOS	45 nm RFSOI	28 nm CMOS	-	45 nm RF CMOS	BiCMOS
Frequency (GHz)	57-64	58.5-63.5	57-64	60	57-66	57-64	58-63.5	
RF BW (GHz)	7	5	7	10	7.2	7	7	5.5
TX/RX Channels	2/4	1/1	2/3	1/	1/1	1/1	2/3	1/3
TX P_{out} (dBm)	4	11.5	10	14.7	8.1	10	11	5
Noise Figure (dB)	10	9.8	12	-	10.5	-	12.5	-
PN@1 MHz (dBc/Hz)	-105	-100	-99.4	-	-92.9	-	-89	-
Total P_{DC} (mW)[a]	900	627[b]	478[b]	510	62	20 (100 Hz)	987	350
Area (mm^2)	20.25	3.72[b]	7.45[b]	1.95	4.13	29	41.6	32.5

[a] Maximum power consumption. [b] Fully or partially off-chip PLL.

works have also shown high performance FMCW radars operating in the 60-GHz band but still consuming hundreds of mW, as shown in Table 1.1. The goal of the present project is to design a fully integrated 60-GHz radar for low-power short-range applications aiming to reduce the power consumption by one order of magnitude compared to commercial products. Some of the target applications are object detection, motion sensing, gesture recognition, and VSM.

The main research of the thesis focuses on the design of a low-power small form-factor mm-wave front-end: TX and RX. These blocks usually dominate in a MIMO scheme because there are several of them compared to the frequency synthesis that is placed just once in the system.

Given the design of a complete radar system is cumbersome, the project was a collaborative effort in which the frequency synthesis is presented in [31]. The complete radar-on-chip (RoC) combining both frequency synthesis and the front-end is presented here. Finally, the opportunity to work with advanced nodes as GF 22-nm FDSOI provides advantages as a back gate and higher maximum frequency to exploit the performance trade-off at mm-wave.

The thesis is organized as follows:

Chapter 2 describes the operating principle of a FMCW radar and the reason why this technology was chosen over other types of radars. It explains theoretically the advantages of using a single frequency reference for the entire systems over having multiple references. Then, a demonstrator operating at 60 GHz is built with components off-the-shelf (COTS) to validate the calculations, simulations, and measurements. Finally, a link budget analysis is conducted in order to set specifications for the low-power RoC.

Chapter 3 focuses on the transistor parameters and how to optimize them for mm-wave operation. There is a section describing passive devices at high frequencies and good practices for their design. It continues with the design of a low-power TX chain adapted for FMCW radars. It is followed by characterization results and lessons learned from this first integration. The chapter finishes with the design of an improved version of the TX chain merging some functionalities to optimize power consumption and area.

Chapter 4 presents a mixer-first RX chain with an active mixer based on a Gilbert cell. Although this first version was not optimized for low-power it set the ground to design the second version based on a passive mixer-first RX chain. There is a study comparing the advantages of integrating it with a voltage-mode or current-mode IF amplifier. The former was found to be the most suitable solution and then the design of a low-noise IF amplifier is described.

Chapter 5 describes the entire 60-GHz FMCW radar system. It explains how the dies were mounted and the design of the test boards including patch antennas. The complete characterization results of the first and second version of the chip are presented. Finally, both chips demonstrate their sensing capabilities and the improvement achieved.

Chapter 6 concludes the dissertation, providing a summary of the achieved results and contributions, and discussing potential research topics for future work.

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2 System Architecture: FMCW RADAR

This chapter explains the operating principle of FMCW radars, including a brief comparison with other types of radars. Then a low-IF architecture is suggested and an analysis of phase noise is presented to prove how radars can benefit from it. The previous study is supported by simulations and measurement results carried out using a radar demonstrator built with components off-the-shelf (COTS). Finally, the radar equation is studied and used to define the design specifications for the target applications.

2.1 FMCW Radar Operating Principle

The main functionality of an FMCW radar is to estimate the range from a target. This feature is used in different cases such as tank level sensing to control the level of a liquid, automotive to detect other cars or obstacles, or VSM to track people and their health. Particularly in the case of VSM the target is a person, and the range from the radar to the person can be written as

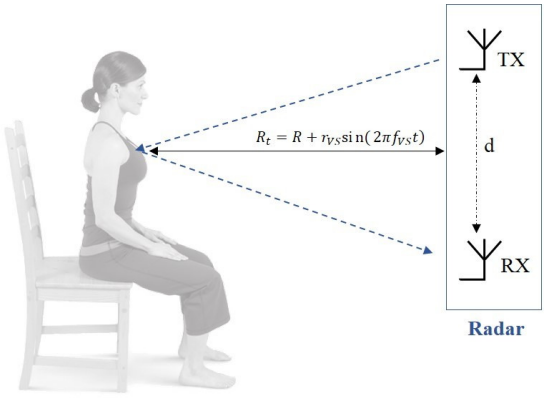

Figure 2.1: Measurement principle of VSM with a RADAR sensor.

$$R(t) = R_0 + r_{vs}\sin\left(2\pi f_{vs}t\right), \tag{2.1}$$

where R_0 is the mean range to the target, r_{vs} is the peak amplitude corresponding to the displacement of the chest due to vital signs such as respiration and heartbeat. The vital sign displacement is assumed to be sinusoidal, with a frequency f_{vs}. For VSM, f_{vs} is assumed to be much slower than the chirp repetition frequency, thus the range $R(t)$ in Eq. (2.1) is assumed constant and equal to R_0 within a single modulation period T_m.

2.1.1 Range and Velocity Estimation

A basic FMCW radar with a single TX and a single RX consists of a continuous-time chirp signal which is transmitted and reflected back from a target located at a distance R_0, as shown in Fig. 2.1. The chirp is usually a linear frequency sweep in time, in this case a triangular modulation is chosen where the instantaneous frequency of the TX chirp signal is given by

$$f_{TX}(t) = \begin{cases} f_L + St, & \text{for ramp-up: } 0 < t < T_c, \\ \left(f_L + 2B\right) - St, & \text{for ramp-down: } T_c < t < T_m, \end{cases} \tag{2.2}$$

where f_L is the lower end of the sweeping bandwidth B up to an upper frequency f_H, T_c is the chirp duration, T_m is the entire modulation time which is equal to $2T_c$, and S is the chirp slope $\frac{B}{T_c}$. The phase of the TX chirp is defined as the integral of the TX frequency, and assuming a initial condition of the phase $\phi(0)$ equal to zero, then the phase of the TX chirp is

$$\phi_{TX}(t) = 2\pi \int f_{TX}(t)\, dt = \begin{cases} 2\pi \left[f_L t + S\frac{t^2}{2} \right], & \text{for ramp-up: } 0 < t < T_c, \\ 2\pi \left[\left(f_L + 2B\right) t - S\frac{t^2}{2} \right], & \text{for ramp-down: } T_c < t < T_m. \end{cases} \tag{2.3}$$

The RX phase is derived from the TX phase taking into consideration three effects of the reflection from the target. The first effect is the delay τ equal to the time-of-flight (ToF) to a target, it is equal to $\frac{2R_0}{c}$, where c is the propagation speed 3×10^8 m/s. The second applies for the general case of a moving target which produces a Doppler frequency shift f_D equal to $-\frac{2f_c}{c}v$, where f_c is the center frequency of the sweeping band $\left(f_H - f_L\right)/2$, and v is the velocity of the target moving away from the radar. The last one is a phase shift ϕ_0 due to the surface reflection and any other shift introduced by the TX and RX paths. Then the RX phase is given by

$$\begin{aligned} \phi_{RX}(t) &= \phi_{TX}(t-\tau) + 2\pi f_D t + \phi_0, \\ &= \begin{cases} 2\pi \left[\left(f_L - S\tau + f_D\right) t + S\frac{t^2}{2} \right] + 2\pi \left(S\frac{\tau^2}{2} - f_L\tau \right) + \phi_0, & \text{for ramp-up: } 0 < t < T_c, \\ 2\pi \left[\left(f_L + 2B + S\tau + f_D\right) t - S\frac{t^2}{2} \right] - 2\pi \left(S\frac{\tau^2}{2} + f_L\tau + 2B\tau \right) + \phi_0, & \text{for ramp-down: } T_c < t < T_m. \end{cases} \end{aligned} \tag{2.4}$$

The RX instantaneous frequency can be calculated by taking the derivative of the phase resulting in

$$\begin{aligned} f_{RX}(t) &= \frac{1}{2\pi}\frac{d}{dt}\phi_{RX}(t), \\ &= \begin{cases} f_{TX}(t) - S\tau + f_D, & \text{for ramp-up: } 0 < t < T_c, \\ f_{TX}(t) + S\tau + f_D, & \text{for ramp-down: } T_c < t < T_m. \end{cases} \end{aligned} \tag{2.5}$$

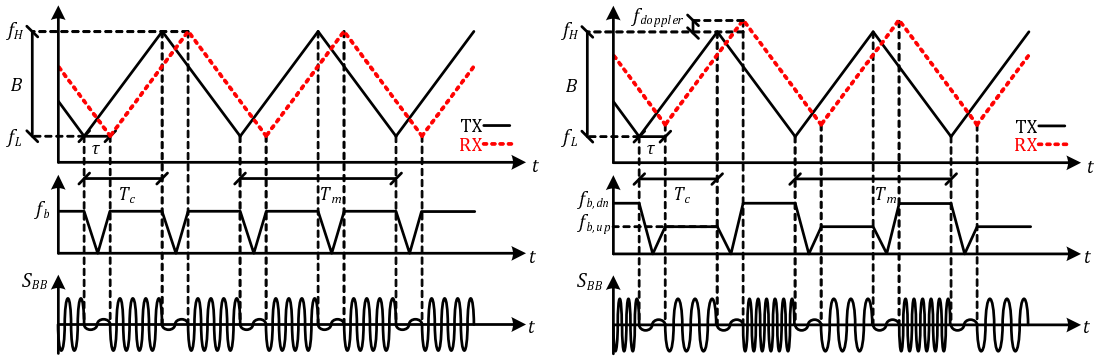

Figure 2.2: FMCW direct down-conversion of the RX signal with the TX signal to obtain the beat signal for a (a) static and (b) moving target.

Fig. 2.2a and Fig. 2.2b show the TX and RX frequency chirps using a triangular modulation in time for a static and moving target, respectively. Must be noted that there are two time intervals equal to the τ when the chirp reaches the maximum and minimum frequency but those intervals are neglected because in the general case of short-range sensing $\tau \ll T_c$. The in-phase baseband signal is obtained by mixing the reflected RX signal with the local TX signal,

$$\begin{aligned} s_{IBB}(t) &= A\cos\left(\phi_{TX}(t)\right)\cos\left(\phi_{RX}(t)\right), \\ &= \frac{A}{2}\left[\underbrace{\cos\left(\phi_{TX}(t)+\phi_{RX}(t)\right)}_{\text{filtered out}} + \cos\left(\phi_{TX}(t)-\phi_{RX}(t)\right)\right], \\ &\approx \begin{cases} \frac{A}{2}\cos\left[2\pi\left(S\tau - f_D\right)t + 2\pi\left(f_L\tau - S\frac{\tau^2}{2}\right) - \phi_0\right], & \text{for ramp-up: } 0 < t < T_c, \\ \frac{A}{2}\cos\left[-2\pi\left(S\tau + f_D\right)t + 2\pi\left(f_L\tau + 2B\tau + S\frac{\tau^2}{2}\right) - \phi_0\right], & \text{for ramp-down: } T_c < t < T_m, \end{cases} \end{aligned} \tag{2.6}$$

where the first term of the cosine product was neglected because it falls at twice the operating mm-wave frequency and it is filtered out by the mixer and subsequent baseband amplifiers

low-pass behavior. Similarly, the quadrature baseband signal is obtained

$$\begin{aligned} s_{QBB}(t) &= A\sin\left(\phi_{TX}(t)\right)\cos\left(\phi_{RX}(t)\right), \\ &= \frac{A}{2}\left[\underbrace{\sin\left(\phi_{TX}(t)+\phi_{RX}(t)\right)}_{\text{filtered out}}+\sin\left(\phi_{TX}(t)-\phi_{RX}(t)\right)\right], \\ &\approx \begin{cases} \frac{A}{2}\sin\left[2\pi\left(S\tau-f_D\right)t+2\pi\left(f_L\tau-S\frac{\tau^2}{2}\right)-\phi_0\right], & \text{for ramp-up: } 0<t<T_c, \\ \frac{A}{2}\sin\left[-2\pi\left(S\tau+f_D\right)t+2\pi\left(f_L\tau+2B\tau+S\frac{\tau^2}{2}\right)-\phi_0\right], & \text{for ramp-down: } T_c<t<T_m. \end{cases} \end{aligned} \tag{2.7}$$

Combining the two I and Q outputs is possible to form the complex baseband signal

$$\begin{aligned} s_{BB}(t) &= s_{IBB}(t)+j\,s_{QBB}(t), \\ &= \begin{cases} \frac{A}{2}\cdot e^{j\left[2\pi\left(S\tau-f_D\right)t+2\pi\left(f_L\tau-S\frac{\tau^2}{2}\right)-\phi_0\right]}, & \text{for ramp-up: } 0<t<T_c, \\ \frac{A}{2}\cdot e^{j\left[-2\pi\left(S\tau+f_D\right)t+2\pi\left(f_L\tau+2B\tau+S\frac{\tau^2}{2}\right)-\phi_0\right]}, & \text{for ramp-down: } T_c<t<T_m. \end{cases} \end{aligned} \tag{2.8}$$

The expression in Eq. (2.8) is also known as the beat signal. The beat frequency is defined for ramp-up and ramp-down as

$$f_b:\begin{cases} f_{b,up}=S\tau-f_D, & \text{for ramp-up: } 0<t<T_c, \\ f_{b,dn}=S\tau+f_D, & \text{for ramp-down: } T_c<t<T_m, \end{cases} \tag{2.9}$$

they are the difference between the chirps shown in Fig. 2.2, and they can be estimated applying a fast Fourier transform (FFT) on the beat signal. Since τ and f_D are included in the beat frequency and they carry the range and velocity information of the target, they can be extracted as

$$R_0=\frac{c}{2S}\left(\frac{f_{b,up}+f_{b,dn}}{2}\right)=\frac{cT_c}{2B}\left(\frac{f_{b,up}+f_{b,dn}}{2}\right), \tag{2.10}$$

$$v=\frac{c}{2f_c}\left(\frac{f_{b,up}-f_{b,dn}}{2}\right)=\frac{\lambda_c}{2}\left(\frac{f_{b,up}-f_{b,dn}}{2}\right). \tag{2.11}$$

2.1.2 Resolution and Precision

Given the earlier assumption of $\tau \ll T_c$, the rectangular observation window for the FFT is equal to T_c, and it is the inverse of the frequency resolution. The frequency resolution imposes the range and velocity resolution. The definition of range resolution is the ability to discriminate between two targets that are close in range, and similarly for the velocity resolution. The calculations of the different resolutions are given by

$$\Delta f = \frac{1}{T_c}, \qquad \Delta R = \frac{c}{2B}, \qquad \Delta v = \frac{\lambda_c}{2T_c}. \tag{2.12}$$

In order to have an idea of the order of magnitude of some of the parameters, a numerical example with realistic values are assumed for the FMCW radar. The sweeping bandwidth is chosen 9 GHz from the 60-GHz band and the chirp slope is set to 10 MHz/μs.

From Eq. (2.12) and Table 2.1 can be observed the advantage of operating in the mm-wave band, where multi-GHz bandwidth are available and benefits the range resolution. The high operating frequency gives a very short wavelength to improve also the velocity resolution. The calculations also confirm the assumption of $\tau \ll T_c$ by 4 orders of magnitude. Something important to notice is that the velocity resolution is actually larger than the speed to be measured, it is because of the short observation window T_c. A solution to improve the velocity resolution is to increase the observation window by grouping multiple modulation periods. For example, observing during 64 sweeps it enhances the velocity resolution to 0.04 m/s.

The derivation of velocity in a moving target was shown here for completeness, nevertheless the target applications do not focus on velocity monitoring but on range measurements and displacement of the target. For range estimation a good range resolution is important to discriminate two nearby targets, however it does not provide information about the precision of the measurement. There is another parameter defined as range accuracy which depends not only on the bandwidth B but also on the signal-to-noise ratio (SNR) of the beat signal. It is given by [1]

$$\sigma_R = \frac{c}{2B}\frac{1}{\text{SNR}}, \tag{2.13}$$

the stronger the beat signal is with respect to noise, the more accurate the range estimation. For target displacement, it is necessary to use what is known as the micro-Doppler effect by observing the beat phase from Eq. (2.8)

$$\phi_b = \begin{cases} 2\pi\left(f_L\tau - S\frac{\tau^2}{2}\right) - \phi_0, & \text{for ramp-up: } 0 < t < T_c, \\ 2\pi\left(f_L\tau + 2B\tau + S\frac{\tau^2}{2}\right) - \phi_0, & \text{for ramp-down: } T_c < t < T_m. \end{cases} \tag{2.14}$$

Table 2.1: Numerical example of a short-range human monitoring FMCW radar.

Parameters	Symbol	Value	Units
Propagation speed	c	3×10^8	m/s
Lowest frequency	f_L	57	GHz
Highest frequency	f_H	66	GHz
Bandwidth	B	9	GHz
Chirp slope	S	10	MHz/μs
Chirp duration	T_c	0.9	ms
Modulation period	T_m	1.8	ms
Center frequency	f_c	61.5	GHz
Wavelength of f_c	λ_c	4.88	mm
Frequency resolution	Δf	1.11	kHz
Range resolution	ΔR	16.67	mm
Velocity resolution	Δv	2.71	m/s
Target range	R_0	5	m
Time-of-Flight (ToF)	τ	33.33	ns
Beat frequency due to ToF	$S\tau$	333.33	kHz
Human speed (man running)	v	3.6	m/s
Doppler shift	f_D	1.48	kHz
Ramp-up beat frequency	$f_{b,up}$	331.86	kHz
Ramp-down beat frequency	$f_{b,dn}$	334.81	kHz

Though one modulation period is sufficient for range estimation, displacement estimation requires information carried in the beat phase and it must be evaluated across several modulation periods. The expression in Eq. (2.14) can be rewritten as a function of time taking into consideration the displacement described in Eq. (2.1), the beat phase is approximated as

$$\phi_b(t) = \begin{cases} \frac{4\pi f_L r_{vs}}{c} \sin\left(2\pi f_{vs} t\right) + \phi_1, & \text{for ramp-up: } 0 < t < T_c, \\ \frac{4\pi (f_L + 2B) r_{vs}}{c} \sin\left(2\pi f_{vs} t\right) + \phi_2, & \text{for ramp-down: } T_c < t < T_m. \end{cases} \tag{2.15}$$

where the quadratic term in Eq. (2.14) is neglected. This approximation can be easily justified by noting that $S\frac{\tau}{2}$ is equal to half the beat frequency due to ToF, then it is in the order of few kHz compared to f_L equal to 57 GHz. The terms $\phi_1 = \frac{4\pi f_L R_0}{c} - \phi_0$ and $\phi_2 = \frac{4\pi(f_L+2B)R_0}{c} - \phi_0$ account for the time-independent terms. The respiration and heart rate can be estimated through the oscillations of the beat phase and this is the reason why coherent detection is required for VSM applications.

2.1.3 Advantages of FMCW against other Radars

Other interesting alternatives to FMCW radar are CW Doppler and impulse radio ultra-wideband (IR-UWB). The CW radar is a simpler implementation because it requires no modulation and does not occupy a wide bandwidth. This is a suitable solution for low-power low-cost applications where only a single target is present because it only provides Doppler information and it is not able to discriminate multiple targets at different ranges. IR-UWB can achieve high range resolution thanks to its wide bandwidth, however it requires a high peak-to-average power ratio (PAPR) to maintain an SNR as good as in FMCW. The high peak power could be better managed in SiGe BiCMOS processes but it is more challenging to be realized in CMOS processes which are necessary for a low-cost solution.

Above the previously mentioned advantage there is a key feature that makes FMCW more attractive than other types of radar. FMCW radar shows a bandwidth compression at the baseband frequency after down-conversion. While IR-UWB radar needs to sample the output of the RX at the same rate of the mm-wave bandwidth, FMCW only needs to sample at the beat frequency which depends on the chirp rate and ToF but it is normally several order of magnitude lower than the mm-wave bandwidth as shown in the numerical example in Table 2.1. Thus, instead of requiring a high-speed ADC in the order GSps that would increase the total power consumption of the system, FMCW can achieve the same resolution with a low-power ADC.

2.2 Modulation Scheme Impact on Phase Noise in Radars

The theory and derivations shown in the previous section correspond to the case of an FMCW radar using a direct down-conversion architecture. This section presents the advantages of moving into a low-IF architecture and its effect on the phase noise performance.

2.2.1 Low-IF Architectures

In the context of VSM, since respiration and heart rate are in the range of sub-Hz to few Hz, the modulation period T_m does not require to be very fast. It can be chosen in the order of milliseconds relaxing the local oscillator (LO) performance. However, the slower the chirp slope the lower the beat frequency (Eq. (2.9)). For example, setting T_m = 10 ms and

maximum range R_{max} = 5 m, the maximum beat frequency falls at 30 kHz, where DC offsets and flicker noise can significantly lower the SNR and consequently degrade the precision of the measurement (Eq. (2.13)). To address this limitation, a low-IF architecture can be implemented to translate the resulting beat frequency farther away from DC offsets and flicker noise. This type of architecture also allows orthogonality which is necessary for in the digital beamforming MIMO scenario because the multiple RX paths must be able to differentiate the signals from multiple TX paths.

One option is to implement orthogonality in time, as in time-division multiplexing (TDM), however it increases the sweep time by the number of TX channels in the radar and they cannot operate simultaneously. Another approach involves the use of orthogonal frequency division multiplexing (OFDM) signals, but they are more sensitive to Doppler frequency shifts which are difficult to compensate for long sweeps [2], which is the case in the context of VSM. Chirp rate division (CRD) [3] is also an alternative but it needs as many frequency synthesizers as TX channels to be able to sweep linearly simultaneously with different chirp rates. Finally, the most suitable solution found for a low-power radar is called beat frequency division (BFD), which consists in adding a frequency shift in the linear FMCW. Each TX channel must have a different frequency shift to implement a frequency-division multiplexing (FDM). The frequency shifts should be large enough to avoid DC offsets and flicker noise, but not arbitrarily high since it would impose unnecessarily strict specifications to the design of the ADC sampling rate.

The three options proposed for implementing BFD in the transmitted signal are: 1) two PLLs with a frequency shift; 2) single-PLL with OOK; and 3) single-PLL with BPSK modulations. The first option is proposed in the MIMO scenario at mm-wave, because of the challenge of distributing the LO signal to all TX and RX paths. Having more than one PLL facilitates the distribution of the signal. There could be for instance a PLL for TX and another one for RX. This example is similar to the case of secondary radars where the TX and RX are physically in different locations. The fact that the PLLs are not the same enables the use of slightly different frequencies to achieve a low IF without requiring a modulation scheme. In the case of single-PLL architectures, OOK and BPSK are proposed since they are fairly simple to implement without increasing circuit complexity, area, and power consumption. The proposed architectures are presented in Fig. 2.3.

The modulating signal frequency-domain spectrum $S_M(f)$ acts as a frequency translation of the baseband signal, it depends on the PLL architecture chosen and it is given by

$$S_M(f) = \begin{cases} \delta\left(f - f_{IF}\right), & \text{2 PLLs} \\ \frac{\delta(f)}{2} + \frac{1}{j\pi k}\left[\delta\left(f - kf_{IF}\right) - \delta\left(f + kf_{IF}\right)\right], & \text{OOK} \\ \frac{2}{j\pi k}\left[\delta\left(f - kf_{IF}\right) - \delta\left(f + kf_{IF}\right)\right], & \text{BPSK} \end{cases} \tag{2.16}$$

where f_{IF} is the modulating frequency, k represents the number of the harmonic. The 2

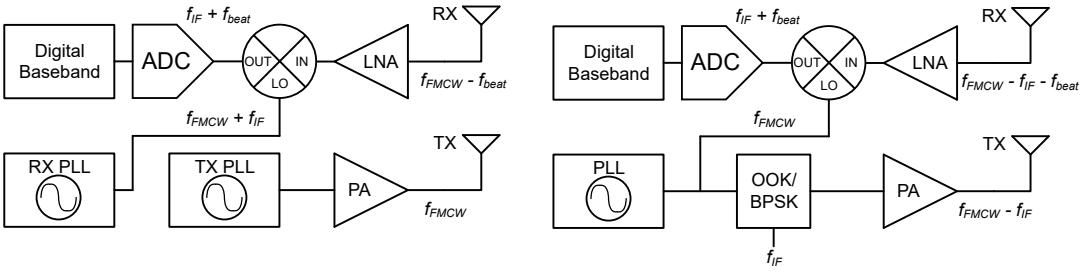

Figure 2.3: FMCW low-IF architecture implemented with (a) 2 PLLs and (b) OOK/BPSK modulations.

PLLs case is not really a modulation but a frequency shift implemented by slightly different synthesized frequencies on the TX and RX PLLs. For the OOK and BPSK modulations ideally only odd harmonics exist because even harmonics are canceled due to symmetry. The main difference is that OOK presents a fundamental component, which is the term $\frac{\delta(f)}{2}$.

2.2.2 Phase Noise Autocorrelation

Another important noise contributor to the SNR is phase noise in the frequency synthesizer. Although phase noise is a problem, there is a well-known attenuation effect studied in [4], which takes place when the down-conversion of the RX signal is performed by the same LO which generated originally the TX. In a few words, phase noise is attenuated if the mixing signals are autocorrelated, which is the case if it uses a single-PLL architecture. The general expression to include the impact of a low-IF architecture and phase noise is given by

$$\begin{aligned} s_{IF}(t) &= s_{BB}(t) \cdot s_M(t-\tau) \cdot e^{j\left[\Delta\phi_{IF}(t,\tau)\right]}, \\ &\approx s_{BB}(t) \cdot s_M(t) \cdot \left[1 + j\Delta\phi_{IF}(t,\tau)\right], \end{aligned} \tag{2.17}$$

where $s_{IF}(t)$ is the new down-converted signal, $s_{BB}(t)$ is the previously calculated baseband signal in Eq. (2.8), $s_M(t)$ is the time-domain modulating signal that represents the low-IF component, and $\Delta\phi_{IF}(t,\tau)$ is the down-converted IF phase noise. The modulating signal experiences also a ToF delay equal to τ but it can be neglected because the low-IF is normally chosen low enough such that its period is much longer than τ. For example, the maximum ToF calculated in Table 2.1 is 33.33 ns and the low-IF in the order of few MHz (hundreds of nanoseconds or few microseconds) to avoid the need of a high-speed ADC. In general, the phase noise term is defined as $\Delta\phi_{IF}(t) = \Delta\phi_{TX}(t) - \Delta\phi_{RX}(t)$, where $\Delta\phi_{TX}(t)$ and $\Delta\phi_{RX}(t)$ are the random phase noise perturbations and they are assumed to be zero mean stationary stochastic processes [4]. In the single-PLL case radar, since the phase noise is autocorrelated, it depends on τ and it can be written as $\Delta\phi_{IF}(t,\tau) = \Delta\phi_{TX}(t) - \Delta\phi_{TX}(t-\tau)$. In practical situa-

tions, the variance of the phase noise is much lower than unity and it allows the exponential term in Eq. (2.17) to be approximated by using Taylor series [4].

The expression in Eq. (2.17), in the time domain, is easier to be understood in the frequency domain, which is given by

$$S_{IF}(f) = S_{BB}(f) * S_M(f) * \left[\delta(f) + S_{\Delta\phi_{IF}}(f,R)\right], \tag{2.18}$$

where the $S_{\Delta\phi_{IF}}(f,R)$ is the phase noise power spectral density (PSD) of the down-converted IF signal, and its dependence on τ is expressed now as a dependence on the range R. The phase noise PSD is obtained from a mathematical model shown in [4]. The phase noise PSD of the down-converted IF signal is given by

$$S_{\Delta\phi_{IF}}(f,R) = \begin{cases} S_{\Delta\phi_{TX}}(f) + S_{\Delta\phi_{RX}}(f), & \text{uncorrelated: 2 PLLs,} \\ 4S_{\Delta\phi_{TX}}(f) \cdot \sin^2\left(2\pi f \frac{R}{c}\right), & \text{correlated: OOK and BPSK.} \end{cases} \tag{2.19}$$

The uncorrelated case in Eq. (2.19) corresponds to having 2 PLLs as in Fig. 2.3a, and the resulting PSD is the sum of both TX and RX phase noise PSD. In the correlated case in Eq. (2.19), the phase noise PSD is written as a function of the range R which has an important role on the single-PLL radar where the term $\sin^2\left(2\pi f \frac{R}{c}\right)$ appears due to the correlation between TX and RX signals. This term has a high-pass transfer function with a cut-off frequency above several MHz even for ranges up to 10 m. Fig. 2.4 shows the phase noise attenuation due to autocorrelation for a target at different ranges. The farther the target the longer the ToF and in turn the weaker the correlation between TX and RX signals.

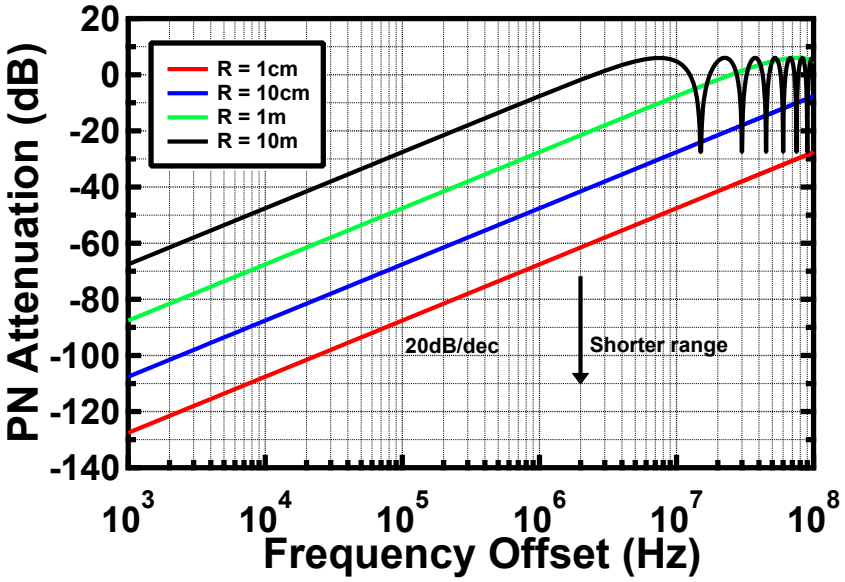

Figure 2.4: Phase noise attenuation due to autocorrelation on the resulting beat signal.

Phase noise autocorrelation proves significantly useful for short range radars, because in FMCW the TX and RX operate simultaneously producing a TX-RX leakage around DC and could potentially cover nearby targets with its phase noise. For example using the parameters from Table 2.1, if the distance between TX and RX is 1 cm and there is a close target at 10 cm, the radar would see a TX-RX leakage at 0.67 kHz and the beat frequency of the target at 6.67 kHz. The beat signal is only 6 kHz apart from the TX-RX leakage frequency component but the phase noise attenuation for 1 cm reflection at 6 kHz frequency offset is −112 dBc/Hz. In an actual radar, the noise attenuation close to the carrier is normally so large that the phase noise is covered by the noise floor of the RX chain.

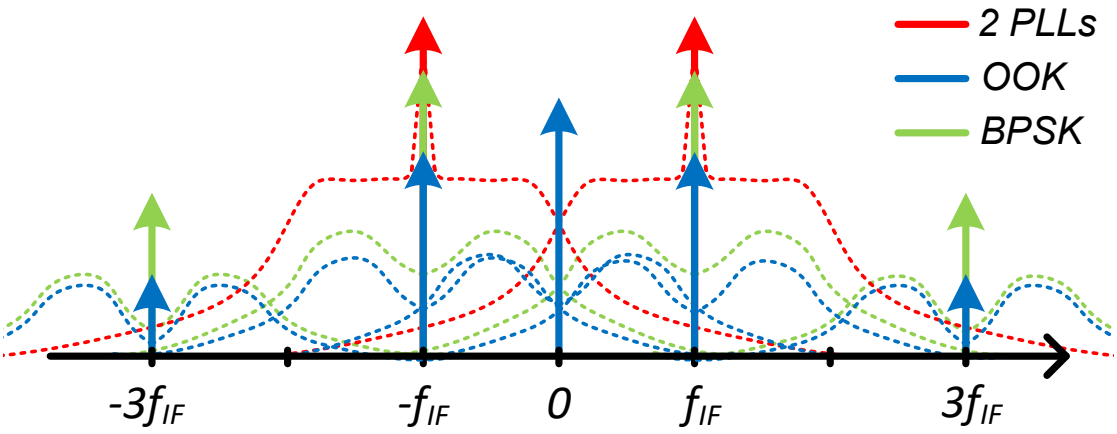

Figure 2.5: Spectrum corresponding to each low-IF translation (solid lines) with its corresponding phase noise (dashed lines).

The impact of the phase noise on the IF signal can be estimated by superimposing the PSD in Eq. (2.19) at each harmonic calculated in Eq. (2.16). The power spectrum corresponding to each architecture frequency translation is sketched in Fig. 2.5 for an arbitrary range. For simplicity, the figure only shows up to the third harmonic. It should be noted that since the ADC follows the signal down-conversion, noise must be filtered out. The filter can be designed to allow some of the harmonics and not to waste the power carried on them; however, the wider the band of the filter is, the faster the ADC needs to sample. As a trade-off, the filter can be designed to pass up to the third harmonic of OOK and BPSK, which already carry more than 90 % of the power. Nevertheless, one of the main disadvantages of OOK is the fundamental component which falls in the flicker noise of the RX chain. It is normally filtered out losing half of the power, making it less efficient compared to BPSK.

2.3 COTS RADAR Demonstrator

A 60-GHz FMCW radar demonstrator was built with components off-the-shelf (COTS) in order to validate the analysis presented in the previous section. The demonstrator was developed in the frame of the project EU H2020 M3TERA [5] and based on [6]. This project targeted low-cost sub-THz technology aiming remote, contact-less, vital sign monitoring. The radar

platform was built with two identical PLLs for TX and RX, similarly to Fig. 2.3a. The PLLs were implemented using the evaluation board EV-ADF4159EB1Z operating at 9.5 GHz. The TX path consists of a RPG TX-75 module which acts also as a frequency multiplier by 6. In the RX path there is an RPG V-LNA 50-75 GHz followed by an OML M15HWD harmonic mixer.

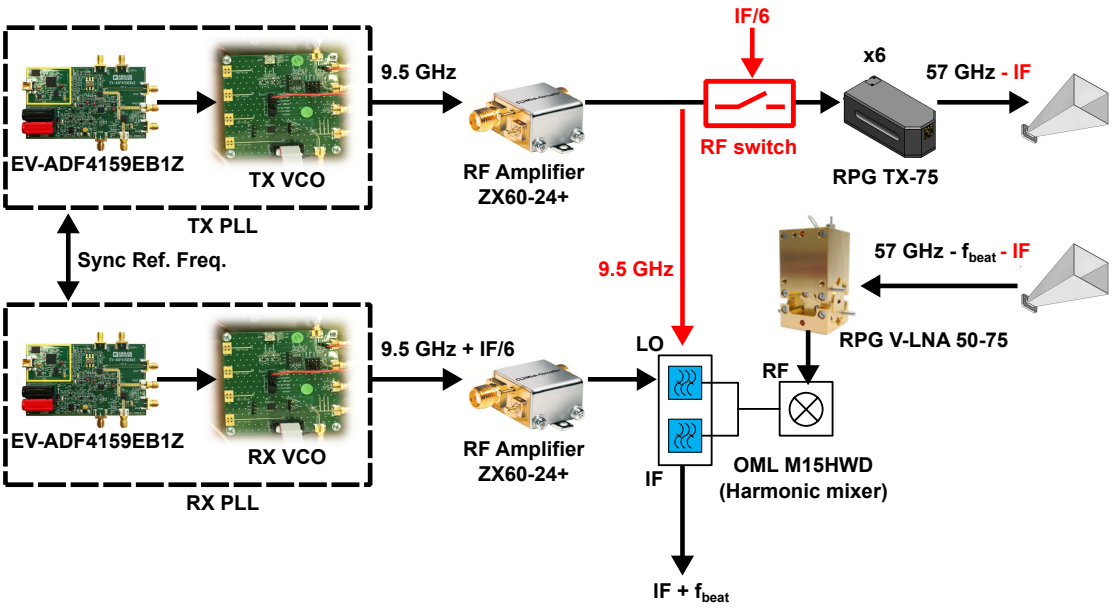

Figure 2.6: 60-GHz FMCW radar demo using a 2-PLL architecture and an alternative OOK modulation (red).

The PLL boards do not use their own voltage-controlled oscillator (VCO) but as part of the EU project a VCO at 20 GHz (with an auxiliary output at 10 GHz) was designed in house. The details of the VCO can be found in [7, 8]. Since the down-conversion is performed through an harmonic mixer, the LO port can work with a fraction of the required LO signal, in this case LO/6. The harmonic mixer includes a diplexer which outputs the down-converted signal through a IF port. Alternative to the 2-PLL architecture, an OOK modulation (drawn in red in Fig. 2.6) can be applied adding a RF switch in the TX path, using the TX PLL signal for down-conversion in the harmonic mixer, and disconnecting the RX PLL signal from the mixer.

2.3.1 Phase Noise Measurements

In order to measure the TX phase noise, the TX PLL output was first connected to an ultra-low SSB phase noise frequency divider-by-four (HMC447LC3), and then connected to a signal source analyzer (E5052B). The TX phase noise is used as a reference together with Eq. (2.16) and Eq. (2.19) to obtain the calculated IF phase noise. While simulated results are obtained importing the TX phase noise in an ADS Keysight environment to compare the different radar architectures: 2-PLL with uncorrelated phase noise, 1-PLL with OOK modulation, and 1-PLL with BPSK modulation. The calculated and simulated phase noise PSDs for the first harmonic are shown in Fig. 2.7, setting the IF to 1 MHz and range to 30 cm. The radar is set to CW mode

for the following measurements to remove uncertainty caused by the FMCW chirp linearity.

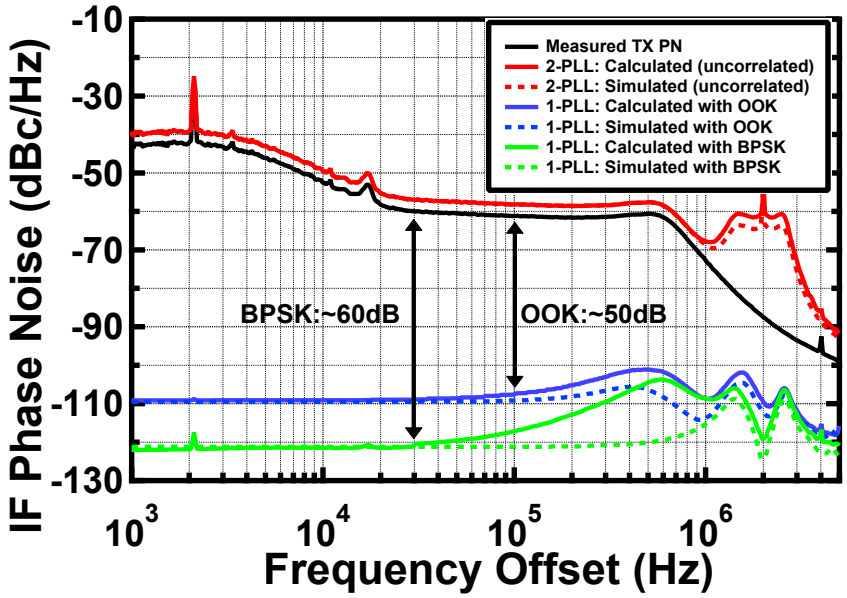

Figure 2.7: Calculated and simulated IF phase noise using 1- and 2-PLL architecture with a f_{IF} = 1 MHz and R = 30 cm.

The black curve represents the measured TX phase noise. The red curves, corresponding to the uncorrelated phase noise PSDs, show a good match between simulations and calculations. Since the TX and RX PLLs are equal then $S_{\Delta\phi_{RX}}(f) = S_{\Delta\phi_{TX}}(f)$ and the total phase noise at IF becomes twice the phase noise at TX, meaning 3 dB larger. A peak is observed at 2 MHz frequency offset due to the phase noise of the negative frequency component (phase noise of red component at the harmonic $-f_{IF}$ in Fig. 2.5). In contrast, the cases of OOK and BPSK present correlation attenuation, reducing the phase noise by more than 50 dB and 60 dB respectively compared to having 2 uncorrelated PLLs. It is especially evident at 2 MHz, where instead of having a peak they show an even lower phase noise due to attenuation around $-f_{IF}$. The OOK modulation presents 9 dB larger phase noise than BPSK because of the phase noise contribution of the fundamental component at DC.

For further validation of calculations and simulations, the phase noise is measured after the harmonic mixer at the IF. The setup is then modified removing the RX PLL and placing a RF switch before the TX module to implement an OOK modulation, similarly to Fig. 2.3b. It is not possible to implement BPSK here because the COTS setup has only available single-ended and not differential signals to realize a chopping modulation. The IF is set to 24 MHz to reduce the impact of DC offsets, and flicker noise, because their presence masks the wanted IF signal.

In the case of the 2-PLL, the IF phase noise cannot be accurately calculated because for the radar to work the 2 PLLs must be synchronized using the same reference frequency, therefore the phase noise is not completely uncorrelated. The reference frequency phase noise will be attenuated due to correlation but the phase noise contribution coming from the charge

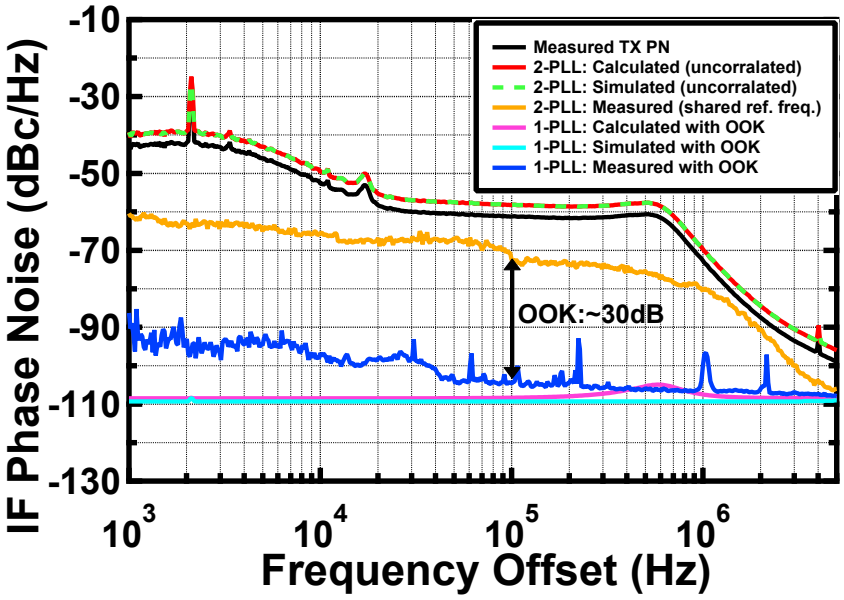

Figure 2.8: Calculated, simulated, and measured IF phase noise using 1- and 2-PLL architecture with a f_{IF} = 24 MHz and R = 30 cm.

pump, loop filter and VCO are uncorrelated, and the resulting IF phase noise is lower than the calculated. The calculated, simulated and measured phase noise are shown in Fig. Fig. 2.8. Although, using a higher IF decreases the impact of phase noise from harmonics in a radar with multiple-PLLs, using a single-PLL radar architecture for short range detection proves to achieve at least 30 dB lower phase noise.

2.3.2 Range Measurements

The previous measurements were performed with the radar configured in CW mode to remove the effect of the beat frequency. In order to enable the FMCW mode and perform range measurements the PLL boards control the capacitor banks of the VCO to produce the FMCW chirp. Considering this COTS demonstrator as an early attempt to evaluate FMCW radar functionalities, the VCO was designed only to cover a fraction of the 60-GHz band. The chirp is configured as a triangular frequency sweep with an initial frequency f_L = 57 GHz, a bandwidth B = 860 MHz, a chirp duration T_c = 500 μs, and a OOK modulation with an IF f_{IF} = 2 MHz.

The equivalent range resolution is only 17.4 cm but it is enough to validate the detection capabilities of the FMCW radar as shown in Fig. 2.9, where targets at different distances are identified successfully. The component at f_{IF} comes from the TX-RX leakage, because even with a low-IF architecture this leakage cannot be avoided. The other smaller peaks are the result of the laboratory clutter where the measurements were carried out.

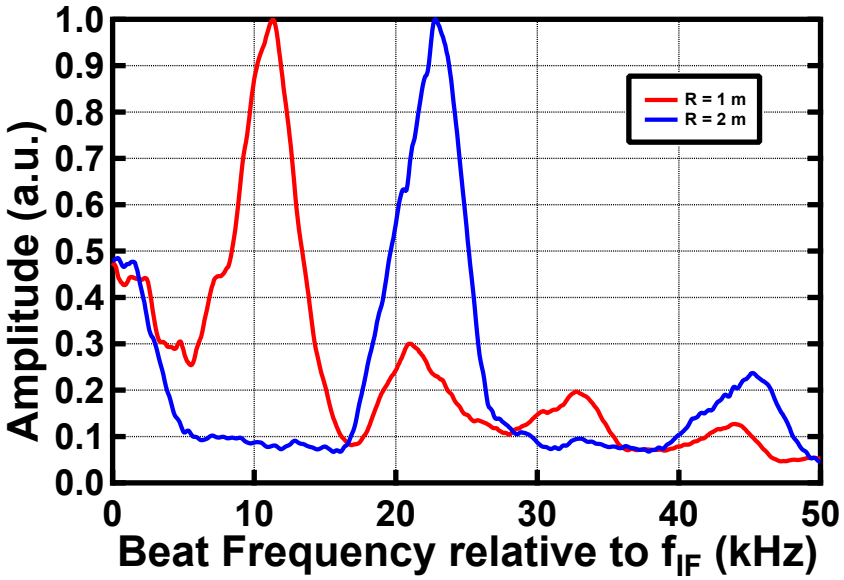

Figure 2.9: Range measurements with the 60-GHz COTS FMCW radar demo at the distance R = 1 m and R = 2 m [8].

2.4 FMCW Radar System Specifications

The results obtained from the COTS radar provided a better insight on how to design an FMCW radar. This section presents the link budget and explains the criteria to define the required specifications of the radar based on the detectability of the target and micro-Doppler extraction for VSM or gesture recognition.

2.4.1 Chirp Limitations

Table 2.2 shows different scenarios for a short-range radar with an estimated sensing rate or pulse repetition frequency (PRF) required depending on the application. The PRF does not strictly impose the modulation period T_m or the chirp duration T_c. In the case of human detection, the radar could be duty-cycled to perform a sweep during 100 ms and remain silent for 900 ms, reducing its average power consumption to only 10 %. Although, in the extreme case that T_c is equal to the inverse of the PRF then the beat frequency is calculated. The disadvantage of using the maximum T_c apart from continuously consuming power is the low beat frequency. Instead, if the radar can synthesis a chirp x10 faster to be configured with a 10 % duty cycle then the beat frequency would be x10 higher, farther away from the impact of TX-RX leakage.

In other scenarios like gesture recognition the required PRF is as high as 10 kHz [9], which already sets a tight constraint on the chirp slope and leaves less room for duty cycling. The fast chirp of 90 MHz/μs would bring the beat frequency of a target at 5 m to fall at 3 MHz. This is not convenient since the low-IF architecture previously discussed would be modulating the

Table 2.2: Beat frequency for different scenarios of a short-range radar with B = 9 GHz.

Sensing Application			Range		
			10 cm	1 m	5 m
Human detection:	PRF = 1 Hz	$\Rightarrow T_{c,max}$ = 1 s	6 Hz	60 Hz	300 Hz
VSM:	PRF = 10 Hz	$\Rightarrow T_{c,max}$ = 100 ms	60 Hz	600 Hz	3 kHz
Gesture recognition:	PRF = 10 kHz	$\Rightarrow T_{c,max}$ = 0.1 ms	60 kHz	600 kHz	3 MHz

beat signal already within few MHz and the idea of choosing an FMCW radar is to profit from the bandwidth compression and avoid the need of a high-speed ADC. In addition, a fast chirp is normally achieved at cost of nonlinearity which is given by [10]

$$\text{Lin} = \frac{\delta f}{B}, \tag{2.20}$$

where δf is the root mean square (RMS) frequency error. This nonlinearity affects the range resolution presented in Eq. (2.12), and it can be re-written as

$$\Delta R = \sqrt{\left(\frac{c}{2B}\right)^2 + (\text{Lin} \cdot R)^2}. \tag{2.21}$$

There is not a practical method to estimate the nonlinearity from the chirp slope to set a constraint but it can be used to set a maximum acceptable RMS frequency error. The ideal range resolution for the 60-GHz band is 16.67 mm, considering a maximum degradation up to 20 mm at a detection range of 5 m, then the nonlinearity should be less than 0.22 % meaning a maximum RMS error of 19.9 MHz. To avoid nonlinearity issues and high-speed ADCs, the fastest chirp is chosen 1 ms to obtain a maximum beat frequency of 300 kHz for a target at 5 m.

On the other hand, for VSM the sensing rate does not need to be very high because an average heart and respiration rate are about 80 beats/min (1.33 Hz) and 16 beats/min (0.27 Hz), respectively. Furthermore, the amplitude of the displacement for VSM does play a role in setting the parameters of the radar. Recalling Eq. (2.15), the amplitude of the beat phase depends on the amplitude of the displacement, and if the phase does not fall within the range $[-\pi, \pi]$ rad it experiences distortion. Taking into account that the beating of the heart and respiration induce a chest peak displacement of approximately 0.6 mm and 10 mm, respectively, then the calculated phase amplitude for heart beating is 1.43 rad, falling in the free-distortion range. However, in the case of respiration the calculated phase amplitude is 23.88 rad, therefore causing nonlinear distortion known as phase wrap around (PWA). Whenever phase detection suffers from PWA large harmonics components are created completely distorting the signal. In order to compensate PWA and perform a phase unwrapping technique the general condition

is given by [11]

$$T_c \leq \frac{c}{8\pi f_L r_{vs} f_{vs}}, \tag{2.22}$$

setting a constraint for the maximum chirp duration, T_c should be shorter than 80 ms.

2.4.2 Link budget and Trade-offs

Generally, when designing radios an important specification is the sensitivity and the SNR required to achieve it. However, in the context of radar the SNR is rather related to two specifications: range accuracy and false alarm ratio (FAR). The first was already introduced in Eq. (2.13) while the second is presented in [1]. There is no direct relationship between both specifications but they can be used independently to set a design constraint on the SNR. For example, a SNR of 15.4 dB is required to obtain a 99 % probability of detection and 10^{-8} probability of false alarm [1]. In addition, sub-mm range accuracy is important especially for short-range detection. A SNR of 12.2 dB is required to achieve a range accuracy of 1 mm according to Eq. (2.13). Since the latter is the most limiting constraint it will be used as reference for the rest of the analysis in this chapter.

The SNR is defined as the ratio between the power of the received signal and the power of the noise floor in the RX path, it can be expressed in dB as

$$\mathrm{SNR} = P_{RX} - \mathrm{N_{floor}}. \tag{2.23}$$

The first term on the right-hand side of Eq. (2.23) is estimated from the link budget equation given by

$$P_{RX} = P_{TX} + \underbrace{10\log_{10}\left[\frac{G_{TX}G_{RX}\lambda^2\sigma}{(4\pi)^3 R^4}\right]}_{\mathrm{FSPL}}, \tag{2.24}$$

where P_{TX} is the transmitted power, G_{TX} and G_{RX} are the TX and RX antennas gain, λ_c is the wavelength of the center frequency in the sweep, σ is the radar cross section (RCS), and R is the distance range from the radar to the target. The last term in Eq. (2.24) is also known as the free space path loss (FSPL). The second term on the right-hand side of Eq. (2.23) is calculated from

$$\mathrm{N_{floor}} = \mathrm{NF} + \underbrace{10\log_{10}\left(\frac{k_B T}{1\,\mathrm{mW}}\right)}_{-174\,\mathrm{dBm/Hz}} + 10\log_{10}(\mathrm{RBW}), \tag{2.25}$$

where NF is the noise figure of the RX path, k_B is the Boltzmann constant, T is temperature, and RBW is the resolution bandwidth. In practice, the latter is determined by the FFT integration window and to prevent introducing discontinuities of the triangular modulation then the observation window is chosen equal to a single chirp duration, setting RBW = $\frac{1}{T_c}$.

Eqs. (2.24) and (2.25) are replaced in Eq. (2.23) and it is solved for the NF to obtain

$$\mathrm{NF} = P_{TX} + \mathrm{FSPL} - \mathrm{SNR} + 174\,\mathrm{dBm/Hz} + 10\log_{10}(T_c)\,, \tag{2.26}$$

where the circuit designer has not much control on the FSPL and SNR, leaving three variables to trade off: P_{TX}, NF, and T_c. The two first corresponds to 1-to-1 trade-off between TX and RX design, for each extra 1 dB on TX power the RX NF can be relaxed by the same amount of 1 dB. For the third variable T_c is a trade-off between lowering the integrated noise by extending the observation window (reducing the RBW) in exchange for time resolution. Each doubling of the chirp duration relaxes in 3 dB any of the other specifications.

As a practical example some assumptions are taken to calculate the FSPL and represent the trade-off. The patch antennas are chosen similarly to [12] with a gain of 7 dBi. Especial attention should be given to the RCS because it depends on the geometry and material of the target, and in the case of monitoring people its modeling becomes a complicated task. According to [13] the RCS of an entire human body over azimuth average is between −7.7 to −3.0 dBsm. The wavelength is taken at the center of the frequency band $\lambda = 4.88$ mm, and the range R is set to 5 m. Fig. 2.10 shows graphically the behavior of Eq. (2.26) exhibiting the trade-offs.

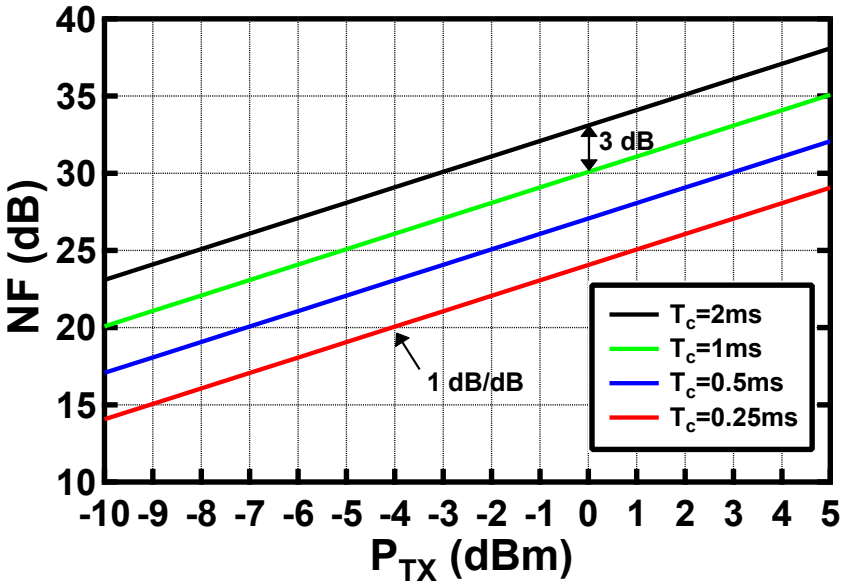

Figure 2.10: Design specification trade-off.

2.4.3 Design Specifications

The targeted radar specifications are chosen based on the range estimation accuracy which is ultimately limited by the SNR. Taking into account the low-power and short-range operation, the TX power is set to 0 dBm. The range detection is chosen to be within $R = [0.1, 5]$ m, and the FSPL are estimated as for Fig. 2.10, giving a calculated RX power of $P_{RX} = [-101, -33]$ dBm. The chirp duration T_c was already chosen equal to 1 ms and in turn the RBW is 1 kHz. These calculations result in a maximum NF of 30 dB to achieve a the desire SNR of 12.2 dB. So far the SNR has been calculated considering only thermal noise while phase noise was neglected thanks to the autocorrelation attenuation effect investigated in section 2.2.2. For the sake of completeness now let's consider both SNR contributions in the following expression

$$\frac{1}{\mathrm{SNR_{TOT}}} = \frac{1}{\mathrm{SNR_{TH}}} + \frac{1}{\mathrm{SNR_{PN}}}, \tag{2.27}$$

where the SNR due to phase noise is determined from the phase variance of the down-converted IF signal and given by

$$\frac{1}{\mathrm{SNR_{PN}}} = 2\sigma^2_{\Delta\phi_{IF}}. \tag{2.28}$$

The phase noise specification in this work is calculated similarly as in [10] based on the theory presented in [14]. The phase variance at the IF output is given by

$$\sigma^2_{\Delta\phi_{IF}} = \int_0^\infty S_{\Delta\phi_{IF}}(f)\, df = \frac{D_\phi}{\pi f_{PLL}} \left[1 - e^{-\frac{4\pi f_{PLL} R}{c}}\right], \tag{2.29}$$

where f_{PLL} is the PLL bandwidth and D_ϕ is the phase diffusivity. The latter is given by

$$D_\phi = 2\pi^2 S_{\phi,LO}(\Delta f) \cdot (\Delta f)^2, \tag{2.30}$$

where $S_{\phi,LO}(\Delta f)$ is the LO phase noise at a specific frequency offset Δf. For the required SNR, setting the PLL bandwidth to 200 kHz and maximum range to 5 m, the phase noise of the LO at 1 MHz frequency offset should be lower than -76.3 dBc/Hz.

Moreover, the SNR of a radar can be improved by two other means: MIMO and averaging. The former is due to the number of TX and RX elements creating an antenna array, compared to the case of a single-input single-output (SISO) radar. The latter is thanks to repeated measurements, where the signal increases by a factor of 6 dB because it is correlated but the noise is uncorrelated increasing only 3 dB. The system SNR is then given by

$$\mathrm{SNR_{SYS}} = \mathrm{SNR_{SISO}} + \underbrace{10\log_{10}(N_{TX}N_{RX})}_{G_{MIMO}} + \underbrace{10\log_{10}(N_{AV})}_{G_{AV}}, \tag{2.31}$$

where the product of TX and RX elements creates the number of virtual channels $N_{TX}N_{RX}$ providing a MIMO gain G_{MIMO}, and G_{AV} is the averaging gain. Finally, the specifications for the FMCW radar system are summarized in Table 2.3. The calculations did not consider the averaging or MIMO gain since the worst case is having only 1 TX, 1 RX, and with no margin on time resolution for averaging. The power consumption is chosen at least one order of magnitude lower than commercial short-range radars [15–17].

Table 2.3: FMCW Radar system target specifications.

Parameters	Symbol	Value	Units
Lowest frequency	f_L	57	GHz
Highest frequency	f_H	66	GHz
Bandwidth	B	9	GHz
Chirp duration	T_c	1	ms
Chirp slope	S	9	MHz/μs
Modulation period	T_m	2	ms
TX Output Power	P_{TX}	0	dBm
RX Noise Figure	NF	30	dB
LO Phase Noise 1 MHz	PN	−76.3	dBc/Hz
Power Consumption	P_{DC}	≤ 50	mW
Frequency resolution	Δf	1	kHz
Range resolution	ΔR	16.67	mm
Range accuracy	σ_R	1	mm
Target range	R	0.1 - 5	m
Beat frequency	f_b	6 - 300	kHz

2.5 Summary

This chapter describes the FMCW radar system with an emphasis on short-range applications. First, the basic concepts of an FMCW radar and equations are derived and applied to an user

case of human monitoring using realistic numbers revised before in Chapter 1. Second, a low-IF architecture is suggested in order to address the shortcomings of having a very low beat frequency because of the short-range detection. Third, a study is presented on the impact of phase noise on the proposed low-IF architecture, the calculations are validated through simulations and later also with measurements performed on a COTS radar. The results corroborate that properly designing a low-IF radar with a single-PLL enhances the phase noise performance especially at short distances from the radar.

Finally, from the results obtained before and a link budget analysis the specifications are chosen for the design of a low-power short-range FMCW radar. Given that this work does not focus on the design of frequency synthesis, the specifications related to phase noise will not be further addressed in the next chapters but it was introduced here given its importance for the operation of the radar system. Moreover, the goal is to use the specifications here to realize the design of the radar TX and RX in the subsequent chapters.

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3 Optimized 60-GHz Low-Power FMCW RADAR Transmitter

This chapter focuses on the design optimization of a low-power mm-wave TX as a part of a fully integrated 57-66 GHz FMCW radar. A TX architecture is proposed including a BPSK modulator and a target output power of 0 dBm. A band-tuning scheme is used for covering the 9-GHz bandwidth and it is tuned as the LO frequency is swept. The design also comprises the LO distribution in a modular approach to be able to extend the number of TX paths for MIMO operation. A second version is also implemented targeting to lower even further the power consumption of the TX path.

3.1 TX Architecture

The proposed TX architecture is shown in Fig. 3.1 and it consists of three stages: 1) LO buffer, 2) modulator, and 3) power amplifier (PA). The purpose of the buffer is to increase isolation between the local oscillator (LO) and the subsequent stages, including additional TX channels. The modulator is used to generate signals that are orthogonal between each TX channel, it operates using BPSK implemented by switching its differential branches. Finally, the PA is designed to deliver 0 dBm output power from a voltage supply of 0.8 V.

3.1.1 Amplification Stage

The three stages of the TX path are designed based on the neutralized bootstrapped cascode (NBC) amplifier topology [1]. The core schematic of this amplification stage is shown in Fig. 3.2 and it implements the three techniques for which is named after. The first technique used in the NBC amplifier is neutralization and it addresses a common problem at mm-wave: capacitances have a relatively small impedance. This is a particular problem in the common source transistor M_{CS} because its gate-to-drain capacitance $C_{CS,gd}$ creates a relatively low-impedance feedback path which can potentially cause stability issues. In order to guarantee an unconditionally stable amplifier, a cross-connected neutralization capacitor C_N is placed between the gate of the common source and the drain of the opposite differential branch to

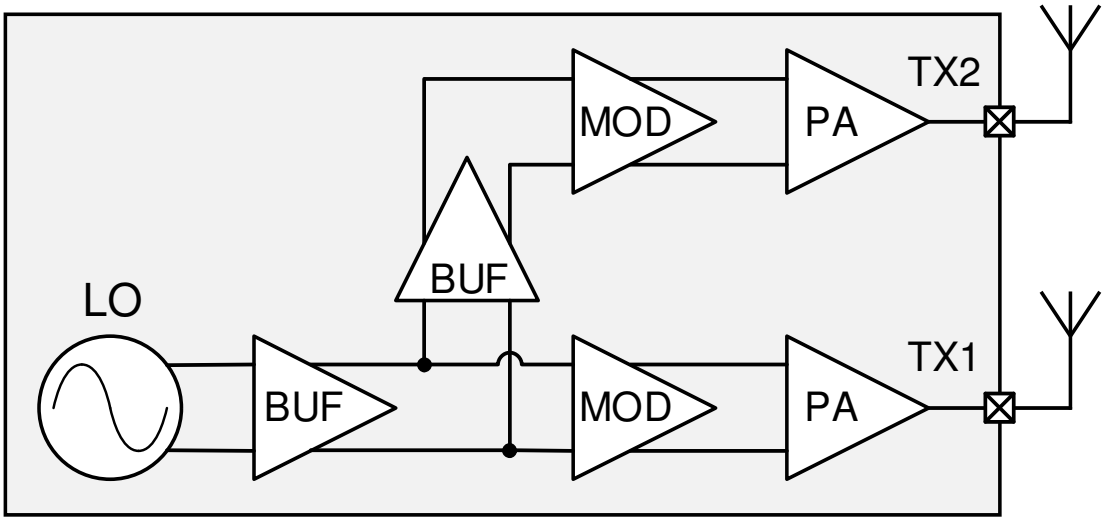


Figure 3.1: TX block diagram.

cancel out the effect of $C_{CS,gd}$.

The second technique is bootstrapping, it refers to the stacked transistor M_{ST} and its drain-to-source capacitance $C_{ST,ds}$ which presents a Miller effect. The resulting Miller capacitor can be seen as a capacitor in parallel to $C_{CS,ds}$. The value of the Miller capacitor is $C_M = (1 - A_{ds})\, C_{ST,ds}$, where A_{ds} is the voltage gain between drain and source of the stacked transistor. Conventionally, the voltage gain in the Miller effect is negative and C_M increases the factor $(1 - A_{ds})$, but in this case the voltage gain is positive and the effect produces a negative capacitance. The Miller capacitance is used to cancel out the parasitic $C_{CS,ds}$ that normally decreases the gain of the amplifier. The problem with increasing $C_{ST,ds}$ is that strengthens a feedback path that could lead to stability issues, therefore it cannot be increased above certain value. These techniques are process dependent because the value of the capacitors C_N and $C_{ST,ds}$ have to be matched to the respective capacitor that needs to be canceled out.

The last technique used in the NBC amplifier is cascoding, it is used to prevent stress in the transistors. The pseudo-differential amplifier is loaded by a transformer and the voltage supply is connected to the center tap (CT), meaning that without considering losses the output voltage could go as high as $2V_{DD} = 1.6\,\text{V}$. However, in the case of this technology node the safe operating area (SOA) for the drain-to-source voltage is $V_{ds,max} = 0.9\,\text{V}$. Two transistors are required to be compliant with SOA rules. A more precise naming for this topology is stacked rather than cascode, because the name cascode normally refers to a low impedance node in the drain of the common source resulting in a small voltage swing. However, in the case of NBC the purpose of the stacked transistor is to split the voltage swing as evenly as possible between the two transistors. This idea is implemented by placing just a relatively small decoupling capacitance in the gate of the stacked transistor allowing this node to have a weak coupling through $C_{ST,gs}$ increasing also the impedance in the drain of the common source and enabling a larger voltage swing.

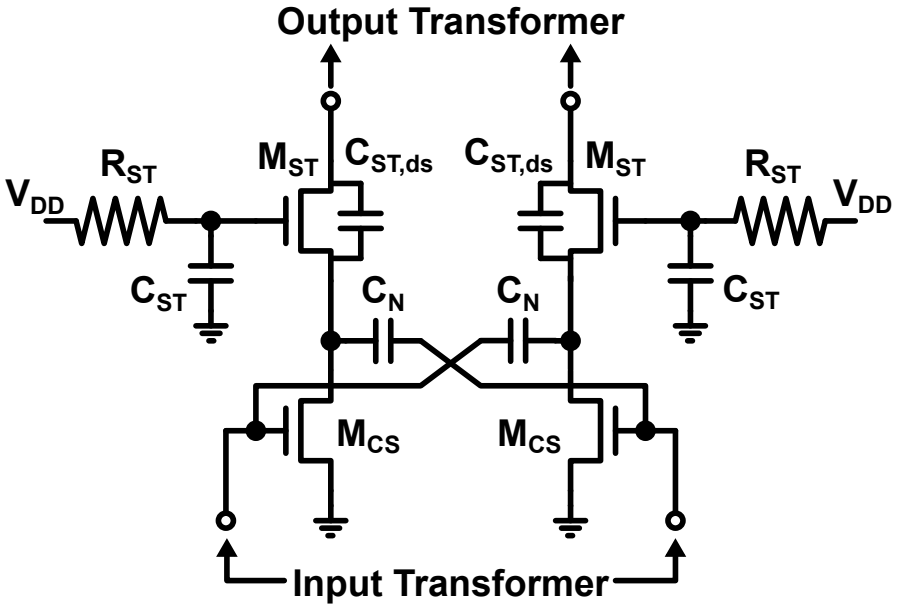


Figure 3.2: Neutralized stacked amplifier.

3.1.2 mm-wave Design Optimization

The performance of a circuit does not only depend on its topology but also on the technology used. There is a frequency limit of operation for transistors, two figures of merits (FoM) are commonly used: transit frequency f_T and maximum frequency f_{max}. The first one is defined as the frequency at which the current gain of a transistor becomes unity, it is measured by applying a test current source in the input and a short in the output. Although it is used as a reference as maximum frequency of operation it is not actually reliable at mm-wave because it neglects the influence of gate resistance and output impedance. They do not have a significant impact in the transistor performance at low frequencies but at mm-wave they do, and they could prevent a PLL from oscillate or drive an amplifier into unstable operation. On the other hand, f_{max} does take those parasitics into account because is defined as the frequency at which the power gain is equal to unity and it is measured for an impedance matched to the complex conjugate of the corresponding port. f_{max} increases with scaling down and it is strongly dependent on layout design [2, 3]. For this reason is required to move to advanced nodes, the technologies available is GF 22-nm FDSOI, which transistors have a f_{max} of more than 200 GHz, provided the layout is carefully designed for minimizing parasitics. The maximum frequency is given by

$$f_{max} \approx \frac{G_m}{2\pi C_{gs}} \sqrt{\frac{r_{ds}}{4R_G}} \approx f_T \sqrt{\frac{r_{ds}}{4R_G}}, \tag{3.1}$$

where G_m is the transistor transconductance which depends on the biasing, C_{gs} is the gate-to-source capacitance, R_G is the gate resistance, and r_{ds} is the drain-to-source resistance.

All of them depend on the total width W_{tot} of the transistor but the gate resistance R_G is the one parameter that strongly depends on how the total width is drawn: the finger width W_f and number of fingers N_f. The main contributors of R_G are shown in Fig. 3.3: gate interconnections $R_{G,int}$, horizontal gate resistance $R_{G,h}$, vertical gate resistance $R_{G,v}$, and non-quasi-static (NQS) resistance $R_{G,NQS}$.

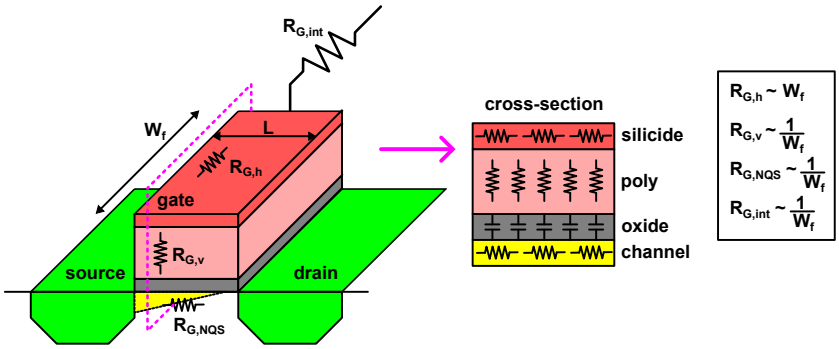
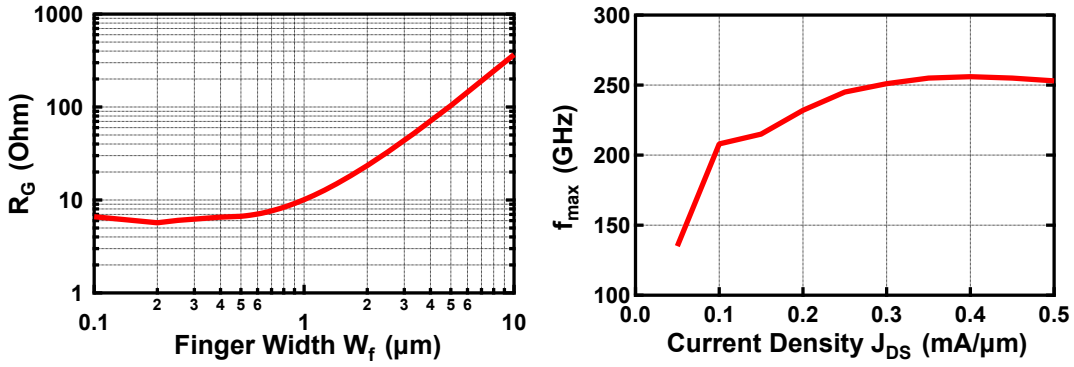


Figure 3.3: Gate resistance contributors [4].

It is important to correctly choose W_f and N_f in a transistor to minimize R_G and, consequently, increase f_{max}. The first step to minimize R_G is to avoid wide gates because $R_{G,h}$ greatly impacts the transistor performance causing voltage drops along the gate and affecting the current profile along the channel. The solution when having wide transistors is to split it into many fingers and use double-side connected gate-lines to each finger, thus the current is distributed more evenly in the transistor. The rest of the contributors are inversely proportional on W_f, the dependencies are shown on the right side of Fig. 3.3. There is an optimum W_f, just before the contribution of $R_{G,h}$ takes over the other contributors. Fig. 3.4a shows simulations performed in a 10-μm wide NMOS transistor for different W_f and N_f, the length is set to the minimum of $L = 20$ nm for better high-frequency performance. The transistor used for the simulations has an RF model which includes the parasitic components associated to interconnections up to metal M1. The result is that for a W_f below 0.2 μm the total gate resistance is due to interconnect, vertical, and NQS resistances, while above that value the horizontal resistance becomes dominant. For the current design a value of $W_f = 0.5\,\mu$m is chosen. Further narrowing of the finger width is not convenient because it limits the number of contacts that can be placed for source and drain connections.

Fixing $W_f = 0.5\,\mu$m and $N_f = 20$, then f_{max} is simulated for different current densities J_{ds} to show the trade-off between low-power design and operating frequencies. In Fig. 3.4b can be observed that a low current density as 0.05 mA/μm drops f_{max} below 140 GHz, nevertheless, the desired value for having enough power gain is at least 3 times the operating frequency. This is the reason why weak inversion is not suitable with sub-THz and mm-wave frequency bands, it is necessary to go to moderate or strong inversion to guarantee the device operation and thus higher power consumption. A value of 0.1 mA/μm is chosen as a good trade-off for low-power, obtaining a $f_{max} = 208$ GHz. For sizing the total transistor width the output impedance must be estimated. Considering an ideal full voltage swing in the PA stage, the



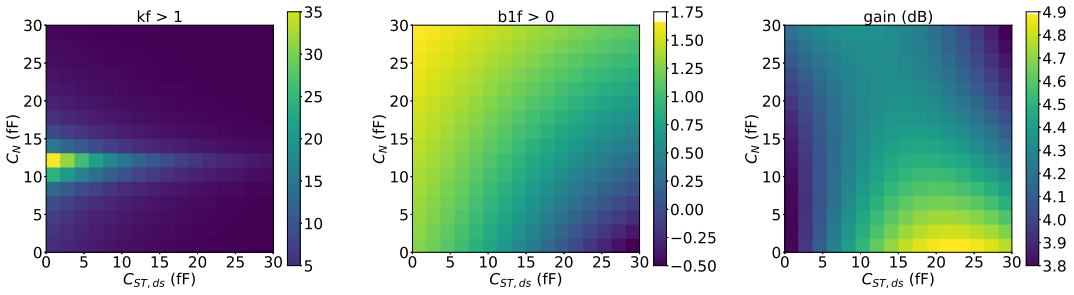
(a) (b)

Figure 3.4: Simulated (a) R_G vs. W_f for a 10-μm NMOS transistor, and (b) f_{max} vs. J_{DS} for W_f = 0.5 μm and N_f = 20.

differential peak voltage is equal to the voltage supply $V_{p,dif} = V_{DD} = 0.8\,\text{V}$. The target output power is 0 dBm, which requires a differential output impedance given by

$$R_{PA} = \frac{V_{p,dif}^2}{2P_{out}} = 320\Omega. \tag{3.2}$$

Both common-source and stacked transistors in the PA were sized with a total width of 48 μm based on the chosen finger width and current density to achieve the required output impedance. Once the PA has been sized correctly according to the inductive load and target output power, then C_N and $C_{ST,ds}$ can be chosen by simulating the Rollet stability factor Kf, the alternative stability factor b1f (appendix A), and the trade-off with power gain. The PA is stable for Kf > 1 and b1f > 0.



(a) (b) (c)

Figure 3.5: Simulated (a) Rollet stability factor Kf, (b) alternative stability factor b1f, and (c) power gain.

Fig. 3.5a shows that the Rollet stability factor is maximized for C_N = 12 fF, meaning that the feedback path created by capacitance $C_{CS,gd}$ is canceled out. On the other side, if $C_{ST,ds}$ is

increased the gain is improved, however, above certain value the PA approaches instability as exhibited by b1f. For a good trade-off between stability and gain the values chosen are C_N = 12 fF and $C_{ST,ds}$ = 18 fF.

3.1.3 Passives and Matching Network Optimization

At 60 GHz the design of passive devices becomes more critical than at lower frequencies because any additional parasitic can shift the resonance frequency out of the band of interest. A brief description of the passives used in the TX signal path is presented in the following sections, all of them were initially synthesized by *VeloceRF* from *Helic*, but for each different stage they had to be customized.

Balun and GSG

The applications for SRD do not require high output power, therefore having a supply of 0.8 V and output load of 50 Ω would consume more power than needed. A balance-to-unbalance (balun) transformer is chosen to be used for four reasons:

- Impedance transformation to implement a large impedance for the required power budget.
- Provides a differential load to the PA output enabling neutralization topology.
- Provides galvanic isolation, no need for electrostatic discharge (ESD) protection which would add larger capacitors.
- Transformers cancel out the magnetic field inside and far outside the turns.

Fig. 3.6 shows the balun model and its layout including the ground-signal-ground (GSG) pads. The matching approach is shown at the bottom of the figure, it is obtained by reflecting the impedances from the secondary to the primary. On the right side of the circuit the capacitor C_S is placed to resonate out the inductance L_S. On the left side of the circuit an L-matching network is implemented to transform the load impedance R_L to match Z_{PA}. The GSG structure is designed to match the load impedance R_L equal to 50 Ω. Furthermore, the goal is to make the secondary inductance L_S resonate without the need to add a functional capacitance. There is a parasitic capacitance already present in the GSG structure. This capacitance is equal to 44.6 fF and plays the role of C_S. On the primary side, the L-matching network is designed for the same frequency as the secondary. Contrary to the transformer-based fourth order matching network [5] that provides a wider bandwidth, this design opts for a tuned transformer for a higher quality factor to improve efficiency. The penalty of this design choice is a narrower band. Nevertheless, this is not a problem for FMCW radars since they do not need a constant wide band. A band-tuning scheme is implemented by a capacitor bank, it tunes the narrow band of the matching network synchronously as the FMCW chirp is swept.

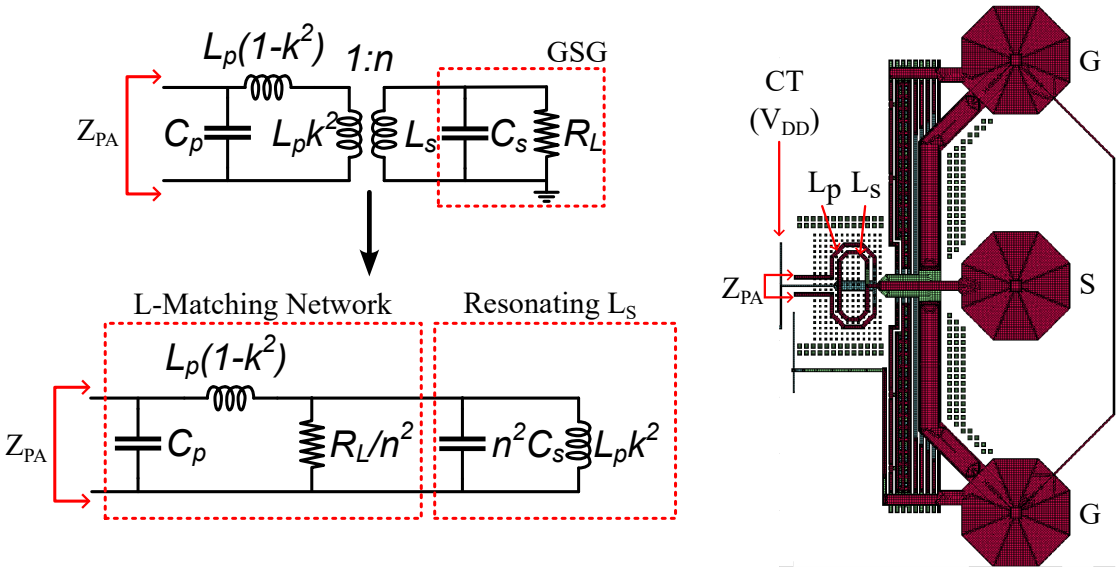
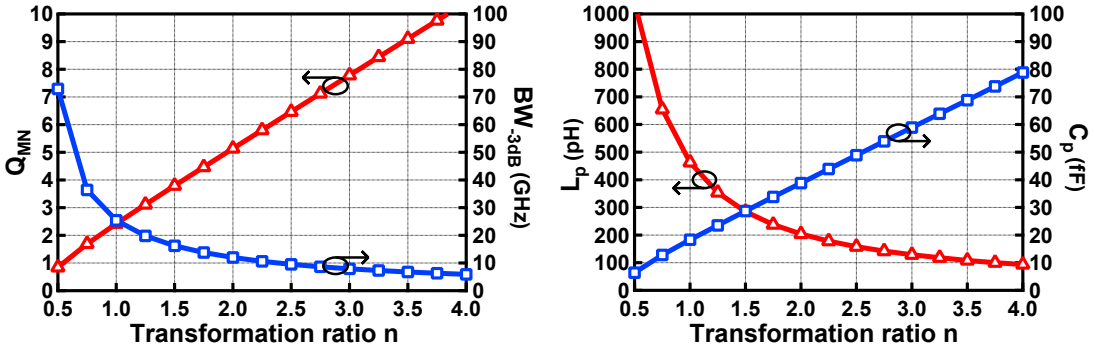


Figure 3.6: Output matching network of PA.

The impedance $Z_{PA} = R_{PA} \,//\, C_{PA} = 342.2\,\Omega//18.48\,\text{fF}$ is determined by a load-pull simulation of the extracted PA layout in order to achieve maximum efficiency. For the given GSG capacitance C_S, the secondary inductance L_S must be designed for 150 pH. The quality factor of the matching network, Q_{MN} is defined by the impedance transformation ratio n,

$$Q_{MN} = \sqrt{\frac{R_{PA}}{R_L/n^2} - 1}. \tag{3.3}$$



(a) (b)

Figure 3.7: Calculated: (a) Quality factor and bandwidth (b) inductance and capacitance on the primary of the balun.

Fig. 3.7a shows the quality factor Q_{MN} and 3dB-bandwidth of the matching network depending on n. Fig. 3.7b shows the corresponding inductance and capacitance required on the primary of the balun to match the impedance to Z_{PA}. Designing the balun for a wide bandwidth requires a small transformation ratio and consequently a lower quality factor. This structure

would be very difficult to design because the required L_P is very large compared to L_S. In addition, the tuning capacitance C_P in the primary is very small, thus leaving very small margin for parasitic capacitances created by interconnections. Instead, the band-tuning design in this paper targets a transformation ratio n = 3.5. It provides a larger margin on the parasitic capacitance in the primary and a smaller inductance ratio feasible to design at mm-wave. The calculated quality factor of the matching network is 9 and the 3-dB bandwidth is approximately 6 GHz. The tuning capacitor banks are designed to switch in 1-GHz steps and are implemented for each of the transformers in the TX path.

The balun layout shown on the right side in Fig. 3.6 is designed as a co-planar structure, it uses the redistribution layer in order to minimize the parasitic capacitance from the bottom surface to the substrate but also to reduce the fringe capacitance compared to the case of using ultra thick layers. This type of structure with lower capacitive and magnetic coupling can achieve higher self-resonances frequency (SRF), maintaining a high quality factor and providing larger margin for parasitic capacitances. The small metal squares around the balun is the dummy filling which is required in higher densities in advanced nodes. The effect of dummy filling decreases the quality factor of the balun but it is a strict rule imposed by the manufacturer and it has to be taken into account during electromagnetic (EM) extractions. Finally, the center tap (CT) needs to be routed to the voltage supply which is on the upper side of the balun. The routing is kept symmetric to the balun until it is far from it to prevent asymmetries on the balanced side of the balun connected to the PA.

Tuning Capacitor Bank

Each stage can be tuned using capacitor bank controlled by thermometer codes to guarantee monotonicity and avoid glitches during the FMCW sweep. The switches are implemented differentially as shown in Fig. 3.8, where V+ and V- are connected to the tank of the amplification stage. The transistors used for the switches are thick gate devices because of the large voltage swing between the RF nodes connected to the drain/source and the control signal (SW) connected to the gate.

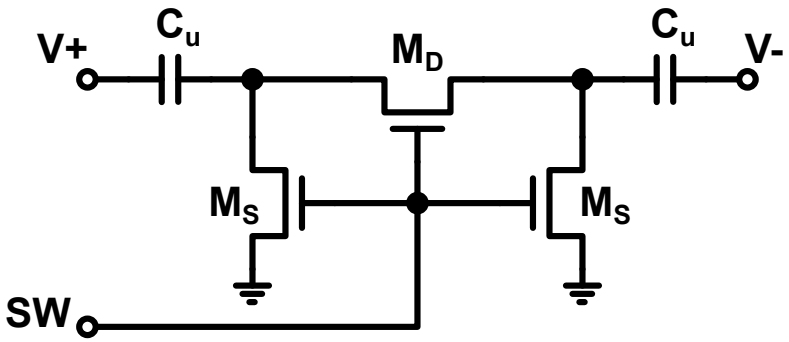


Figure 3.8: Differential switch capacitor schematic.

The idea of this differential switch is to halve the on-resistance of the differential transistor

M_D which appears in series with the unit capacitors C_u. It allows to achieve a given series resistance with half the transistor width required. The single-ended transistors M_S are placed to define a common-mode level to the drain and source of M_D, thus they can be minimum-size devices [6]. All transistors have their front and back gate shorted to achieve a better R_{on}/R_{off} ratio.

Interstage Transformer

The interstage transformer is a more efficient way to couple the output signal of one stage to the input of the next stage because at high frequencies the quality factor of inductances is higher than capacitances. This transformer shown in Fig. 3.9 is designed with stacked turns for high coupling factor which provides a wider operating bandwidth. The disadvantage of having a stacked transformer is the lower SRF compared to a co-planar transformer and the reduced margin for parasitic capacitors. Moreover, it is difficult to synthesize a large characteristic impedance on-chip because it is proportional to $\sqrt{\frac{L}{C}}$, where the parasitic capacitance usually sets an upper limit. Given that the transistors are kept relatively small to achieve a high enough f_{max} (see Fig. 3.4b), the input impedance of the amplification stage is in the order of hundreds of Ω or a few $k\Omega$. The interface transformer-amplifier cannot be matched but the transformer is designed to target the maximum impedance possible, and accounting for dummy filling, it reached an impedance ratio of 100 Ω:100 Ω. This structure is used as load for the modulator and buffer stage.

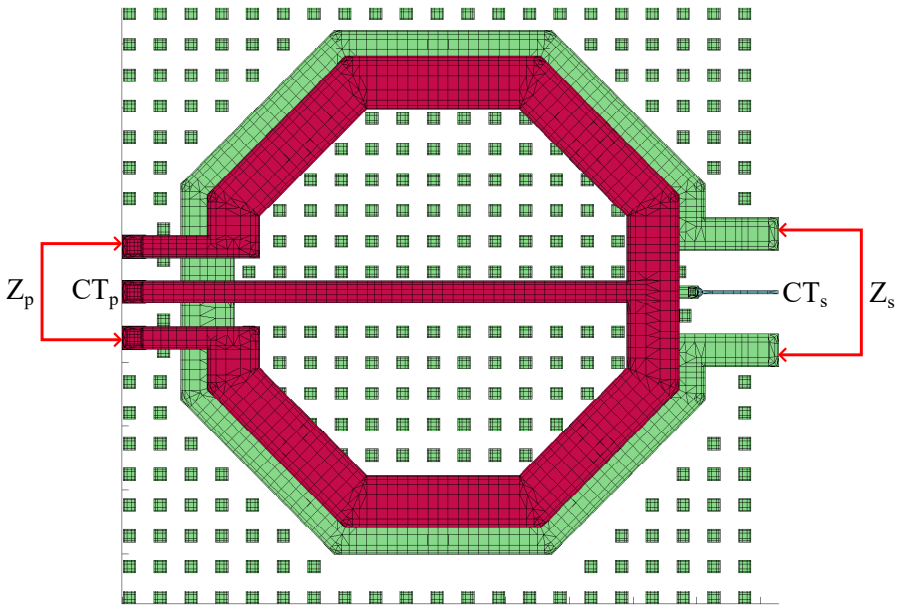


Figure 3.9: Interstage transformer layout.

100-Ω Differential TL

A 100-Ω differential transmission line (TL) is designed to distribute the 60-GHz differential signal. The TL is designed as a coplanar waveguide as shown in Fig. 3.10 with a total width of 14 μm. Its small dimensions make it suitable to be placed in narrow places such as in between TX stages. The TL is routed with thick metal (in cyan), while the ultra thick metal is reserved for supply lines that require very low resistive losses. The compactness of the TL also comes at the cost of relatively high losses and they should not be used to route long connections. The main parameters of the TL can be seen in Table 3.1.

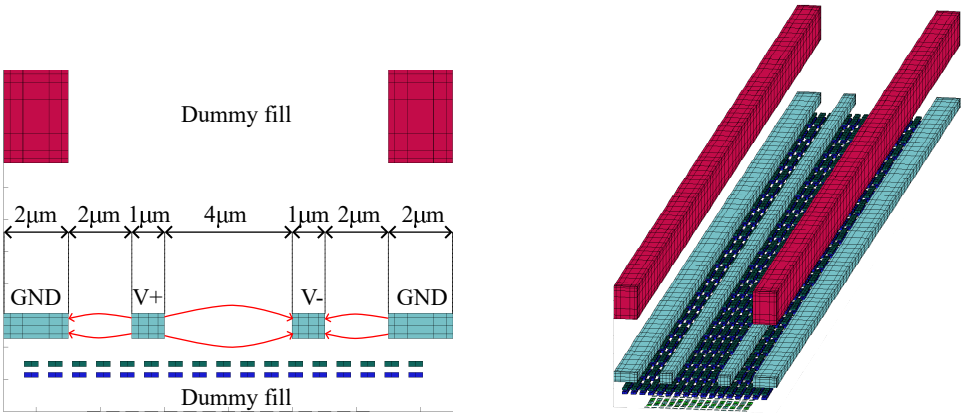


Figure 3.10: Differential TL layout: (a) Cross-section, and (b) 3D view.

Table 3.1: Characteristics of the 100-Ω differential TL 61.5 GHz.

Parameters	Symbol	Value	Units
Real characteristic impedance	$Re(Z_C)$	112.90	Ω
Imaginary characteristic impedance	$Im(Z_C)$	−8.92	Ω
Attenuation constant	α	2.24	dB/mm
Phase constant	β	172.30	deg/mm
Quality factor $\beta/2\alpha$	Q	5.84	-
Effective dielectric constant	ϵ_{eff}	5.46	-
Propagation velocity	v_p	1.28×10^8	m/s
Guided wavelength	λ_{guided}	2.09	mm

3.1.4 Simulation Results

The complete TX path is driven by the LO and it consists of three stages. The LO driving the TX channel is an on-chip 60-GHz Digital-Controlled Oscillator (DCO) with a peak amplitude of 200 mV. The first stage of the TX path is a LO buffer, its schematic is shown in Fig. 3.11. The topology and transistors size is based on the previous discussion in sections 3.1.1 and 3.1.2. The LO buffer was closely co-designed with the DCO to maintain a symmetric load and isolate it from the impact of potential harmful blocks such as the PA. The coupling capacitor used to connect the DCO with the buffer is large enough not to attenuate the signal and the entire structure was extracted with an EM tool to account for all parasitic components.

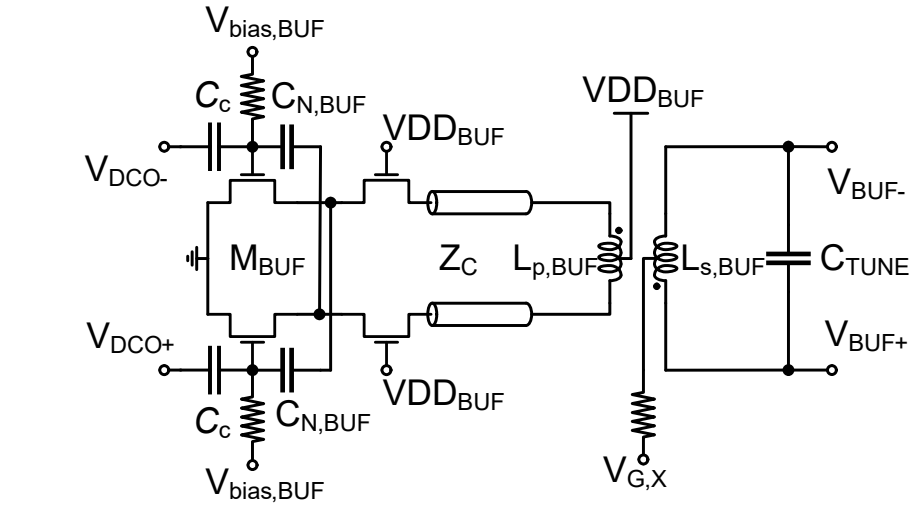
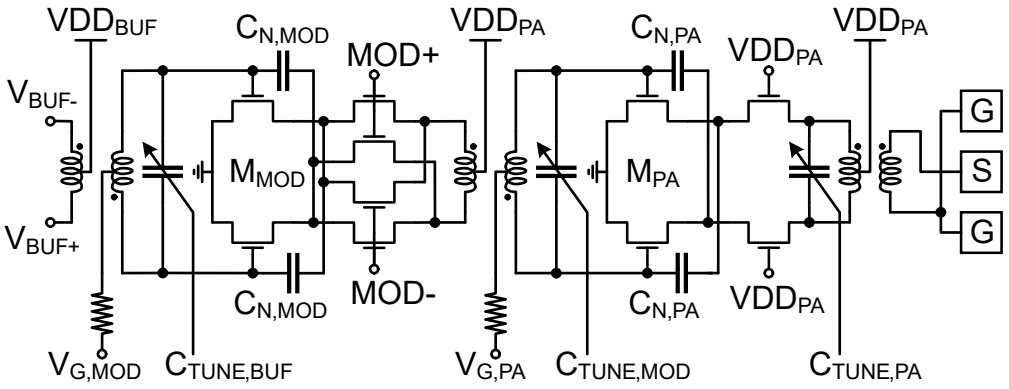


Figure 3.11: LO buffer schematic.

The schematic of the rest of the TX path is shown in Fig. 3.12. The second stage is a BPSK modulator used to implement the low-IF architecture. This stage includes two more branches of stacked transistor cross-connected. The low-IF modulating signal is applied to the gates of these four stacked transistors as in a double-balanced mixer. The BPSK modulators are orthogonal for each TX path to be able to separate signals in RX. The third and last stage is the PA, it is designed to deliver 0 dBm output power on a voltage supply of 0.8 V.

The center tap of each primary coil is connected to the corresponding supply voltage. These supplies are provided by different low-dropout (LDO) regulators to increase isolation and prevent coupling between stages. The center tap of each secondary is used to bias the common-source transistor of the amplification stage, where the biasing is controlled by a 4-bit current DAC. The full TX path has been extracted using Calibre RCC including all tuning capacitor banks and biasing circuits. All passive structures such as transformers, balun, and TL have been extracted using EMX.

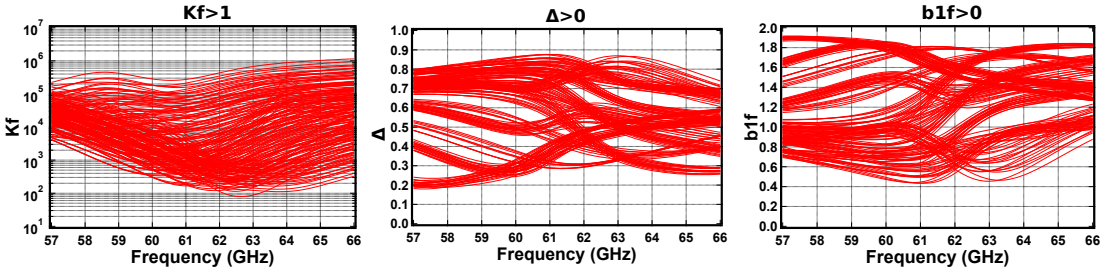


MOD	M_{MOD} = 16µm/20nm $L_{p,MOD}$=114pH $L_{s,MOD}$=117pH $C_{TUNE,MOD}$= 6-27fF $C_{N,MOD}$ = 4fF $Q_{p,MOD}$=14.1 k_{MOD}=0.83 $Q_{s,MOD}$=13.8
PA	M_{PA} = 48µm/20nm $L_{p,PA}$=99pH $L_{s,PA}$=160pH $C_{TUNE,PA}$ = 24-39fF $C_{N,PA}$ = 12fF $Q_{p,PA}$=8.4 k_{PA}=0.59 $Q_{s,PA}$=7.3

Figure 3.12: TX schematic: Modulator + PA.

Stability

The most critical part for an amplification stage is stability, because if unconditional stability is not guaranteed then the amplifier itself could start oscillating. As mentioned before, it is particularly important at mm-wave since capacitances represent smaller impedances adding stronger undesired feedback paths leading to instability. For this type of simulation an input port is used rather than the actual DCO.



(a) (b) (c)

Figure 3.13: Simulated: (a) Rollet stability factor Kf, (b) determinant Δ, and (c) alternative stability factor b1f, across all corners: T = −40, 27, 85 °C, VDD_{BUF}, VDD_{PA} = 0.8 V ± 10 %.

In order to guarantee unconditional stability, a S-parameter analysis is performed for all corners: TT, FF, SS, FS, SF, for temperature of −40, 27, 85 °C, and supply voltage of 0.8 V within a 10 % margin. The figure of merit (FoM) used to measure stability is the Rollet stability factor Kf and its determinant Δ, shown in Fig. 3.13. The former must be larger than 1 while the latter must be positive, proving that for all cases the TX path is unconditionally stable. An additional

validation is done through the b1f parameter which is the alternative stability factor given by the Spectre simulator and it also proves stability across the wide operating bandwidth.

3.1.5 Measurement Results

The TX was fabricated in GF 22-nm FDSOI CMOS technology and was tested mounted on a board through on-chip probing using 200-μm pitch GSG probes (Picoprobes Model VMM65). The probe is connected through a coaxial 1-mm cable to a coax-to-waveguide adapter (V281C). The operating frequency was measured by means of a Keysight PXA Signal Analyzer N9030A using a Waveguide Harmonic Mixer M1970V to extend the range from 50 to 75 GHz. Power measurements are conducted using an Agilent Power meter E4419B with a waveguide adapter for 50 to 75 GHz. The chip microphotograph with two TX channels is shown in Fig. 3.14. The upper TX1 ground pad overlaps with the lower TX2 ground pad, the ground pad is shared to save area and shorten connections.

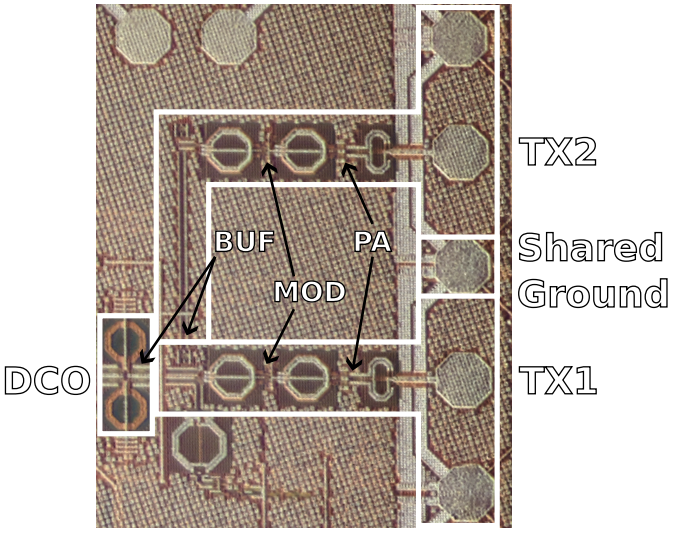
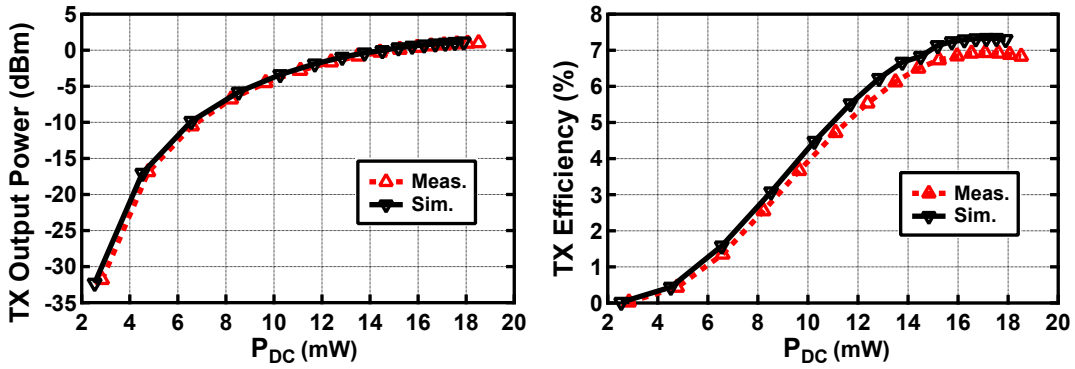


Figure 3.14: TX microphotograph.

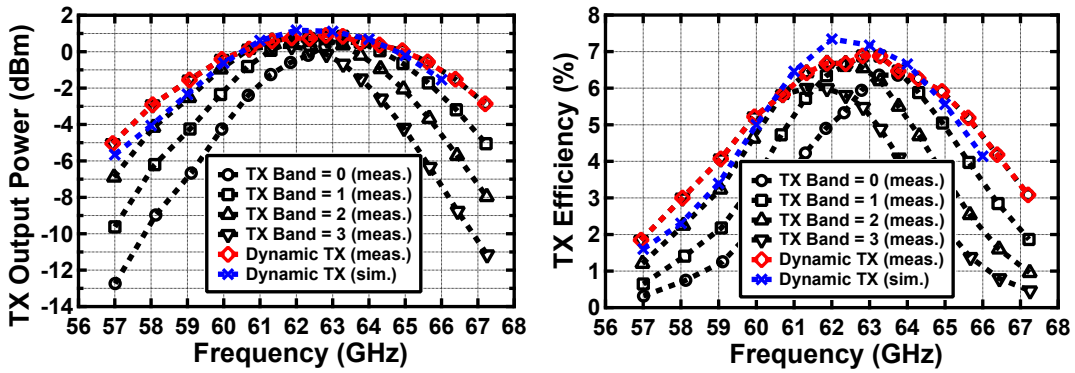
The LO driving the TX channel is a DCO with a peak amplitude of 200 mV covering a wide frequency range in the 60-GHz band. The efficiency of the TX is defined as the ratio between the output power and the total DC power consumption of the entire TX path (buffer + modulator + PA). In Fig. 3.15, the output power and TX efficiency are measured for a fixed frequency of 62 GHz versus the power consumption which is increased by controlling the current biasing DAC. The saturated output power is 1 dBm consuming as low as 17.1 mW for maximum TX efficiency. A good matching between measurements and simulations results is observed with only a small degradation on the TX efficiency coming from underestimated resistive losses in the ground connection routing.

Fig. 3.16 shows the saturated output power and efficiency versus the frequency for the multiple tuning bands. The output power varies from −5 to 1 dBm across the 9 GHz bandwidth. In



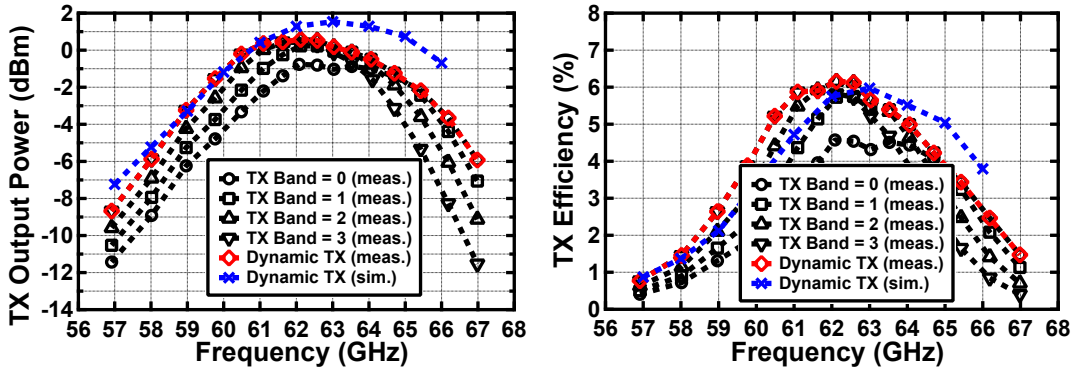
(a) (b)

Figure 3.15: TX Measurements versus power consumption at 62 GHz: (a) Output Power (b) TX Efficiency.



(a) (b)

Figure 3.16: TX1 Measurements versus frequency: (a) Output Power (b) Efficiency.



(a) (b)

Figure 3.17: TX2 Measurements versus frequency: (a) Output Power (b) Efficiency.

Fig. 3.17, the measurements of channel TX2 show a slightly narrower band compared to TX1. The parasitic capacitance in the TL distributing the LO signals to the TX2 was underestimated. This TL can be observed vertically in Fig. 3.14 routed from TX1 to TX2 with an approximated

length of 400 μm. The reason for the underestimated parasitic capacitance is due to several supply, ground, and control lines crossing this long TL that were not included in the EM extraction. Thus the band-tuning step is smaller than the expected 1-GHz step and the saturated output power is lower at the edges of the operating band. The power consumption of buffer, modulator, and PA is 3 mW, 4.3 mW, and 9.8 mW respectively.

3.1.6 Lessons Learned

The good matching between simulation and measurement results shown in the previous section were obtained after correcting a few mistakes done during the design phase. There are three main modifications to take into account for future passives design at mm-wave: 1) ports, 2) ground extractions, and 3) symmetry.

Port types

During the design phase of the presented TX, the EM tool used for extracting the S-parameters of passive structures was Ansys RaptorX (former Helic). This EM tool proved to be accurate for extracting inductors and transformers, however when extracting a structure as GSG pads it was less accurate. Later on another EM tool, Cadence EMX, became available. This tool introduced the concept of edge and internal ports. The edge port assumes the current is uniformly injected through the entire edge. The internal port assumes that the current is injected uniformly into a square of the specified size around the port (from top). To the best of our knowledge, RaptorX does not handle the concept of internal ports which is actually the exact case for structures such as GSG where the current is injected from the top with the probes and not through an edge. In Fig. 3.18, the layout of the GSG pads is shown depicting where the current is injected in each corresponding port case.

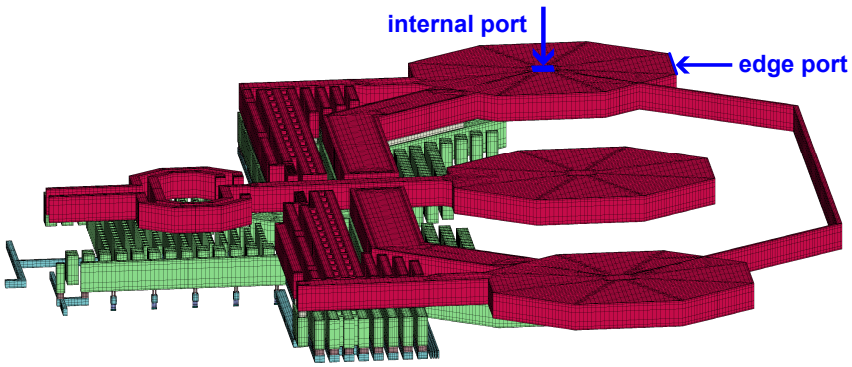


Figure 3.18: Type of port in the EM extraction of the GSG pads.

Ground extraction

The second lesson learned is to extract as exhaustively as possible the passive structure and do not take for granted that any of the ground routing is negligible. A section of the PA ground connection is drawn using a minimum-width thick metal and, since it has relatively low sheet resistance, the connection was assumed negligible and it was not extracted. Nevertheless, that ground connection has a non-negligible resistance of 1.89 Ω causing a voltage drop of ~ 24 mV which degraded the performance of the PA.

The effects of port type and complete ground extraction are simulated and compared to measurements in Fig. 3.19. The edge port simulation using RaptorX on the GSG pads overestimates the output power and bandwidth. The simulations replacing the edge port for an internal port using EMX get closer results to measurements. Finally, including the proper ground extraction provides the most precise matching to measurements.

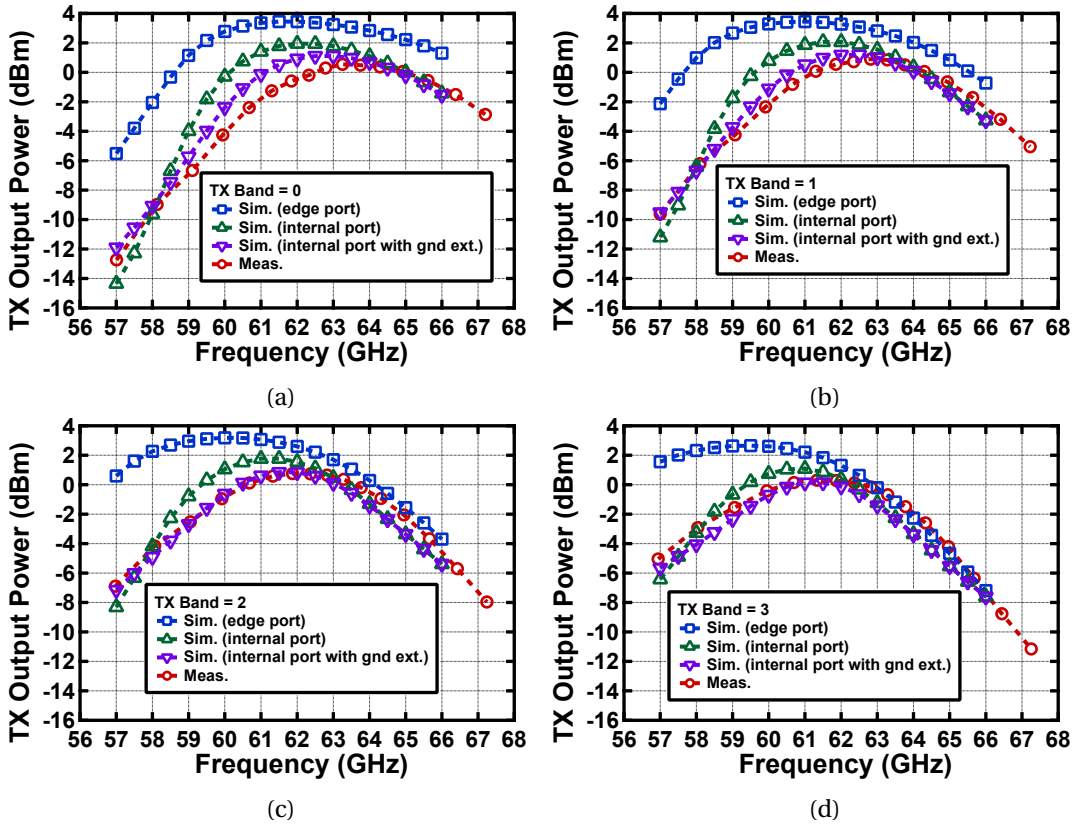
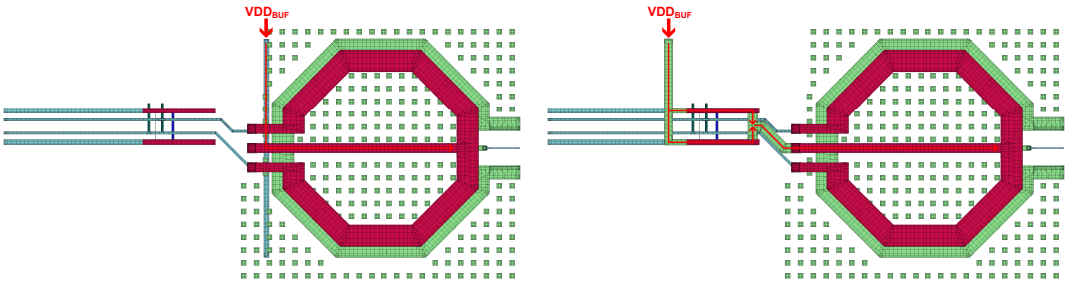


Figure 3.19: TX1 EM extraction improvement.

Symmetry

The third lesson to keep in mind is symmetry in our differential and balance circuits. For instance, in the LO buffer stage the transformer used should be a balanced-balanced structure. However, asymmetries are difficult to avoid in actual implementations such as in Fig. 3.20a

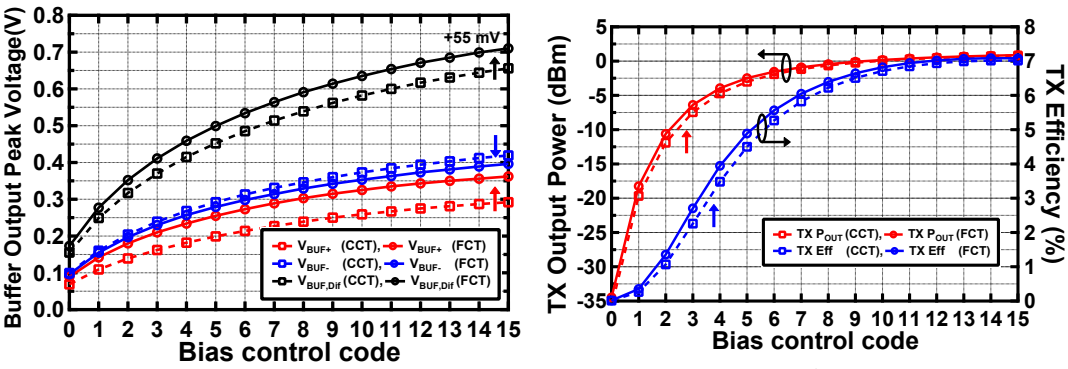
where the connection of the primary CT of the transformer is routed upwards to the LDO supplying VDD_{BUF}.



(a) (b)

Figure 3.20: LO buffer transformer layout: (a) Close asymmetric CT connection (b) Far asymmetric CT connection.

In Fig. 3.20b is shown how the asymmetry has been moved farther from the transformer by routing the CT connection below the ground shields of the TL. Once the CT routing is far enough from the transformer it is routed upwards to the LDO. The comparison of the close CT (CCT) connection and far CT (FCT) connection is shown in Fig. 3.21a through the buffer output peak voltage. The output voltage difference between V_{BUF+} and V_{BUF-} nodes in the buffer with a CCT is around 150 mV. This difference reduces to 40 mV with a FCT making the structure more symmetric and enhancing the overall performance of the differential buffer by an increase of 55 mV in the differential voltage $V_{BUF,Dif}$. On the other hand, the output power and efficiency are only marginally improved because the modulator and PA stages are dominant compared to the buffer, however symmetry must be reinforced whenever possible. For practical reasons the asymmetry of routing towards the voltage supply cannot be avoided in most cases, a solution is to move the asymmetry as far as possible from the transformer coils.



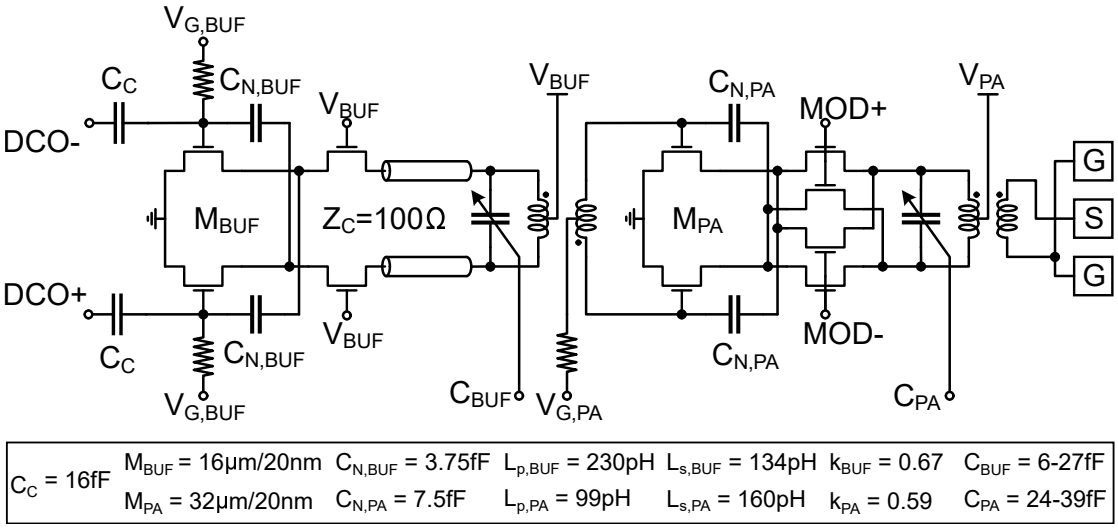
(a) (b)

Figure 3.21: Asymmetry effect on the LO buffer output: (a) Output Peak Voltage (b) TX Output Power and Efficiency.

3.2 TX Power Mixer

3.2.1 Merging Functionalities

A second version of the TX path was designed aiming to maintain a similar performance to the previous and further lower the power consumption. The idea in this new TX is to merge functionalities. The modulator and PA stages present in section 3.1 have been combined into a single stage named Power Mixer (PAMIX) in order to save power and area. The buffer stage has been kept the same as before but the PAMIX transistors have been modified with a scale factor of 2/3 of the original PA design for maximum efficiency based on load-pull simulations.



C_C = 16fF	M_{BUF} = 16µm/20nm	$C_{N,BUF}$ = 3.75fF	$L_{p,BUF}$ = 230pH	$L_{s,BUF}$ = 134pH	k_{BUF} = 0.67	C_{BUF} = 6-27fF
	M_{PA} = 32µm/20nm	$C_{N,PA}$ = 7.5fF	$L_{p,PA}$ = 99pH	$L_{s,PA}$ = 160pH	k_{PA} = 0.59	C_{PA} = 24-39fF

Figure 3.22: TX schematic: LO buffer + PAMIX.

Another important modification was the redesign of the balun in which the redistribution layer is replaced by the ultra thick layer enlarging the bandwidth and reducing insertion losses.

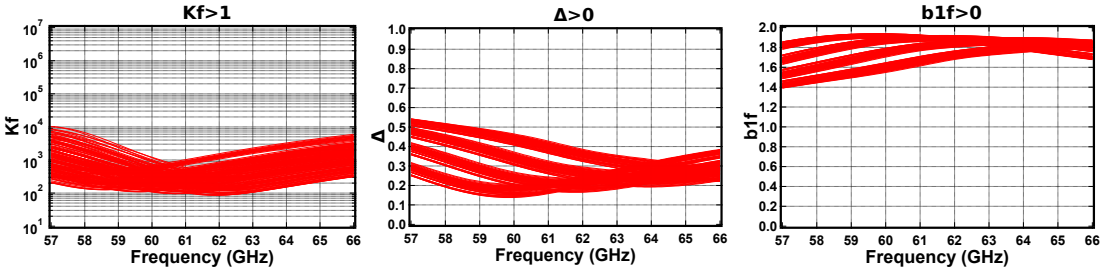
3.2.2 Simulation Results

Stability

The stability of the new TX with the PAMIX is simulated to guarantee that the amplifier does not oscillate. A S-parameter analysis is performed for all corners TT, FF, SS, FS, SF, for temperature of −40, 27, 125 °C, and supply voltage of 0.8 V within a 10 % margin. Unconditional stability is validated in Fig. 3.23.

Safe Operating Area (SOA) and Aging

According to manufacturer, there are safe operating area (SOA) rules to avoid stressing the transistors thus shortening their lifetime and performance. A potential problem was identified



(a) (b) (c)

Figure 3.23: Simulated: (a) Rollet stability factor Kf, (b) determinant Δ, and (c) alternative stability factor b1f, across all corners: T = −40, 27, 125 °C, VDD_{BUF}, VDD_{PA} = 0.8 V ± 10 %.

in the PAMIX regarding the maximum drain-gate voltage V_{dg}, specifically in the switching stacked transistors. Whether modulation is enabled or not, there are always two transistors that remain off, as indicated in the red circle in Fig. 3.24. The DC voltage of the drain node in the stacked transistors is the same as the voltage supply of 0.8 V because it is connected through the CT of the balun. The voltage in the nodes can be observed by running a transient simulation, setting MOD+ to 0.8 V and MOD- to 0 V, then V_{dg} ranges from 0.4 to 1.2 V stressing the transistors over the SOA limit of 0.9 V. This problem was not seen in the section 3.1 because the stacked transistors in the modulator were thick gate devices to tolerate the voltage stress at the cost of a larger voltage threshold. However, the PAMIX is the last stage of the TX path and any loss would have a greater impact in the final output power, therefore faster thin gate devices are chosen for all transistors.

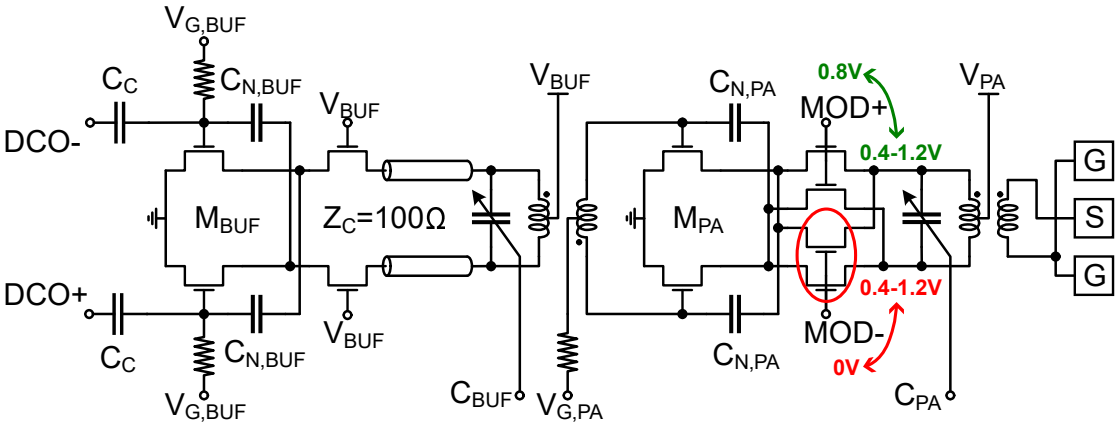


Figure 3.24: Voltage swing in the PAMIX cascode above SOA limits.

The design was intended to operate in stress to benefit from performance of thin gate instead of using thick gate transistors. The impact of stress has been simulated by using Spectre Native aging simulator. This tool runs three different simulation scenarios: fresh, stress, and aged. The fresh one is a typical simulation, the stress one should be run with increased voltage supplies and temperature, and the aged one uses the information of the stress simulation to estimate the performance in the future.

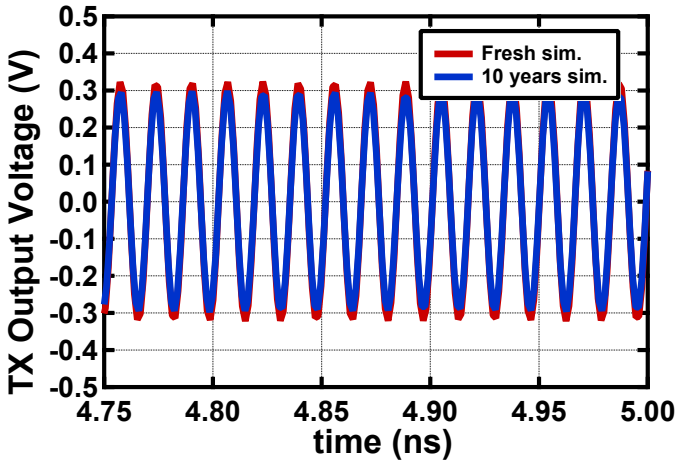


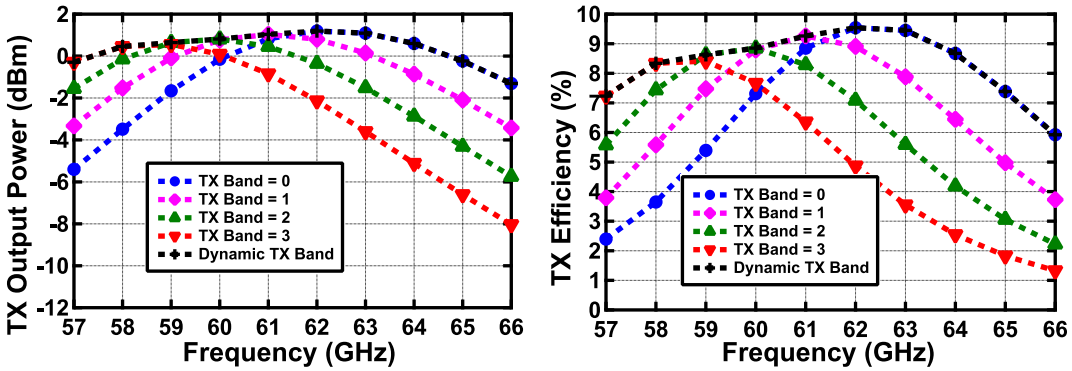
Figure 3.25: Transient fresh vs. aged simulation @ 61 GHz.

The voltage supplies are stressed to 1.1 V instead of the typical 0.8 V, and temperature is set to 125 °C instead of 27 °C. In order to simulate the worst-case scenario, MOD+ is set to 0.8 V and MOD- to 0 V in the fresh and stress simulation to stress the transistors in the red circle, but for the aged simulation MOD+ is set to 0 V and MOD- to 0.8 V to operate the transistors that have been stressed. The simulator does not support Harmonic Balance (HB) thus a transient simulation is chosen and the results are shown in Fig. 3.25. The calculated output power from the transient simulation is degraded only 0.8 dB after 10 years, proving that the voltage stress does not have critical effects in the lifetime operation of the radar TX.

TX Output Power and Efficiency

The TX path is composed of a LO buffer and a PAMIX, each stage has a current DAC to control its biasing. The TX was designed to operate as a saturated class AB amplifier which is one of the most power efficient designs considering that others like switching amplifiers cannot achieve square waves at mm-waves. The output power is not constant along the wide bandwidth because of the limited bandwidth of the amplification stage and its respective passive load. The implementation of band-tuning scheme using the thermometric capacitor banks makes it possible to have a more similar output power delivered along the 9 GHz bandwidth. The power consumption also varies along the bandwidth and thus the efficiency. The simulation results are given in Fig. 3.26 for output power and TX efficiency, for the four bands, and the dynamic tuning.

The maximum output power is in the center of the band and the performance degrades as it goes to the lowest and highest end of the band. The output power ranges from −1.3 to 1.2 dBm. The TX efficiency ranges from 6 to 9.5 %. The current and power consumption are almost constant for the DCO buffer, 4 mA and 3.2 mW.

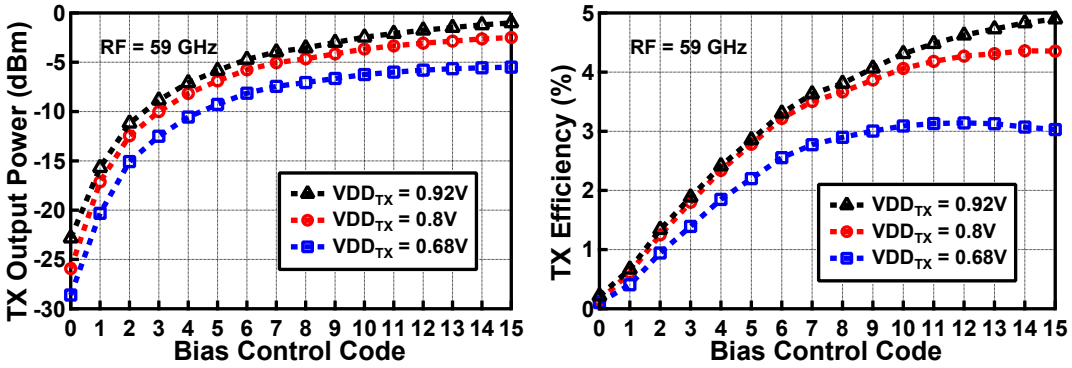


(a) (b)

Figure 3.26: TX1 simulations versus frequency with VDD_{TX} = 0.8 V: (a) Output Power (b) Efficiency.

3.2.3 Measurement Results

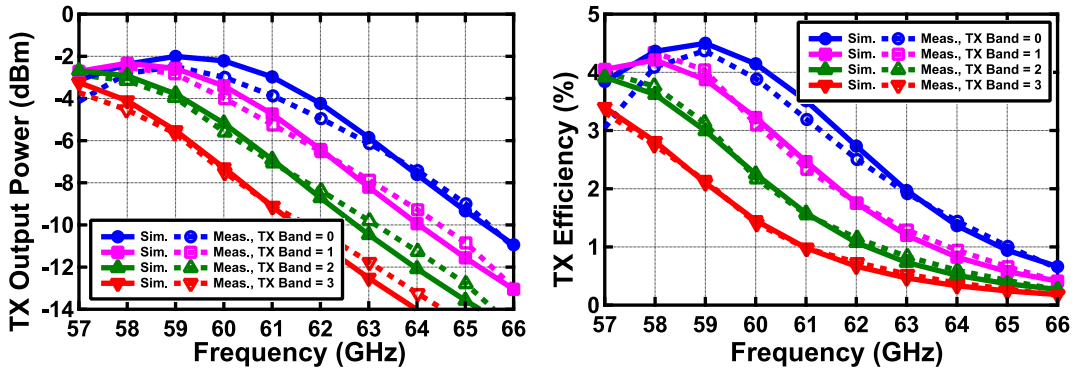
The nominal voltage supply for TX is 0.8 V, but the TX is also characterized for supplies of 0.68 V and 0.92 V. Fig. 3.27 shows the output power and efficiency of the TX path at a fixed frequency of 59 GHz versus the bias control code. The saturated output power reaches −1 dBm when the supply voltage is increased to 0.92 V.



(a) (b)

Figure 3.27: TX Measurements versus bias control code at 59 GHz: (a) Output Power (b) TX Efficiency.

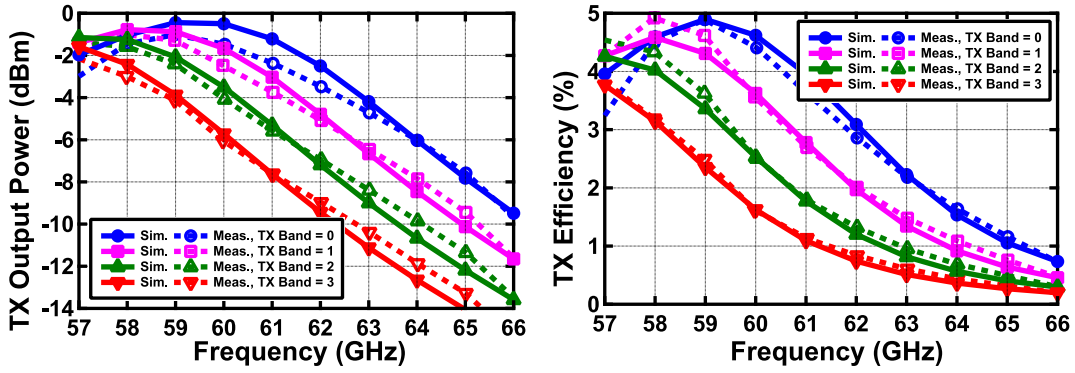
The band-tuning mechanism is implemented with two 3-bit thermometric capacitor banks, they are placed at the differential output of the buffer and PAMIX respectively. Fig. 3.28 shows the output power across the entire 9-GHz bandwidth with nominal supply of 0.8 V. There is a 3 GHz frequency shift and 3 dB discrepancy from simulations shown in Fig. 3.26. It was found that an underestimation of parasitic capacitance in parallel to the thermometric capacitor banks de-tuned the behavior of the TX path. By the addition of a 5 fF and 35 fF capacitors at the buffer and PAMIX differential outputs, respectively, the simulation achieved to match the measurement results.



(a) (b)

Figure 3.28: TX1 Measurements versus frequency with VDD_{TX} = 0.8 V (accounting for the additional parasitic capacitances): (a) Output Power (b) Efficiency.

TX can be set to the maximum output power and hence current consumption with the supply of 0.92 V. The TX performance is shown in Fig. 3.29. The current consumption of the entire TX path is approximately 17.5 mA (I_{Buffer} = 4.5 mA + I_{PAMIX} = 13 mA), compared to the first integration which was 22 mA. It delivers a maximum saturated output power of −1 dBm at 59 GHz.



(a) (b)

Figure 3.29: TX1 Measurements versus frequency with VDD_{TX} = 0.92 V: (a) Output Power (b) Efficiency.

3.3 Summary

Two low-power band-tuning 60-GHz TX has been implemented in GF 22-nm FDSOI CMOS technology. Several mm-wave design techniques and matching network optimization have been used in order to achieve a good performance for low-power FMCW radars. The tuned matching network for each TX stage allows to benefit from a higher quality factor in a narrower band and synchronously sweep LO and TX bands to cover the entire 9 GHz band. The output power variations across the bandwidth do not severely affect the operation of the radar system

because the range information is carried in the frequency of the beat signal and not in its amplitude.

Table 3.2: Comparison with the state-of-the-art 60-GHz radar transmitters.

Ref.	Tech.	Freq. (GHz)	VDD (V)	P_{out} (dBm)	P_{DC} (mW)	TX Eff. (%)
[7]	65-nm Bulk	56.4-63.4	1.2	5	41	7.7
[8]	350-nm SiGe	57-64	3.3	4	990[a]	-
[9]	130-nm SiGe	59.5-70.5	3.3	8.1	115	5.6
[10]	28-nm Bulk	57-64	0.9	10	63[b] / 137.5[c]	15.9[b] / 7.3[c]
[11]	28-nm Bulk	57-72	0.9	10	33.6[b] / 78.6[c]	29.8[b] / 12.7[c]
This Work PA	**22-nm FDSOI**	**57-66**	**0.8**	**1**	**13.5[b] / 17.6**	**9.3[b] / 7.2**
This Work PAMIX	**22-nm FDSOI**	**57-66**	**0.92**	**-1**	**10.4[b] / 14**	**7.6[b] / 5.7**

[a] Entire radar power consumption (LO+2TX+4RX). [b]LO distribution (buffers) not included.

[c]Estimated including LO distribution.

The TX performance is compared to state-of-the-art radar TXs in Table 3.2. Most of the work in literature target applications that require higher output power, which makes this work one of the first optimized TX for such a low output power. To the authors knowledge this work is also the first 60-GHz FMCW radar TX implemented in a FDSOI technology, which makes easier to fully integrate with high performance digital processing compared to other technologies such as SiGe. Some prior works report the TX power consumption and efficiency without considering the LO distribution. The buffers distributing the LO signal at mm-wave can consume as much as the TX PA. The power consumption of LO buffers is estimated in [10] and [11] for allowing a fair comparison. The TX efficiency is comparable to other state-of-the-art FMCW TX in the 60-GHz band while reducing the power consumption as much as one order of magnitude as in the case of [10]. The first TX implementation achieved a saturated output power of 1 dBm with a power consumption of only 17 mW. The second TX implementation has a lower saturated output power of −1 dBm while consuming as little as 14 mW. Both designs are validated in a complete FMCW radar system in chapter 5.

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4 Mixer-First 60-GHz Low-Power FMCW RADAR Receiver

This chapter describes the mixer-first RX architecture chosen based on the target application and specifications derived in chapter 2. Short-range sensing allows to relax the required specifications such as the NF and trade it off for lower power consumption and area. The trade-off consists of translating the low-noise operation from mm-wave to a low-IF taking a penalty on the NF, assuming the power consumption of a low-noise amplifier (LNA) operating at IF should be lower than at 60 GHz. In addition, implementing an IF LNA would also take less area than the mm-wave LNA because of the absence of inductors or transformers. Two versions of mixer-first RX are presented in this chapter: 1) an active mixer and, 2) a passive mixer.

4.1 Active Mixer Design

The first design of the 60-GHz RX path consists of an active mixer-first with I and Q LO buffers driving the mixer. The schematic of the RX path is shown in Fig. 4.1, it uses a balun to have its input matched to a 50 Ω impedance and transformers to couple the I and Q signals to drive the mixer. The balun is similar at the one used in the TX, and it is chosen to provide galvanic isolation and avoid the need to place ESD protection which would add significant parasitic capacitance at the RX GSG pads making more difficult to achieve good impedance matching. The use of the balun can provide voltage gain and differential signal. Having the differential RF signal available, then a double-balance mixer becomes an attractive option due to its rejection of amplitude noise in the LO signals and even harmonics rejection.

The core of the LO buffers is identical to the ones described in chapter 3 except for the capacitor banks which are placed in the secondary of the transformer load instead of the primary. The I and Q LO distribution lines are also longer requiring to use the differential TL described in chapter 3. The output of the double-balanced mixer is connected to IF voltage followers to output the IF signals off-chip. In this first prototype RX, the entire baseband path is implemented on a test board.

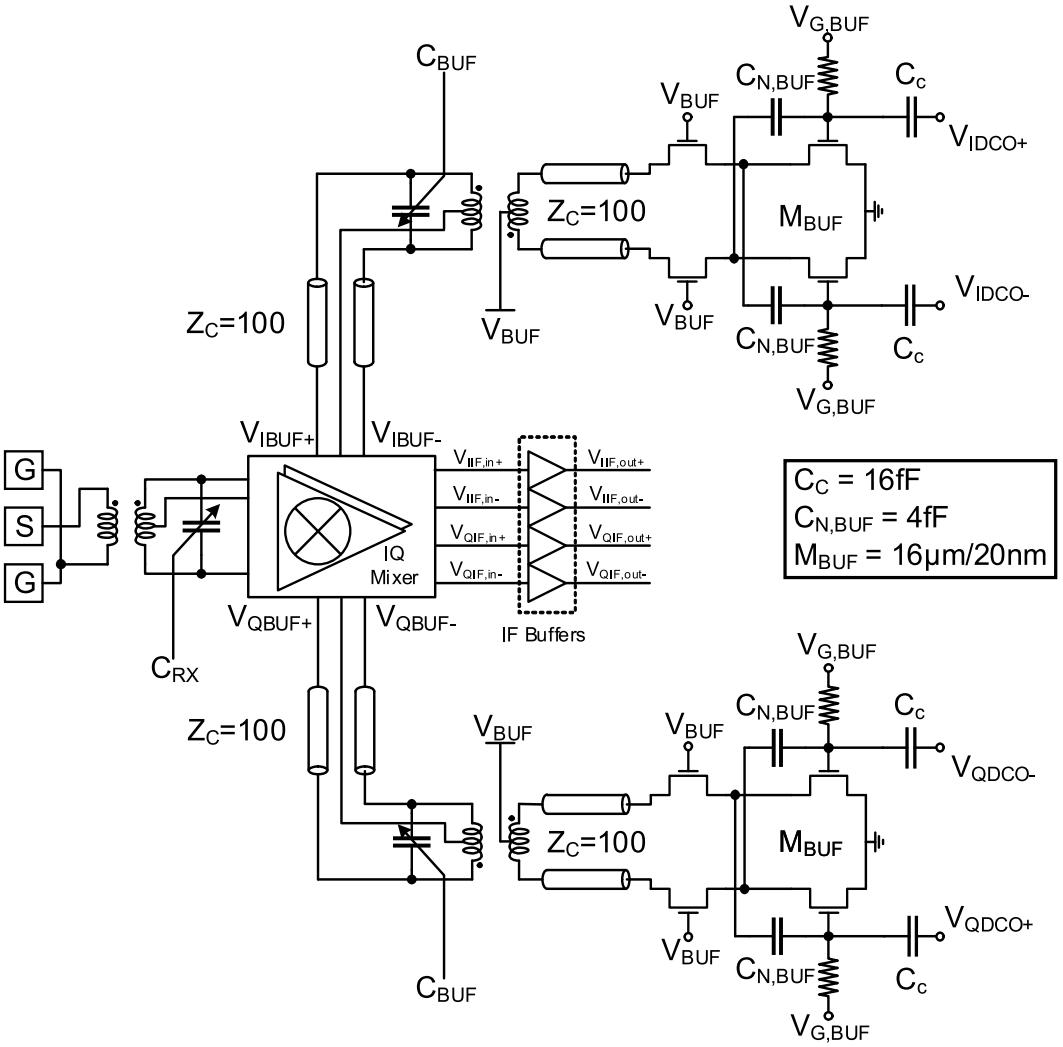


Figure 4.1: RX schematic: I and Q LO buffers + active mixer + IF buffers.

4.1.1 Gilbert Cell

The double-balanced active mixer is based on a down-conversion Gilbert cell chosen for its conversion gain which is convenient to have for attenuating the noise of subsequent stages. Two Gilbert cell mixers are required for the I and Q paths. The core of the active mixer is shown in Fig. 4.2. All transistors are forward body biased with the back gate of the NMOS and PMOS connected to the supply voltage and ground, respectively. According to [1] the conversion gain for a double-balanced active mixer is given by

$$Av_{mix} = \frac{V_{IF,dif}}{V_{RF,dif}} = \frac{2G_{m,CS}}{\pi G_{m,P}}\left(1 - \frac{2\Delta T}{T_{LO}}\right), \tag{4.1}$$

where $G_{m,CS}$ is the transconductance of the common source transistor which performs the

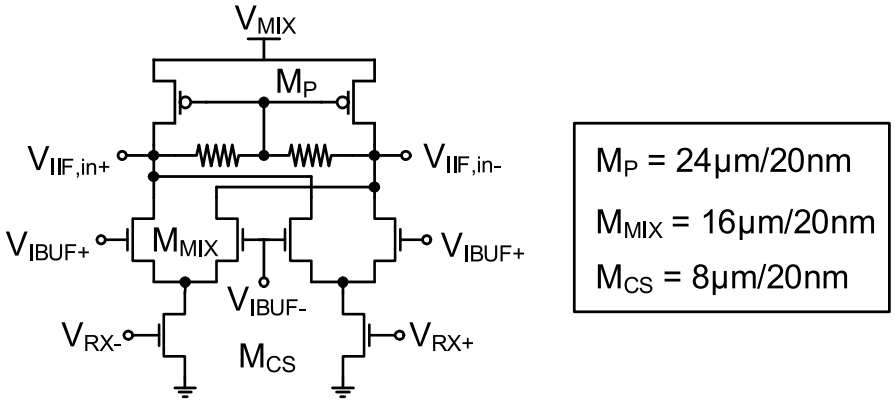


Figure 4.2: RX active down-conversion mixer schematic.

conversion from RF voltage to current, and $\frac{1}{G_{m,P}}$ is the output load which converts the IF current to voltage at the output. The expression in the parenthesis in Eq. (4.1) is to account for the fact that the LO signals are sinusoidal instead of square-wave which is not possible to achieve at mm-wave frequencies in CMOS technologies. ΔT is the fraction of time in which the differential signals remain approximately equal, and T_{LO} is the period of the LO signal. The load in the active mixer is self-biased through a resistor which is chosen much larger than the equivalent resistance of the diode-connected transistor. The output of the mixer is connected to an IF buffer consisting of a PMOS voltage follower used to output the IF signals off-chip. The band-tuning scheme to cover the 9-GHz bandwidth is implemented for the RX input matching and the transformers for the LO buffers.

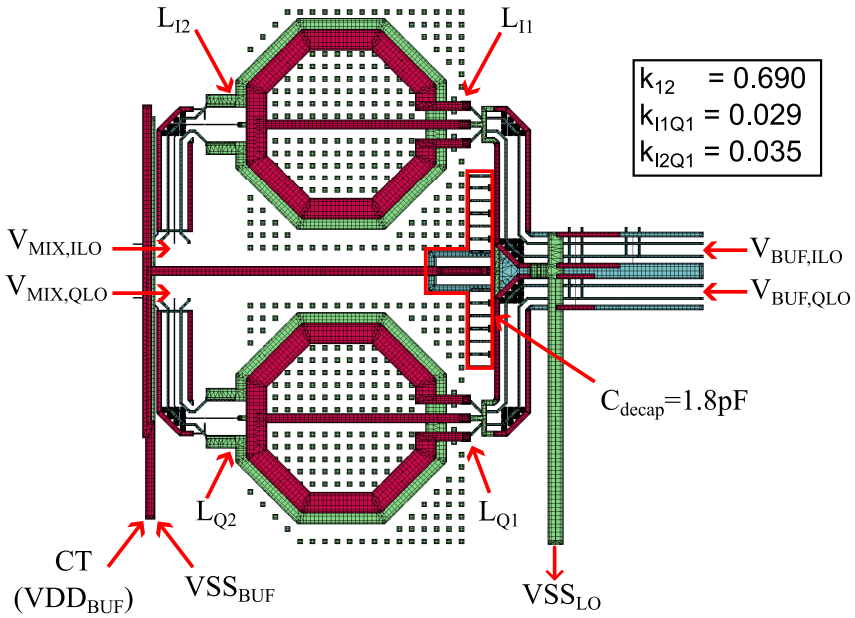


Figure 4.3: I and Q transformers layout.

The I and Q transformers are a very sensitive part of the design because they must maintain the quadrature between the LO signals. It is also a very efficient way to couple the output signal of one stage to the input of the next stage because at high frequencies the quality factor of inductances is higher than the one of capacitances. Fig. 4.3 shows the layout of the I and Q transformers, they are designed with stacked turns for high coupling factor which provides a wider operating bandwidth. The disadvantage of having a stacked transformer is the lower SRF compared to a coplanar transformer and the reduced margin for parasitic capacitors. The transformers were designed for a 100 Ω:100 Ω impedance.

This structure is used as the load for the LO buffers. There is a trade-off between area and the coupling between I and Q paths, and it must be addressed in order to prevent a large phase error between the quadrature signals. The transformers are carefully placed with a distance of 115 μm from each other center, it is equivalent to a separation of 32.3 μm between the edges of the I and Q coils. The resulting coupling between different coils is shown on the right hand side in Fig. 4.3, the coupling factor of each transformer from its primary to secondary is basically 20 times larger than the coupling to the other transformer.

The LO signals come from the right side in Fig. 4.3, they are distributed using the 100-Ω differential TLs upwards and downwards, for I and Q signals respectively. On the left of these vertical TLs some local decoupling capacitors are placed as close as possible to the transformers CT. These local capacitors help to maintain a more stable $\mathrm{VDD_{BUF}}$ supply for the LO buffers, the total value of the local decoupling capacitors is 1.8 pF. The voltage supply $\mathrm{VDD_{BUF}}$ and ground $\mathrm{VSS_{BUF}}$ are drawn one on top of the other and between the two transformers in order to prevent coupling and maintain symmetry between structures. On the left side of the transformers are routed the connections to the mixer switches, including the biasing voltage to the CT of the secondary coils.

4.1.2 Baseband Amplifier

The active mixer was designed as a first prototype where the analog baseband is implemented off-chip on the test PCB. It provides amplification and filtering required to properly acquire the down-converted signal. It consists of two stages, the first one biases the on-chip IF followers and converts the signal from differential to single-ended. The second stage adds gain and band-pass filters the signal to suppress LO-RX leakage and flicker noise around DC. In Fig. 4.4, the IF signals of the mixer are connected to the IF buffers, which are implemented as PMOS voltage followers biased with an off-chip source resistor R_1 on a supply $\mathrm{VDD_{IF}}$ = 1.8 V. The voltage gain of the first stage is given by

$$Av_{IF,1} = G_{m,IF}R_1 = \frac{2.4k}{300} = 8 = 18dB. \tag{4.2}$$

Since the integrated mixer does not provide large gain to attenuate noise from following stages it is important that the OPAMPs used in the analog baseband are low noise. Therefore, the

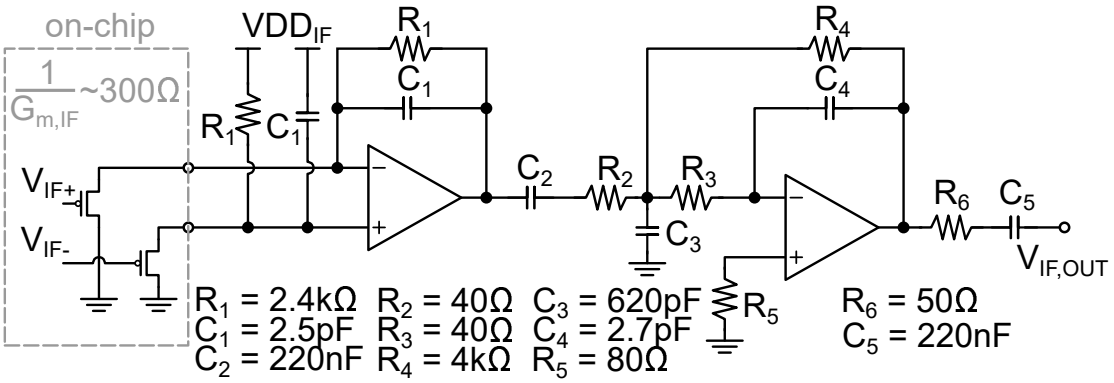


Figure 4.4: IF amplification and filtering implemented on PCB.

OPAMP chosen is the ultra-low voltage noise LTC6228 with only 0.88 nV/$\sqrt{\text{Hz}}$. The second stage is designed as a multiple feedback (MFB) filter, the voltage gain in the second stage is chosen as

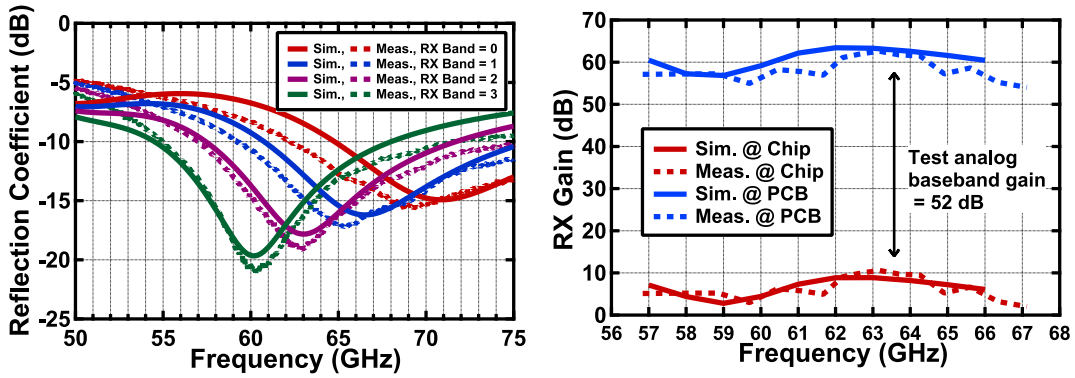
$$Av_{IF2} = \frac{R_4}{R_2} = \frac{4k}{40} = 100 = 40dB, \tag{4.3}$$

Furthermore, the resistors R_2 and R_3 must be set to the same value and equal to 40 Ω to improve noise [2], while the bandwidth and poles are set by C_3 = 620 pF and C_4 = 2.7 pF to improve noise and distortion for an upper cut-off frequency of 10 MHz. The series capacitors $C_2 = C_5$ = 220 nF are chosen to set the lower cut-off frequency around 20 kHz. The output series resistor R_6 is placed to match the instrument impedance equal to 50 Ω. The total gain after the mixer is set by Eq. (4.2), Eq. (4.3), and halve by the output matching resistor R_6 to obtain 52 dB gain.

4.1.3 Simulation and Measurement Results

The RX input matching measurement is performed using the vector network analyzer R&S ZNA40 with the frequency converter ZVA-Z75. Fig. 4.5a shows the simulated and measured reflection coefficient validating the good input matching with a value always below −10 dB in the band of interest. The RX gain at the chip output and test analog baseband are shown in Fig. 4.5b. The gain is not completely flat from 57 to 66 GHz because the input transformer and the LO buffer signals driving the down-converter mixer do not have a flat response across the entire 9-GHz band. The amplitude variations across the bandwidth do not severely affect the operation of the radar system because the range information is carried in the frequency of the beat signal and not in its amplitude.

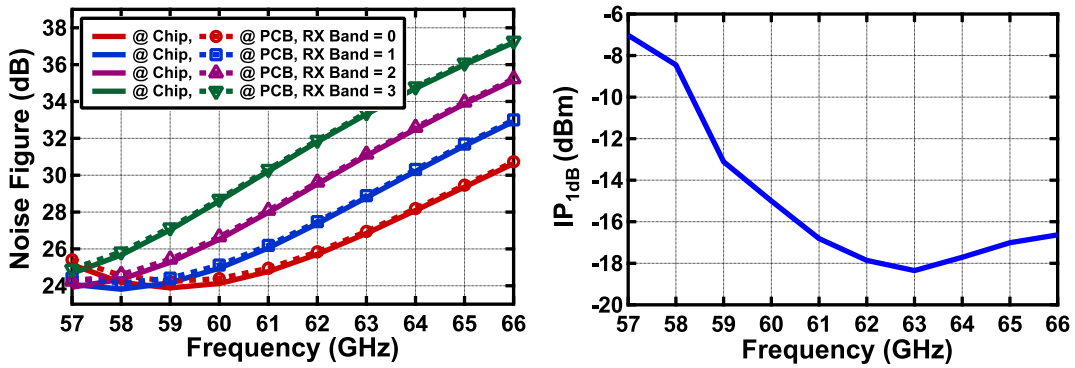
The NF is relatively high but it is acceptable for the target application of short-range monitoring. Fig. 4.6a shows the NF at the output of the chip and PCB, it proves that the NF in the RX is dominated by the noise of the active mixer and the fact that it does not add enough gain to



(a) (b)

Figure 4.5: RX Measurements versus frequency: (a) Reflection Coefficient (b) gain.

mask the noise coming from subsequent stages such as the IF buffers. The worst-case input power 1-dB compression point (IP_{1dB}) in the RX path is −18 dBm (Fig. 4.6b) and the measured LO-RX leakage is −38 dBm, maintaining a linear RX path operation with a margin of 20 dB. The power consumption of both RX buffers is 4.8 mW for I and Q paths, while the active mixer consumes 2.4 mW.



(a) (b)

Figure 4.6: RX Simulations: (a) Noise Figure (b) Input Power 1-dB Compression Point.

The use of an active mixer at 60 GHz was found non-optimal because of the low conversion gain at mm-wave frequencies in addition to a large penalty on the NF and power consumption. Instead, a passive mixer is investigated in this section looking into further reducing the power consumption and noise contributors such as the flicker noise from transistors in the active mixer.

4.2 Passive Mixer Design

4.2.1 Theoretical Introduction

The theory behind passive mixer-first has been studied in detail in [3, 4], where the authors present a linear time-invariant (LTI) equivalent circuit, shown in Fig. 4.7. A shunt resistor R_{SH} is introduced to represent the loss due to harmonic reupconversion and dissipation [3]. There is also the term ζ acting on the baseband impedance Z_B as a scaling factor. Considering the case of a four phases mixer, the scaling factor can be approximated to

$$\zeta = \frac{2}{\pi^2} \approx 0.2. \tag{4.4}$$

Assuming an antenna impedance R_a constant across all frequencies, the shunt resistor can be written as

$$R_{SH} = \left(\sum_{n=3,5...}^{\infty} \frac{1}{n^2} \frac{1}{R_a(n\omega_{LO}) + R_{SW}} \right)^{-1} = \frac{4\zeta}{1-4\zeta} (R_a + R_{SW}) \approx 4.3 (R_a + R_{SW}). \tag{4.5}$$

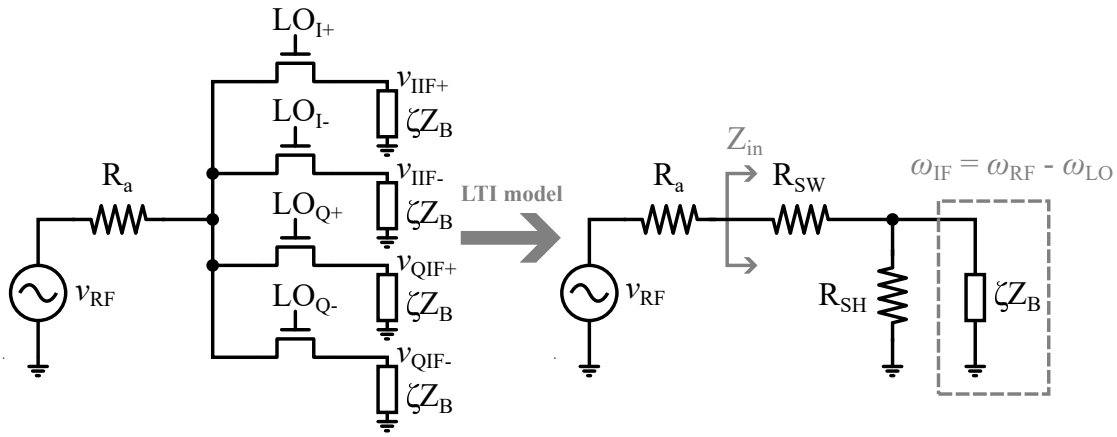


Figure 4.7: Passive Mixer-First LTI equivalent circuit.

Input Matching

Once the elements of the LTI model are defined the input impedance is calculated from the equivalent circuit in Fig. 4.7 as

$$Z_{in}(\omega_{IF}) = R_{SW} + R_{SH} // \zeta Z_B(\omega_{IF}), \tag{4.6}$$

where the term $Z_B(\omega_{IF})$ explicitly shows its dependence on the IF rather than RF. This is done

to clearly state that the rest of the circuit calculates the impedance operating at RF (in case there are reactances) and the baseband load impedance is calculated at IF. The dependence of the input impedance on the mixer load is known as the transparency property of the passive mixer. It also means the input impedance is bounded on the lower end for a zero baseband impedance and on the upper end for an infinite baseband impedance

$$R_{SW} < R_{in} < R_{SW} + R_{SH} \approx 4.3R_a + 5.3R_{SW}. \tag{4.7}$$

Considering an antenna impedance $R_a = 50\,\Omega$ and a switch ON-resistance $R_{SW} = 5\,\Omega$, the input impedance behavior is shown in Fig. 4.8. The minimum input impedance is $R_{SW} = 5\,\Omega$ and it flattens at $4.3R_a + 5.3R_{SW} = 241.5\,\Omega$. Impedance matching occurs for $R_B = 275\,\Omega$.

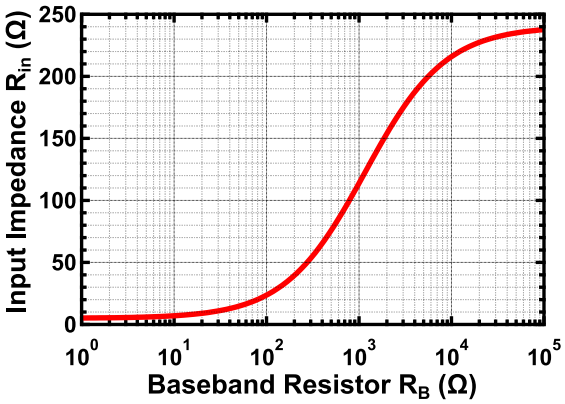


Figure 4.8: Mixer-first input impedance calculation example.

Conversion Gain

The passive mixer by nature introduces loss rather than gain, but in this section, it is defined as a gain and its value is expressed in -dB. The baseband impedance is decomposed as a parallel R_BC_B circuit and its impedance is given by

$$Z_B(\omega_{IF}) = \frac{R_B}{1 + j \cdot \omega_{IF} R_B C_B}. \tag{4.8}$$

Then the voltage gain is calculated as in [3]

$$A_v(\omega_{IF}) = \frac{v_{IF}}{v_{RF}} = \frac{2\sqrt{2}}{\pi} \frac{Z_B(\omega_{IF})}{Z_B(\omega_{IF}) + 4\,(R_a + R_{SW})}. \tag{4.9}$$

The maximum voltage gain is reached for an infinite baseband impedance. As a practical example, consider $R_a = 50\,\Omega$, $R_{SW} = 5\,\Omega$, $C_B = 50\,\text{pF}$, the behavior of the voltage gain with respect to the baseband resistance is shown in Fig. 4.9. The saturated voltage gain is reached

when the baseband resistance is infinite, and it is equal to −0.95 dB. The voltage gain when the input is matched ($R_B = 275\,\Omega$) is −6 dB.

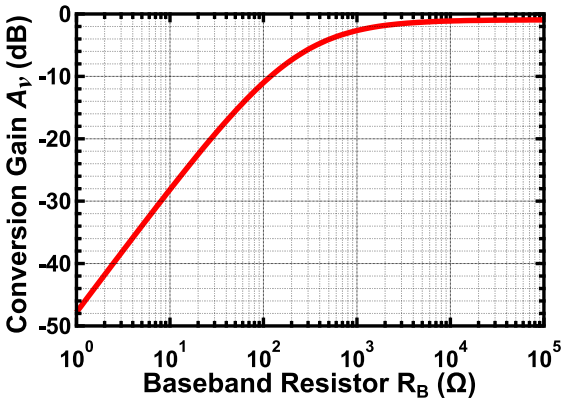


Figure 4.9: Mixer-first voltage gain calculation example.

Narrowband Filtering

There is also a filtering behavior coming from the baseband capacitance. The 3-dB cut-off frequency is calculated from the gain expression in Eq. (4.9) as

$$\omega_{IF-3dB} = \frac{1}{C_B\,[R_B//4\,(R_a + R_{SW})]}. \tag{4.10}$$

Since $R_B = 275\,\Omega$ for input matching and the switch resistance is normally designed to be small, then there is only C_B which can be chosen for setting the cut-off frequency in the passive mixer. As a practical example, consider $R_a = 50\,\Omega$, $R_{SW} = 5\,\Omega$, $R_B = 275\,\Omega$, Fig. 4.10 shows different filter responses for several values of $C_B = 50$ pF, 200 pF, 800 pF. Unfortunately, in this example it takes a very large capacitor to achieve a narrow filtering around the target IF of 1 MHz.

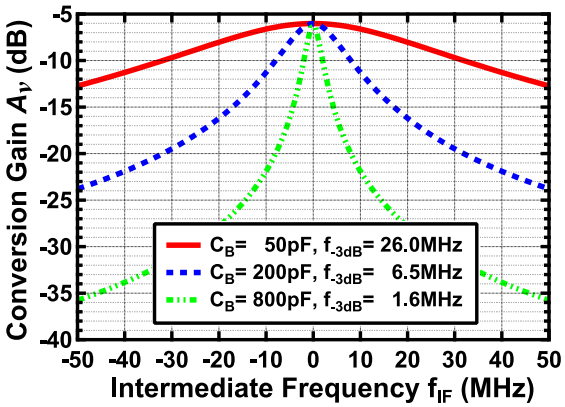


Figure 4.10: Mixer-first filter response calculation example.

Noise Figure

The passive mixer noise can be studied from the LTI model, Fig. 4.11 shows the noise sources of the different components,

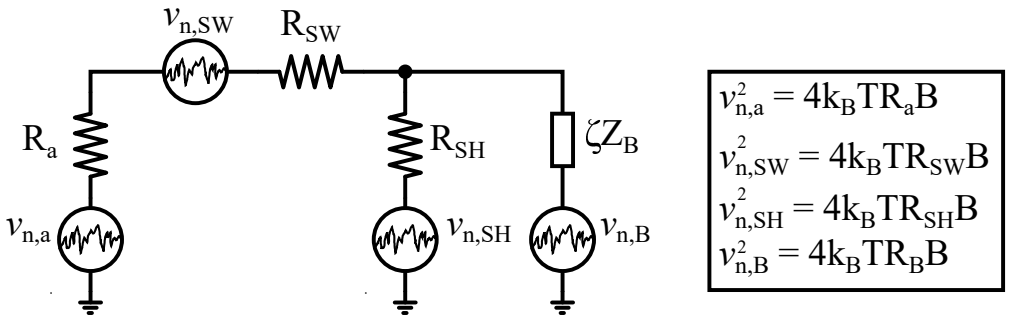


Figure 4.11: Mixer-first noise sources.

where k_B is the Boltzmann constant, T is the temperature, and B is the baseband bandwidth. Then the NF is calculated from this model and it is given by

$$F = 1 + \frac{v_{n,SW}^2}{v_{n,a}^2} + \frac{v_{n,SH}^2}{v_{n,a}^2}\left(\frac{R_a + R_{SW}}{R_{SH}}\right)^2 + \frac{v_{n,B}^2}{v_{n,a}^2}\left(\frac{R_a + R_{SW}}{\zeta Z_B}\right)^2, \tag{4.11}$$

it can be further simplified to

$$F = 1 + \frac{R_{SW}}{R_a} + \frac{(R_a + R_{SW})^2}{R_{SH}R_a} + \frac{(R_a + R_{SW})^2}{\zeta Z_B R_a}. \tag{4.12}$$

As a practical example the values of the components are set to $R_a = 50\,\Omega$, $R_{SW} = 5\,\Omega$, T = 27 °C, and the NF is plotted against baseband resistance.

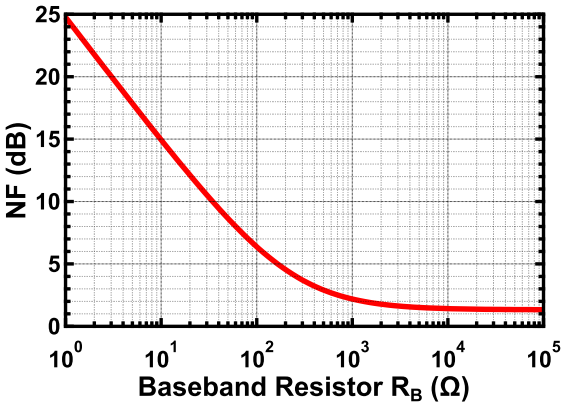


Figure 4.12: Mixer-first NF calculation example.

The scenario is slightly different in the case of placing an amplifier following the passive mixer.

The baseband impedance is set by the feedback resistor of the amplifier and its gain. The equivalent circuit with its corresponding noise sources is shown in Fig. 4.13 and the NF is given by

$$F = 1 + \frac{R_{SW}}{R_a} + \frac{(R_a + R_{SW})^2}{R_{SH} R_a} + \frac{(R_a + R_{SW})^2}{\zeta R_F R_a} + \zeta \frac{v_{n,A}^2}{4 k_B T R_a} \left(\frac{R_a + R_{SW}}{\zeta R_F} + \frac{R_a + R_{SW} + R_{SH}}{R_{SH}} \right)^2 . \quad (4.13)$$

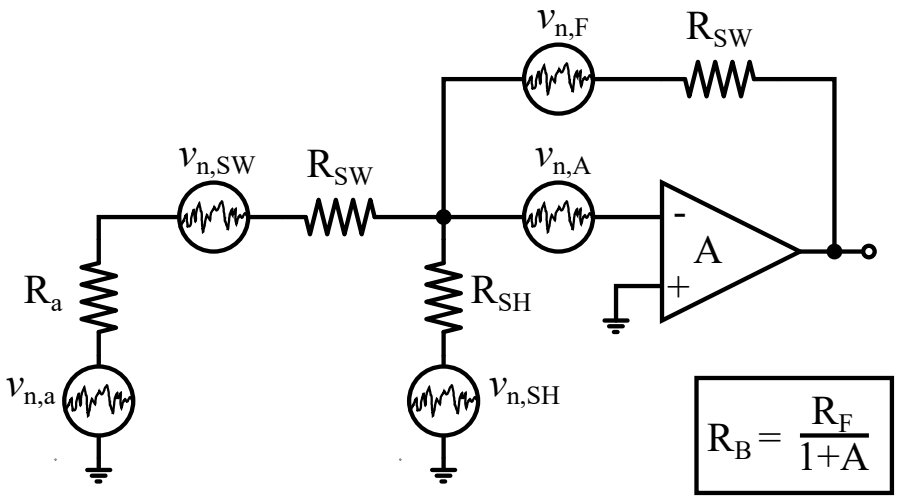


Figure 4.13: Mixer-first noise sources with an amplifier.

Summary

Important parameters as conversion gain and NF show better performance for large baseband impedance. In addition, designing for large baseband impedance means designing in a region where the input impedance, gain, and NF are close to constant and thus more robust against PVT variations. Unfortunately, it is impossible to have a good matching in this region because in most cases the antenna impedance R_a is 50 Ω, and even with zero switch resistance R_{SW} the maximum input impedance is bounded by

$$R_{in,sat} > 4.3 R_a = 215\Omega. \quad (4.14)$$

4.2.2 mm-wave Design

Designing the passive mixer-first architecture at mm-wave frequencies carries many challenges because of the higher losses at very short wavelength. The parasitic components as routing resistances and capacitances have a greater impact on impedances and matching networks. For instance, the input impedance analysis in section 4.2.1 must take into account

as well input parasitic capacitances C_{in} added from pads, ESD diodes, and switches [5]. The main effect of the parasitic capacitance is that complicates the input matching network and adds extra losses which translate directly to NF degradation because there is no gain to mask the noise from subsequent stages.

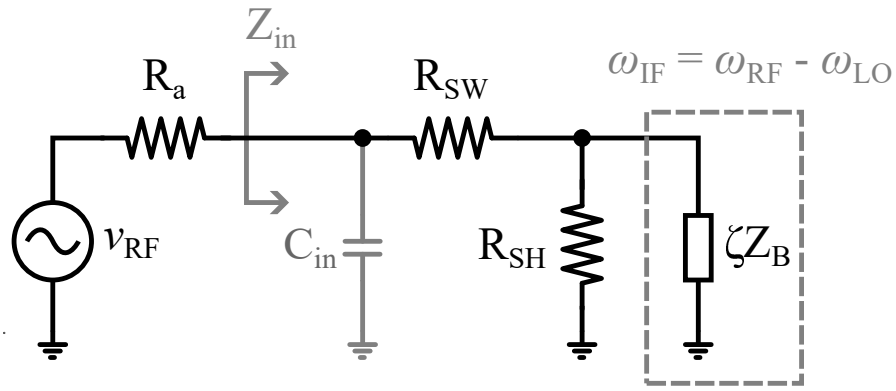


Figure 4.14: Input parasitic capacitance in mixer-first LTI.

The proposed solution is to add a transformer at the input of the RX path. The advantages of implementing this architecture at mm-wave are 1) highly compact solution, 2) the transformer matching network absorbs the parasitic capacitor from the pads and mixer switches, 3) adds voltage gain, 4) reduces harmonic reupconversion and dissipation losses of mixer-first operation, and 5) input impedance boosts allowing for smaller switches that relaxes the power-hungry mm-wave LO buffer design.

Harmonics Impact at mm-wave

The fourth point mentioned above brings an important advantage for impedance matching at mm-wave, the impact of higher harmonics is much lower because they appear so far from the frequency of interest and also much higher than the f_{max} of the transistors. The general expression for the shunt impedance is given by [3]

$$Z_{SH} = \left(\sum_{n=3,7,11...}^{\infty} \frac{1}{n^2} \frac{1}{Z_a^*(n\omega_{LO}) + R_{SW}} + \sum_{n=5,9,13...}^{\infty} \frac{1}{n^2} \frac{1}{Z_a(n\omega_{LO}) + R_{SW}} \right)^{-1}, \tag{4.15}$$

where the operator * corresponds to the complex conjugate. In addition, placing a transformer in front of the passive mixer further decreases the impact of higher harmonics filtering them out. Without higher harmonics there is no reupconversion and dissipation losses associated with the antenna impedance, consequently the input impedance tuning range in Eq. (4.7) is narrower. It can be assumed $|Z_a(n\omega_{LO})| \ll R_{SW}$, and assuming a 1:1 impedance transformation ratio, then the tuning range of the impedance of the mixer-first is calculated as

$$Z_{SH} = R_{SH} = K_{SW} R_{SW} = \frac{4\zeta}{1-4\zeta} R_{SW} \approx 4.3 R_{SW}, \tag{4.16}$$

$$R_{SW} < R_{mix} < 5.3 R_{SW}. \tag{4.17}$$

This result shows that the input matching would only depend on R_{SW} and it can be sized accordingly to achieve a good matching. There is no more the need of very wide transistors to make a negligible switch resistance, instead, a value of $R_{SW} \approx 10\,\Omega$ provides already a good matching while having small transistors. The small size transistors prevent large parasitic capacitance which are harmful at mm-wave and need to be absorbed by the transformer matching network. Narrower transistors are also desirable because the gate capacitance is smaller, and the LO buffers are less heavily loaded.

Overlapping sinusoidal LO signals

Another important consideration when operating at mm-wave is that the LO signals are not non-overlapping square waves anymore but sinusoidal signals. The overlapping effect can be modelled by a resistor $R_{OL} = K_{OL} R_{SW}$, parallel to resistor R_{SH} [4] [6], where K_{OL} is the harmonic loss factor and it is a function of the I and Q signals overlap, they can be merged into just one shunt resistor given by

$$R'_{SH} = (K_{SW} // K_{OL})\, R_{SW} = K R_{SW}. \tag{4.18}$$

The LO drivers provide I and Q signals with a peak amplitude of 200 mV. The transistors are super-low voltage threshold NMOS devices with minimum length which are optimal for high frequency operation. Although, actively driving the backgate was considered it was finally avoided to prevent underestimating parasitics in the wells and substrate which could lead to a degradation of performance in the LO buffers. Instead, forward biasing was implemented connecting the backgate of the switches to a local supply of 0.8 V provided by a local LDO. The DC voltage of the LO signals is adjusted to bias the gate of the switches to drive them in class C ($V_{LO,bias} = 0.15\,\text{V}$) and minimize the I and Q signal overlapping to obtain a $K_{OL} \approx 2.5$. The resulting input impedance tuning range is

$$Z_{mix}(\omega_{IF}) = R_{SW} + R'_{SH} // (\zeta Z_B(\omega_{IF})) = R_{SW} + K R_{SW} // (\zeta Z_B(\omega_{IF})), \tag{4.19}$$

$$R_{SW} < Z_{mix} < (1+K)\, R_{SW} = 2.6 R_{SW}. \tag{4.20}$$

The disadvantage of overlapping effect is the reduced tuning range of the mixer impedance

Z_{mix}. It basically requires R_{SW} to be large enough to be able to match the antenna impedance ($R_a = 50\,\Omega$). However, must be noted that the larger R_{SW} the higher the noise contribution of the switches.

Design Procedure

The schematic of the proposed passive mixer-first is shown in Fig. 4.15 for a generic baseband impedance.

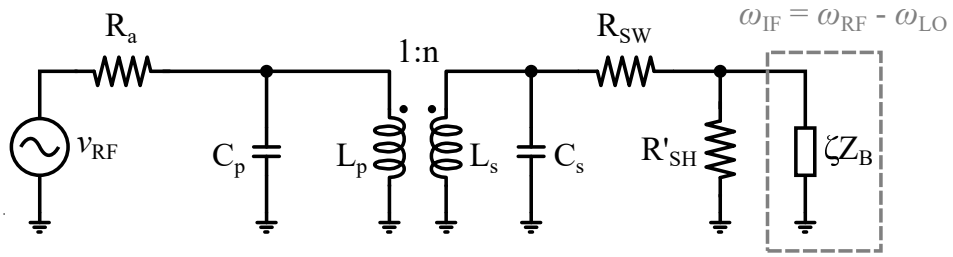


Figure 4.15: Proposed mm-wave passive mixer.

In Fig. 4.16, the ON-resistance of the switches R_{SW}, the shunt resistor R'_{SH} accounting for the already mentioned losses and the baseband impedance $\zeta Z_B(\omega_{IF})$ are replaced by an equivalent RC parallel circuit, and the total mixer impedance seen at its input is defined as

$$Z_{mix}(\omega_{IF}) = R_{SW} + KR_{SW} \,//\, (\zeta Z_B(\omega_{IF}))\,. \tag{4.21}$$

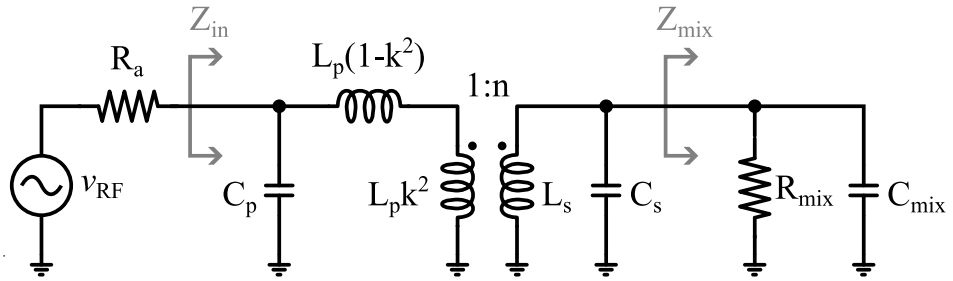


Figure 4.16: Input impedance in the mm-wave passive mixer.

The transformer is split in the leakage inductance $L_p\left(1-k^2\right)$ which accounts for the flux that does not participate in the coupling, and the magnetizing inductance $L_p k^2$ which models the portion of the primary inductance that does participate in coupling. The coupling factor is defined as k, while the secondary-to-primary turns ratio is defined as n. The relationship between n and k is given by

$$n = \frac{1}{k}\sqrt{\frac{L_s}{L_p}}. \tag{4.22}$$

The input matching network analysis is shown in Fig. 4.17, where the secondary inductance is designed to resonate with the parasitic capacitance C_s on the secondary and the equivalent mixer capacitance C_{mix}. Then, a L-matching network is designed on the primary with the primary inductance and the GSG pads parasitic capacitance C_p.

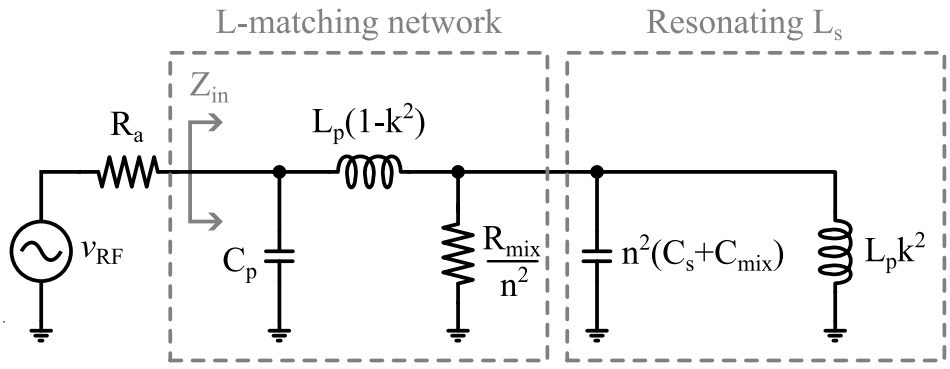


Figure 4.17: Input matching network analysis.

The transformer is designed with co-planar primary and secondary turns routed in ultra-thick metal to reduce losses. The transformer layout and parameters are shown in Fig. 4.18.

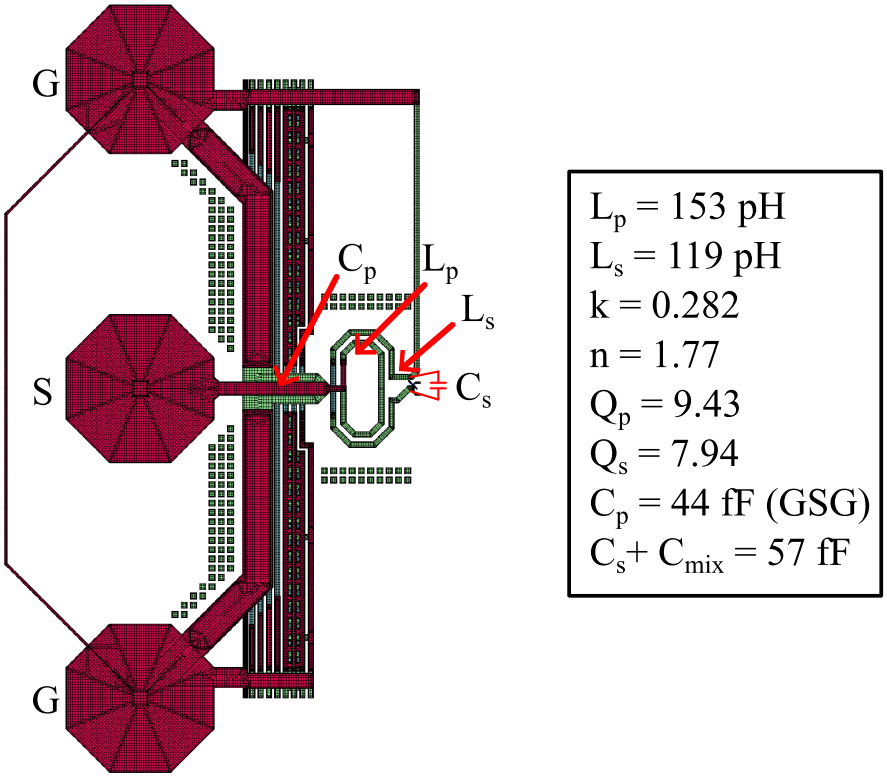


Figure 4.18: Input transformer with GSG pads and its extracted parameters.

According to the L-matching network shown in Fig. 4.17, the required ON-resistance of the

switch is calculated for the infinite baseband impedance case as follows

$$X_{C_p} = \frac{1}{2\pi f_{RF} C_p}, \tag{4.23}$$

$$Q_{MN} = \frac{R_a}{X_{C_p}}, \tag{4.24}$$

$$R_{SW} = \frac{R_a n^2}{2.6\left(Q_{MN}^2 + 1\right)} \approx 35\Omega. \tag{4.25}$$

Fig. 4.18 shows that the capacitance required to resonate L_s should be equal to 57 fF and is composed by C_{mix} and C_s. The former is the capacitance coming from the baseband load plus the switch capacitance, while the latter is the capacitance of the secondary of the transformer and can also account for functional capacitor to be placed in order to tune the matching network. Unfortunately, already the parasitic capacitance of a 35-Ω switch is larger than 57 fF driving the secondary of the transformer out of resonance. The solution is to use a narrower transistor than the calculated, with a higher ON-resistance and lower parasitic capacitance. This is not the optimal value for matching at infinite baseband impedance though, and it will slightly degrade both the conversion gain and NF.

Several trials were performed to find a suitable transistor size, Table 4.1 shows a summary of the most interesting simulation results. The transistor length is chosen minimum for high-speed operation and the total width W_{TOT} is a trade-off between improving NF (wider transistor) and minimizing parasitic capacitor C_{mix} (narrower transistor). The mixer capacitance is shown to know how much functional capacitance C_s needs to be added for reaching the required 57 fF to resonate L_s. The LO DC bias is also adjusted to efficiently drive the switches into class C operation to obtain the best overall performance for a given transistor width.

Table 4.1: Mixer switch sizing at 61.5 GHz, with $V_{LO,pk}$ = 200 mV.

Case	W_{TOT} (μm)	C_{mix} (fF)	C_s (fF)	$V_{LO,bias}$ (mV)	R_{SW} (Ω)	A_v (dB)	NF (dB)
1	8	16	41	160	66	-6.6	9.1
2	12	24	33	130	58	-6.3	8.6
3	16	32	25	110	53	-6.0	8.3

Simulation case 3 in Table 4.1 shows that a total width transistor of 16 μm can provide a ON-resistance of 53 Ω while still leaving a good margin of 25 fF for C_s foreseeing extra parasitic capacitance coming from the secondary of the transformer and layout parasitics of the switch itself. It provides as well the lowest NF and largest gain of the shown cases.

4.2.3 IF Low-Noise Amplifier

The passive mixer does not provide gain, therefore a low-noise IF amplifier must be designed following the mixer to provide enough gain to mask noise coming from subsequent stages, and the amplifier itself should add as little noise as possible. The design of the IF amplifier can define whether the mixer operates in current-mode or voltage-mode. In the case that the input impedance of the mixer is much larger than its output impedance, the mixer is said to operate in current-mode. Conversely, if the input impedance is much smaller than its output impedance the mixer operates in voltage-mode.

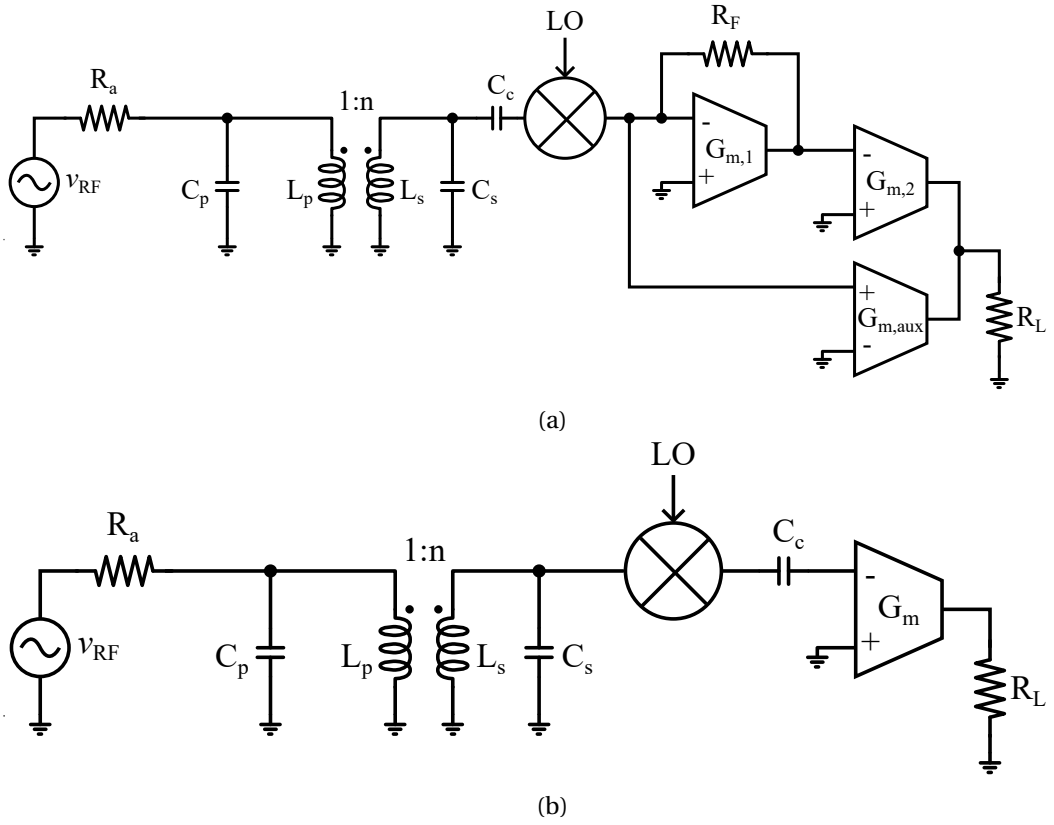


Figure 4.19: RX architectures: (a) Mixed-mode with noise cancelling, and (b) voltage-mode IF amplifier.

Given the mixer-first design shown in section 4.2.2, the impedance seen at the input of the mixer is expected to be relatively small. The 50-Ω input load is boosted by the transformer-based matching network but, nevertheless, it is still in the order of few hundreds of Ω. The voltage-mode mixer seems to be the best fit because of the small input impedance and moreover, from the theory seen in section 4.2.1, a large output impedance exploits the performance of the passive mixer-first in terms of gain and NF. However, there is an intermediate scenario whenever the difference between the input and output impedance of the mixer is not very large, the mixer is said to operate in mixed-mode. Adding a feedback resistor in the IF amplifier allows to control the output impedance of the mixer to operate it in mixed-mode and opens

the possibility to implement a noise cancelling scheme (NC) in the IF path. The mixed-mode (MM) and voltage-mode (VM) implementation are shown in Fig. 4.19.

IF Amplifier for Mixed-Mode Mixer

The entire RX-IF architecture of the MM mixer with NC is shown in Fig. 4.19a. The NC scheme is based on [7], where the noise generated by the transconductor $G_{m,1}$ is cancelled out through an auxiliary path by a transconductor $G_{m,aux}$. Each of the transconductor has a particular purpose, $G_{m,1}$ is sized to obtain the required impedance for the output of the mixer and it provides voltage gain through the feedback resistor R_F. The second stage, $G_{m,2}$, is designed relatively small to prevent distortion and it also converts the voltage output of the first stage to an output current that can be added to the auxiliary path. Finally, $G_{m,aux}$ is used to obtain a copy of $G_{m,1}$ noise with the opposite phase than in the main path in order to cancel it out while the signals in both paths are added in phase obtaining larger gain. The output current noise is calculated from the simplified circuit shown in Fig. 4.20. The entire IF amplifier accounts for the baseband impedance described in the mixer-first LTI model and it is reflected to the input, thus multiplying all impedances and voltages by the scaling factor ζ, whereas the transcondutances, capacitors and currents are divided by the same factor. The resistor R_{Th} is the equivalent Thevenin resistance of the mixer-first which is necessary to calculate the output noise generated by $G_{m,1}$.

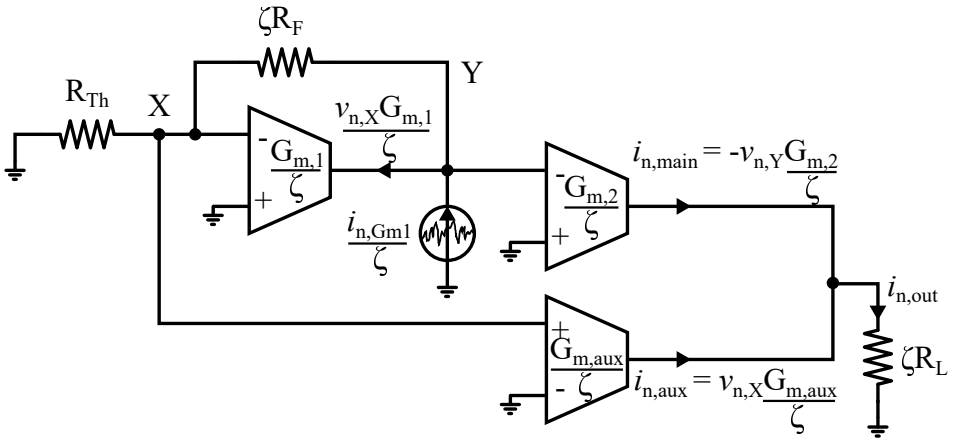


Figure 4.20: Equivalent circuit for calculating the output noise from $G_{m,1}$ in the MM mixer with NC.

The noise cancelling analysis focuses on the noise generated only in the first transconductor $G_{m,1}$, which is normally the largest noise contributor. As a first step the voltage noise in the node X is calculated as a function of the voltage in the node Y

$$v_{n,X} = \frac{R_{Th}}{R_{Th} + \zeta R_F} v_{n,Y}. \tag{4.26}$$

Second, the current noise expression is calculated for the node Y

$$\frac{i_{n,Gm1}}{\zeta} = v_{n,X}\frac{G_{m,1}}{\zeta} + \frac{v_{n,Y}}{R_{Th}+\zeta R_F}, \tag{4.27}$$

and Eq. (4.26) is replaced in Eq. (4.27) to simplify it into

$$v_{n,Y} = \frac{R_{Th}+\zeta R_F}{\zeta + G_{m,1}R_{Th}} i_{n,Gm1}. \tag{4.28}$$

Finally, the voltage noise $v_{n,X}$ and $v_{n,Y}$ are converted into current noise in the main and auxiliary paths, respectively. These currents are added and the output current noise is given by

$$\begin{aligned} i_{n,out} &= i_{n,main} + i_{n,aux} = -v_{n,Y}\frac{G_{m,2}}{\zeta} + v_{n,X}\frac{G_{m,aux}}{\zeta}, \\ &= \frac{i_{n,Gm1}}{\zeta}\left[\frac{G_{m,aux}R_{Th} - G_{m,2}\left(R_{Th}+\zeta R_F\right)}{\zeta + G_{m,1}R_{Th}}\right], \end{aligned} \tag{4.29}$$

where the numerator of this expression demonstrates that there is a condition for which the output current noise is completely cancelled out. The NC condition is given by

$$\frac{G_{m,aux}}{G_{m,2}} = 1 + \frac{\zeta R_F}{R_{Th}}. \tag{4.30}$$

The main advantage of this technique is that it allows to break the trade-off between input impedance and noise. For instance, the input impedance of a single transconductor with feedback resistor is estimated as $\frac{1}{G_{m,1}}$ and its thermal noise is given by $4k_BT\frac{\zeta}{G_{m,1}}$. If the input impedance needs to be match to tens or hundreds of Ω then $G_{m,1}$ needs to be relatively small, consequently generating significantly large thermal noise. In the NC scheme $G_{m,1}$ can be chosen as small as required because its noise is cancelled at the output. The noise generated by $G_{m,2}$ is less critical because it can be designed small enough to be masked by the voltage gain of the first stage. The main constraint is placed on $G_{m,aux}$ which must be very large to make its noise negligible.

Fig. 4.21 shows the circuit used to calculate the equivalent Thevenin resistance R_{Th}. Contrary to Eq. (4.22) where the procedure was to reflect the impedance of the secondary to the primary, here it is simpler to define n_p to reflect the impedance of the primary to the secondary.

$$n_p = \frac{1}{k}\sqrt{\frac{L_p}{L_s}} \approx 4. \tag{4.31}$$

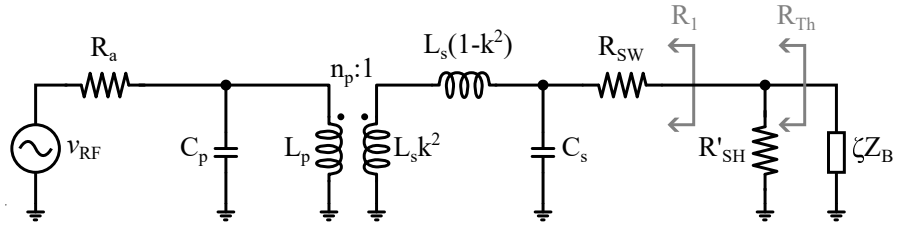


Figure 4.21: Equivalent circuit used to calculate R_{Th} of the mm-wave passive mixer.

The calculation of R_{Th} is performed for the resonance frequency of the matching network, same assumption as previously in Fig. 4.17. An auxiliary resistance R_1 is calculated from the circuit in Fig. 4.22. Using the design parameters shown in Fig. 4.18, it can be proven that for the resonance frequency the terms in parallel in Eq. (4.32) tend to infinity.

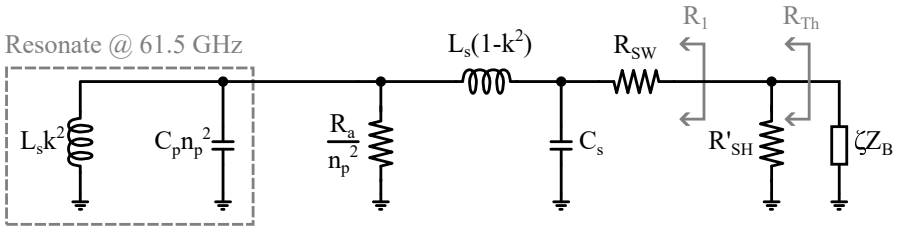


Figure 4.22: Impedance of the primary reflected to the secondary to calculate R_{Th} of the mm-wave passive mixer.

$$R_1 = R_{SW} + \frac{1}{sC_s} // \left[\frac{R_a}{n_p^2} + sL_s\left(1-k^2\right) \right] \approx \infty. \tag{4.32}$$

Then, the equivalent Thevenin resistance is given by

$$R_{Th} = R_1 // R'_{SH} \approx R'_{SH} \approx 1.6 R_{SW} \approx 90\Omega. \tag{4.33}$$

As a practical example to have a complete MM mixer-first RX, a NC IF amplifier is designed based on the circuit shown in Fig. 4.23 [8]. This design takes advantage from both NMOS and PMOS transconductances to obtain a power-efficient amplifier. The three transconductors are DC-coupled saving the area that AC-coupling capacitors would take. The DC voltage in each stage is controlled by using the backgate that FDSOI technology provides, this is performed maintaining the common-mode voltage V_{cm} around half the voltage supply V_{DD} by using local DC loops connected to the backgate of the PMOS devices. While the backgate of the NMOS devices is used to set the bias current defined by the reference devices shown on the left side in Fig. 4.23.

The intrinsic gain and transconductance efficiency obtained by such amplifier are $\frac{G_m}{g_{ds}} = 155$ and $\frac{G_m}{I_D} = 43.57\,\mathrm{V}^{-1}$. As mentioned before, the gain of the first stage should be large enough to

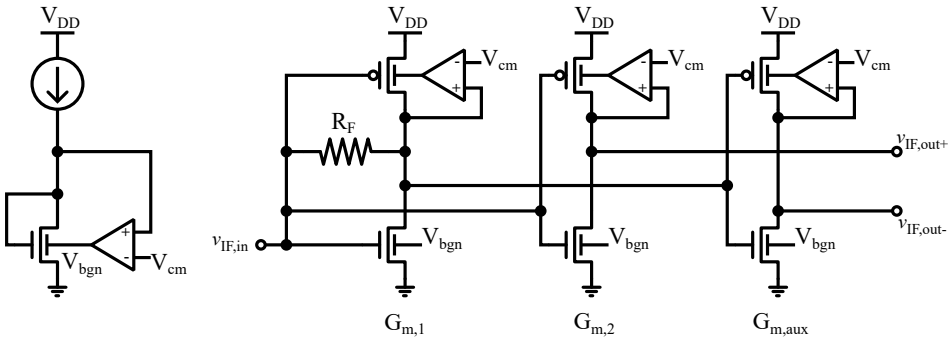


Figure 4.23: NC IF amplifier used in the MM mixer-first RX architecture [8].

mask the noise generated by the second stage $G_{m,2}$, thus the voltage gain Av_1 is chosen equal to -10. Since the RX operates as a MM mixer, the input impedance of the IF amplifier must be finite, however a large value still benefits the performance of the mixer then the IF amplifier is designed for a Z_{in} of 10 kΩ. The expression for the voltage gain in the first stage and input impedance are given by

$$Av_1 = 1 - \frac{G_{m,1}R_F}{1 + R_F g_{ds,1}} = -10, \tag{4.34}$$

$$Z_{in} = \frac{1 + R_F g_{ds,1}}{G_{m,1}} = 10k\Omega, \tag{4.35}$$

from which R_F and $G_{m,1}$ are calculated to be 110 kΩ and 0.1 mS, respectively. The current can be also estimated from the transconductance efficiency as $I_{D,1}$ = 2.3 μA. Having the estimate values for R_{Th} and R_F, it is possible to analyze the NC condition from Eq. (4.30)

$$1 + \frac{\zeta R_F}{R_{Th}} = \frac{G_{m,aux}}{G_{m,2}} \approx 250. \tag{4.36}$$

Considering the voltage gain of 10 in the first stage, the second stage $G_{m,2}$ must be designed for a similar transconductance or larger than $G_{m,1}$ to guarantee negligible noise contribution. In this design exercise it is chosen half the value of $G_{m,1}$, 0.05 mS. Even though this value is very small, the NC condition demands a very large ratio $\frac{G_{m,aux}}{G_{m,2}}$ which would required a $G_{m,aux}$ of 12.5 mS. This means the auxiliary stage would consume almost 300 μA, 125 times more than the first stage.

IF Amplifier for Voltage-Mode Mixer

Given the results derived in the design of the IF amplifier for the MM mixer, a question arises: is it better to design only a single transconductor with a value as large as $G_{m,aux}$

without a feedback resistor, thus obtaining an infinite input impedance and lower noise?. This alternative design would provide theoretical infinite impedance to the mixer-first, therefore operating it as a VM mixer. Table 4.2 shows a summary of the IF amplifier parameters for the case of a VM and MM mixer.

Table 4.2: Design comparison of IF amplifier parameters for a VM vs. MM with NC mixer.

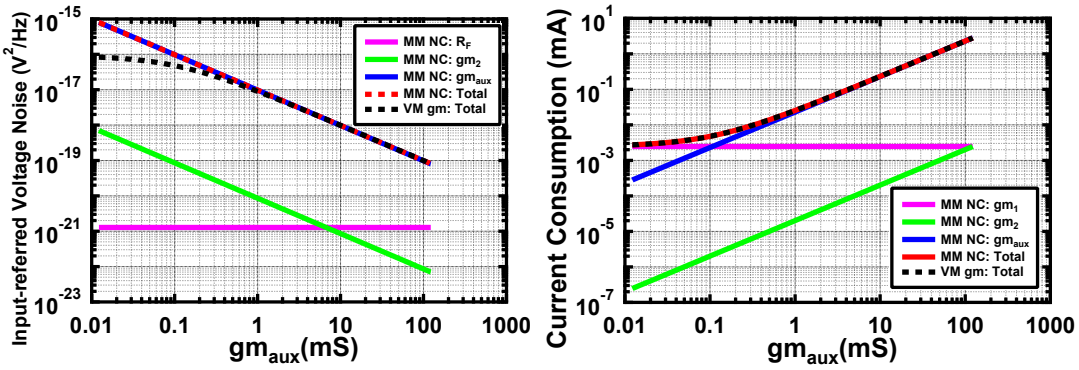
Parameters	Voltage-mode	Mixed-mode
Current budget	I_D	$I_{D,1} + I_{D,2} + I_{D,aux}$
Input impedance	∞	$\frac{1+R_F g_{ds,1}}{G_{m,1}}$
Transconductance	G_m	$\left(\frac{G_{m,1}R_F}{1+R_F g_{ds,1}} - 1\right) G_{m,2} + G_{m,aux}$
Amplifier input voltage noise	$4kT\frac{\gamma}{G_m}$	$4kT\frac{\left(G_{m,2}^2 R_F + \gamma G_{m,aux}\right)}{\left[\left(G_{m,1}R_F - 1\right)G_{m,2} + G_{m,aux}\right]^2}$

In order to have a fair comparison between VM and MM mixers, the IF amplifier is designed for the same current budget and same bias conditions. It means that the transconductance in the VM IF amplifier is equal to the sum of all transconductances in the MM IF amplifier, $G_m = G_{m,1} + G_{m,2} + G_{m,aux}$. For the same current budget the VM case exhibits a higher total transconductance. The amplifier input voltage noise depends on the biasing of transistors, weak inversion is assumed for all transistors in this design to have a higher transconductance efficiency. The term γ represents the excess noise factor of a transistor and, in the case of weak inversion, it is equal to 2/3. In the case of the VM it is clear the need of a higher G_m for lower noise, while in the case of the MM is not straightforward however it can be noted that a higher $G_{m,aux}$ reduces the overall noise.

The first stage of the MM IF amplifier is designed as in the previous section: $G_{m,1} = 0.1$ mS and $R_F = 110\,\text{k}\Omega$. The NC condition imposes that $\frac{G_{m,aux}}{G_{m,2}} = 250$, but the value of $G_{m,aux}$ (and in turn $G_{m,2}$) is a design variable that can be explored to find out whether is better to use a VM or MM mixer for the mm-wave mixer-first RX architecture.

Fig. 4.24 shows the VM and MM IF amplifier performance in terms of noise and current consumption for different values of $G_{m,aux}$. As presumed, the input-referred voltage noise is always lower for the VM, even with the NC scheme the MM only matches the performance of the VM when the auxiliary stage is much larger than the others. The current budget is set equal in both designs, but it is important to remark that for the range where the noise performance of MM reaches the VM, most of the consumption is due only to $G_{m,aux}$.

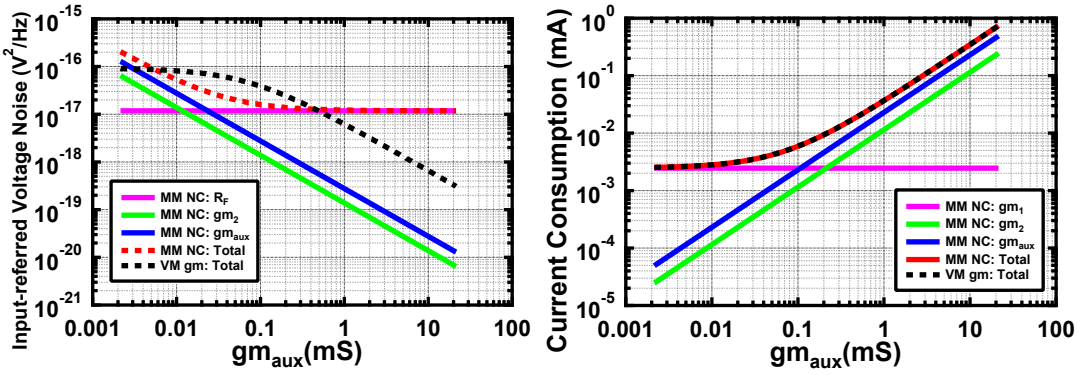
The calculated results in Fig. 4.24 make clear that for the mm-wave mixer-first RX is more suitable to use all the current budget in a single transconductor and operate the mixer in VM. Nevertheless, it is interesting to evaluate in which case would the MM mixer outperform the VM mixer. The main constraint in this design is the large ratio ratio between the auxiliary



(a) (b)

Figure 4.24: Calculated comparison between mixed-mode with noise cancelling and voltage-mode IF amplifier: (a) Input-referred voltage noise, and (b) current consumption.

and secondary stage imposed by the NC condition. Let's imagine a scenario where $R_{Th} = \zeta R_F = 22k\Omega$, hence the NC condition becomes $\frac{G_{m,aux}}{G_{m,2}} = 2$. Fig. 4.25 shows the noise and current consumption for said scenario. There is a design range for $G_{m,aux}$ in which the MM IF amplifier contributes with less noise than the VM one. Although the NC IF amplifier is not suitable for mm-wave mixer-first architectures it has been demonstrated that given a larger input impedance at the mixer, for instance using a LNA in the previous stage, the NC scheme could provide better performance than the VM.



(a) (b)

Figure 4.25: Calculated comparison between mixed-mode with noise cancelling and voltage-mode IF amplifier: (a) Input-referred voltage noise, and (b) current consumption.

As a final validation both MM and VM mixer-first have been simulated. The transconductors have been designed differentially based on the schematic shown in Fig. 4.23. The current budget is $I_{D,1} = 20\,\mu$A, $I_{D,2} = 10\,\mu$A, $I_{D,aux} = 200\,\mu$A, for the MM amplifier and $I_D = 230\,\mu$A for the VM amplifier. Must be noted from the current budget that the NC condition is not met because noise is traded off by power consumption. The chosen design ratio $\frac{I_{D,aux}}{I_{D,2}} = \frac{G_{m,aux}}{G_{m,2}} = 20$ is found as a good compromise to partially cancel the noise of the first stage while maintaining low power consumption. The simulation includes the mm-wave mixer-first designed in

section 4.2.2 with mixer switches extracted netlist and EM extractions for the GSG pads and transformer. Fig. 4.26 shows the performance comparison across the wide frequency band for the MM mixer with NC disabled and enabled, and for the VM mixer. The NC scheme is said to be disabled when the auxiliary path containing $G_{m,aux}$ is disconnected.

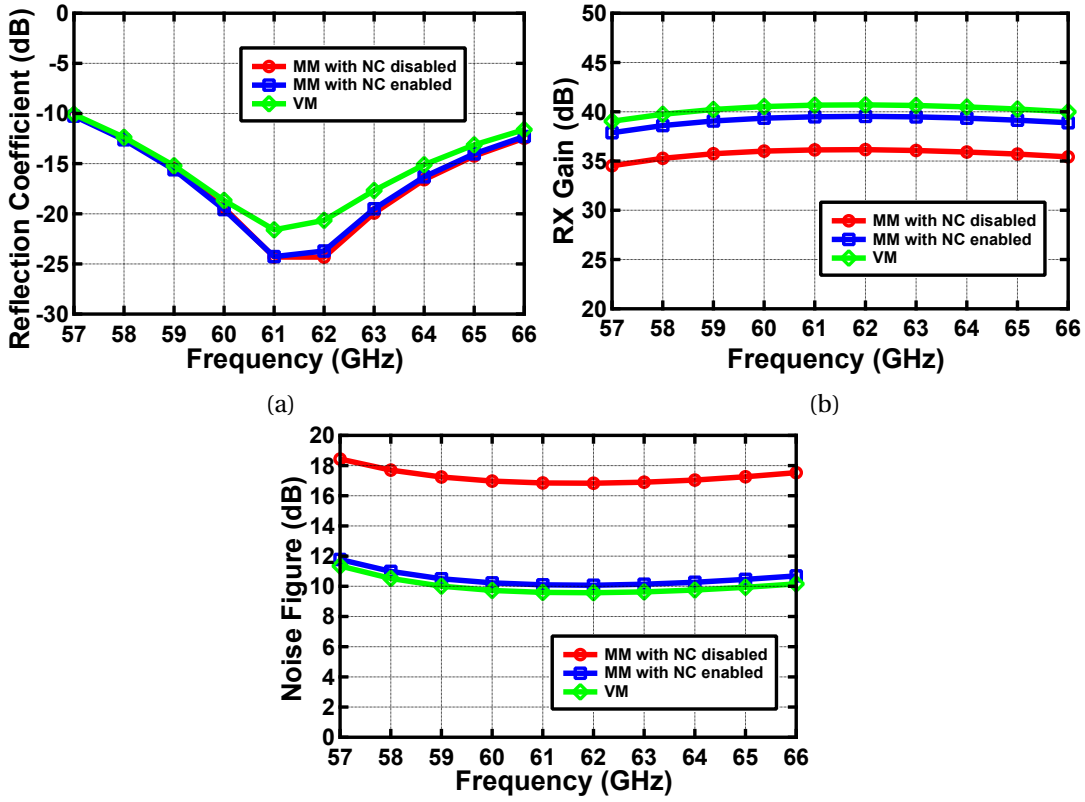


Figure 4.26: Simulated performance comparison between MM with NC disabled and enabled, and VM IF amplifier: (a) Reflection coefficient S11, (b) RX gain, and (c) Noise Figure.

Fig. 4.26a shows the reflection coefficient S11 always below −10 dB proving a good impedance matching, this is due to the fact that both MM and VM IF amplifiers are designed to provide a very large load impedance to the mixer-first. Fig. 4.26b shows that the gain of the VM is larger than the MM amplifier because the latter provides a larger load impedance to the mixer-first thus boosting its gain. The gain is even lower when the NC is disabled because the auxiliary path is not providing any gain, it is neither consuming any current though. Fig. 4.26c shows that effectively the MM and VM mixers have very similar NF performance as estimated in Fig. 4.24a, they achieve a NF of about 10 dB in the center of the band. The MM mixer with the NC scheme disable degrades its NF to almost 17 dB, though consuming only 13 % of the total current budget. Based on these simulation results, the VM amplifier is chosen to be implemented.

Amplifier Design

The entire design of the RX path is shown in Fig. 4.27a. One of the main advantages of the VM amplifier is the topology without a feedback resistor which does not decrease the baseband resistor that the mixer sees at its output. Moreover, a capacitive coupling is chosen to be able to set the bias of the amplifier independently of the bias of the mixer-first. Considering that the IF is around 1-4 MHz, then the coupling capacitor and biasing resistor are chosen 2 pF and 6 MΩ. A current re-use gm-R amplifier is designed to benefit from both NMOS and PMOS transistor for a fixed current budget. The biasing of the NMOS is fixed but the PMOS is controlled by a common-mode feedback (CMFB) circuit to adjust the common-mode output voltage within the ADC buffer range around 500 mV, the ADC is yet not integrated in this prototype. The voltage gain is set by a programmable output resistor R_{out} = [10 kΩ,20 kΩ,40 kΩ,80 kΩ]. This resistor should be matched to the resistor used in the PTAT that provides the bias current to the differential pairs for the gain to be constant across PVT variations.

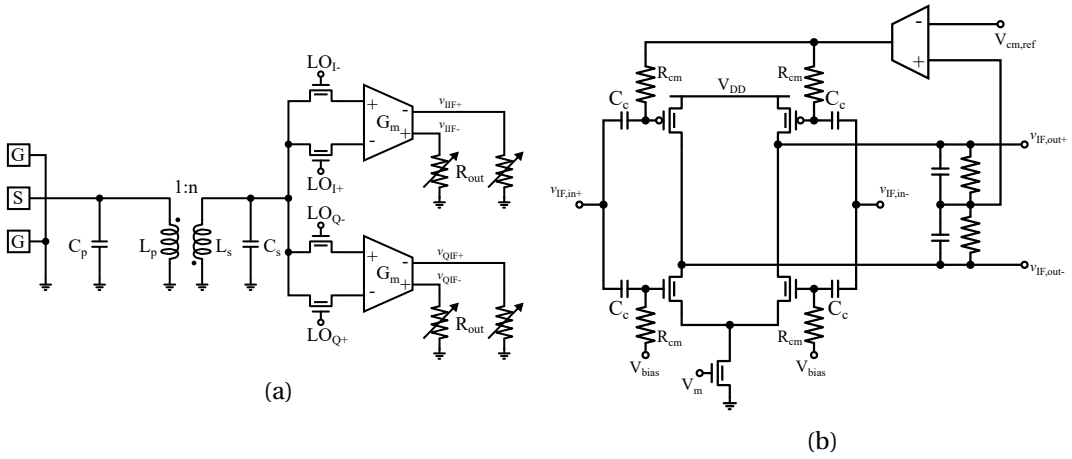


Figure 4.27: RX schematic: (a) Passive mixer-first, and (b) low-noise IF amplifier.

4.2.4 Simulation Results

The complete RX path was simulated together, it includes extracted netlists from Calibre for LO buffers, mixer, IF amplifier, biasing circuits, and EMX S-parameter extractions for all the passives structures. These simulations were performed with a LO input signal of 200 mV peak amplitude. The simulation performed is HB (Harmonic Balance) together with the HBSP for S-parameters, HBAC for RX conversion gain, and HBNOISE for Noise Figure (NF).

There are basically two parameters that can be adjusted: IF amplifier gain, and LO DC bias. The later is used to drive the switches whether into class C to reduce phase overlap and NF or towards class B to improved linearity. The register to control the gain can be configured from 0 to 3, with a 3-dB step, from 18 to 27 dB. The register to control the LO DC bias voltage can be configured from 0 to 7, with a 10-mV step, from 60 to 130 mV. The simulations are performed across the RF bandwidth that ranges from 57 to 66 GHz, and the IF bandwidth

which is designed from 10 kHz to 10 MHz. The IF would depend on the BPSK modulation applied on the TX plus the beat frequency depending on the distances to the target.

Impedance Matching

In order to avoid power reflections and efficiently transfer the input power from the RX GSG interface to the rest of the path it needs to be match to 50 Ω. Fig. 4.28 shows the reflection coefficient S11 for the RX path and the input power 1-dB compression point. The former proves the good input matching achieved with the transformer-based matching network across the wide bandwidth of 9 GHz. The later shows that the RX path does not exhibit linearity issues below an average of −16 dBm input power across the 9 GHz bandwidth. The measured TX-RX isolation is the same as reported in section 4.1, it is around 38 dB.

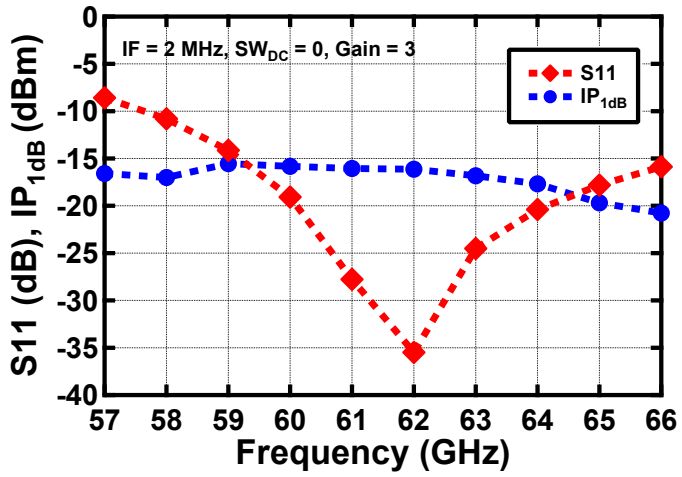


Figure 4.28: Reflection coefficient S11 and Input Power 1-dB Compression Point.

The simulation was performed with an IF of 2 MHz, switches driven in class C, and maximum voltage gain. S11 does not vary if the previous parameters are changed. In the case of IP_{1dB} the gain does not affect because compression is taking place in the switches and not in the IF amplifier, however, the change of SW_{DC} drives the switches towards class B and linearity can be improved.

Conversion Gain: IF Bandwidth

The voltage gain in the RX path is controlled by the output resistors in the IF amplifier shown in Fig. 4.27a. This resistor is matched to the resistor used in the PTAT which is used to bias the differential pair of said amplifier. Therefore, the gm-R product in the amplifier is constant across PVT variations.

The voltage gain is controlled by connecting segments of the output resistor. The IF response of the RX path is shown in Fig. 4.29, with a minimum gain of 18 dB up to the maximum of

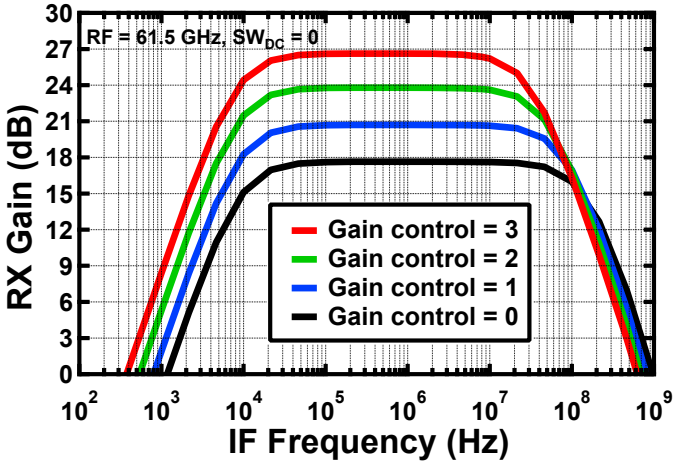


Figure 4.29: IF response on RX conversion gain.

27 dB. The 3-dB bandwidth for the case of maximum gain goes from 10 kHz to 30 MHz. The simulation is performed with an RF signal at 61.5 GHz and mixer switches driven in class C for maximum gain.

Conversion Gain: RF Bandwidth

The programmable gain in the IF amplifier barely affects the NF because the minimum gain (Gain control = 0) is enough to mask the noise from subsequent stages. However, the gain variation across the 9 GHz bandwidth comes from the frequency-dependent performance of the mixer and LO buffers. This means that any additional loss in the mixer is not masked by the IF amplifier, and it is added directly to the NF.

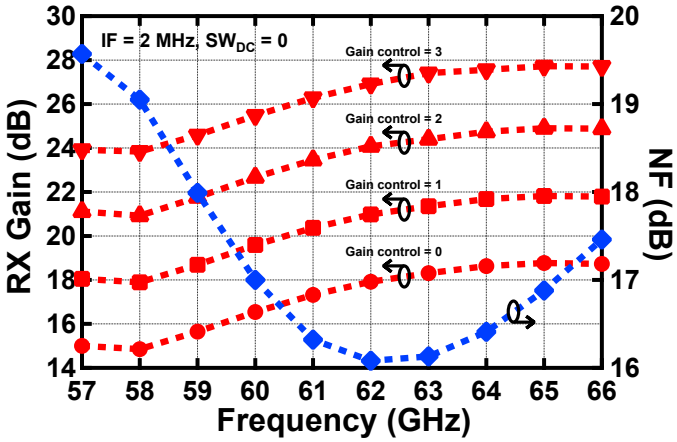


Figure 4.30: RX gain and NF.

In Fig. 4.30 can be observed that the gain step is always 3 dB, same as shown in Fig. 4.29, but it varies across the RF bandwidth. At the upper limit of the band, 66 GHz, the gain is maximum and approximately 4 dB higher than the minimum gain occurring at the lower limit of the

band, 57 GHz. This almost 4 dB difference is reflected in the NF curve (same curve regardless of gain setting). The best performance is obtained around 62 GHz. The simulations were performed with an IF of 2 MHz, and mixer switches driven in class C for maximum gain, low linearity.

Input Power 1-dB Compression Point (IP_{1dB})

The TX-RX leakage is an important limitation for FMCW radars which have both TX and RX operating simultaneously. As reported before in chapter 3, the TX peak output power is approximately 0 dBm, it means that assuming a worst-case TX-RX isolation of 20 dB, the RX requires at least −20 dB IP_{1dB}. The assumption of 20 dB isolation comes from literature, however, in the case the isolation is worse than predicted, the RX can be reconfigured to improve its IP_{1dB}. The transistors used as switches have a threshold voltage around 170 mV, it means that setting the register to SW_{DC} = 0 the gate of the switch is biased at 60 mV, driving them in class C, thus more gain and less linearity. The DC voltage can be increased setting SW_{DC} up to a maximum value of 7 corresponding to 130 mV, where the switches are bias towards class B showing better linearity, but trading off conversion gain which is happening before the IF amplifier means it adds directly to the NF.

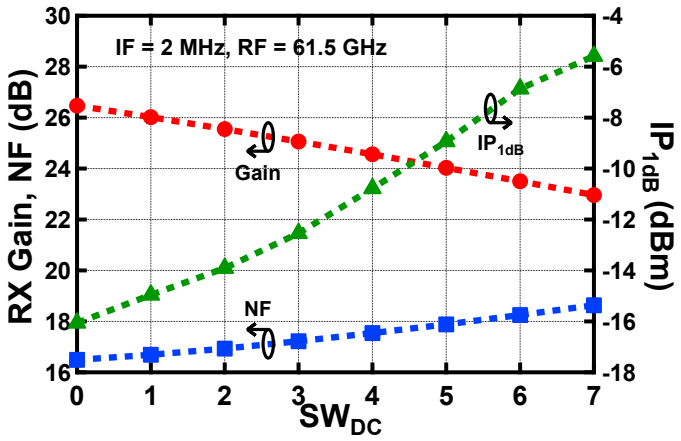


Figure 4.31: RX Mixer switches tuning to improve IP_{1dB}.

Fig. 4.31 shows the trade off between IP_{1dB} versus conversion gain and NF. The simulation is performed at RF of 61.5 GHz, with an IF of 2 MHz, and with a maximum gain set to 3. The RX can trade approximately 3 dB of gain and NF for an increase in linearity from −16 to −6 dBm, in case of large TX-RX leakage or a blocker.

Current Consumption

The RX path current consumption is negligible compared to the rest of mm-wave blocks because it is a passive mixer. Most of the current consumed related to the RX is due to the LO buffers and a relatively small consumption by the IF amplifiers. Fig. 4.32 shows the trade

off between the NF and the current consumption of the LO buffers. Only the buffers current consumption is observed because it is the one impacting the NF before any gain mask the noise from subsequent stages.

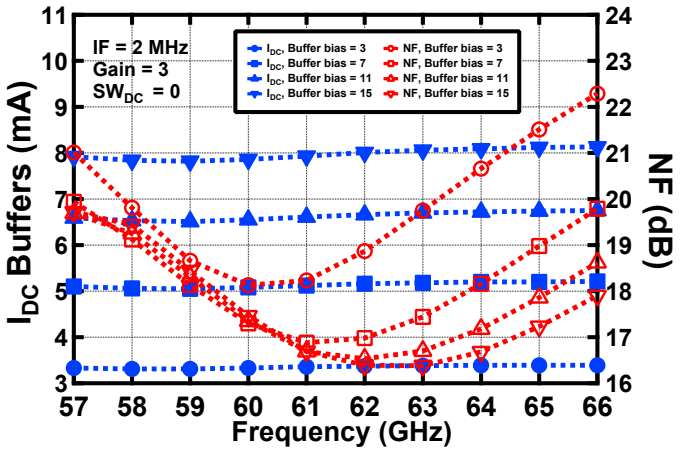


Figure 4.32: Trade-off between NF and current consumption.

The simulation across the entire RF bandwidth at IF of 2 MHz, maximum IF amplifier gain set to 3, and minimum SW_{DC} set to 0, shows that consuming more current in the buffers and in turn larger LO amplitude, decreases the NF in the passive mixer. The buffer current bias can be configured from 0 to 15, consuming each I and Q buffer a maximum of 4 mA, a total of 8 mA. It can also be noted that the current consumption across the RF bandwidth does not vary much for the various bias setting.

As stated before, the current consumption of the entire RX path is dominated by the I and Q LO buffers. Fig. 4.33 shows a comparison between the current consumption of the buffers and IF amplifiers across the RF bandwidth. The average IF amplifiers current consumption is 375 μA, almost negligible compared to the I and Q buffers operating at mm-wave and consuming more than 20 times more.

4.3 Summary

This chapter presented two low-power 60-GHz mixer-first RX architectures implemented in GF 22-nm FDSOI CMOS technology. The first design is an active mixer based on a down-conversion Gilbert-cell. The main advantages of this mixer is that it does not require a large LO swing and it can provide voltage gain. However, the noise contribution of the active components significantly degrades the total NF in a mixer-first architecture. The second RX design proposes a passive mixer-first with a transformer-based input matching network. This design profits from the fact that at mm-wave the harmonic reupconversion and dissipation effects are almost negligible. On the downside, the LO buffers require larger voltage swing to drive the switches and they consume more than in the active mixer, although the mixer itself does not consume any active power. The mixer operates in voltage-mode with an IF amplifier

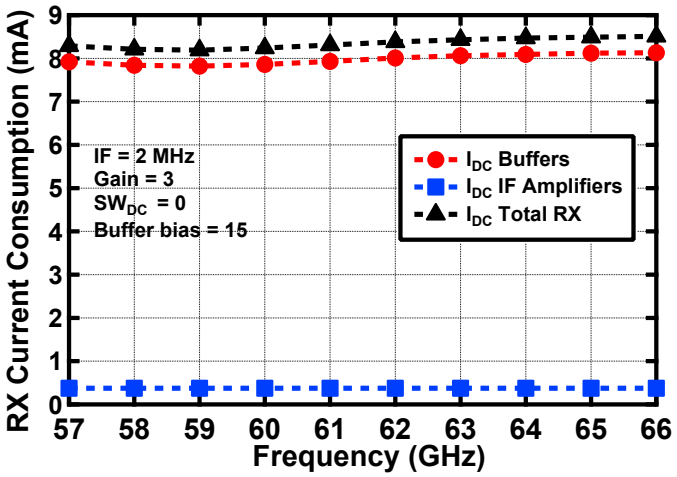


Figure 4.33: RX current consumption: I and Q LO buffers, IF amplifiers, and total.

based on a gm-R stage with configurable gain and CMFB loop.

Table 4.3: Comparison with the state-of-the-art 60-GHz radar receivers.

Ref.	Tech.	Freq. (GHz)	Gain (dB)	NF (dB)	IP_{1dB} (dBm)	P_{DC} (mW)
[9]	350-nm SiGe	57-64	19	9.5	-8.5	990[a]
[10]	130-nm SiGe	58.5-63.5	24	9.8	-12	218
[11]	65-nm Bulk	76-81	78.8	15.3	-8.5	78[b]
[12]	28-nm Bulk	57-64	77	12	-12	40[b]
[13]	28-nm Bulk	57-66	46	10.5	-	5.6[b]
This Work active mixer	**22-nm FDSOI**	**57-66**	**6**	**30**	**-18**	**7.2**
This Work passive mixer	**22-nm FDSOI**	**57-66**	**26/23[c,d]**	**16/19[c,d]**	**-16/-6[c,d]**	**6.4**

[a] Entire radar power consumption (LO+2TX+4RX). [b]LO distribution (buffers) not included.

[c]Mixer switches driven in class C/class B. [d]Simulation.

The RX performance is compared to state-of-the-art radar RXs in Table 4.3. The passive mixer

implementation allows to further reduce the power consumption down to 6.4 mW including the LO buffers. The NF is 16 dB meeting the specifications defined in chapter 2 for short-range radars. The passive mixer also provides enough margin to tolerate large TX-RX leakage. Thanks to the DC bias control in the switches the RX can trade off NF and gain for IP_{1dB}, particularly important for very close targets. Measurements in the second prototype of the RX could not be performed due to technical problems with the probe station and sample dies. The active and passive mixers capabilities are validated in FMCW radar measurements in chapter 5.

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5 An Ultra Low-Power Short-Range 60-GHz FMCW RADAR

This chapter presents two prototypes of the ultra-low power 60-GHz FMCW RoC implemented in GF 22-nm FDSOI CMOS. The first prototype includes the TX and RX circuits presented in section 3.1 and section 4.1, respectively. The second prototype includes the power-optimized versions of the TX and RX in section 3.2 and section 4.2. The performance of the frequency synthesizers of both chips is reported to complement the results shown in chapter 3 and chapter 4. Finally, the two chips are mounted in radar platforms built to demonstrate their ranging capabilities in short-range scenarios.

5.1 First Prototype

The radar block diagram of the first prototype is shown in Fig. 5.1, consisting in 2 TXs and 2 RXs. The frequency synthesis is based on an all-digital phase-locked loop (ADPLL) with a quadrature digital-controlled oscillator (QDCO) to be able to perform coherent detection for phase estimation. The in-phase (I) and the quadrature (Q) outputs of the ADPLL are followed by two buffers each to minimize the impact of the load to the QDCO as much as possible. The first I buffer is used to drive the TX, the first Q buffer is used to close the ADPLL following a frequency divider chain. The second I and Q signals are used in the RX for down-conversion. The TX-RX slices are designed and layouted with a modular approach to facilitate the addition of more TX and RX slices. After the first TX-RX slice, the distribution of the LO to the next slices require additional DCO buffers, shown vertically in Fig. 5.1. Note that in this chapter the LO buffers mentioned in the previous chapters are referred as DCO buffers. The ADPLL includes also a time-to-digital converter (TDC), a digital-to-time converter (DTC), and a digital loop filter. The latter is implemented off-chip on an FPGA platform to provide flexibility to the design and test of the filter.

The 60-GHz FMCW radar is designed and fabricated in GF 22-nm FDSOI CMOS process (see Fig. 5.2a). The die dimensions are 2.5 mm × 1.25 mm including passive test structures, however the actual radar area is only 1 mm × 1.25 mm. The chip has been characterized, as shown in Fig. 5.2b, by on-chip probing on the TX and RX pads with 200-μm pitch GSG

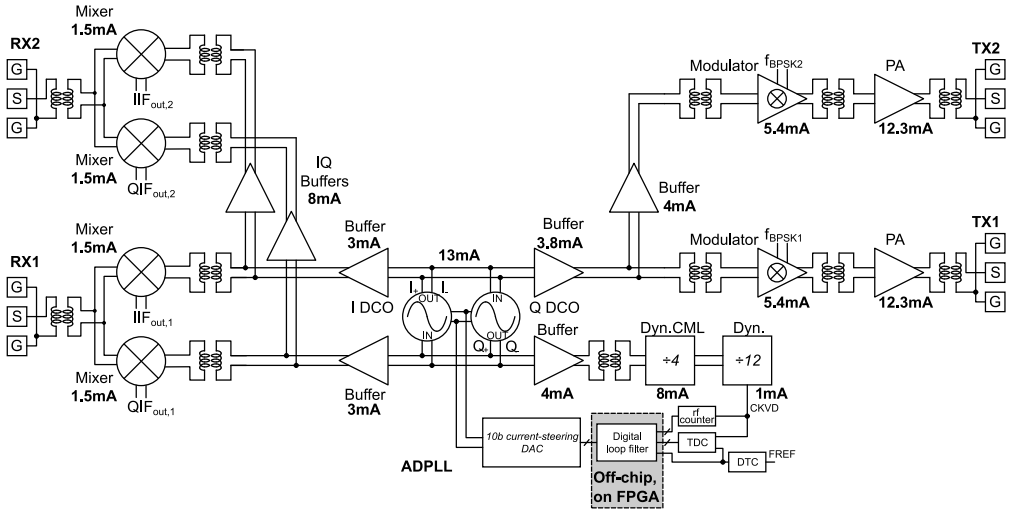


Figure 5.1: FMCW radar block diagram of the first prototype.

probes (Picoprobes Model VMM65). Each probe is connected to a 1-mm coaxial cable to a coax-to-waveguide adapter (V281C). The rest of the low frequency signals have been wire-bonded. In order to build a demonstrator and validate the radar capabilities some of the chips have the TX and RX GSG pads also wire-bonded to connect to the antennas on the PCB. To minimize the length of the bondwires, especially for the TX and RX signals, the chip was mounted on a trench in the PCB to lower the height of the pads, and glob-top was added to provide protection.

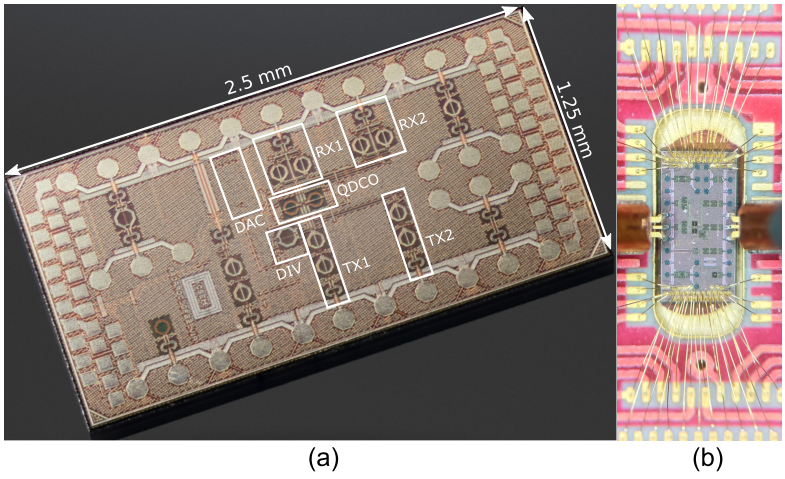


Figure 5.2: (a) Die microphotograph, and (b) on-chip probing.

5.1.1 RADAR Setup

The device under test (DUT) is connected to an FPGA where the loop filter is implemented in order to close the loop of the ADPLL. The QDCO frequency is measured directly at 60 GHz us-

ing a Keysight PXA Signal Analyzer N9030A (with harmonic mixer M1970V). However, it is not possible to measure PN and frequency chirp directly at 60 GHz with the available instruments. The signal is required to be downconverted, amplified and divided using commercial components shown in Fig. 5.3. Downconversion is performed by means of a waveguide passive mixer (PE12D1002) driven by a 77 GHz carrier generated by the up-conversion of a 12.83 GHz signal (HP 83620B and R&S ZVA-Z75). The downconverted signal is amplified (ZX60-24-S+) and divided by two ultra low SSB PN frequency divider-by-4 (HMC447LC3 and HMC365). After the divider stages, the signal falls in the frequency range from 0.6875 to 1.25 GHz. The PN is measured by a signal source analyzer (E5052B), and the frequency chirp by a high frequency oscilloscope (Teledyne LeCroy SDA 813Zi-B). The measured PN is calibrated from the division gain: $20\log_{10}(16) = 24$ dB.

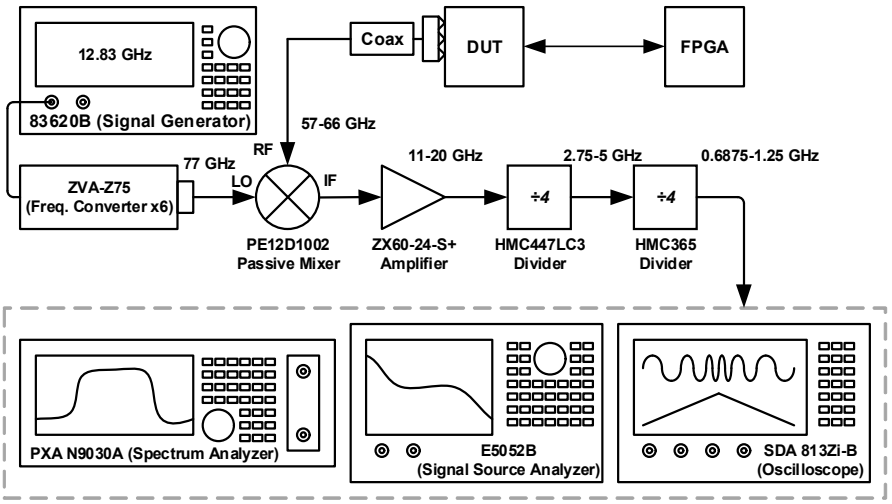


Figure 5.3: Measurement setups for PN and frequency chirp.

5.1.2 Measurement Results

The QDCO was first presented in [1], moreover the work is complemented in this section by adding closed-loop and radar measurements. The open-loop QDCO frequency and power consumption versus DAC control code measurements and simulations are shown in Fig. 5.4a and Fig. 5.4b. There are 8 sub-bands available for static calibration in Fig. 5.4a. Each of the sub-bands covers between 10.7 and 12 GHz, while the total tuning range is 16.7 GHz (26 %) from 54.8 to 71.5 GHz. The current consumption depends on the coupling within the QDCO and it increases with frequency as shown in Fig. 5.4b, the results are only shown for one capacitor band because the difference between sub-bands is negligible. Current consumption ranges from 6.3 to 18.3 mA across one sub-band, with an average of 13 mA considering a linear frequency sweep. For further measurements the QDCO sub-band is set to 5 where the frequency sweep is centered around the target band.

The CML and dynamic dividers used to close the ADPLL loop consume 6.4 mW and 0.8 mW,

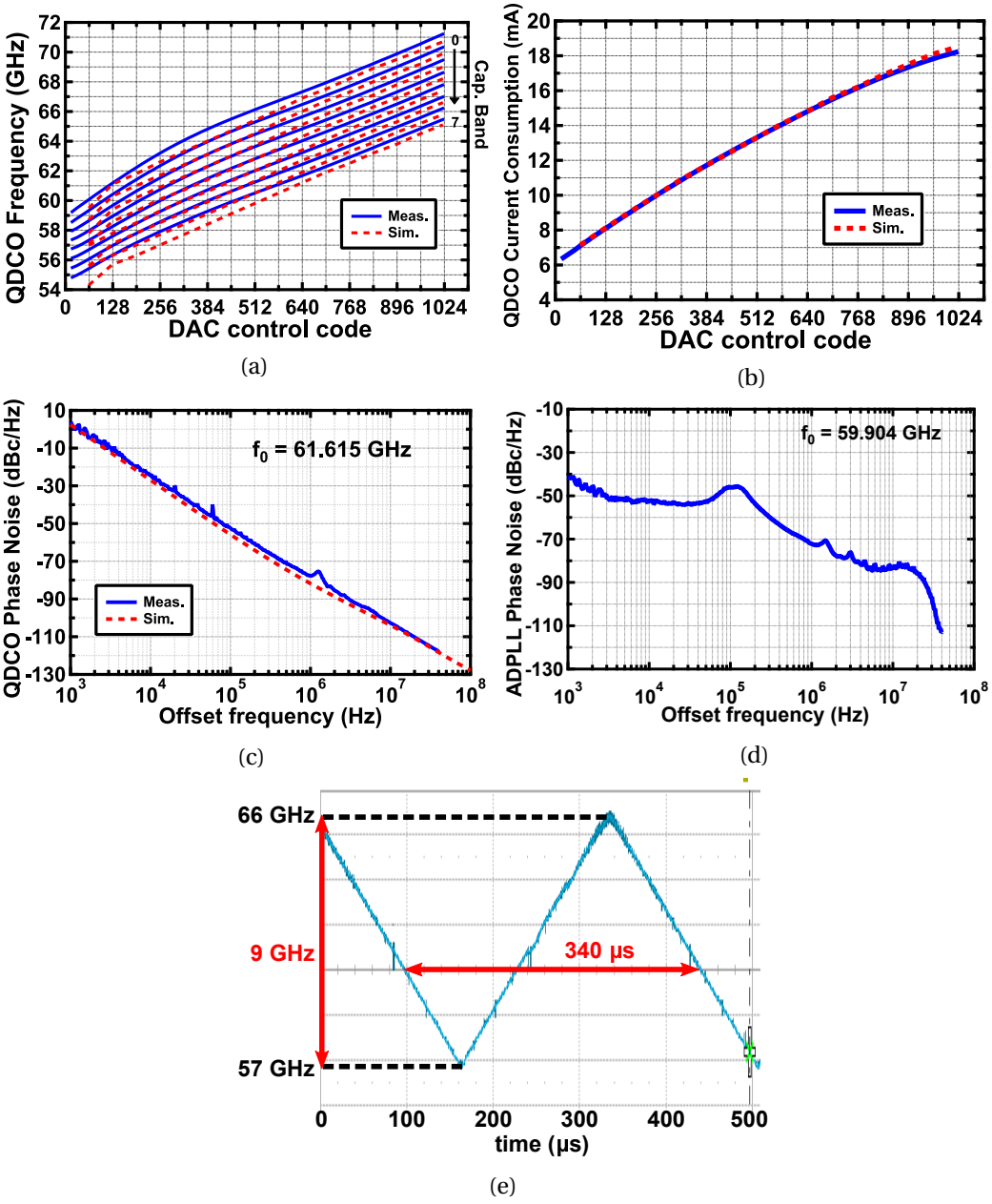


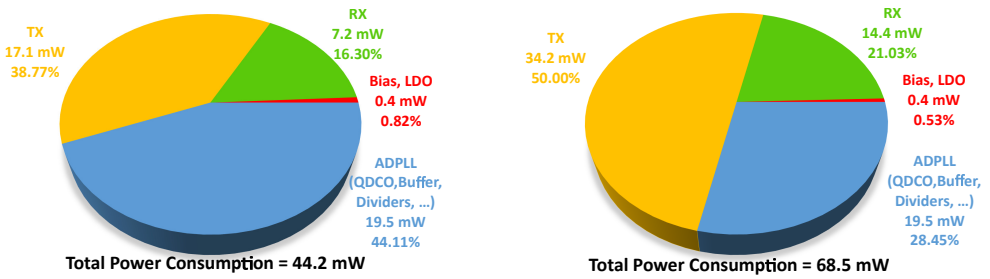
Figure 5.4: First prototype QDCO measurements: (a) QDCO Frequency (b) Current consumption. ADPLL Measurements: (c) Open-loop PN, (d) Closed-loop PN, and (e) FMCW chirp versus time.

respectively. The dynamic topology used in the second divider helps to maintain low power operation of the overall system. Furthermore, to the authors knowledge, this is the first demonstration of dynamic logic based dividers operating at such high frequencies as 15 GHz [1]. The PN is measured in open-loop and closed-loop with a PLL bandwidth of 200 kHz, as shown in Figs. 5.4c and 5.4d. The PN is −73 dBc/Hz at 1 MHz frequency offset. The oscillator was not optimized for PN and it was rather traded to achieve the wide tuning range in the DCO. A

relatively high PN can be afforded as long as the same frequency synthesizer is used in TX and RX thanks to the autocorrelation attenuation effect previously demonstrated in section 2.2.2. Although other works on QDCO have reported PN as low as −95 dBc/Hz [2], this work prioritizes to achieve a wide tuning range to benefit from a better range resolution for FMCW radar applications. The trade-off of this seamless wideband tuning mechanism is the quality factor degradation because it does not operate at the resonance frequency. Moreover, the tuning technique requires to bias each transistor pair of the oscillators independently, therefore the QDCO is designed with parallel coupling which further degrades noise performance. The figure of merit considering the tuning range (FoM_T) is −177 dBc/Hz, proving to be as low as other state-of-the-art DCOs at mm-wave [1].

Since the ADPLL is closed off-chip by means of an FPGA, the digital control signals from TDC, DTC, and DCO are connected off-chip to level-shifters on the test board which are then connected to the FPGA GPIOs. Unfortunately, the delay time is not guaranteed to be the same in every control signal. Some of the DCO control signals arrive before others and produce glitches. The triangular FMCW chirp is shown in Fig. 5.4e, successfully sweeping 9 GHz with a ramp-up duration as short as 170 μs, and a repetition period of 340 μs.

The average power consumption of the chip is only 44.2 mW for 1TX/1RX and 68.5 mW for 2TX/2RX. The power consumption breakdown corresponding to the on-chip radar is shown in Fig. 5.5. In the case of 1TX/1RX most of the power is consumed by the ADPLL. Nevertheless, it is the TX-RX slice which usually dominates the total power consumption in a MIMO scheme because they are replicated while the ADPLL is placed only once. This radar has four virtual channels considering the configuration with 2TX/2RX, meaning that the power consumption per channel is only 17.1 mW.



(a) (b)

Figure 5.5: Power consumption breakdown of the first radar prototype for a configuration of (a) 1TX/1RX, and (b) 2TX/2RX.

A platform built based on the proposed FMCW radar using patch antennas fabricated on PCB is shown in Fig. 5.6a, the antennas are designed based on [3], with a gain of 7 dBi. A corner reflector with triangular faces is used to measure ranges from 20 to 50 cm, the setup including the FPGA is shown in Fig. 5.6b. The length of the side edges of the three isosceles triangles is 12 cm, giving a calculated RCS of approximately 15 dBsm[4]. The FMCW sweep is configured for a ramp-up duration of 340 μs. The beat frequency is measured using the

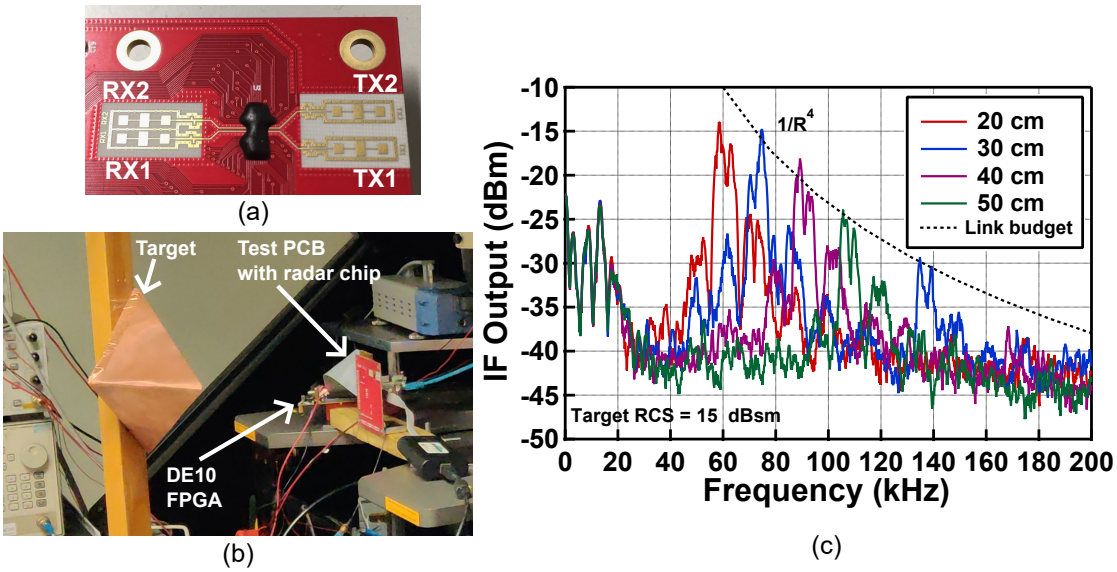


Figure 5.6: (a) Test board with antennas, (b) Radar setup, and (c) Range measurements with the radar prototype with a corner reflector at the distance of 20, 30, 40, and 50 cm.

Keysight PXA Signal Analyzer N9030A with a RBW = 1 kHz which provides extra processing gain and the results are shown in Fig. 5.6c. Although the analysis in chapter 2 does not account for the losses in the bondwires and PCB interface to the antennas, additional loss is added in the calculations to demonstrate that the measurement results follow the $1/R^4$ behavior from the radar equation. The discrepancy at 20 cm is explained by the fact that the antenna beamwidth is not large enough to illuminate the entire reflector at this distance, resulting in having a lower RCS for this particular measurement. The theoretical frequency step between 10-cm spaced measurements is 17.65 kHz, while the actual measurement is approximately 16 kHz, corresponding to a relative error of 9.3 %. There are extra delays between the TX and RX interfaces of our chip to the antennas adding for a frequency/range systematic offset, this is the reason why the frequency error discussed here is taken from relative measurements and not absolute ones. The radar sensing capability is verified by several range measurements successfully detecting the target.

5.2 Second Prototype

The block diagram of the second radar prototype is shown in Fig. 5.7. The most important modifications compared to the first prototype is the implementation of the PAMIX (section 3.2) and the passive mixer-first (section 4.2) to lower the overall power consumption. In addition, the ADPLL now includes the digital loop filter and it is now fully integrated discarding the need of the FPGA previously used. The LO buffers driving the mixer switches consume slightly more because the passive mixer requires a larger swing than the active mixer in the first prototype. The number of channels also increases to 4 TXs and 4 RXs paths, the radar can potentially have 16 virtual channels. The chip also includes a crystal oscillator (XO) and bandgap reference.

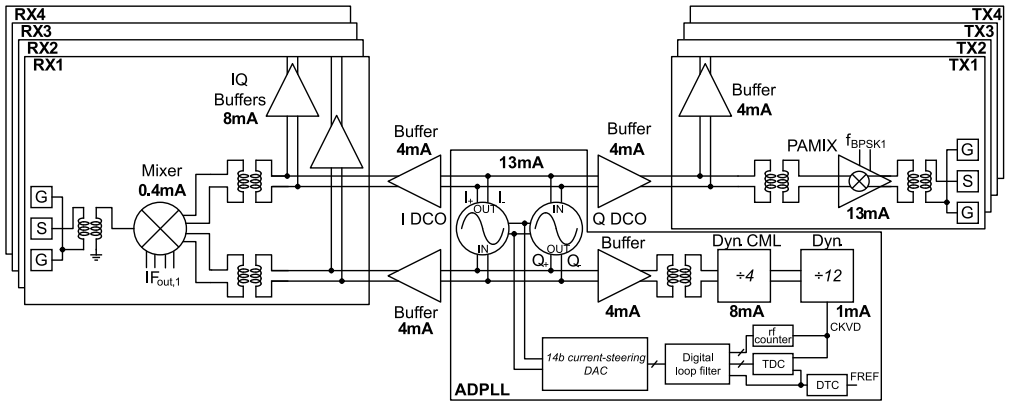
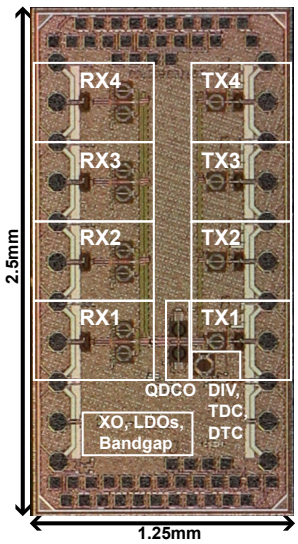


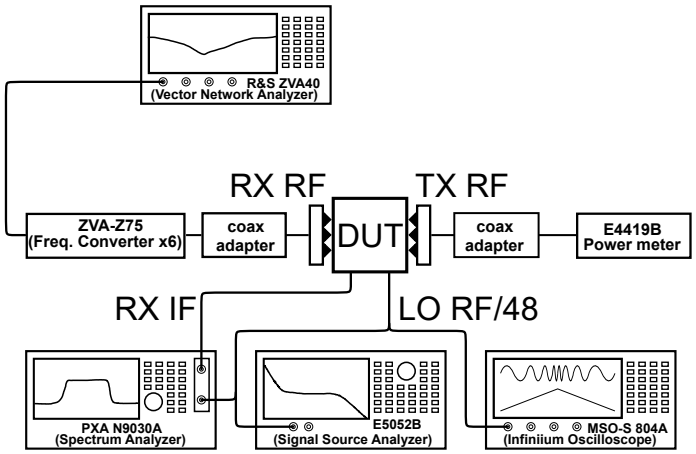
Figure 5.7: FMCW radar block diagram of the second prototype.

5.2.1 RADAR Setup

The measurement setup diagram is shown in Fig. 5.8b. This new prototype also includes a test buffer which outputs the divided DCO signal divided by 48. This divider buffer greatly simplifies the characterization of the DCO and ADPLL because it avoids the need of probing and the measurements are performed through the μFL connector. The spectrum analyzer (N9030A) is used to measure the frequency, the signal source analyzer (E5052B) measures accurately the phase noise in both open and closed loop, and an Infiniium oscilloscope (MSO-S 804A) for frequency chirp measurements.



(a)



(b)

Figure 5.8: (a) Die microphotograph, and (b) measurement setups for characterization of the second prototype.

Fig. 5.8b also shows the characterization setup used for the TX and RX carried out in a probe station. The TX output power was measured with a power meter and the RX was characterized

injecting a signal from a signal generator (or using the VNA) followed by a frequency converter (ZVA-Z75) and the IF output is measured with a spectrum analyzer or oscilloscope.

5.2.2 Measurement Results

QDCO Performance

The QDCO core is designed as in the first prototype to cover the frequency band from 57 to 66 GHz. The frequency tuning was modified adding 4 more control bits to obtain a 14-bit current-steering DAC. As in the first prototype, the QDCO also includes a coarse capacitor bank to correct any potential frequency shift in the operating bandwidth.

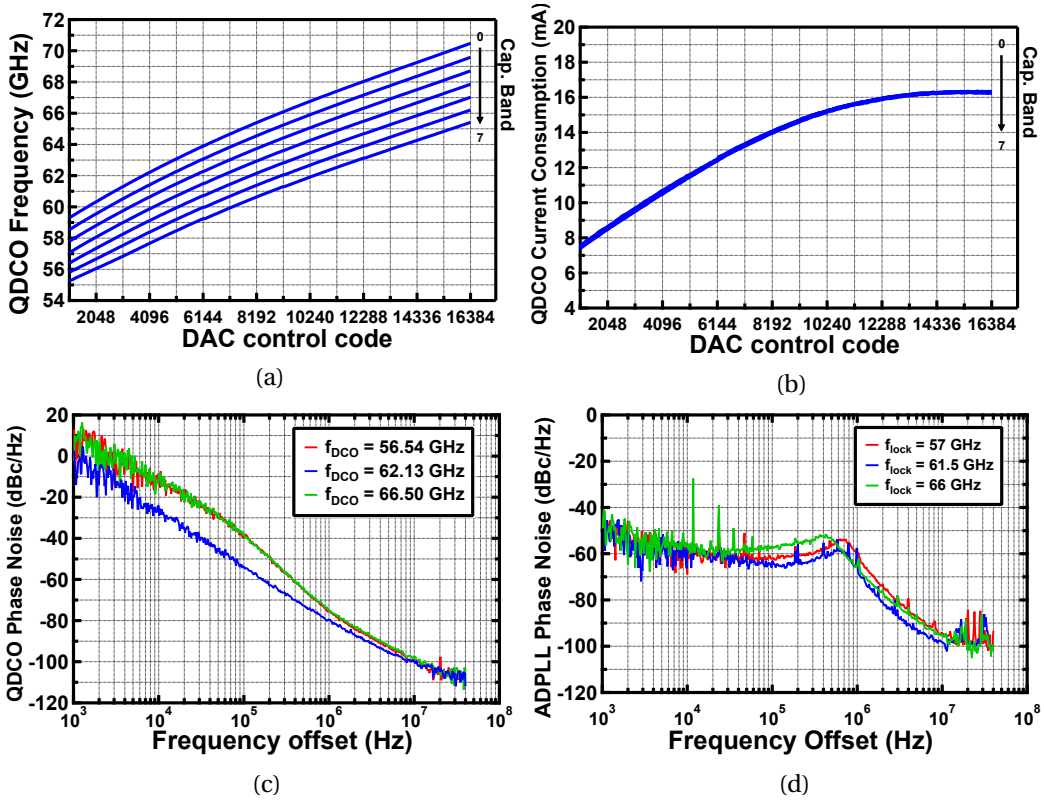
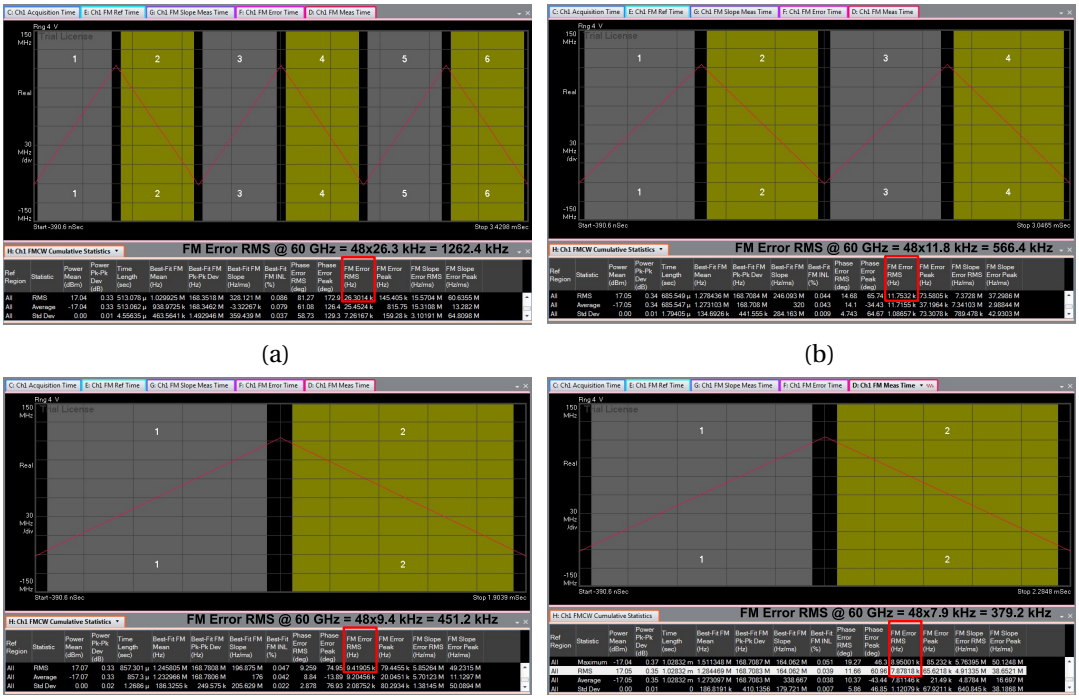


Figure 5.9: Second prototype QDCO measurements: (a) QDCO Frequency (b) Current consumption. ADPLL Measurements: (c) Open-loop PN, and (d) Closed-loop PN.

The QDCO achieves seamless frequency tuning over more than 10.6 GHz using the current steering mechanism and up to 15.8 GHz (25.7 %) using the 3-bit capacitor sub-bands, as shown in Fig. 5.9a. The nominal frequency step for the seamless frequency tuning is 700 kHz. The current consumption shown in Fig. 5.9b ranges from 7.7 mA and 16.5 mA. The QDCO PN is measured after the on-chip division by 48 with the ADPLL divider followed by a buffer and scaled by the frequency ratio. Fig. 5.9c shows the open loop PN spectrum at the beginning, the middle and the end of the tuning range.

ADPLL Performance

The ADPLL closed-loop PN is shown in Fig. 5.9d, it is −72 dBc/Hz at 1 MHz frequency offset. The frequency chirp measurement is performed in closed-loop, and it has been measured for different chirp slopes through the test buffer at the divided-by-48 LO frequency by means of the Infiniium oscilloscope (MSO-S 804A). There is a register named *ckrate* to control the rate at which the frequency step is applied. The value '0' corresponds to the fastest sweep rate, it means the larger the value of *ckrate* the slower the sweep rate. Fig. 5.10 show frequency chirps from 57 to 66 GHz with *ckrate* from 2 to 5.



(a) (b)

(c) (d)

Figure 5.10: Frequency chirp from 57 to 66 GHz measured at the divided-by-48 buffer output with: (a) *ckrate* = 2, (b) *ckrate* = 3, (c) *ckrate* = 4, and (d) *ckrate* = 5.

In all cases shown in Fig. 5.10 the swept bandwidth BW is 9 GHz, they also show the RMS frequency error δf at LO/48. The FM nonlinearity can be calculated as follows

$$Lin = \frac{\delta f}{BW}. \tag{5.1}$$

The nonlinearity can be translated to a degradation of range resolution given by

$$\Delta R = \sqrt{\left(\frac{c}{2 \cdot BW}\right)^2 + (Lin \cdot R)^2}, \tag{5.2}$$

where c is the propagation velocity, and R is the range at which a target is located. In the ideal case of zero nonlinearity the theoretical range resolution is 16.67 mm. Table 5.1 shows a summary of the nonlinearity effects for different chirp rates.

Table 5.1: Measured FM nonlinearity.

Chirp rate	Chirp slope @ 60 GHz	δf @ 60 GHz	FM Nonlinearity
ckrate = 2	0.328 x 48 = 15.75 MHz/μs	26.3 x 48 = 1262.4 kHz	140×10^{-6}
ckrate = 3	0.246 x 48 = 11.81 MHz/μs	11.8 x 48 = 566.4 kHz	63×10^{-6}
ckrate = 4	0.197 x 48 = 9.45 MHz/μs	9.4 x 48 = 451.2 kHz	50×10^{-6}
ckrate = 5	0.164 x 48 = 7.28 MHz/μs	7.9 x 48 = 379.2 kHz	42×10^{-6}

Fig. 5.11 depicts the range resolution dependence on range for different chirp rates. The resolution degradation due to nonlinearity of the FMCW chirp is theoretically calculated using the measured RMS frequency error. The ADPLL is found suitable for the target short-range applications (< 5 m) adding negligible degradation on the range resolution even for the fastest chirp rate (*ckrate* = 2).

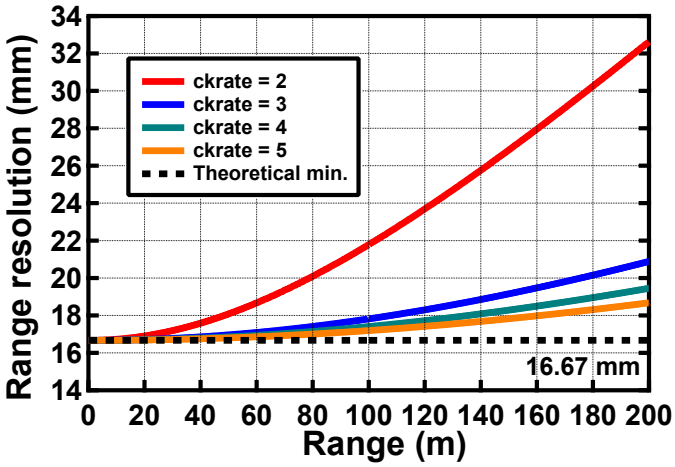
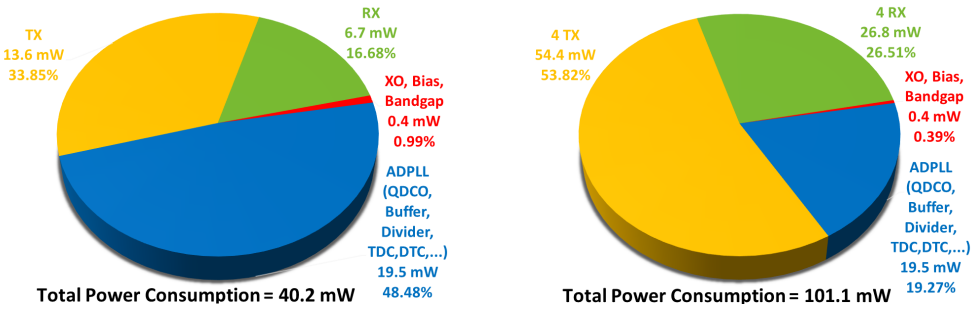


Figure 5.11: Range solution calculation vs. range for different chirp rates.

Radar Measurements

The power consumption breakdown of 1TX/1RX and 4TX/4RX configurations are shown in Fig. 5.12. In the former most of the power is consumed by the ADPLL with 48.48 % out of the total of 40.2 mW. While it is the TX-RX slices which dominates in the MIMO scheme, particularly the TX which consumes 53.82 % out of the total of 101.1 mW.

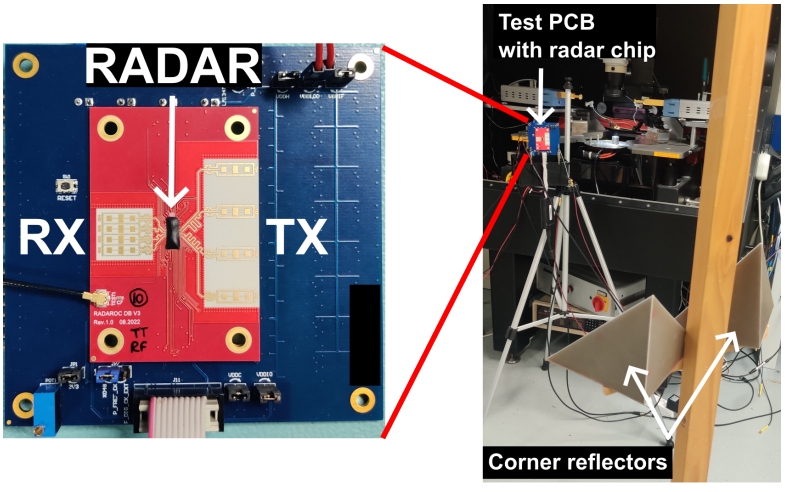
The range measurements are performed using the same patch antenna design as in the first



(a) (b)

Figure 5.12: Power consumption breakdown of the second radar prototype for a configuration of (a) 1TX/1RX, and (b) 4TX/4RX.

prototype. The main difference is that now the antennas are fabricated on a daughterboard alone to save costs on the RO4350B substrate, while the rest of the test board, including the IF amplification and filtering (see section 4.1.2), are fabricated on a FR4 substrate for the motherboard. The patch antennas shown in Fig. 5.13a have a gain of 7 dBi. Fig. 5.13b shows the triangular corner reflectors used as targets. Two plane reflectors are also used, for range resolution measurements which are smaller and can be placed close next to each other. The RCS for triangular corner and plane reflector are calculated as shown below [4].



(a) (b)

Figure 5.13: Radar measurements setup with corner reflectors.

$$RCS_{corner} = \frac{4\pi l_{side}^4}{3\lambda^2} = 18.3\,\text{dBsm} \;@\; 61.5\,\text{GHz}, \tag{5.3}$$

$$RCS_{plane} = \frac{4\pi A_{side}^2}{\lambda^2} = 18.8\,\text{dBsm} \;@\; 61.5\,\text{GHz}, \tag{5.4}$$

As mentioned before, the TX has a BPSK modulator to implement a low-IF architecture and translate the resulting beat frequency away from DC offsets and flicker noise. Fig. 5.14 shows the advantage of using a low-IF BPSK modulation in TX over direct down-conversion, providing 4 dB higher SNR measured at 60 cm.

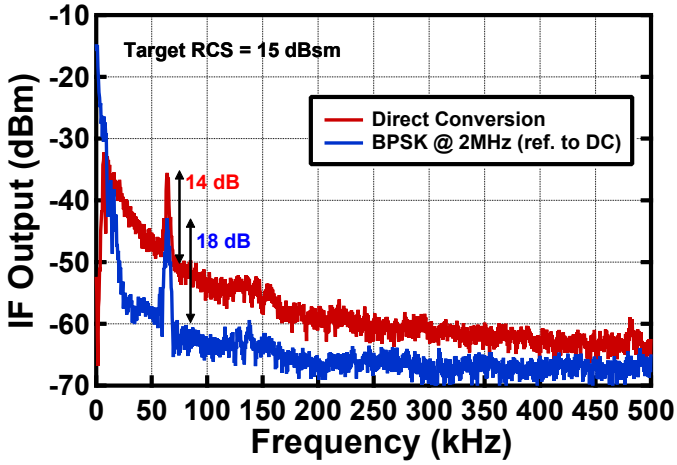


Figure 5.14: Direct down-conversion vs low-IF mode.

Range resolution is measured with a FMCW chirp of 8 GHz/500 μs and two plane reflectors with a RCS of 18.8 dBsm. Fig. 5.15 shows that the radar achieves a resolution frequency of 2 kHz equivalent to a range resolution of 1.9 cm, with a peak separation of 9.57 dB.

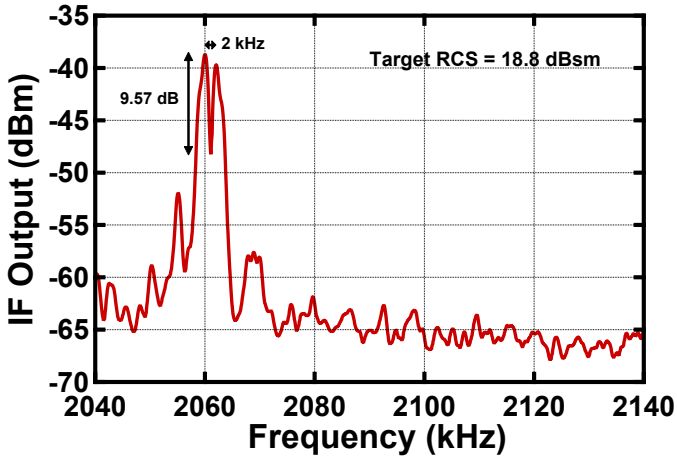


Figure 5.15: Range resolution using the low-IF mode.

5.3 Summary

This chapter presents two ultra low-power 60-GHz FMCW radar prototypes fabricated in GF 22-nm FDSOI. Additional measurements concerning the LO synthesizer are reported to complement the work published in [1, 5]. Both radar prove their range estimation capabilities

and, thanks to the fully integrated ADPLL in the second prototype, the frequency chirp could be better controlled to validate also the range resolution. Table 5.2 summarizes the results and compares the two presented works with state-of-the-art radars.

Table 5.2: Comparison with the state-of-the-art FMCW radar.

Reference	**This Work 1st Chip**	**This Work 2nd Chip**	TI ISSCC'21 [6]	IMEC TMTT'21 [7]	Infineon RFIC'20 [8]	IHP JSSC'17 [9]	Infineon JSSC'16 [10]
Technology	**22-nm FDSOI**	**22-nm FDSOI**	45-nm CMOS	28-nm CMOS	28-nm CMOS	130-nm SiGe	350-nm SiGe
Frequency (GHz)	**57-66**	**57-66**	57-64	57-66	57-64	58.5-63.5	57-64
RF BW (GHz)	**9**	**9**	7	7.2	7	5	7
TX/RX Channels	**2/2**	**4/4**	3/4	1/1	2/3	1/1	2/4
TX P_{out} (dBm)	**1**	**-1**	11.8	8.1	10	11.5	4
RX Gain (dB)	**6**	**27**	-	46	77	24	19
NF_{DSB} (dB)	**30**[c]	**18**[c]	12.5	10.5	12	9.8	9.5
RX IP_{1dB} (dBm)	**-18**[c]	**-6**[c]	-14	-	-12	-12	-8.5
PN@1 MHz (dBc/Hz)	**-73**	**-72**	-93	-92.9	-99.4	-100	-105
Total P_{DC} (mW)[a]	**68.5**	**101.1**	3100	62	478[d]	594[d]	990[d]
P_{DC}/channel (mW)[b]	**17.1**	**6.3**	258.3	62	79.67[d]	594[d]	123.75[d]
Area (mm^2)	**1.25**	**3.125**	-	4.13	7.45[d]	3.72[d]	20.25[d]
Area/channel (mm^2)[b]	**0.31**	**0.2**	-	4.13	1.24[d]	3.72[d]	2.53[d]
$P_{DC,SISO}$ (mW)	**44.2**	**40.2**	258.3[e]	62	335.67	594	123.75[e]

[a] Maximum power consumption. [b] MIMO channel is calculated by $N_{TX} \times N_{RX}$.

[c] Simulated. [d] Fully or partially off-chip PLL.

[e] Minimum estimated from P_{DC}/channel because no SISO information is reported.

The final prototype achieves a record low power consumption per virtual channel of only 6.3 mW. In the single-input-single-output (SISO) configuration, the power consumption is 40.2 mW, the lowest compared to similar works. Nevertheless, the low power consumption comes at the cost of reduced output power and NF, which consequently translate in a more limited maximum range than other radars reported in the state-of-the-art.

Each TX-RX slice occupies only 0.4 mm × 1.25 mm and the total chip area is 2.5 mm × 1.25 mm, due to the extensive use of transformers for coupling stages and direct frequency synthesis at 60 GHz. In conclusion, this work shows an ultra low-power 60-GHz FMCW radar for short-range applications with the lowest power consumption and smallest form factor reported today.

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6 Conclusion

6.1 Summary of Research Topics

The main objective of this research is the development of a low-cost low-power fully integrated FMCW radar operating in the 60-GHz band. The core of the work focuses particularly on the design of a TX and RX path tailored for short-range applications such as object detection motion sensing, gesture recognition, or vital signs monitoring. The power consumption reduction is the main target for the design optimization of the different mm-wave blocks because currently the market is driven by automotive industry where they can afford power consumption of several Watts, however there is a lack of ultra low-power solutions. Therefore, the research aims to pave the way for developing a battery-powered solution that could be more versatile and be used as portable or long-autonomy miniature sensors.

The FMCW radar provides several advantages for sensing such as baseband bandwidth compression and low peak output power. The first step in this work was to fully understand the operating principle of a FMCW radar and determine which specifications could be traded off to reduce the power consumption. Since the radar is meant to operate at short range then the link budget is relaxed allowing to reduce the output power and NF. Nevertheless, a less obvious parameter that is also relaxed is the phase noise thanks to the stronger noise correlation at short distance. The effect of the latter was confirmed in practice through experiments reported in chapter 2.

For the design of the TX and RX paths it was critical to optimize the passive devices such as transformers and efficiently use them to couple the signal across the multiple stages. Furthermore, the strategy to save power on the TX output stage was also to merge functionalities as the modulator and PA output stage. On the RX side, a mixer-first architecture was an interesting alternative to avoid burning power in a mm-wave LNA. Besides the power saved, the design choices taken for both TX and RX allowed to further reduce the dimension of the TX-RX slice by removing two potential transformers and bringing blocks closer together. The advantage of having a smaller form factor, apart from the cost, is to reduce the LO distribution power budget.

It is difficult to compare this work with industrial products because they are designed for high-performance while instead the radar presented here opts for a low-power alternative. As an attempt to see where our radar stands compared to industrial products, one of the most established radars in the market is taken as a reference: TI IWR6843. Both TI and our radar have similar channel configuration with 3TX/4RX and 4TX/4RX, respectively. In terms of output power and noise the TI radar is clearly superior. The surface of the analog part in the TI radar is estimated to 22 mm^2 from [1], this is 7 times larger than the 3.125 mm^2 of our chip. The cost per mm^2 in GF 22-nm FDSOI is 2× more expensive than in the TI's 45-nm CMOS [2], consequently making our chip 3.5× cheaper on the analog part. The advantage will be even further once the digital part is integrated. The range resolution is 2.25× better because our chip achieves a wider ramp bandwidth, and the power consumption is 30× lower. Although not conclusive, this comparison suggests that the radar presented here has the potential to be competitive in the market. Moreover, this thesis constitutes an important step towards a fully integrated low-power solution for short-range applications.

6.2 Main Achievements

As a product of the conducted research work, some interesting contributions are made in the field. The most important achievements are listed here:

- An analysis on the impact of phase noise in different low-IF radar architectures. Three FMCW radar architectures implementing a low-IF transceiver are studied: two PLLs at different frequencies, single-PLL with OOK, and single-PLL with BPSK modulations. The analysis helps to understand the phase noise correlation effect in radars. The calculations are validated by comparing simulations to measurements performed with a demonstrator. The results prove the advantage of using a single-PLL architecture due to the attenuation of correlated phase noise in the TX and RX paths [3]. It was experimentally proven an improvement of at least 30 dB on phase noise.

- The design of a low-power band-tuning 60-GHz TX. Several mm-wave design techniques and a matching network optimization have been used in order to achieve a good performance for low-power FMCW radars. The band-tuning matching network for each TX stage allows to benefit from a higher quality factor in a narrower band and synchronously sweep LO and TX bands to cover the entire 9 GHz band. Most of the works in literature and industry target applications that require higher output power, which makes this work one of the first optimized TX for such a low output power. The TX efficiency is comparable to other state-of-the-art FMCW TX in the 60 GHz band [4].

- An analysis of passive mixer-first RX architecture is conducted to evaluate its feasibility at mm-wave. Understanding the optimal mode of operation for the mixer was critical to achieve a good performance in terms of gain, NF, IP_{1dB}, and matching. Although the voltage-mode mixer is preferred in the context of this radar, it was found that

implementing a mixed-mode mixer with a noise-cancelling scheme could provide better performance when a larger impedance is available at the input of the mixer.

- An ultra low-power 60-GHz FMCW radar implemented in GF 22-nm FDSOI CMOS technology. The chip integrates the full mm-wave front-end presented in this thesis including an ADPLL first documented in [5, 6]. The fruitful collaboration of the mentioned works brings a record low power consumption for a mm-wave FMCW radar. The capabilities of the radar are demonstrated through experiments in chapter 5.

- This work is the first integrated mm-wave transceiver developed by the CSEM RF & Analog IC Design group. It helped to build the expertise within the team for future developments at such high frequencies.

6.3 Future Works

Besides the several achievements accomplished throughout this work there is still a long road to reach the final goal of having a complete solution for the market. Moreover, there are also few things that could have been done differently which are worth mentioning in order to make the necessary improvements for the future prototypes. A list of the possible directions to continue the development of the project is described here:

- One of the main points regarding the RX is the integration of the rest of the analog baseband, which for the moment is partially off-chip. Further amplification and anti-aliasing filtering stages are necessary to condition the beat frequency to be acquired by a following ADC. Although these blocks are designed for baseband and most likely they would consume much less power than the mm-wave blocks, it is important to pay attention to the power consumption because there are 4 RX paths each one with I and Q channels, resulting in a total of 8 baseband channels.

- Following the ADC, once in the digital domain there is signal conditioning and processing to be implemented before transmitting the signal off-chip. Some of the operations suggested according to [7] are divided in these two categories:

  - Signal conditioning: IF demodulation, down-sampling, I&Q imbalance compensation, gating, windowing, and filtering.
  - Signal processing: CFAR detection, FFT, TF transform, and integration processing.

  Not all of these operations need to be implemented, however there are few of them that are strongly recommended. For instance, down-sampling will be most likely a must to be able to lower the required data rate to output the signal off-chip. Other important operations are windowing and filtering to suppress spectral leakage and improve the SNR, respectively. Another useful feature to have is a FFT to estimate the beat frequency (and range) on-chip.

- The design of passive devices as inductors, transformers and transmission lines (TL) should be routed with thick or ultra-thick metals. In this work it was decided to use the two thickest metals to route the supplies and grounds. Even though the DCO inductor and TX/RX transformers are designed with ultra-thick metal, the TLs are routed only in the third thickest metal. The performance of passive devices should have been prioritized over supply routing because otherwise the TLs become very lossy, specially for the LO distribution at 60 GHz.

- The radar should be designed to be mounted as a flip-chip and avoid using long bond-wires. Instead, using bumps shortens the interconnection reducing the parasitic inductance and resistance associated to the interface of the die to the board or package. This decision should be taken in the beginning of the design phase to provide the designer of the TX and RX a S-parameter file with the specific load characteristics.

- The addition of a test buffer to output the divided-by-48 LO signal in the second prototype was of great help during characterization but it would be useful to include more circuits to facilitate the measurements and debugging of the chip. For instance, RF detectors should be integrated in intermediate nodes such as the LO buffers to be able to monitor the amplitude of the LO distribution and possibly implement calibration. In general, the suggestion is to design the next prototypes following a built-in-self-test (BIST) approach.

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A Stability Considerations

This appendix summarizes the stability parameters to take into account for the design of two-port circuits such as power amplifiers (PA) or low-noise amplifiers (LNA). The fact that transistors are not unilateral means that under certain conditions they can both reverse and forward transmission from one port to the other. For instance, in the context of cellular circuits the output of the transmitter PA is connected to an antenna that, depending on what is in the close vicinity to the mobile phone, could vary its impedance thus potentially driving the PA into an oscillating mode.

A parameter known as the Rollet stability factor is used to characterize a two-port circuit, it is given by

$$\mathrm{Kf} = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2\,|S_{12}||S_{21}|}, \tag{A.1}$$

where Δ is known as the determinant and defined as

$$\Delta = S_{11}S_{22} - S_{12}S_{21}. \tag{A.2}$$

A two-port circuit is unconditionally stable, meaning for any combination of input and output impedance, if $\mathrm{Kf} > 1$ and $\Delta < 1$. In addition, Cadence offers an alternative stability factor b1f which is defined as

$$\mathrm{b1f} = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2. \tag{A.3}$$

The circuit is said to be stable when $\mathrm{b1f} > 0$.

List of Publications

Conference Papers

- S. Cerida Rengifo, F. Chicco, E. Le Roux, and C. Enz. “Modulation Scheme Impact on Phase Noise in FMCW Radar for Short-Range Applications”. In: 2021 IEEE International Symposium on Circuits and Systems (ISCAS). 2021 IEEE International Symposiumon Circuits and Systems (ISCAS). ISSN: 2158-1525.May 2021, pp. 1–4.
- S. Cerida Rengifo, F. Chicco, E. Le Roux, and C. Enz. “An Optimized Low-Power Band-Tuning TX for Short-Range FMCW Radar in 22-nm FDSOI CMOS”. In: ESSCIRC 2021 - IEEE 47th European Solid State Circuits Conference (ESSCIRC). ESSCIRC 2021 - IEEE 47th European Solid State Circuits Conference (ESSCIRC). Sept. 2021, pp. 1–4.
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Journal Papers

- S. Cerida Rengifo, F. Chicco, E. Le Roux, and C. Enz. “An Ultra-Low Power Short-Range 60-GHz FMCW Radar in 22-nm FDSOI CMOS”. In: IEEE Transactions on Microwave Theory and Techniques (Accepted on May 23rd, 2023).
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My primary research interest is the design of RF/mm-wave front-end transceivers. In recent years, my research focus has been on low-power RF circuits (PA, LNA, Mixer) operating in the 60-GHz band in deep sub-micron CMOS technologies. My work included as well co-design with other critical blocks as oscillators and dividers, performing exhaustive electromagnetic simulations, PCB design, and on-chip probing measurements.

Work Experience

Current – Apr 2023 | **Senior Design Engineer at STMicroelectronics**
MDG | General Purpose Microcontroller Sub-Group | RF-Analog IC Design.

Mar 2023 – Jan 2018 | **PhD Student at Centre Suisse d'Électronique et de Microtechnique (CSEM) and École Polytechnique Fédérale de Lausanne (EPFL)**
Design of a Low-Power Front-End Transceiver for a 60-GHz Frequency-Modulated Continuous-Wave (FMCW) RADAR in 22nm FDSOI technology.
Thesis Director: Christian Enz (EPFL)
Supervisors: Erwan Le Roux and Franz Pengg (CSEM)

Mar-Sep 2017 | **Master Thesis Intern at EM Microelectronic**
Architecture investigations and analysis of Next-Generation UHF RFID Analog Front-End. Study on different rectifier architectures, build testbenches to investigate their performance and optimize them. Finalize implementation of the most suitable solution, design layout and tapeout.
Supervisors: Paul Muller, Goran Stojanovic and Thomas Coulot

Jul-Sep 2016 | **Intern at Integrated Circuits Laboratory (ICLAB) EPFL**
Research in thermal noise analysis, specifically in OTA-based switched-capacitor (SC) circuits. Study and development of a new method for simple thermal noise estimation of OTA-based SC circuits. Validation of the estimation method using ELDO Transient Noise simulations performed in analog blocks as filters, integrators, amplifiers, and track-&-hold circuits.
Supervisors: Assim Boukhayma and Christian Enz

Sep 2015 – Sep 2014 | **Research Assistant at Pontifical Catholic University of Peru**
Microelectronics Laboratory
Lead and advise student projects based on FPGA platforms and electronic design. Software and license administrator at the laboratory. Organize workshops, short courses and seminars.

Sep 2015 – Mar 2013 | **Teaching Assistant at Pontifical Catholic University of Peru**
Lecture the course *Digital Circuits Laboratory*. Assist the courses: *Basic Electronics, Analog Circuits, Electronic Design I* and *Microelectronics*.

Jan-Mar 2014 | **Researcher at Jicamarca Radio Observatory (JRO), Peru**
Development of a Gigabit Ethernet controller for the JRO Acquisition Radar System (JARS) project based on a Spartan 6 FPGA platform.

Education

Sep 2017 Sep 2015	Student of the Master's Degree in Micro and Nanotechnologies for Integrated Systems **Politecnico di Torino, Grenoble INP, and École Polytechnique Fédérale de Lausanne (EFPL)** *Recipient of ERASMUS and EXPLORA scholarships.*
Dec 2013 Mar 2008	Bachelor in Electrical Engineering, **Pontifical Catholic University of Peru** *First Class Honours* Thesis: "Design of a Low-noise Low-power Neural Amplifier" | Supervisor: Manuel Monge
Aug 2012 Dec 2012	Exchange Semester at **University of Alberta**, Edmonton, Canada *Recipient of the Emerging Leader in the Americas Program (ELAP) scholarship.*

Workshops and Certificates

July 2019	IC Mask Design Very Deep Submicron Layout. **CSEM, Neuchâtel.**
Feb 2017	NSCAD Microelectronics Introduction to RFIC design. **Pontifical Catholic University of Peru.**
Mar 2014	SYNOPSYS Analog Design Workshop. **Pontifical Catholic University of Peru.**
Jul 2012	Escuela Argentina de Micro-Nanoelectrónica, Tecnología y Aplicaciones (EAMTA) Full-custom Digital Design Workshop. **National University of Cordoba, Argentina.**

Languages

Spanish: Mother Tongue
English: Advanced Proficiency
French: Intermediate Proficiency

Technical Skills

Cadence Design Tools:

Full-custom design flow, experience working with Advanced Nodes as TSMC28nm and GF22nm

- Virtuoso Schematic and Layout Design
- Spectre, Spectre RF, and APS simulation environment
- Aging and reliability simulations using Spectre-native and RelXpert methods.
- Calibre DRC, LVS and PEX

Electromagnetic Simulation:

- EMX
- Keysight Momentum/RFPro
- Helic

FPGA:

- ISE Xilinx and Altera Quartus

PCB Design:

- Altium Designer

Measurement Instruments:

- Vector Network Analyzer
- Spectrum Analyzer
- Signal Source Analyzer
- Power Meters

Interests and Activities

- Shotokan Karate (1st Dan, black belt).
- Soccer, Hiking.