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# Dc-Link Ripple Suppression of Cascaded H-Bridge Based MV Grid Emulator Apparatus for Analysis and Testing of Grid-Tied Converters in Distribution System

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***Abstract*—The medium-voltage grid emulator is gaining popularity for testing grid-code compliance of large-capacity converters for renewable energy resources. The cascaded H-bridge converter based on active-front-ends is a promising candidate for high-power grid emulators owing to its high modularity and extendibility. However, the cascaded H-bridge topology-based grid emulator suffers the undesired and unpredictable large dc-link voltage ripple under output voltages with multiple-frequency components, e.g., when emulating the grid voltage flickers and harmonics. In this paper, the dc-link voltage ripple characteristics under multi-frequency output conditions are analyzed and a dc-link ripple suppression method adopting harmonic current injection is proposed. The injected current reference is generated by reconstructing the dc-link output current and added to the original active-front-end current control loop. Compared with the existing control methods, e.g., proportional-integral-resonant (PIR), the proposed method has a good voltage ripple suppression effect, especially for multi-frequency outputs. Furthermore, the proposed idea does not need complicated calculation or extra control loops and provides a feedforward reference for the current control, leading to a good dynamic response of dc-link voltage control. Finally, the performance of this suppression control scheme is verified on two 1200V@40kW power electronics building blocks of a cascaded H-bridge converter.**

***Index Terms*—grid emulator, cascaded H-bridge converter, active front end, multi-frequency output, voltage ripple suppression, harmonic current injection**

## I. Introduction

THE renewable energy resources are highly desirable and rushing into the power system as they can reduce carbon emissions from the power source effectively [1]. Electric power networks are experiencing significant changes as a result of the widespread adoption of power electronics-based apparatuses. And yet the power electronics-based grid-connected converters and grid-forming converters lack mechanical-electrical inertia in the modern power grid, which necessitates extra measures to assure power grid stability. Therefore, the behavior of these grid-connected converters must be investigated before putting into real transmission and distribution grid [2]. And building an artificial grid based on power electronics converters is a prevalent approach for the safe and flexible pre-testing [3].

The cascaded H-bridge (CHB) multilevel converters have become one of the most promising candidates for medium-voltage (MV) applications, particularly in MV motor drives and MV power grid emulators [4]–[6]. The topology has a good modularity, extendibility and power quality for different voltage and power levels. The popular CHB converters are commonly based on the diode-front-end (DFE) and inherit the shortcoming of the uncontrollable diodes, which lack the ability to handle regenerating power from load to the grid. When the power converters operate in a regeneration mode, the energy will rush into the dc-link capacitors and may result in over-voltage [7], [8]. To solve this problem, the active-front-end (AFE) using the controllable insulated gate bipolar transistor (IGBT) has been proposed to replace the DFE in each cell. The AFE-based CHB converter has sufficient control degrees of freedom and can realize four-quadrant operation, attracting a lot of research interests and widespread applications in recent years [9], [10].

However, one of the critical problems of AFE-based CHB converters is the much bigger dc-link energy storage requirement. Due to the single-phase output in each cell, the double output frequency ripple current flows into the dc capacitors instead of the AFE. Then massive and costly electrolytic capacitors are usually installed in parallel to absorb the pulsating power, which can take up about half of the cell volume in 50Hz/60Hz output applications [11], [12]. Furthermore, the double output frequency ripple is significantly increased under very low-frequency output operation, which accelerates the aging of capacitors and consequently limits the tolerable operation frequency range [13].

To address this issue, a variety of control algorithms have been proposed in [11]–[17]. Even though their specific realizing methods are different, the essential idea is the same, which is: to control the AFE unit to produce equal power to balance the required pulsating power from the single-phase output unit. In the single-phase AFE topology, an additional circuit is usually adopted to transfer the ripple power to other energy storage elements [18]–[20]. Fortunately, the three-phase AFE has enough control flexibility to adjust both active power and ripple power. The idea of instantaneous power generated from AFE and transferred directly to output was initially proposed in [21]. An extra current reference is added to the d-axis current controller of the AFE rectifier. The reference is actively calculated according to the single-phase output voltage and current without any additional sensors. The original proportional-integral (PI)

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regulator is kept to control both active power current and extra injected current. Then [15] pointed out that the limited bandwidth of PI controller cannot achieve a good performance due to the oscillatory ac current reference in $d-q$ rotating frame. Hence a model predictive control is employed to obtain a decoupled and quick tracking. Similarly, [14] proposed a proportional-integral-resonant (PIR) controller for both the outer voltage control loop and the inner current control loop. Only the information about the H-bridge inverter frequency is needed for the AFE control. In this way, the active power current reference and pulsating current reference are generated from the voltage control loop. However, the resonant regulator in the outer voltage control loop might introduce instability in some operating range [12].

In the above-mentioned control schemes, because of the ac reference in the d-axis, the AFE rectifier will introduce two frequency components. One frequency is $\omega_g + 2\omega_o$, and another one is $|\omega_g - 2\omega_o|$, where $\omega_g$ is the fundamental grid frequency and $\omega_o$ is the H-bridge output frequency. In [22], the influences of the injected current were accurately characterized. The injected current will distort the three-phase AFE input current but keep the grid current symmetrically sinusoidal owing to the zigzag phase shifting transformer. Besides, the current compensation increases the modulation index and current stress, which would lead to over-modulation and power derating. Therefore, to avoid the drawback of undesired modulation index increase, paper [11] chooses to only inject the low-frequency current into the AFE rectifier directly in the $abc$ frame, with a lower voltage drop across the filtering inductor. However, the injected current reference of this scheme is obtained from the current and power angle of the motor, which is rarely available in a typical induction motor control system. Moreover, the feedforward calculation is still an open-loop control, which requires many accurate circuit parameters [13], [17].

As a solution to this drawback of feedforward calculation, an extra voltage control loop is established for frequency-adaptive ripple suppression based on the dc-link voltage measurement directly [12], [16]. A resonant controller with lead-compensated phase compensation is required to be tuned to gain enough stability margin. Due to the frequency variation of the load side, it is difficult to accurately detect the amplitude and phase angle of the dc voltage ripple in real time.

Up to now, there does not exist related research on the dc-link voltage ripple suppression of CHB with multi-frequency output. For instance, it is an essential requirement that the medium-voltage power grid emulator based on CHB topology should have the ability to generate the fundamental frequency waveform with different frequency harmonics [23], [24]. It is of great significance for testing other high-power converters before putting them into operation [25], [26]. With different harmonic outputs, the dc link capacitors are required to provide pulsating power at many frequencies. Especially when simulating the subsynchronous oscillation of the power grid [27], [28], the output voltage/current consists of 50/60 Hz and lower frequency components ranging from 4 Hz to 40 Hz, which causes severe voltage fluctuation on the dc-link capacitor [29]–[31]. However, although some adaptive filters can detect variable frequency output, it is quite challenging to extract the information from the multiple-frequency waveform on-line and very difficult to design many controllers to suppress dc-link ripples at different frequencies.

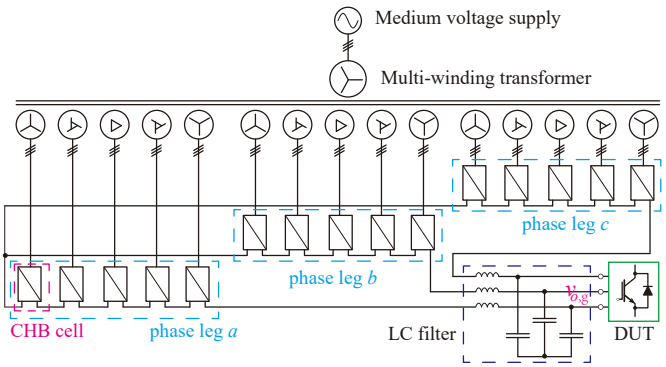


Fig. 1. Cascaded H-bridge converter topology-based medium voltage grid emulator.

In this paper, the dc-link voltage ripple characteristics of CHB-based grid emulator are analyzed with multi-harmonics output voltage and current, and the complex composition of dc-link ripples is revealed. Then, this paper proposes a novel harmonic current injection method to suppress the dc-link voltage ripples, using only very few parameters to accurately calculate the injected current reference. No extra measurements, filters or controllers are required in this method. And the reference calculation and controller do not need to know the amplitude and frequency information of the ripple. Compared with the existing method, this proposed idea has a wide applicability. Apart from the occasion of single frequency output, the complex situation of variable frequency output and fundamental output with different frequency harmonics can also employ the proposed suppression control. Besides, the proposed current injection method does not influence the grid current, which is very friendly to the MV grid.

The rest parts are organized as follows. Section II reveals the relationship between the dc-link voltage ripple and the multiple-frequency output, and some cases are studied to clarify the voltage ripple characteristics under multi-frequency output conditions. The details of the proposed control strategy to tackle this problem are investigated in Section III. Then some simulation and experiment results are illustrated to prove the suppression effectiveness in Section IV. Finally, the conclusion is made in Section V.

## II. DC-Link Voltage Ripple Characteristics Under Multi-Frequency Output Conditions

A typical topology of the cascaded H-bridge multilevel converter-based MV grid emulator is shown in Fig. 1. There are three phase legs and each leg contains a series of three-phase input and one-phase output cells whose inputs are connected to a multi-winding transformer. The cell number is configured according to the required voltage class. The cascaded connection of cells increases apparent switching frequency seen at the output. The LC filter is needed for the grid emulator to obtain small high-order harmonics. Each cell, as shown in Fig. 2, is composed of a three-phase DFE or AFE rectifier, a series of dc-link capacitors, and an H-bridge inverter. In grid emulator applications, the AFEs must be configured to achieve bidirectional power flow. It is indifferent whether the multi-winding transformer has a phase shift angle among secondary windings or not as AFE current is controllable.

The AFE-based CHB attracts more research interests owing to its bidirectional power flow ability. The basic control diagram of

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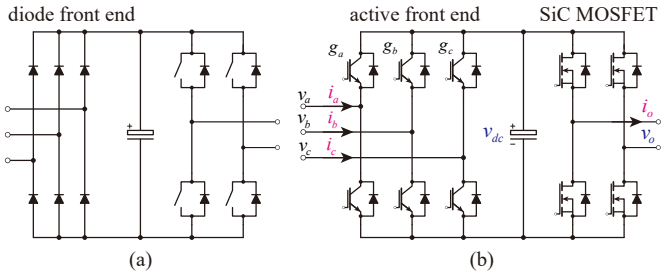


Fig. 2. Diode-front-end converter and active-front-end converter for MV CHB cell.

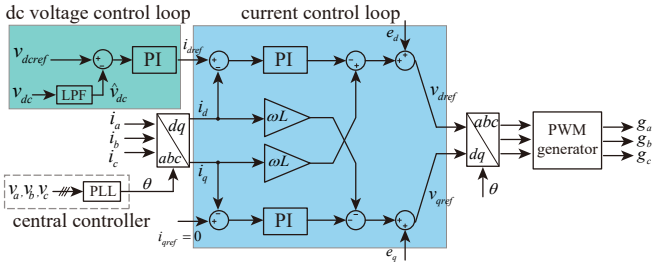


Fig. 3. Basic control diagram of single AFE cell.

each AFE cell is presented in Fig. 3, generally including an outer dc voltage control loop and an inner AFE current control loop. A low pass filter (LPF) or notch filter is usually added to eliminate the influence of dc-link double output frequency ripple. In some applications, extra input filters are required for AFE operation. However, these AFE filters take a significant share of AFE cell's volume, weight, cost, and cooling effort. Therefore, to avoid the bulky and costly input filters, the leakage inductance of the MV transformer is used as AFE cell input filter, only MV input voltage can be measured for phase-locked loop (PLL), which is done by the central controller. The secondary windings' phase angles are calculated according to the phase-shifting angle between primary and secondary and given to all local controllers directly [32]. The PI regulators are adopted to compensate for the two control loops. The H-bridge inverter can be simply modulated according to the modulation wave given from the central controller.

When the CHB-based grid emulator operates with multiple frequency output, the ripple power/voltage analysis methods are similar to the single frequency output but with more complicated results. Supposing that the H-bridge output voltage $v_o$ and current $i_o$ have two different frequency components, defined as

$$\begin{cases} v_o = V_1 \sin(\omega_1 t + \varphi_1) + V_2 \sin(\omega_2 t + \varphi_2) \\ i_o = I_1 \sin(\omega_1 t + \varphi_3) + I_2 \sin(\omega_2 t + \varphi_4) \end{cases} \tag{1}$$

where $\omega_1$ and $\omega_2$ are the two output angular frequencies. $V_1$, $V_2$, $I_1$, $I_2$ and $\varphi_1$, $\varphi_2$, $\varphi_3$, $\varphi_4$ are the voltage/current amplitude and phase angle of each frequency output, respectively.

Hence, the instantaneous output power provided by the H-bridge can be calculated in (2).

From (2), the dc items represent the average active power $P_o$ from dc capacitors, which can also be considered as transferred from the AFE rectifier. There are ac items with four frequencies, which are $2\omega_1$, $2\omega_2$, $\omega_1+\omega_2$ and $|\omega_1-\omega_2|$, respectively. Here, $\omega_2$ could be larger than $\omega_1$, so the sign $||$ indicates the absolute value

TABLE I: Study Cases: 50 Hz with added 10 Hz/40 Hz/150 Hz output

| Parameters | Case I | Case II | Case III |
|---|---|---|---|
| $U_{dc}$ | | 1200 V | |
| $C$ | | 1 mF | |
| $\omega_1/\omega_2$ | 50 Hz/10 Hz | 50 Hz/40 Hz | 50 Hz/150 Hz |
| $V_1/V_2$ | | $0.8U_{dc}/0.2U_{dc}$ | |
| $I_1/I_2$ | | 75 A/18.75 A | |
| $\varphi_1/\varphi_2/\varphi_3/\varphi_4$ | | 0/0/0/0 | |
| $P_o$ | | 38.25 kW | |
| $p_{2\omega_1}$ | | 36 kVAR @ 100 Hz | |
| $p_{2\omega_2}$ | 2.25 kVAR @ 20 Hz | 2.25 kVAR @ 80 Hz | 2.25 kVAR @ 300 Hz |
| $p_{\omega_1+\omega_2}$ | 18 kVAR @ 60 Hz | 18 kVAR @ 90 Hz | 18 kVAR @ 200 Hz |
| $p_{\omega_1-\omega_2}$ | 18 kVAR @ 40 Hz | 18 kVAR @ 10 Hz | 18 kVAR @ 100 Hz |
| $\Delta u_{2\omega_1}$ | 47 V @ 100 Hz | 47 V @ 100 Hz | 23 V @ 100 Hz |
| $\Delta u_{2\omega_2}$ | 16 V @ 20 Hz | 9 V @ 80 Hz | 1 V @ 300 Hz |
| $\Delta u_{\omega_1+\omega_2}$ | 39 V @ 60 Hz | 28 V @ 90 Hz | 11 V @ 200 Hz |
| $\Delta u_{\omega_1-\omega_2}$ | 60 V @ 40 Hz | 242 V @ 10 Hz | 23 V @ 100 Hz |

of $\omega_1 - \omega_2$. Even assuming that only one of the output voltage $v_o$ or $i_o$ has harmonic output, such as $V_2 = 0$ or $I_2 = 0$, there are still three different frequency ac items. The ac items stand for the reactive power $p_{ac}$, generally absorbed by the dc capacitors. Each pulsating power of each frequency will raise the dc voltage fluctuation of the corresponding frequency, as expressed in (3), where $C$ is the dc-link capacitance and $U_{dc}$ is the average dc voltage.

According to (2) and (3), sufficiently big capacitors are required to suppress the dc-link voltage ripple caused by the four frequency pulsating power, especially when CHB converter outputs very low frequency components. For example, when the CHB converter simulates the subsynchronous oscillation of the power grid, a waveform with fundamental 50/60 Hz and very low frequency such as 10 Hz should be generated. Then, the voltage ripple caused by 10 Hz output is significant. Besides, with the item $|\omega_1-\omega_2|$, even if the two frequencies are high, the dc voltage ripple could also be very high with two close frequencies. For example, if H-bridge output contains 50 Hz and 60 Hz, the voltage ripple has a large 10 Hz component.

To show the ripple characteristics clearly, several sets of specific parameters are brought into (1)-(3) for calculating the voltage ripple of different frequencies. One case is 50 Hz plus 10 Hz output, one is 50 Hz plus 40 Hz output and another is 50 Hz plus 150 Hz output. The output voltage/current expressions are written in (4)-(6). The calculation result is given in Table I and Fig. 4.

$$\begin{cases} v_o = 960V \sin(2\pi \cdot 50t) + 240V \sin(2\pi \cdot 10t) \\ i_o = 75A \sin(2\pi \cdot 50t) + 18.75A \sin(2\pi \cdot 10t) \end{cases} \tag{4}$$

$$\begin{cases} v_o = 960V \sin(2\pi \cdot 50t) + 240V \sin(2\pi \cdot 40t) \\ i_o = 75A \sin(2\pi \cdot 50t) + 18.75A \sin(2\pi \cdot 40t) \end{cases} \tag{5}$$

$$\begin{cases} v_o = 960V \sin(2\pi \cdot 50t) + 240V \sin(2\pi \cdot 150t) \\ i_o = 75A \sin(2\pi \cdot 50t) + 18.75A \sin(2\pi \cdot 150t) \end{cases} \tag{6}$$

As can be seen in Fig. 4(a), when there exists 10 Hz harmonic with small amplitude in the fundamental 50 Hz output, the main frequencies of the ripple are 40 Hz and 60 Hz and 100 Hz, which

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$$
\begin{aligned}
p_o = v_o i_o = \frac{1}{2}\Big\{ & \underbrace{V_1 I_1 \cos(\varphi_1 - \varphi_3) + V_2 I_2 \cos(\varphi_2 - \varphi_4)}_{\text{active power } P_o} - \\
& \underbrace{V_1 I_1 \cos(2\omega_1 t + \varphi_1 + \varphi_3)}_{\text{ripple power } p_{2\omega_1}} - \underbrace{V_2 I_2 \cos(2\omega_2 t + \varphi_2 + \varphi_4)}_{\text{ripple power } p_{2\omega_2}} - \\
& \underbrace{V_1 I_2 \cos[(\omega_1 + \omega_2) t + \varphi_1 + \varphi_4] - V_2 I_1 \cos[(\omega_1 + \omega_2) t + \varphi_2 + \varphi_3]}_{\text{ripple power } p_{\omega_1+\omega_2}} + \\
& \underbrace{V_1 I_2 \cos[(\omega_1 - \omega_2) t + \varphi_1 - \varphi_4] + V_2 I_1 \cos[(\omega_1 - \omega_2) t + \varphi_2 - \varphi_3]}_{\text{ripple power } p_{\omega_1-\omega_2}}\Big\} \\
= P_o + p_{ac} = P_o + p_{2\omega_1} + p_{2\omega_2} + p_{\omega_1+\omega_2} + p_{\omega_1-\omega_2}
\end{aligned} \tag{2}
$$

$$
\Delta u_{dc} = \frac{1}{C U_{dc}} \left( \frac{p_{2\omega_1}}{2\omega_1} + \frac{p_{2\omega_2}}{2\omega_2} + \frac{p_{\omega_1+\omega_2}}{\omega_1 + \omega_2} + \frac{p_{\omega_1-\omega_2}}{|\omega_1 - \omega_2|} \right) \tag{3}
$$

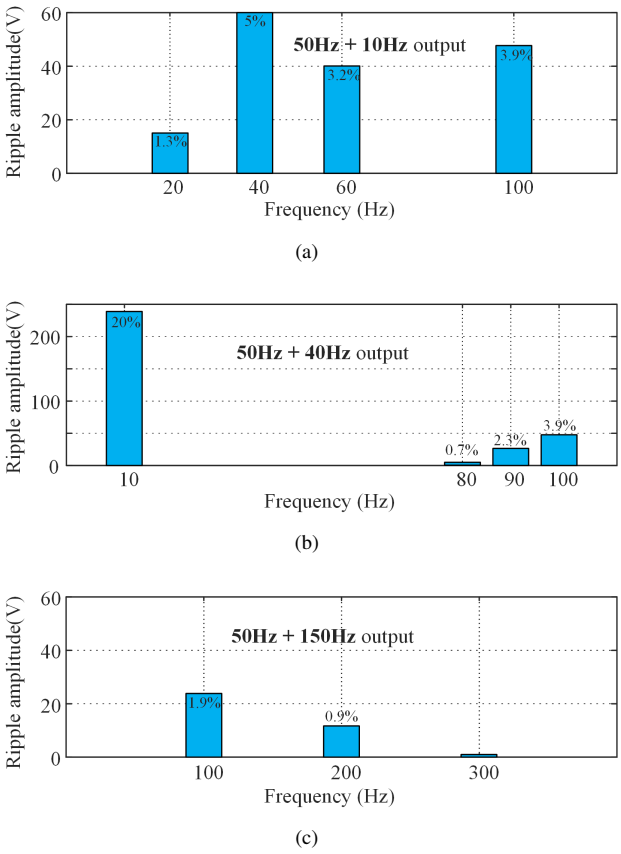


Fig. 4. Dc-link voltage ripple calculation under different frequency output. (a) 50 Hz + 10 Hz output. (b) 50 Hz + 40 Hz output. (c) 50 Hz + 150 Hz output.

are corresponding to $\omega_1 \pm \omega_2$ and $2\omega_1$. In contrast, when the output are composed of a big 50 Hz component and a small 40 Hz component, there will exist a large ripple component at 10 Hz (corresponding to $\omega_1 - \omega_2$), whose amplitude is almost 5 times of 100 Hz, as shown in Fig. 4(b). Thus, even though the output voltage or current does not contain low-frequency part, a considerable low-frequency ripple could be introduced. In Fig. 4(c), when the H-bridge outputs 50 Hz and 150 Hz, there are ripples with only three frequencies. Because the components at $2\omega_1$ and $\omega_1 - \omega_2$ (100 Hz) overlap with opposite phase, the ripple amplitude at 100 Hz is smaller than the former two cases. It is also possible that two ripple components at different frequencies overlap with same phase, so the ripple will be augmented under these circumstances. In such a situation, if a traditional current injection method based on fundamental-frequency output power is employed to suppress the voltage ripple, an over-compensation or under-compensation could happen. Further, the ripple at high frequency is relatively low, so the following analysis will focus on the low-frequency output conditions.

## III. Proposed Dc-Link Voltage Ripple Suppression Method

In the occasions with multi-harmonics output voltage and current, the existing methods are not suitable to be implemented to suppress the dc-link voltage ripples with such many different frequency components. Firstly, it is hard to extract the amplitude and phase angle of each frequency ripple. Secondly, the feedforward calculation of the injected current reference for each frequency is not an easy task. And thirdly, it is impractical to design resonant or other kinds of controllers for each frequency of injected current. Therefore, this section will propose a widely applicable harmonic current injection method to suppress the dc-link voltage ripples. The new control frame with a novel current injecting block is explained. The control parameter tuning principle and the influence of injected current will be also generally analyzed.

### A. Proposed Control Structure

The basic idea of the proposed control scheme is to let the AFE unit provide both average power and instantaneous power for the H-bridge output so that the pulsating power will not flow through the dc capacitors. Only the pre-existing measurements and parameters from the controller are used to calculate to injected current reference. The complete control block diagram of this method is presented in Fig. 5. The outer voltage control loop is kept but without the low pass filter or double output frequency notch filter, since the dc-link has multiple frequency

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ripple components. Without any filters in dc-link voltage control loop, the response speed of voltage control can be faster than the classical control shown in Fig. 3.

The injected current reference calculation is shown in the yellow rectangle of Fig. 5. The H-bridge output current $i_o$ is usually measured by one local controller or the central controller. $g_o$ is the switching function of the H-bridge defined in (7) or the modulation wave function of the H-bridge, which can be easily obtained without any error. In this way, the current from the dc-link capacitors $i_{dc}$ can be reconstructed according to $g_o$ and $i_o$. Then LPF is employed to get rid of the switching frequency components of the H-bridge unit. If $g_o$ is the continuous modulation wave instead of discontinuous switching signal, the LPF is no longer required. The feedforward unit only contains measurements and basic calculations, so the open-loop feedforward has no conflict with the existing current control loop and voltage control loop. By multiplying dc voltage $v_{dc}$, the instantaneous power consisting of both average active power and pulsating power can be calculated, which should be completely provided by the three phase AFE unit. Assuming that the converter is loss-free and the voltage drop on the AFE filtering inductor is small, the instantaneous output power should be totally supplied by the AFE unit. Therefore,

$$g_o = \begin{cases} 1, & \text{if switch } \mathrm{S_1} \text{ and } \mathrm{S_4} \text{ are turned ON} \\ -1, & \text{if switch } \mathrm{S_2} \text{ and } \mathrm{S_3} \text{ are turned ON} \\ 0, & \text{other switching states of H-bridge} \end{cases} \tag{7}$$

$$p_{dc} = LPF\left(g_o i_o\right) v_{dc} = \frac{3}{2}\hat{v}_{ac} i_d \tag{8}$$

where $S_1$-$S_4$ are the H-Bridge switches indicated in Fig. 5, the LPF means a low pass filter is applied to the element in brackets, $\hat{v}_{ac}$ is the phase voltage amplitude and $i_d$ is the $d$-axis current in the $d-q$ frame.

Finally, the injected current reference in the $d$-axis is obtained, which is

$$i_{dref2} = \frac{2}{3}\frac{p_{dc}}{\hat{v}_{ac}} = \frac{2}{3}\frac{LPF\left(g_o i_o\right) v_{dc}}{\hat{v}_{ac}} \tag{9}$$

In light of the similar expression between $g_o$ and $v_o$ in (1), the injected current reference in the $dq$ frame has the same frequencies of components as the output power in (2), which are dc item, items at frequency $2\omega_1$, $2\omega_2$, $\omega_1+\omega_2$ and $|\omega_1-\omega_2|$. After the proportional-integral regulator and $dq$-$abc$ transformation, the injected harmonic current contains four pairs of positive-sequence and negative-sequence components at frequency $2\omega_1 \pm \omega_g$, $2\omega_2 \pm \omega_g$, $\omega_1+\omega_2 \pm \omega_g$ and $\omega_1-\omega_2 \pm \omega_g$ in $abc$ frame, as deduced in (10)–(11). In (10)–(11), $m_{dq}$ is the modulation signal [$v_{dref}$, $v_{qref}$] in $dq$ frame, $m_a$, $m_b$, and $m_c$ are the modulation signals after $dq$ to $abc$ transformation in the $abc$ frame. It can be easily proved that the injected currents multiplied by the AFE three-phase voltage can generate the desired pulsating power of the single-phase H-bridge. As a result, the dc-link capacitors are not required to give the fluctuating power and the voltage ripple can be reduced significantly.

$$m_{dq} = \begin{bmatrix} v_{\mathrm{dref}} \\ v_{\mathrm{qref}} \\ 0 \end{bmatrix} = \begin{bmatrix} m\sin\theta_o \\ 0 \\ 0 \end{bmatrix} \tag{10}$$

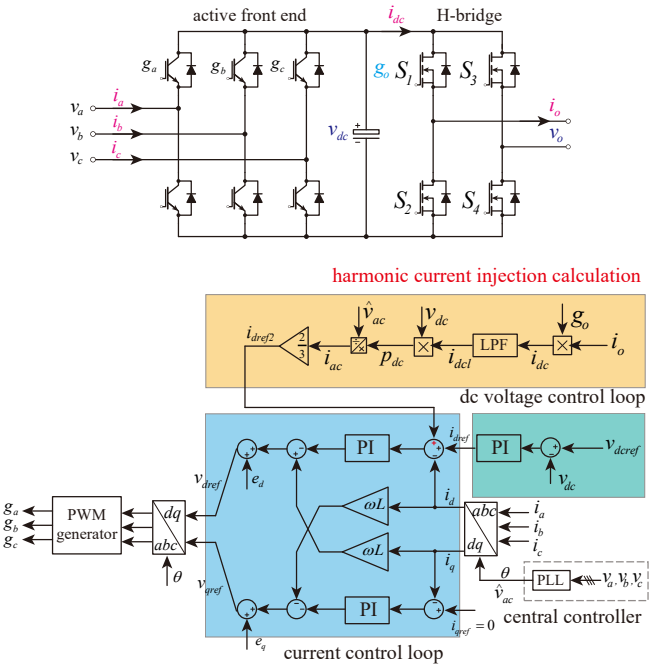


Fig. 5. Control block diagram of CHB cell with proposed dc-link voltage ripple suppression control.

In (9), there are four variable parameters in total. $\hat{v}_{ac}$ is the AFE input phase voltage amplitude, which is normally constant and defined by the grid voltage and transformer. H-bridge output current $i_o$ and dc-link voltage $v_{dc}$ can be directly measured in real time. The switching function $g_o$ can also be obtained from the central controller and no calculation is required. The low pass filter only filters out the switching frequency ripple, which has little influence on the close loop bandwidth. In a word, the proposed current injection calculation method is quick and accurate. Besides, this method is also applicable to any type of H-bridge output, including single-frequency output and fundamental frequency output with multiple harmonics.

### *B. Discussion on Controller Design*

Since the added current reference has a series of different frequency components and these frequencies may change with time, it is very challenging to design many adapting resonant controllers for each frequency. Hence, the classic PI regulator is used to compensate for the current loop gain and phase margin.

Ideally, the current control loop should be selected with as much bandwidth as possible to achieve a good tracking of the current reference that contains many different ac items. In practice, the controller bandwidth is limited by the switching frequency and control period. Particularly in the high power medium voltage application, high-voltage but low-switching-frequency power modules are usually employed. For example, the preferred switching frequency of 1700 V/150 A IGBT module is lower than 5 kHz, usually 1–3 kHz [33]. Given 3 kHz switching frequency, the designed current loop bandwidth can reach up to 300 Hz. The Bode plot of the open-loop transfer function with the parameters given in Table II of AFE current loop is shown in Fig. 6(a). The crossover frequency is 300 Hz with 76° phase margin. As a result, the traditional PI regulator can cover the low-frequency range. And without dc voltage filters, the bandwidth

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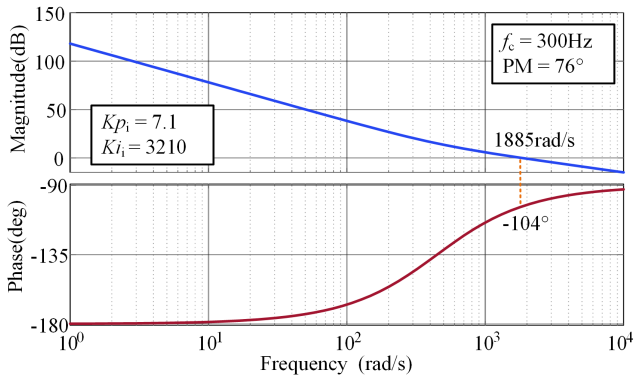
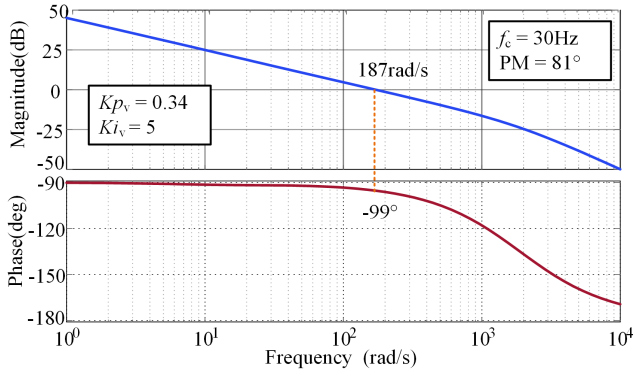
$$\begin{bmatrix} m_a \\ m_b \\ m_c \end{bmatrix} = T_{dq-abc} m_{dq} = \begin{bmatrix} \cos\theta_g & \sin\theta_g & 1 \\ \cos(\theta_g - 2/3\pi) & \sin(\theta_g - 2/3\pi) & 1 \\ \cos(\theta_g + 2/3\pi) & \sin(\theta_g + 2/3\pi) & 1 \end{bmatrix} \begin{bmatrix} m\sin\theta_o \\ 0 \\ 0 \end{bmatrix}$$
$$= \frac{m}{2} \begin{bmatrix} \sin(\theta_o + \theta_g) + \sin(\theta_o - \theta_g) \\ \sin(\theta_o + \theta_g - 2/3\pi) + \sin(\theta_o - \theta_g + 2/3\pi) \\ \sin(\theta_o + \theta_g + 2/3\pi) + \sin(\theta_o - \theta_g - 2/3\pi) \end{bmatrix} \tag{11}$$




(a)




(b)

Fig. 6. Bode plot of the open-loop transfer function of current loop and voltage loop. (a) AFE current loop. (b) Dc-link voltage loop.

of voltage control loop can be designed higher than classical control. The dynamic performance of dc-link voltage control is guaranteed. Moreover, the output bandwidth of the whole system, which is normally determined by the central control strategy, will not be influenced by the control-loop bandwidth of AFE.

Compared with conventional solutions, the low pass filter or notch filter with a specific frequency of voltage control loop is removed, so the phase margin of dc voltage control loop can be enhanced. Besides, owing to the injected current reference's dc components related to the average active power, the current injection has a feedforward control effect. Once the H-bridge output has a load change, the controller does not rely on the slow response of dc-link voltage control. Instead, the injected current can compensate for the needed power from AFE directly. For this reason, the proposed suppression can have a good dynamic performance on dc link voltage control and avoid severe voltage overshoot during the transient process.

### C. Impact of Proposed Current Injection Method

The proposed control can also bring a fast response to the dc-link voltage control loop. With the actively injected current, once the output power changes, the feedforward calculation unit will update the needed active power and pulsating power in one control period, and then the corresponding current is injected into the AFE unit with a fast current control loop. Therefore, it can be predicted that the dc-link voltage has a much smaller overshoot or drop compared with the classical control.

For each frequency pulsating power of the H-bridge output, the added $d$-axis current reference will lead to extra current with two different frequencies, $2\omega_o + \omega_g$ and $2\omega_o - \omega_g$, because of the inverse $d-q$ transform, where $\omega_o$ is the frequency of the output pulsating power, $\omega_g$ is the grid frequency. The two frequency components have the same amplitude. The additional injected current with the high frequency results in a high voltage drop on the transformer leakage inductance. Thus, the rectifier needs to offer a percentage of its modulation index to balance the voltage drop [16], [22]. Usually, the original modulation index is designed to be higher than 0.8, and the modulation index margin left for the injected current is very limited. If the injected current is high, the AFE rectifier might work under over-modulation conditions, which limits the dc-link voltage ripple suppression effect.

The injected current with a series of different frequencies will distort the AFE input current, especially improving the current amplitude. This will cause higher current stress for AFE switches and transformer windings. And the operating point would influence the loss distribution significantly and may cause unbalanced loss distribution among the three phases. Fortunately, as long as the three phase output of CHB is symmetrical, it can be easily proved that the injected harmonic currents only flow inside AFEs and transformer secondary windings and cancel out each other in the primary side [16]. Hence, the MV grid current can keep sinusoidal with the harmonic current injection-based voltage ripple suppression control. If the three-phase output of the CHB-based grid emulator is asymmetrical or unbalanced, the phase with higher output power should be injected with higher harmonic currents in this approach. Therefore, the amplitudes of the injected currents in the three phases of CHB are no longer equal. The currents of three-phase secondary windings can not cancel out each other, leading to an asymmetrical current at the grid side. In conclusion, further study is needed to explore the implementation of additional control or add hardware compensation to balance grid-side current.

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TABLE II: Key parameters of simulation model and experimental setup

| Description | Value |
|---|---|
| Primary line voltage | 6.3 kV |
| Grid frequency | 50 Hz |
| Grid-tied inductance | 3 mH |
| Secondary line voltage | 710 V |
| Rated dc-link voltage | 1200 V |
| Dc-link capacitor | 2.6 mF |
| Cell rated power | 40 kW |
| AFE switching frequency | 3 kHz |
| AFE current control loop bandwidth | 300 Hz |
| AFE current control parameters | $Kp_i$=7.1, $Ki_i$=3210 |
| Dc-link voltage control loop bandwidth | 30 Hz |
| Dc-link voltage control parameters | $Kp_v$=0.34, $Ki_v$=5 |
| H-bridge switching frequency | 20 kHz |
| Sampling frequency | 20 kHz |

## IV. Simulation and Experimental Verification

### A. Simulation Results

Verification of the proposed calculation and control method is performed on a CHB model in PLECS software. The key parameters are given in Table II. The input voltage is 6.3 kV and there are 5 cells in each phase leg. The cell dc-link voltage is 1200 V, so the AFE switching devices are 1700 V IGBT modules, which adopt 3 kHz switching frequency to achieve a balance between speed and power loss. For the H-bridge output, Silicon-Carbide (SiC) MOSFETs whose switching frequency is 20 kHz are installed to extend the output frequency range. The rated power of CHB converter in Fig. 1 is 600 kW and each cell is 40 kW. To restrict the dc-link voltage ripple within ±4% of the average value under 50 Hz output, the dc-link capacitance is designed as 2.6 mF. The following results will show the suppression control effect under steady state and dynamic conditions.

Fig. 7 shows the CHB cell operation waveform with multi-frequency output. The output parameters are the same as Table I, 50 Hz+10 Hz in Fig. 7(a), 50 Hz+40 Hz in Fig. 7(b) and 50 Hz+150 Hz in Fig. 7(b). At 0.5 s, the proposed dc-link voltage suppression control strategy is enabled, and the dc-link ripple is reduced from ±50 V to ±10 V for 50 Hz+10 Hz output and reduced from ±110 V to ±15V for 50 Hz+40 Hz output. For 50 Hz+150 Hz output, as analyzed in Section II, the ripple at 100 Hz is much smaller even with the same fundamental output power. Nevertheless, the ripple is still well suppressed without any over-compensation. Under different outputs conditions, the original dc-link voltage ripple can reach up to 9% of the average value, and the ripple is limited to 0.8% of the average value with the proposed control. Therefore, the size of the dc-link capacitors can be approximately reduced to 10% of the original value. On the other hand, there exists harmonic current in AFE cell, which distorts the three phase current and increases the amplitude.

Fig. 8 presents the MV grid side current under 50 Hz plus 10 Hz output before and after the ripple suppression control. As analyzed before, when the CHB three phase outputs are symmetrical, the injected harmonic current of all AFEs is canceled out by each other on the transformer secondary side. So three phase currents of the MV grid side are maintained symmetrical,

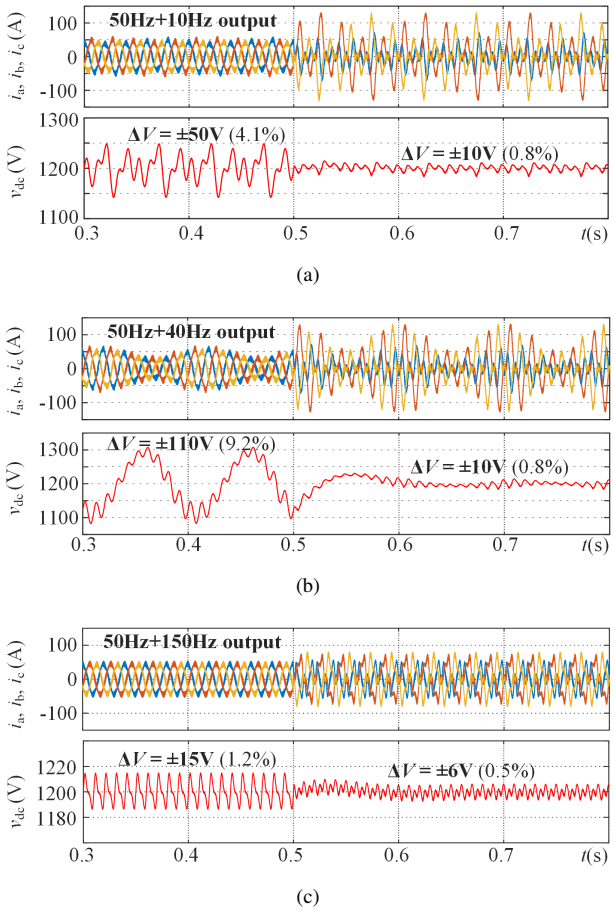


Fig. 7. Dc-link voltage ripple suppression effect with different multi-frequency output. (a) 50 Hz+10 Hz. (b) 50 Hz+40 Hz. (c) 50 Hz+150 Hz.

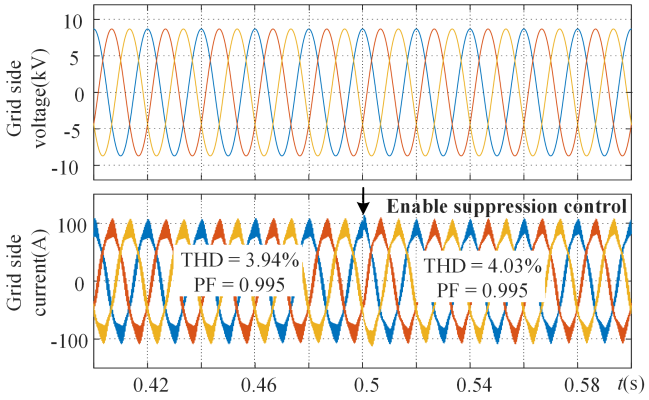


Fig. 8. Waveform of transformer grid side current without and with proposed control.

as shown in Fig. 8. However, considering the power losses of the converter in reality, the MV three phase current should be increased slightly. Before and after the suppression, the power factor remains at 0.995. The proposed method has no obvious influence on the power factor on the grid side.

Then, the Fast Fourier Transform (FFT) of AFE three-phase current and dc-link voltage is done to analyze their composition. According to Fig. 9(a) and Fig. 10(a), there exist mainly four frequency ripples on dc-link, and the frequency and magnitude

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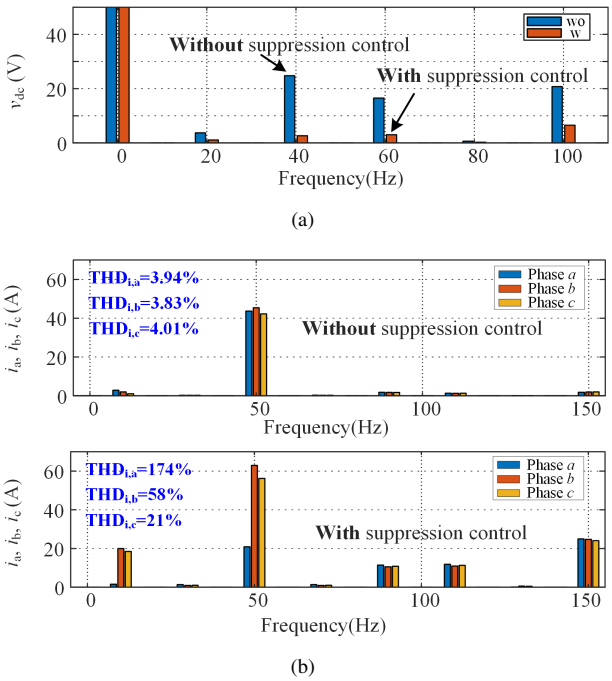


Fig. 9. FFT analysis of 50 Hz+10 Hz output waveform. (a) Dc-link voltage. (b) Three phase current of AFE unit.

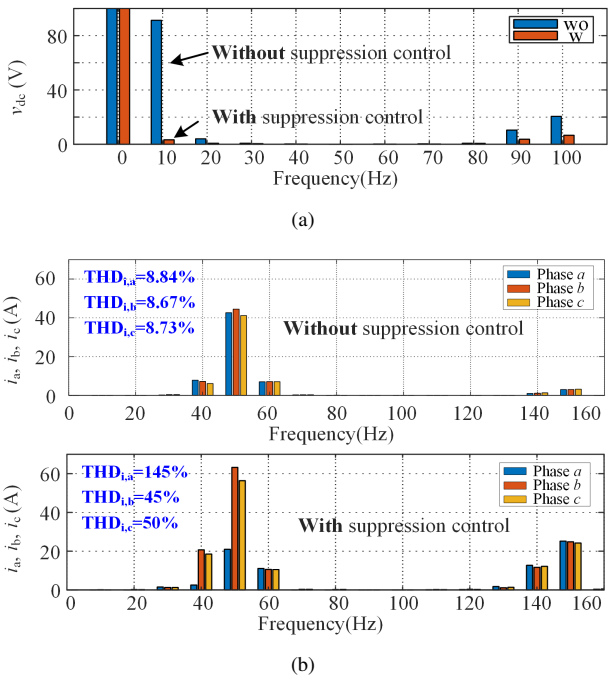


Fig. 10. FFT analysis of 50 Hz+40 Hz output waveform. (a) Dc-link voltage. (b) Three phase current of AFE unit.

of the dc-link ripple are corresponding to the theoretical analysis in Section II. And with the proposed suppression control, the voltage ripple of each frequency is reduced below 10 V, especially effective at low frequencies. But the cost is harmonic current with different frequencies which is injected to AFE. As shown in Fig. 9(b) and Fig. 10(b), without suppression control, the main current is symmetrical 50 Hz component. After the suppression control, harmonics at $2\omega_o \pm \omega_g$ for each output frequency are injected. For example, in Fig. 9, when the dc-link ripple contains mainly 20 Hz, 40 Hz, 60 Hz and 100 Hz, harmonic current at 10 Hz, 30 Hz, 50 Hz, 70 Hz, 90 Hz, 110 Hz and 150 Hz are injected. With the injected harmonic current, the AFE three-phase current becomes unbalanced. Besides, even the THD of AFE input current with the suppression method is worsened and unbalanced compared with without suppression control condition, the THD of the grid current and the power factor on the grid side is not influenced by the proposed method, as demonstrated in Fig. 8.

To demonstrate the good dynamic performance of the proposed control, the load step change, frequency change and power flow reverse are simulated. In Fig. 11, the load change waveform with conventional control and the proposed control are compared. In the conventional control, the load has a step up from 20 kW to 40 kW at 0.4 s, and the transient voltage drop is more than 100 V with more than 50 ms transient time. While in the proposed control, shown in Fig. 11(b), the output power steps from 4 kW to 40 kW at 0.5s and steps down to 4 kW at 0.7 s. There is no obvious voltage dip or overshoot on dc-link, because the injected current reference $i_{dref2}$ has a fast real-time update. This forward calculation brings the benefits of quick response to the output current change. Similarly, in Fig. 12, at 0.6 s, the output frequency changes from 50 Hz+10 Hz to 50 Hz+40 Hz. The suppression effect keeps good performance without an obvious

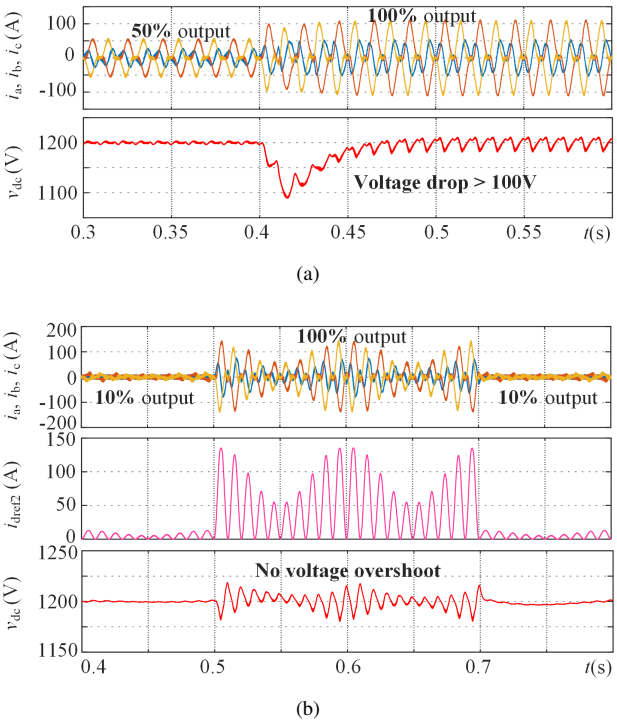


Fig. 11. Load step change waveform with conventional control and proposed control. (a) Conventional control. (b) Proposed control.

transient process.

One of the biggest challenges for dc-link voltage control is the switching of power flow direction. In the conventional control, the dc-link voltage control mainly depends on the response of the voltage control loop. However, the voltage loop bandwidth is much lower than the current loop. As illustrated in Fig. 13(a), the power flow direction suddenly changes and a significant

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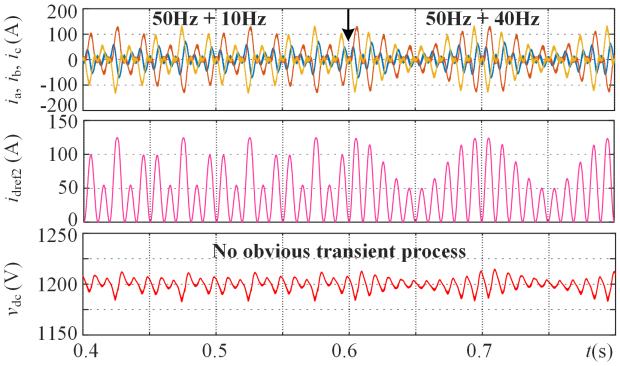


Fig. 12. Output frequency change waveform with proposed control.

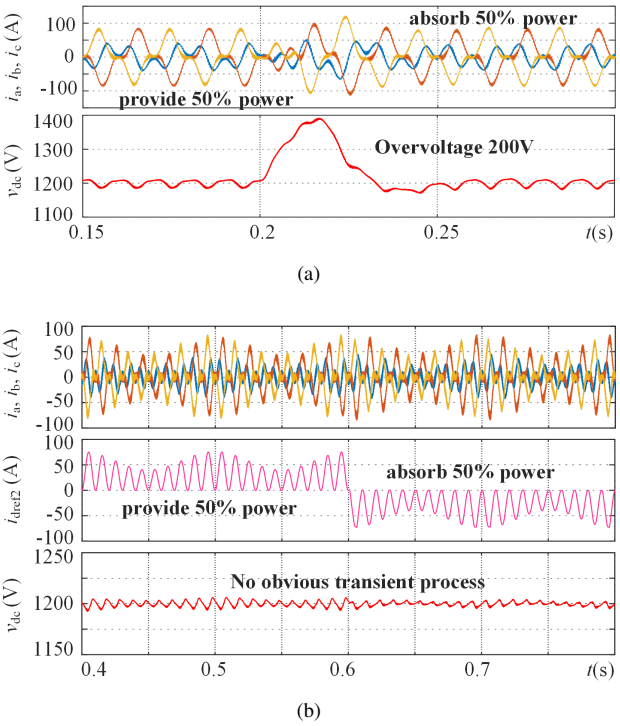


Fig. 13. Power flow reverse waveform with conventional control and proposed control. (a) Conventional control. (b) Proposed control.

over-voltage, more than 200 V, surges on dc capacitors, which could damage the capacitors or the power switching devices. By contrast, by employing the proposed control scheme, when the power flow changes, the injected current reference is updated at the same time. Consequently, the dc-link voltage voltage stays at the average value of 1200 V.

It is worth mentioning that the proposed control is based on the fast and accurate feedforward calculation. In reality, there exists some measurement error or noise and some disturbance, so the dynamic performance may not be as perfect as the simulation result. Nevertheless, the dynamic performance is better than the traditional control strategy depending on the slow voltage control loop. This is presented next.

The extra current increases the current amplitude, resulting in higher conduction losses and switching losses of AFE switches. The total power losses of a single AFE unit are extracted in PLECS software for the two study cases, 50 Hz+10 Hz and

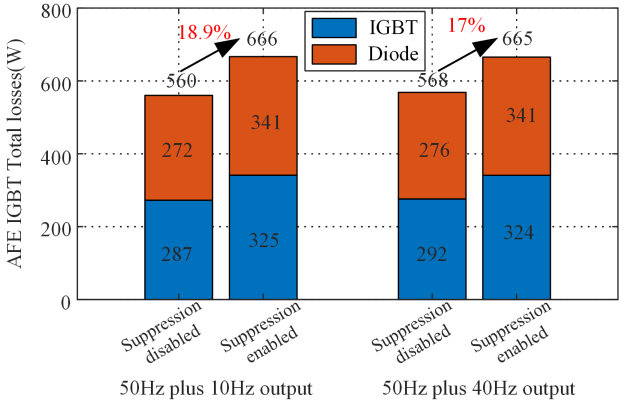


Fig. 14. AFE losses comparison under 40 kW output.

50 Hz+40 Hz. Without suppression control, the AFE unit only transfers the average active power to the H-bridge, so the three phase losses are very close, about 560 W. With harmonic current injection, the total losses increase to 660 W for both cases, an increase of about 18%. More specifically, the IGBT losses increase by 13% and the anti-parallel diode losses increase by about 25%. The AFE efficiency decreases from 98.6% to 98.3%, only 0.3% reduction. So, the proposed control has very limited influence on the AFE efficiency. The heatsink should be properly sized to satisfy the thermal dissipation requirement, considering the extra power loss brought by harmonics. In addition, the injected harmonic current will produce more losses on the transformer secondary side windings. Thus, the extra current stress should be considered in the design of the multi-winding transformer. Fortunately, similar current stress has been well understood and considered in phase-shifted transformer design for high-power applications [34].

### B. Experimental Results

Two CHB cell prototypes are built to verify the effectiveness of the proposed suppression strategy. The two cells' inputs are connected to a multi-winding transformer's secondary side and their H-bridge outputs are connected through an inductor, as shown in Fig. 15(a), which is configured as a back-to-back power test. The leakage inductance of the transformer is used as the filter inductor of the AFE. More details on the leakage inductance of the medium-voltage phase-shift transformer can be found in [35]. One cell is set as a voltage source (Master in the figure) and another is operating to control the current (Slave in the figure) so that the power is circulating inside the transformer and two cells. The H-bridge can output any desired voltage and current flexibly. In the following experimental waveform, the dc-link voltage $v_{dc}$, the three phase current $i_a, i_b, i_c$ of AFE unit and the output current $i_o$ of H-bridge in the Master cell are measured. The auxiliary winding is connected to a 380 V power grid to compensate for the power losses of the testing. The CHB cell photo is presented in Fig. 15(b), where the dc link capacitors occupy half of the total volume. Therefore, if a lower output frequency such as 10 Hz is required, more capacitors are needed to be installed. The key experiment parameters are the same as Table II.

In Fig. 16, the suppression performance under different output frequencies is illustrated. When the output has only single fre-

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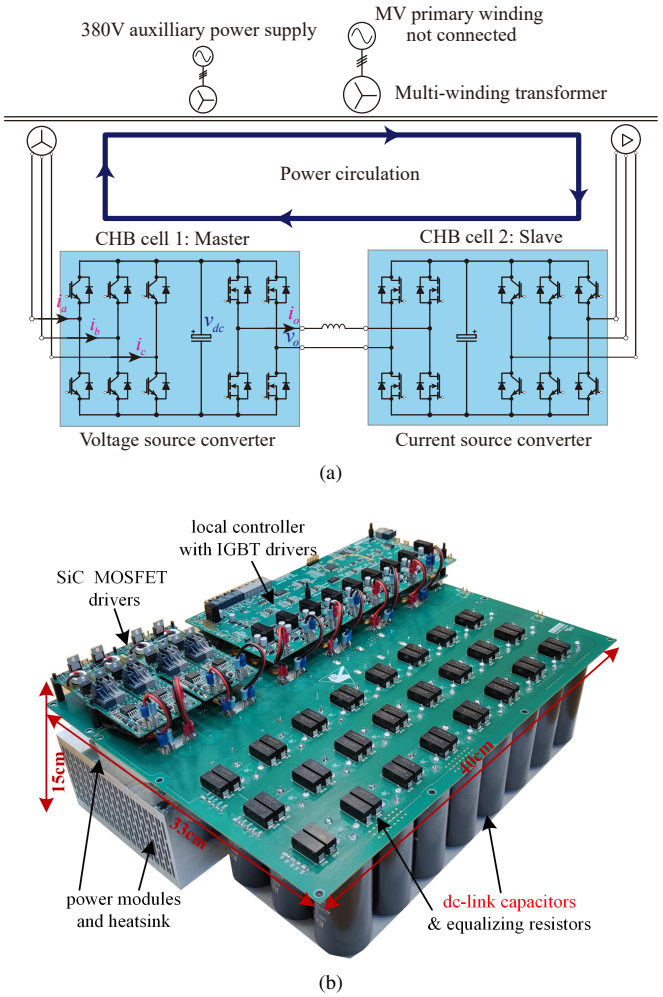


Fig. 15. Experiment configuration and laboratory prototype photo. (a) Experiment configuration setup. (b) 1200 V @ 40 kW CHB cell photo.

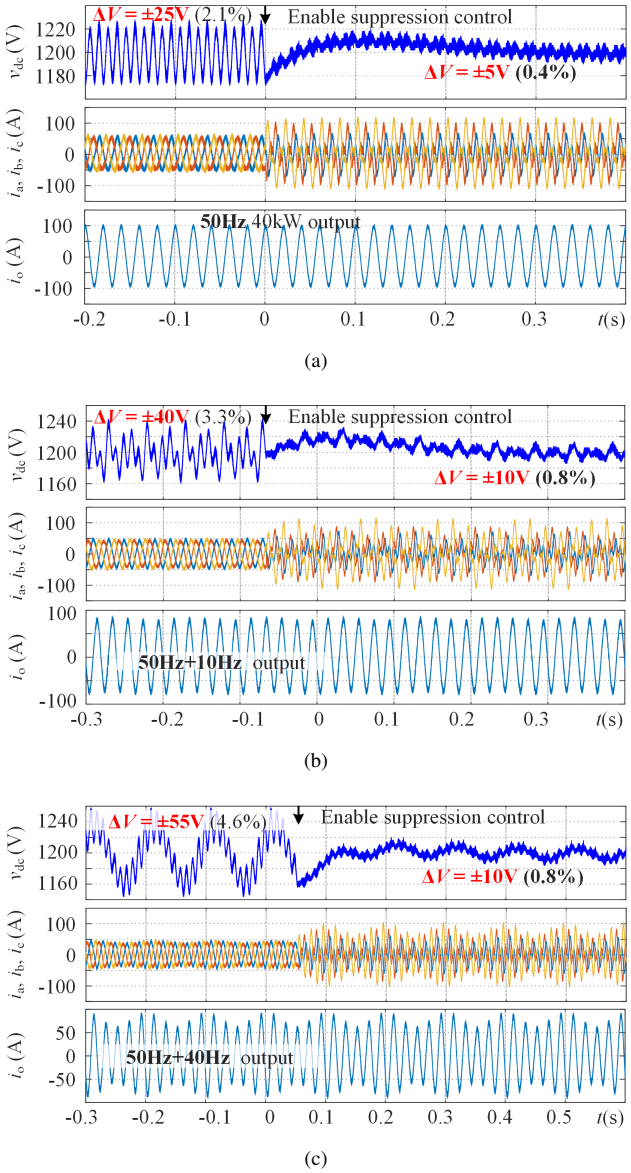


Fig. 16. Experimental effect of proposed suppression method under different frequency output.(a) 50 Hz output. (b) 50 Hz + 10 Hz output. (c) 50 Hz + 40 Hz output.

quency 50 Hz, in Fig. 16(a) the dc-link voltage ripple is about ±25 V without any suppression control. When the proposed current injection is enabled, the voltage ripple is mitigated within ±5 V. Obviously, there is no transient voltage drop or overshoot during the enable process. As analyzed before, the influence is the distortion of the sinusoildal current waveform and the increase of AFE current amplitude. When the output has multiple frequency outputs, such as 50 Hz+10 Hz and 50 Hz+40 Hz, in Fig. 16(b) and (c), the suppression effect is as perfect as the simulation and the voltage ripple is mitigated within ±10 V even with some measurement noise. It is remarkable that no adaptive filters or resonant controllers are designed for variable output frequencies. With this proposed control scheme, the dc link capacitance can be reduced significantly. In other words, the output frequency range and application areas can be expanded with the same dc link capacitance.

When the load condition changes, the dynamic features are also verified by experiment. For example, in Fig. 17 (a), the load has a step change between half load 20 kW and full load 40 kW. The voltage ripple is always suppressed at a low level, less than ±10 V. Besides, the transient voltage is about 40 V due to some inevitable disturbance, such as converter losses. The experimental prototype can also simulate the regenerative operation mode. In Fig. 17 (b), once the power flow reverses from -20 kW to +25 kW, the feedforward calculation can update the injected current reference immediately. The voltage ripple is still suppressed within ±10 V. This control can avoid undesired large voltage overshoot or drop for dc-link voltage capacitors, in this case less than 40 V drop, because the H-bridge output power is compensated directly by the AFE unit instead of the dc capacitors during the transient process.

The dynamic performance of output frequency change is also tested. In Fig. 17 (c), the output frequency changes from 50 Hz+40 Hz to 50 Hz+10 Hz. The different frequency ripples are suppressed rapidly even with no obvious transient voltage. Compared with existing methods, no extra control loop or variable frequency detection filter is added in this control to adapt the frequency change, which makes it more easily implemented in different applications.

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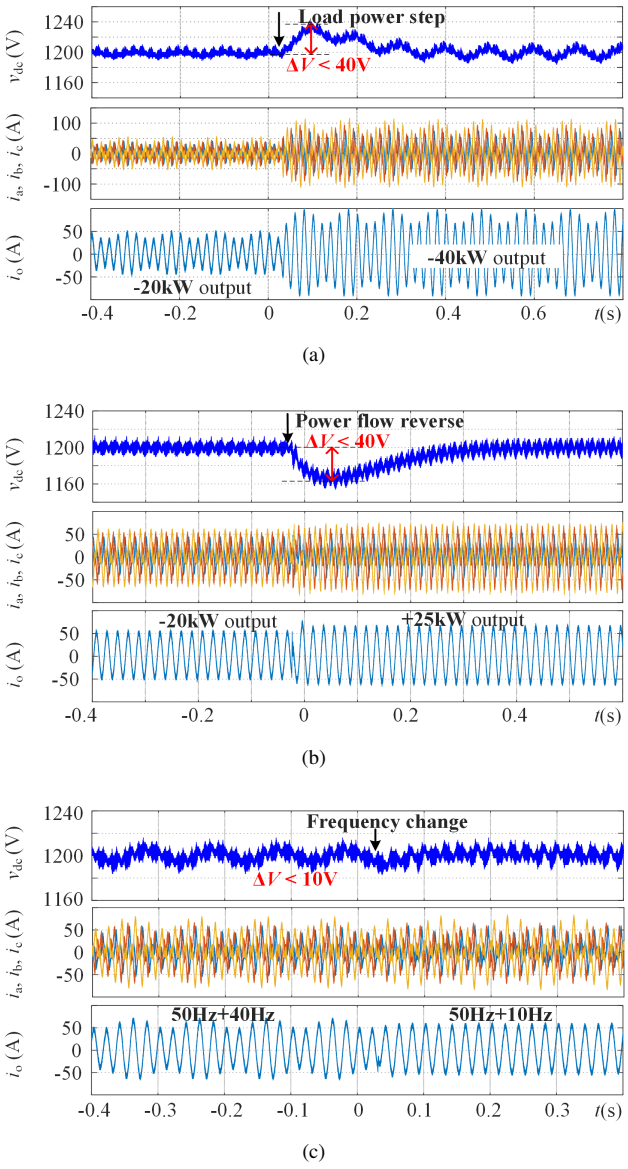


Fig. 17. Dynamic waveform of proposed ripple suppression control. (a) Load changes from 20 kW to 40 kW. (b) Power flow reverses from -20 kW to +25 kW. (c) Output frequency changes from 50 Hz + 40 Hz to 50 Hz + 10 Hz.

## V. Conclusion

The cascaded H-bridge converter based MV grid emulator with high flexibility is a feasible and necessary approach for the analysis and testing of grid-tied power electronics converters in distribution system. This paper reveals the dc-link voltage ripple characteristics of CHB based MV grid emulator with multi-harmonics output voltage and current. When the grid emulator output contains $\omega_1$ and $\omega_2$ two frequency components, the dc-link capacitors mainly suffer $2\omega_1$, $2\omega_2$, $\omega_1+\omega_2$ and $|\omega_1-\omega_2|$ four frequency ripples. To suppress these voltage ripples, reduce the dc-link capacitance and extended low-frequency output range, a novel ripple suppression method based on harmonic current injection has been proposed. The injected current reference is calculated according to the H-bridge switching function and output current. The feedforward calculation is fast and accurate, which is suitable and adaptive for single-frequency and multi-frequency output occasions. With the proposed control, the dc-link capacitance can be reduced to 10% of the original design. Furthermore, compared with the existing approaches in single-frequency output, this idea has a faster response to dynamic output change. The cost is that the injected harmonic current will increase the current stress and power losses. Fortunately, the distorted AFE three-phase current only flows within the converter side and the MV grid side current and the grid emulator output will not be affected. Finally, the effectiveness and implementability are verified in the simulation and experiment.

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