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Active Power Decoupling for Single-Phase Input-Series-Output-Parallel Solid-State Transformers

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***Abstract*—Solid-state transformers with input-series output-parallel structures are being considered for a variety of applications requiring MVAC to LVDC conversion. Due to the single-phase AC/DC conversion at the input side, all floating cells of the solid-state transformer suffer from the well-known second harmonic pulsating power. Large DC link capacitors are typically employed to smooth the ripple voltage created by the pulsating power, which leads to low power density. An alternative solution is to adopt active power decoupling technology, which can buffer the pulsating power in separate energy storage components. This paper investigates the feasibility and potential benefit of applying active power decoupling to single-phase input-series output-parallel solid-state transformers. The buck-type active power filter is selected, and the design of a prototype is presented. Simulation and experimental results show that a significantly lower second harmonic ripple voltage is achieved with active power filters and very small DC link capacitance.**

***Index Terms*—active power decoupling, active power filter, solid-state transformer, input-series output-parallel, second harmonic ripple voltage suppression.**

I. Introduction

The solid-state transformer (SST) is a technology that has the potential to revolutionize many fields, including traction systems, renewable energy, data centers, and smart grids [1]–[9]. One of the most common SST applications is MVAC to LVDC conversion. In this case, the input-series output-parallel (ISOP) structure is typically employed by the SST due to the high input voltage.

The ISOP SST, as shown in Fig. 1, contains multiple cells that are connected in series at the input to interface MV grid and connected in parallel at the output to provide a large output current. Each of the cells is made up of an AC/DC converter and a DC/DC converter with MV galvanic isolation. DC link capacitors are installed on both the MV and LV sides of the cell to provide stable DC voltages. The ISOP structure greatly reduces the power rating of each cell and allows the easy expansion of the input voltage ratings, provided that galvanic isolation is sufficiently rated.

The instantaneous power from the single-phase AC grid contains not only a constant component but also a pulsating component at the double AC line frequency. This pulsating power causes the second harmonic ripple voltage on the DC link, which impairs the converter's operation. The ISOP SST suffers from a similar issue, resulting in second harmonic ripple voltages on the MV side DC links. Depending on the type and control method of the DC/DC converter, the pulsating power could be propagated to the LV side and influence the LVDC output as well [10]. It is worth noting that three-phase ISOP SSTs also suffer from the second harmonic ripple

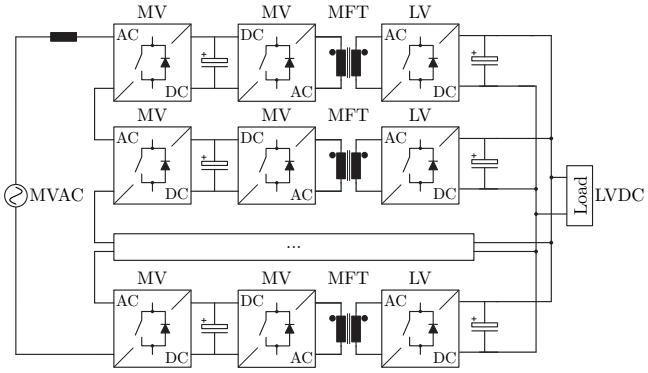


Fig. 1. MVAC to LVDC solid-state transformer with input-series output-parallel structure.

voltages on the MV side DC links because the phase-separated configuration is usually adopted in which the three-phase power is processed by three identical single-phase ISOP SSTs independently. In this case, significant ripple voltages remain on the MV side DC links even if the ripple voltage on the LV side DC link has been neutralized.

A bulky DC link capacitor is typically installed as a passive harmonic suppressing device to buffer the pulsating power. Considering that ISOP SSTs normally target MV applications and MW level ratings, these capacitors have significant ratings and may occupy a large portion of the volume of the entire SST. The majority of ISOP SSTs use this solution, resulting in a poor power density of employed power stages. Another passive alternative is the LC trap filter, which provides a selective low-impedance loop for the second harmonic ripple current [11]. Yet, because the LC branch's resonance frequency is typically low (33.4Hz for railway 16.7Hz, 100Hz or 120Hz for utility grids), the size and weight of the passive components are considerable.

Various control strategies for harmonic suppression in three-phase ISOP SSTs have been proposed. Given that the ripple voltage on the LV side DC link will be neutralized, the requirements of MV side DC link capacitance can be reduced by transferring the pulsating power from the MV side to the LV side. This method requires the DC/DC converter in the SST to be equipped with power flow control capability, which usually refers to the dual active bridge (DAB) converter [12]–[17]. For SSTs using LLC converters as DC/DC stage, a similar power flow control is introduced in [18]. The third-harmonic voltage injection technology is a common solution for the second harmonic ripple suppression in modular converters, such as cascaded H-bridge converters [19], [20] and modular

Fig. 2. The LV PETT, which serves as the SST hardware platform for this research. The nine APFs have been installed.

multilevel converters (MMC) [21]. Similar approaches can be applied to ISOP SST as well [22]. Unfortunately, these suggested methods are no longer applicable to single-phase ISOP SST.

Active power decoupling (APD) is an appealing solution for second harmonic ripple suppression [23]–[29]. By introducing an additional active circuit in each of the floating DC links on the MV side, the pulsating power is diverted from the DC link capacitor and stored in separate components where a large ripple voltage is allowed. As a result, the pulsating power is buffered more effectively. APD has been extensively studied in single-level converters. In recent years, APD has also been applied in multi-level converters, such as MMC [30]–[33] and cascaded H-bridge converters [34], [35]. In most cases, APD is applied to all of the floating cells [31]–[35], while [30] proposes another configuration where centralized active power filters (APF) are installed in each phase leg of the MMC. However, the research on APD in the specific field of SST is still very limited. The application of APD in a single-phase single-stage current-source soft-switching SST with an 83% DC link capacitance reduction is reported in [36]–[38]. The APD control and main SST control are coupled, and a predictive control method is adopted to stabilize the low-inertia inductive DC link. However, the APD implementation adopted in this work is tailor-made for its unique SST topology and is not generally applicable to other SST configurations.

In this paper, the practicality and benefits of applying APD to single-phase ISOP SST are examined. A buck-type APF with capacitive energy storage is selected. The APFs are inserted in all of the ISOP SST's floating cells as independent pulsating power buffers, while the SST's original architecture and control remain unchanged, other than for adaptations of some control gains. The APD method introduced in this paper is generic and applicable to other SSTs that suffer from second harmonic pulsating power. Simulation and experimental results

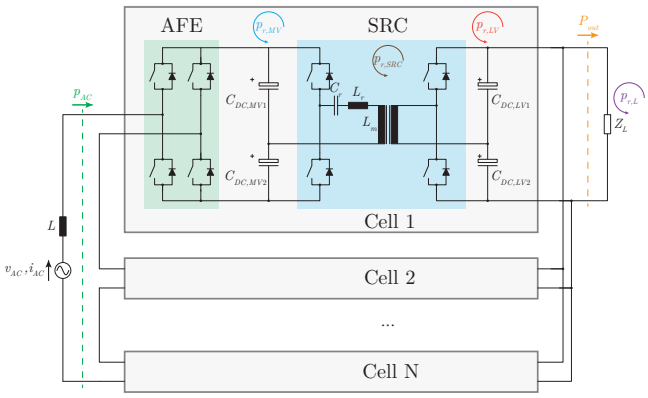


Fig. 3. The topology and power flow of the LV PETT.

prove that the APD method enables ISOP SST to achieve a smaller ripple voltage and a substantial DC link capacitance reduction, which in the experimental setup used in this work has been decreased by over 85% compared to the original values.

The rest of the paper is organized as follows: Section II analyzes the second harmonic power flow and the corresponding ripple voltage in the ISOP SST; Section III introduces the configuration of ISOP SST with APF installed and selects the best-suited APF topology; Section IV gives the working principle, control algorithm, and hardware design of the APF; Section V provides the simulation and experimental results for verification; and Section VI summarizes the conclusion of the work.

II. Second Harmonic Pulsating Power and Ripple Voltage in ISOP SST

The ISOP SST analyzed in this paper, as shown in Fig. 2, is the low-voltage prototype of the power electronic traction transformer (LV PETT), which is described in [6]. The LV PETT was originally developed by ABB as an analog simulator with modest power ratings for control hardware and software verification of a corresponding medium-voltage prototype named MV PETT [7]. It was generously donated to the Power Electronics Laboratory of EPFL by Hitachi Energy (former ABB) and now serves as an SST research platform.

The LV PETT utilizes the ISOP structure with nine cells that are comprised of an H-bridge active front end (AFE) converter and a series resonant converter (SRC) operating in open-loop at a fixed switching frequency. Although the LV PETT is designed to be a bidirectional converter, this paper only considers the case where power flows from MVAC to LVDC. The structure and power flow of the LV PETT are presented in Fig. 3. In the rest of the paper, LV PETT is further termed SST.

The calculation of the second harmonic pulsating power for an SST is the same as for a typical single-phase AC/DC converter, which can be derived from the grid voltage v_{AC} and current i_{AC} [23]. The instantaneous power from the grid

TABLE I
RATINGS AND PARAMETERS OF THE SST

Parameters		Value
Rated Power	P_{out}	54kW
Line Voltage	$V_{AC,RMS}$	1.5kV
Line Frequency	f_{AC}	50Hz
Line Inductor	L	25mH
Number of Cells	N_{cells}	9
DC Link Voltage	V_{DC}	360V
MV side DC Link Capacitance	$C_{DC,MV}$	4mF
LV side DC Link Capacitance	$C_{DC,LV}$	2.2mF
Switching Frequency of AFE	f_{AFE}	317Hz
Switching Frequency of SRC	f_{SRC}	1500Hz
Resonant Capacitance	C_r	60μF
Resonant Inductance	I_r	135μH
Magnetizing Inductance	L_m	13mH
Transformer Turns Ratio	N_1/N_2	1

can be expressed as:

$$\begin{aligned} p_{AC} &= v_{AC} i_{AC} = V_{AC} \sin(\omega t) I_{AC} \sin(\omega t - \phi) \\ &= \frac{V_{AC} I_{AC}}{2} \cos\phi - \frac{V_{AC} I_{AC}}{2} \cos(2\omega t - \phi) \end{aligned} \tag{1}$$

where V_{AC} and I_{AC} represent the amplitude of the grid voltage and current, respectively; ϕ is the phase angle between the grid voltage and current; and ω is the angular frequency of the grid. It should be noted that the conversion loss and reactive power of the grid filter are neglected.

From (1), one can see that the SST's input instantaneous power is made up of a constant power P_{out} and a pulsating power p_r.

$$\begin{aligned} P_{out} &= \frac{V_{AC} I_{AC}}{2} \cos\phi \\ p_r &= -\frac{V_{AC} I_{AC}}{2} \cos(2\omega t - \phi) \end{aligned} \tag{2}$$

P_{out} is the power that is transferred to the load, while p_r is the second harmonic pulsating power causing the ripple voltage on the DC link. The power flow of the entire SST is evenly distributed into each cell under normal operation. The AFE feeds each fraction of the power into the cell, and the pulsating power introduces second harmonic ripple voltages on the MV side DC links. The SRC operates at a fixed frequency and can be considered as a DC transformer between the MV and LV side DC links. Although this minimizes control complexity, it also leads to the inevitable propagation of the second harmonic pulsating power from the MV side to the LV side. Excessive DC link ripple voltage affects AFE control, introduces harmonics into the line current, and shortens components' lifetime. In typical ISOP SSTs, bulky capacitors are installed on both the MV and LV side DC links to limit the second harmonic ripple voltages, leading to a low power density.

According to Fig. 3, the pulsating power distribution inside the SST can be represented as:

$$\begin{aligned} p_r &= p_{r,cell} N_{cells} + p_{r,L} \\ &= (p_{r,MV} + p_{r,LV} + p_{r,SRC}) N_{cells} + p_{r,L} \end{aligned} \tag{3}$$

where $p_{r,cell}$ is the pulsating power in each SST cell, $p_{r,L}$ is the pulsating power buffered by the load, N_{cells} is the number of cells. $p_{r,MV}$, $p_{r,LV}$ and $p_{r,SRC}$ are the pulsating power buffered by the MV side DC link capacitors, LV side DC link capacitors and the SRC, respectively. Usually, the resonant capacitance C_r in the SRC is much lower than the DC link capacitance, and the pulsating power buffered by the SRC is relatively small, that is $p_{r,SRC} \ll p_{r,MV}$ and $p_{r,SRC} \ll p_{r,LV}$. If the load is capacitive or inductive, the pulsating power buffered by the load can be considerable. Otherwise, if the load is resistive, $p_{r,L}$ is negligible.

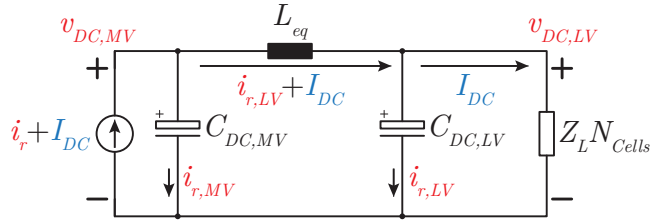


Fig. 4. The equivalent circuit of the two-stage SST cell.

The propagation mechanism of second harmonic pulsating power in two-stage AC/DC converters has been investigated in [39]–[42], which can be adopted to analyze the relationship between $p_{r,MV}$, $p_{r,LV}$, and p_r. Fig. 4 presents the equivalent circuit of the two-stage SST cell. For simplicity, $p_{r,SRC}$ and $p_{r,L}$ are neglected in the following analysis, which means all the pulsating power is buffered by the DC link capacitors.

Because the switching frequency f_{SRC} is close to its resonant frequency f_{res}, the voltage gain of the SRC is close to 1 considering the 1:1 transformer turns ratio. In this case, the average DC link voltages on both the primary and secondary sides can be approximated as V_{DC}, and the equivalent output current of the AFE is:

$$i_{AFE} = i_r + I_{DC} = \frac{p_r}{V_{DC}} + \frac{P_{out}}{V_{DC}} \tag{4}$$

where i_r is the equivalent second harmonic current from the grid. $C_{DC,MV}$ and $C_{DC,LV}$ are the equivalent DC link capacitors on both sides. $i_{r,MV}$ and $i_{r,LV}$ are the second harmonic current buffered by $C_{DC,MV}$ and $C_{DC,LV}$ with $p_{r,MV} \approx V_{DC} i_{r,MV}$ and $p_{r,LV} \approx V_{DC} i_{r,LV}$. According to the method proposed in [39], [40], the impedance of the SRC can be represented by the equivalent inductor L_{eq}, which is derived using the averaged piecewise sinusoidal current [40] and can be written as:

$$L_{eq} = L_r \left(\frac{\pi f_{res}}{f_{SRC}} \right)^2 \tag{5}$$

where L_r is the resonant inductance of the SRC.

In the Laplace domain, the second harmonic current on both sides can be expressed as:

$$\begin{aligned} i_{r,MV}(s) &= i_r(s) \frac{\frac{1}{sC_{DC,MV}} \parallel \left(sL_{eq} + \frac{1}{sC_{DC,LV}} \right)}{\frac{1}{sC_{DC,MV}}} \\ i_{r,LV}(s) &= i_r(s) \frac{\frac{1}{sC_{DC,MV}} \parallel \left(sL_{eq} + \frac{1}{sC_{DC,LV}} \right)}{\left(sL_{eq} + \frac{1}{sC_{DC,LV}} \right)} \end{aligned} \tag{6}$$

It can be seen that the distribution of the pulsating power between the primary and secondary sides is mainly determined by the relationship between $C_{DC,MV}$, $C_{DC,LV}$, and L_{eq}.

Assuming that the ripple voltage is much lower than V_{DC}, the amplitude of the pulsating power $P_{r,MV}$ and $P_{r,LV}$ can be written as:

$$\begin{aligned} P_{r,MV} &\approx 2\omega \Delta V_{DC,MV} V_{DC} C_{DC,MV} \\ P_{r,LV} &\approx 2\omega \Delta V_{DC,LV} V_{DC} C_{DC,LV} \end{aligned} \tag{7}$$

$\Delta V_{DC,MV}$ and $\Delta V_{DC,LV}$ are the amplitude of the ripple voltages. It shows that only a small portion of the capacitor's energy storage capacity is used to buffer the pulsating power if the ripple voltage is kept low.

Table I gives the parameters of the original SST. Limited by availability and ratings of the single-phase input step-up transformers, the SST operates at 750V AC line voltage with a maximum output power of 6kW in this paper, and the DC link voltage drops to 220V accordingly. Nevertheless, the presented principles are not power rating dependent. Fig. 5 shows the experimental waveform of the SST with reduced ratings. The SST operates with a unity power factor and supplies 6kW of power to a resistive load. v_{AC} and i_{AC} are the AC line voltage and current, respectively. $v_{AC,out}$ is the multilevel voltage waveform measured at the AC terminal of the SST. The second harmonic ripple appears on the MV side DC link voltage of cell 1 $v_{DC,MV1}$, LV side DC link voltage $v_{DC,LV}$, and output current i_{out}. Because the AFE adopts unipolar pulse width modulation (PWM), harmonic components at the double switching frequency of AFE appear on MV side DC link voltages. The PWM carriers of the AFE and SRC in the nine cells are phase-shifted by $360°/9 = 40°$, leading to a high equivalent switching frequency. Thanks to the parallel connection of the output, the switching frequency ripple voltage is greatly reduced at the LV side. The amplitude of the resonant tank current of cell 1 $i_{res,1}$ reflects the instantaneous power transfer through the SRC, and the second harmonic power flow can be clearly observed.

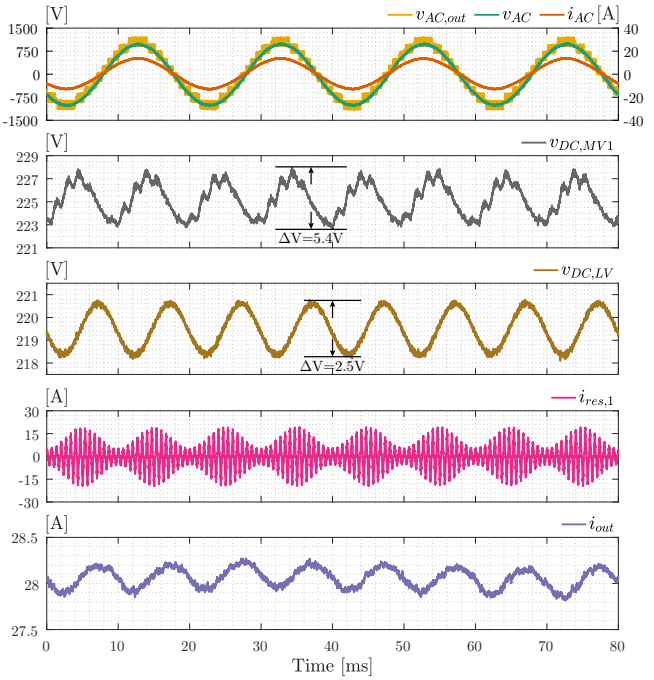


Fig. 5. Nominal operating waveform of the SST at 6kW.

III. Proposed APD method for ISOP SST

The aforementioned analysis shows that using the DC link capacitor to buffer the second harmonic pulsating power is not cost-effective because only a small fraction of the energy storage capacity is utilized. To solve this problem, APD is developed to divert the pulsating power to a separate energy storage component where a higher ripple voltage is allowed, and a large portion of the energy storage capacity can be utilized. As the DC link capacitor is fully decoupled from the pulsating power, it can be designed small enough to address the switching frequency ripple only. As of today, APD has been extensively employed in single-phase AC/DC converters with low ripple voltage tolerance [23]–[29].

To achieve the maximum capacitance reduction, the best way to integrate APF into ISOP SST is to insert APF on the MV side DC link of each cell. In this configuration, the pulsating power from the AFE can be buffered by the APF completely, leaving the rest of the SST free of second harmonic ripple voltage. On the other hand, installing the APF on the LV side DC link buffers the pulsating power locally, while the MV side DC links still suffer from the pulsating power, and large DC link capacitors are required.

APD has been a hot research topic in recent years, with multiple APF topologies developed. However, not all of them are applicable in ISOP SST. Several typical APF topologies are given in Fig. 6. Both inductors and capacitors can be employed as the energy storage components of the APF. Fig. 6a gives an example where the pulsating power is buffered by an inductor [24]. Two active switches regulate the inductor current to be sinusoidal. However, this solution is not considered due to the low power density of the inductor, and APF topologies with capacitive energy storage are preferable.

Fig. 6b demonstrates an APF topology in which the energy storage capacitor is connected to the AC side [25]. This topology has the advantage that the capacitor voltage is sinusoidal, which is easy for the controller to track. However, these types of AC-side APF usually require additional inductors on the AC input port of each cell and considerable hardware modification to the original structure of ISOP SST.

Preferably, the APF should be connected in parallel to the existing circuit and operate independently. As shown in Fig. 6c, the APF topology based on a boost converter meets this requirement [26], [27]. In this topology, however, the voltage rating of switching devices and capacitors must be higher than the DC link voltage. This drawback is especially noticeable in MV applications like ISOP SST. An APF with a full-bridge circuit, as shown in Fig. 6d, where the APF is connected in series to the DC link capacitor, is proposed in [28]. The advantage of this approach is that the APF only needs to process a fraction of the pulsating power, which leads to higher efficiency. Yet, this comes at the expense of more active switches and increased energy storage requirements.

Both of the last two candidates, as shown in Fig. 6e and

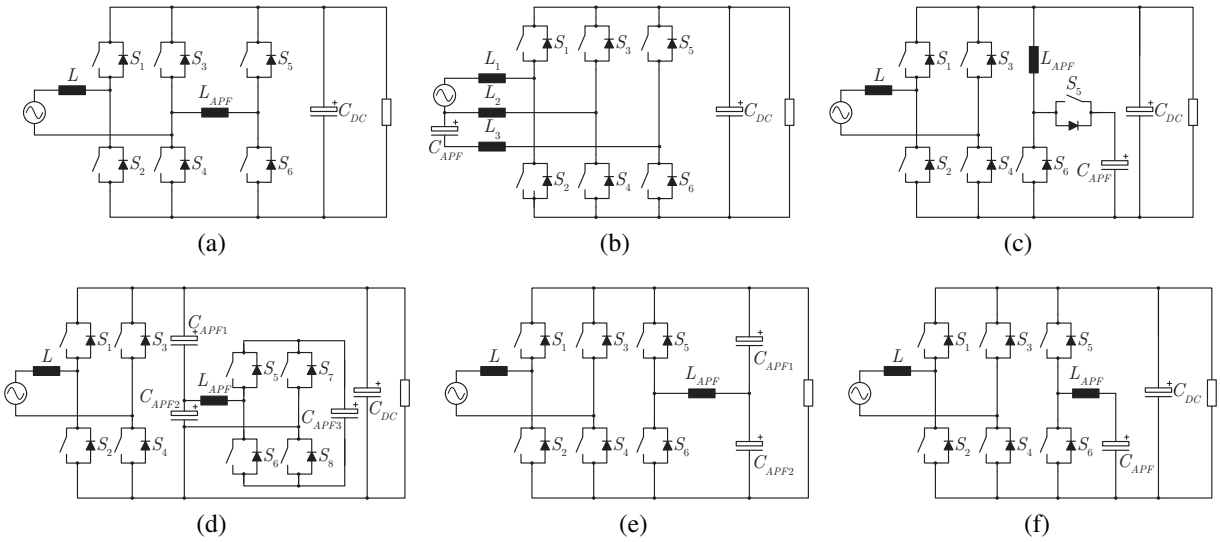


Fig. 6. Typical APF topologies in a single-phase system: a) Inductor-based APF b) AC-side APF c) Boost-type APF d) Stacked APF e) DC-split-capacitor APF f) Buck-type APF.

Fig. 6f require only two active switches with the same voltage rating as the SST cell. [29] analyzes an APF topology with dc-split-capacitor circuit. This APF has two identical capacitors connected in series to form a DC link capacitor, while the midpoint is connected to a half-bridge circuit through an inductor. The sinusoidal capacitor voltage of this topology facilitates the controller design. No additional DC link capacitor is required as the APF capacitors are directly supporting the DC link. On the other hand, the buck-type APF, which is described in [23], has only one energy storage capacitor. The APF capacitor can be fully charged and discharged, where the highest energy storage utilization is achieved. Even with the additional DC link capacitor, the buck-type APF can buffer the same pulsating power with less capacitance than the dc-split-capacitor APF. The disadvantage of the buck-type APF is that the capacitor voltage is not sinusoidal and contains high-order harmonics. These issues, however, can be overcome by properly designing controllers. Because the primary purpose of this research is to reduce the DC link capacitance in the SST, the buck-type APF is chosen for its lowest energy storage capacitance requirements.

The SST is adopted as the test platform to verify the proposed APD method. Fig. 7 shows the modified SST cell with buck-type APF installed. The APF is connected in parallel

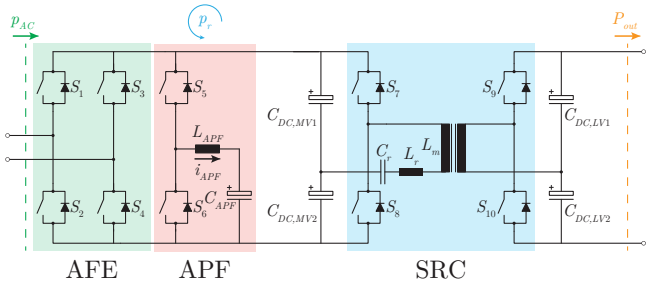


Fig. 7. Modified SST cell with buck-type APF installed.

to the MV side DC link capacitor. The APF can be considered as a controlled current source, injecting a sinusoidal current at the double line frequency to compensate for the second harmonic pulsating power. The APF operates independently with a given reference power. The AFE and SRC are controlled by the SST controller [6], regulating the average value of DC link voltage to be the desired reference. As APF is employed, bulky capacitors are no longer required. In the new configuration, $C_{DC,MV}$ is reduced from 4mF to 0.375mF, while $C_{DC,LV}$ is reduced from 2.2mF to 0.55mF.

IV. Design of the Buck-type APF

A. Operating Principles

As shown in Fig. 7, the buck-type APF is composed of a half-bridge circuit, an auxiliary inductor L_{APF}, and an energy storage capacitor C_{APF} [23]. The inductor current i_{APF} and capacitor voltage v_{APF} are determined by the switching state of S_5 and S_6. L_{APF} is only for the energy transfer between DC link and C_{APF}, and the energy stored in L_{APF} is negligible. Therefore, pulsating power generated by the APF can be calculated as follows:

$$\begin{aligned} p_{APF} &= v_{APF} i_{APF} \\ &= v_{APF} C_{APF} \frac{\mathrm{d}v_{APF}}{\mathrm{d}t} \end{aligned} \tag{8}$$

Considering the APF generates a pulsating power at the double line frequency:

$$v_{APF} C_{APF} \frac{\mathrm{d}v_{APF}}{\mathrm{d}t} = P_{APF} \cos\left(2\omega t - \phi\right) \tag{9}$$

Integrating both sides of the equation yields:

$$\begin{aligned} \frac{C_{APF} v_{APF}^2}{2} &= E_0 + \frac{P_{APF}}{2\omega} \sin\left(2\omega t - \phi\right) \\ &= E_0 + E_{r,max} \sin\left(2\omega t - \phi\right) \end{aligned} \tag{10}$$

where E_0 is the capacitor energy in the initial state, $E_{r,max}$ is the amplitude of the second harmonic pulsating energy. When

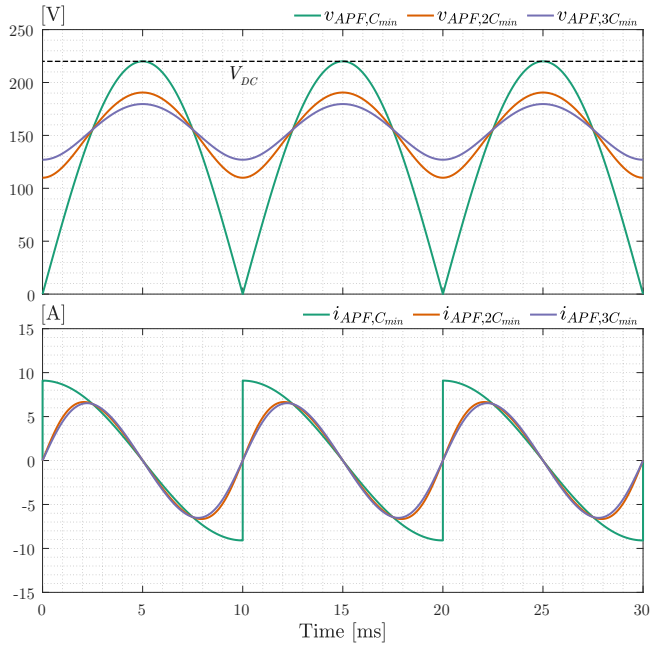


Fig. 8. The waveform of v_{APF} and i_{APF} with different capacitance value C_{APF} when buffering 1kVA pulsating power at 220V DC link voltage. The greater the capacitance C_{APF}, the more similar the waveforms are to sine waves.

the pulsating power is completely buffered by the APF, i.e $p_{APF} = p_{r,cell}$, the corresponding capacitor voltage can be derived as:

$$v_{APF} = \sqrt{V_{APF,avg}^2 - \frac{V_{AC} I_{AC}}{2\omega C_{APF} N_{cells}} \sin(2\omega t - \phi)} \quad (11)$$

where $V_{APF,avg} = \sqrt{2E_0/C_{APF}}$ is the capacitor voltage at the beginning of each cycle. As long as the pulsating power of the ISOP SST is determined, the reference voltage of each APF can be obtained by (11).

B. Parameter Design

During the operation of the APF, v_{APF} should always be above zero and lower than V_{DC}. Considering the energy storage capacity of C_{APF}, the following constraints can be obtained:

$$\begin{aligned} E_0 - E_{r,max} &> 0 \\ E_0 + E_{r,max} &< \frac{C_{APF} V_{DC}^2}{2} \end{aligned} \quad (12)$$

To maximize the power buffer capacity of the APF, E_0 should be half of the maximum energy of C_{APF}.

$$\begin{aligned} E_0 &= \frac{C_{APF} V_{DC}^2}{4} \\ V_{APF,avg} &= \frac{V_{DC}}{\sqrt{2}} \end{aligned} \quad (13)$$

The minimum required capacitance of the APF can be obtained where all the energy storage is utilized to buffer the pulsating power:

$$\begin{aligned} \frac{C_{APF,min} V_{DC}^2}{2} &= 2E_{r,max} \\ C_{APF,min} &= \frac{2P_{APF}}{\omega V_{DC}^2} \end{aligned} \quad (14)$$

For the work in this paper, the APF is designed to provide up to 1kVA ripple power compensation capability at a DC link voltage of 220V. According to (14), the minimum required capacitance is 131.5μF. Fig. 8 plots the waveform of capacitor voltage v_{APF} and current i_{APF} with C_{APF} equals $C_{APF,min}$, $2C_{APF,min}$ and $3C_{APF,min}$. When the minimum capacitance value is adopted, the capacitor is fully charged and discharged in every cycle. The voltage and current of the capacitor have large and sudden rates of change, which are difficult for the controller to track. As capacitance increases, the waveform gets similar to a sine wave, and APF's stability against sudden load change also increases. However, higher capacitance implies that energy storage is not fully utilized and the power density is low. In this research, C_{APF} is selected to be 360μF.

The inductor L_{APF} can operate in continuous conduction mode (CCM) or discontinuous conduction mode (DCM). In DCM, L_{APF} is very small, and the size of APF can be further reduced. However, the peak current of i_{APF} in DCM is high, and semiconductor devices with high current ratings are required. On the contrary, CCM reduces the stress on switches at the cost of reduced power density. This research aims to provide a reference for the design of MV SSTs where a high power and high current are processed. The disadvantage of high current stress in DCM is even more critical in such applications. Therefore, CCM is chosen as the operating mode of APF. In this research, L_{APF} is 200μH. Although LV SiC MOSFETs, which can operate at more than 100kHz, are adopted, the switching frequency of APF in this research is set to 10kHz to illustrate hard-switching HV SiC MOSFETs

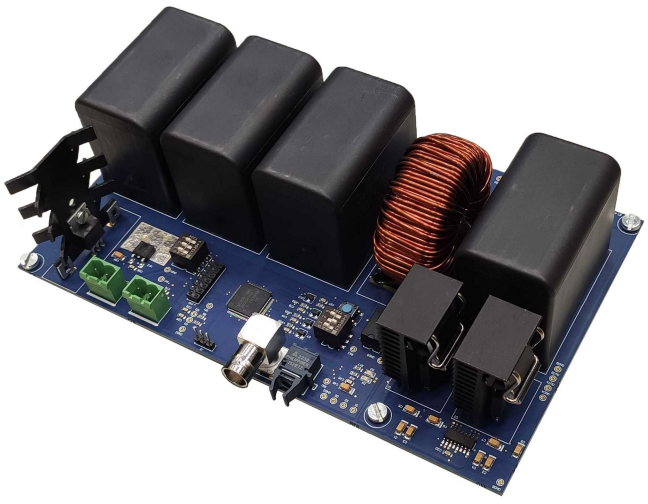


Fig. 9. The 1kVA buck-type APF prototype. Nine identical units are produced.

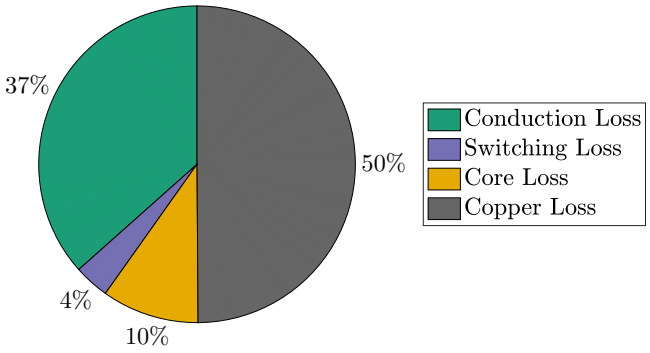


Fig. 10. The loss distribution of the APF.

in practical MV SSTs. The current ripple is limited to 50% at 10kHz switching frequency.

C. Hardware Implementation

Based on the above analysis, a 1kVA buck-type APF prototype is constructed, as illustrated in Fig 9. The APF has an energy storage capacitance of 360μF, which is composed of three Vishay MKT1820712255 250V/120μF metallized film capacitors. The connection between the APF and the MV side DC link capacitor of the SST contains a significant amount of stray inductance, causing voltage spikes on the switching devices. Therefore, an additional 120μF DC link capacitor, which is connected in parallel to the main DC link of the cell, is installed close to the switches to reduce the effect of the loop inductance. To achieve low core losses, the molypermalloy powder core 55439 from Magnetics is selected for the 200μH inductor. Two 650V/20A SiC MOSFET IMW65R039M1H from Infineon are selected for the switches S_5 and S_6. Based on the loss simulation of switching devices and inductor, an estimated efficiency of 99.19% is achieved when compensating 1kVA pulsating power, and the loss distribution is shown in Fig. 10. The volume of the APF prototype is 750cm^3, and only natural cooling is required. The control of the APF is implemented on a Texas Instruments TMS320F28069 MCU. Table II summarizes the key parameters of the buck-type APF.

TABLE II
PARAMETERS OF THE 1KVA BUCK-TYPE APF

Parameters		Value
Rated Power	P_{APF}	1kVA
DC Link Voltage	V_{DC}	220V
DC Link Capacitor	C_{DC}	120μF
APF Capacitor	C_{APF}	360μF
APF Inductor	L_{APF}	200μH
Average APF Voltage	$V_{APF,avg}$	155V
APF Switching Frequency	f_{APF}	10kHz

D. Control Method

Fig. 11 shows the control structure of the APF. To achieve a proper compensation of the pulsating power, the reference power p^*_{APF} and the corresponding reference voltage v^*_{APF} need to be calculated. The APF is equipped with a current sensor which measures the line current i_{AC}. Considering the SST operates at a unity power factor towards the grid, the line voltage v_{AC} is estimated to be in phase with i_{AC}, while its amplitude is known. Therefore, the reference voltage v^*_{APF} can be calculated from (11) relying solely on the line current measurement.

A cascaded closed-loop control scheme based on Proportional-Integral-Resonant (PIR) controllers is employed to regulate the capacitor voltage v_{APF}. As the selected value of C_{APF} is much larger than $C_{APF,min}$, the waveform of v_{APF} is close to a sine wave. A non-ideal Proportional-Resonant controller, which is synchronized to the double line frequency, is adopted to guarantee a zero steady-state error when tracking the distorted sinusoidal term of v^*_{APF}. An additional integral term is added to keep the average value of v_{APF} at $V_{APF,avg}$. The output of this controller is the

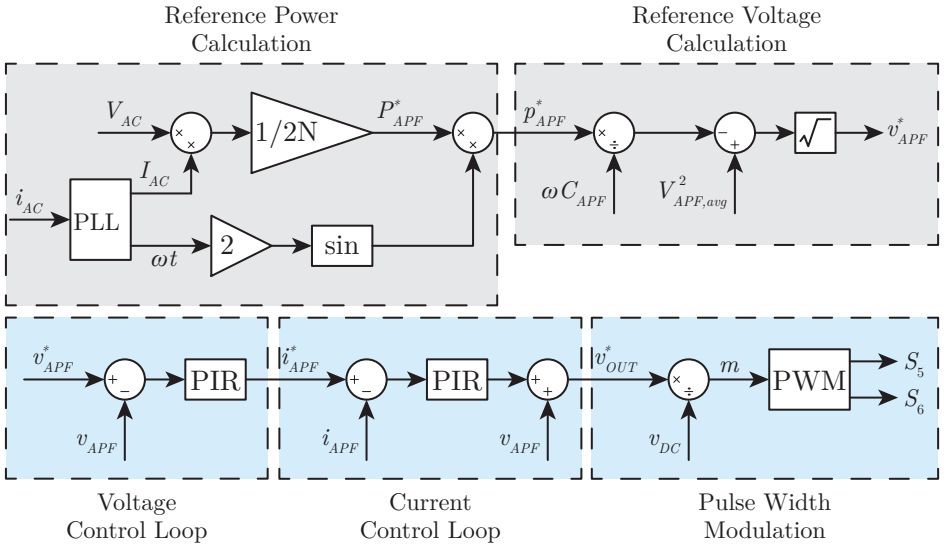


Fig. 11. Block diagram of APF's control algorithm.

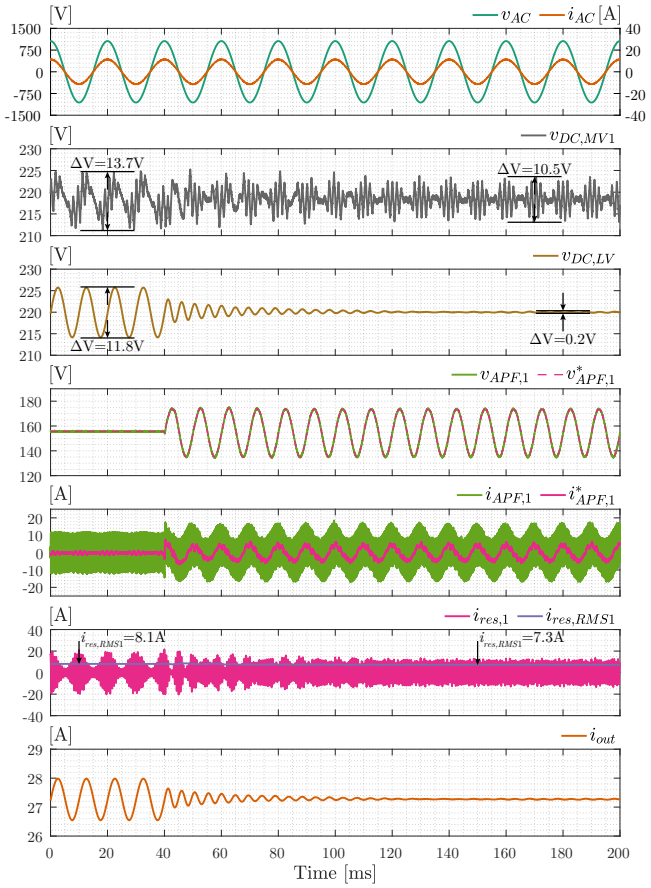
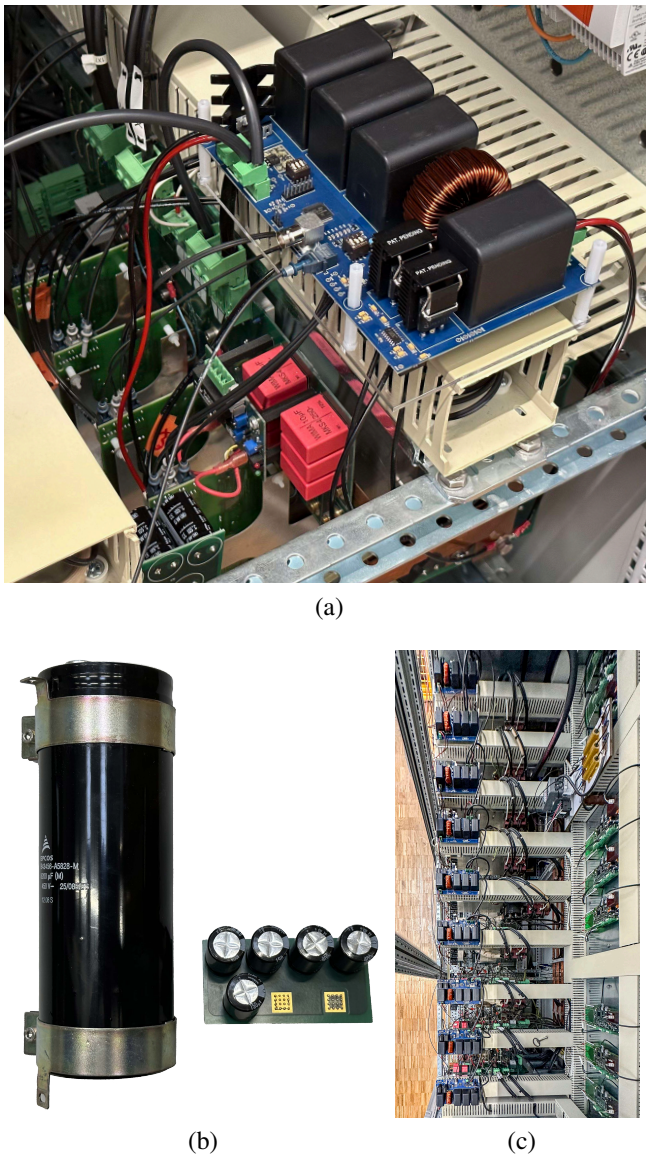


Fig. 12. Simulation result of the SST with APF installed. The APFs are activated at $t = 40$ms.



(a)

(b) (c)

Fig. 13. SST with APF installed: a) SST cell with APF b) Comparison of the original 8mF capacitor and the reduced 0.75mF capacitor. Each cell requires two identical capacitors connected in series. c) Top view of the nine cells with APF.

inductor reference current i^*_{APF}. Another PIR controller is implemented on the i_{APF}, and the measured v_{APF} is added to the controller output as a feed-forward term. The output of the inductor current controller is the reference output voltage of the half-bridge circuit v^*_{out}. A typical PWM is used where the duty cycle d is obtained by dividing v^*_{out} by v_{DC}, and the switching signal of S_5 and S_6 is generated by comparing d with a triangular carrier signal.

V. Simulations and Experiments

A. Simulation Results

The simulation model of the SST with APF installed is built in PLECS to verify the performance of the proposed APD method, and the waveform is provided in Fig. 12. Apart from a tiny difference caused by the phase shift operation of AFE and SRC, the waveforms of $v_{DC,MV}$, v_{APF}, i_{APF} and i_{res} from different cells are nearly identical. Therefore, only the waveforms from cell 1 $v_{DC,MV1}$, $v_{APF,1}$, $i_{APF,1}$ and $i_{res,1}$ are shown in the plot. Initially, the SST is operating at 6kW with reduced $C_{DC,MV}$. The second harmonic ripple voltage can be clearly observed on $v_{DC,MV1}$ and $v_{DC,LV}$, while the ripple voltage at the double switching frequency of APF only appears on $v_{DC,MV1}$. The reference voltage of the APF is $V_{APF,avg}$, and no pulsating power is generated.

At $t = 40$ms, the APFs are activated, and the reference of APF is switched to v^*_{APF}, which is calculated with (11) based on the line current measurement. Thanks to the cascaded PIR controller, the APF voltage $v_{APF,1}$ always tracks the reference value, while it takes around 100ms for the SST to reach a new steady state. The peak-to-peak amplitude of MV side DC link ripple voltage $\Delta V_{DC,MV1}$ is reduced from 13.7V to 10.5V as the switching frequency ripple voltage is dominating, and the APF is designed to suppress only the second harmonic ripple voltage. A significant reduction of $\Delta V_{DC,LV}$ from 11.8V to 0.2V is observed. The pulsating term of the envelope of resonant tank current $i_{res,1}$ is greatly reduced, and only a DC term remains. It shows that most of the pulsating power is buffered by the APF, and only the constant power can pass through the SRC. The ripple of the output current i_{out} is also

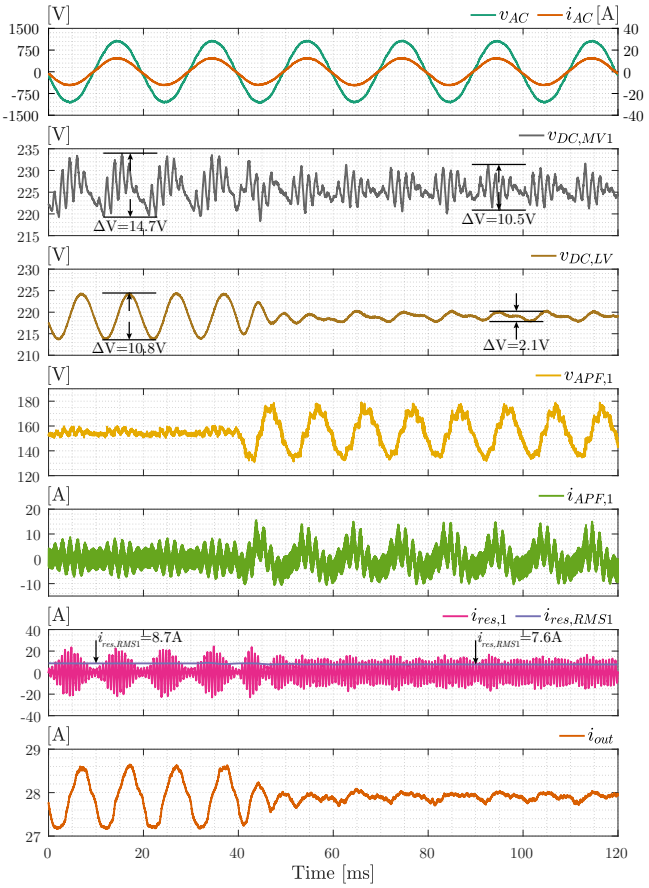


Fig. 14. Experimental result of the SST when APFs are enabled at $t = 40$ms.

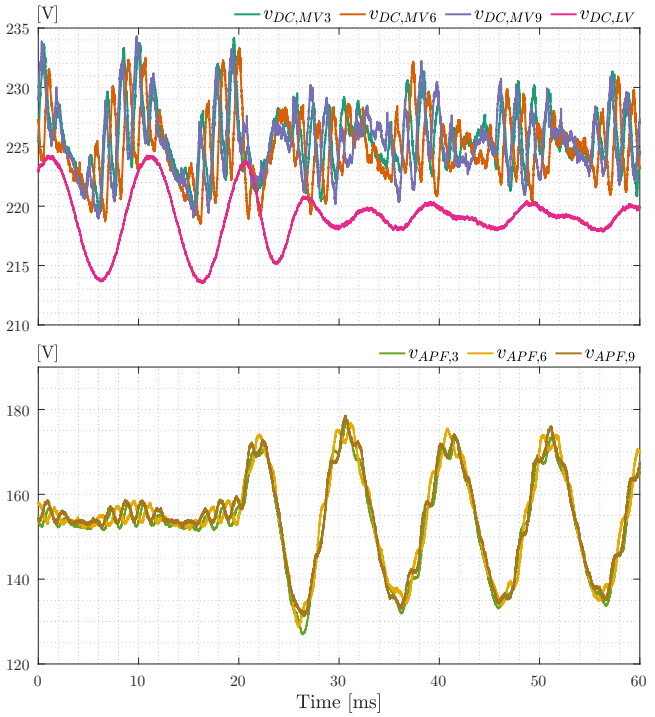


Fig. 15. The waveform of Cell 3, 6, and 9 of the SST when APFs are enabled $t = 20$ms.

significantly decreased, indicating an improved power quality.

B. Experimental Results

To verify the performance of the proposed APD method for ISOP SST, nine buck-type APFs are manufactured and installed on the MV side DC links of the SST. As shown in Fig. 13a, the APF is placed on the top of each cell. The APF obtains its auxiliary power from the gate power supply of the AFE, which ensures that the potential of the APF is the same as that of the AFE. The main circuit of APF is connected in parallel to the MV side DC link of the cell. An optical link is established to control the operation of APF. Fig. 13c gives the top view of all nine cells with APF inserted.

In the original configuration of the SST, two 8mF electrolytic capacitors are connected in series to form the MV side DC link capacitor of each cell, which occupies a volume of 2600cm^3. Taking into account the 2.2mF LV side DC link capacitor, the overall installed capacitance is 56mF. With the installation of APF, the capacitance can be reduced as the constraint of ripple voltage level is lifted. In the new configuration, two 0.75mF electrolytic capacitors are adopted as the new MV side DC link capacitor. The size of the new capacitors is only 170cm^3, and Fig. 13b shows the comparison of old and new capacitors. The 2.2mF LV side DC link capacitor is also reduced to 0.55mF. The total installed capacitance of the SST is reduced to 8.4mF, which is an 85% reduction. Even considering the 750cm^3 additional volume from the APF, a 67.8% volume reduction of the overall DC link capacitor is still achieved in the new configuration.

Fig. 14 depicts the transient of the SST when APFs are enabled. In the first 40ms, the APFs are disabled. Due to the reduced DC link capacitance in the system, $\Delta V_{DC,MV1}$ reaches 14.7V, while $\Delta V_{DC,LV}$ is 10.8V. At $t = 40$ms, the APFs are enabled with the capacitor voltage $v_{APF,1}$ regulated to the computed reference value. The second harmonic voltage ripple is gradually reduced and finally neutralized in 20ms. A 10.5V ripple voltage at the double switching frequency of AFE still remains on the MV side DC link, while $\Delta V_{DC,LV}$ is greatly decreased to 2.1V. The presence of residual ripple voltage on the DC link indicates an incomplete pulsating power compensation. The error is mainly due to control error, mismatch of parameters, and the reactive power contribution of grid filters. The double switching frequency ripple voltage on the MV side DC link is propagated to the APF due to the low control bandwidth, yet it does not influence the pulsating power compensation capability of the APF.

Fig. 15 gives the transient of Cell 3, 6, and 9 of the SST when APFs are enabled. Due to the equal power sharing between cells and the synchronous operation of all nine APF, the waveforms of three cells are almost the same, despite the slight difference in the phase of double switching frequency ripple due to the phase shift operation of AFE.

Fig. 16 gives the FFT analysis of the DC link voltage. With the pulsating power buffered by APF, the second harmonic component of the MV side DC link voltage is reduced from 3.79V to 0.61V, while the double switching frequency components remain unaffected. A reduction from 5.22V to 0.83V

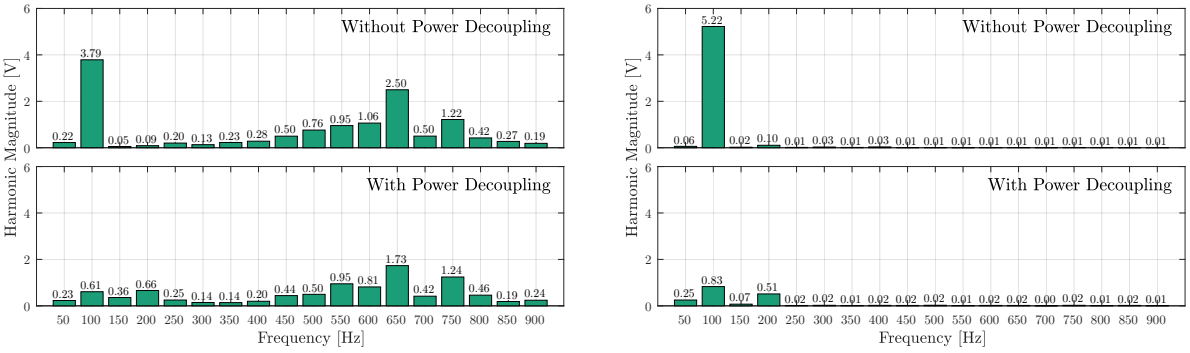


Fig. 16. FFT analysis of the DC link voltage: a) MV side DC link b) LV side DC link.

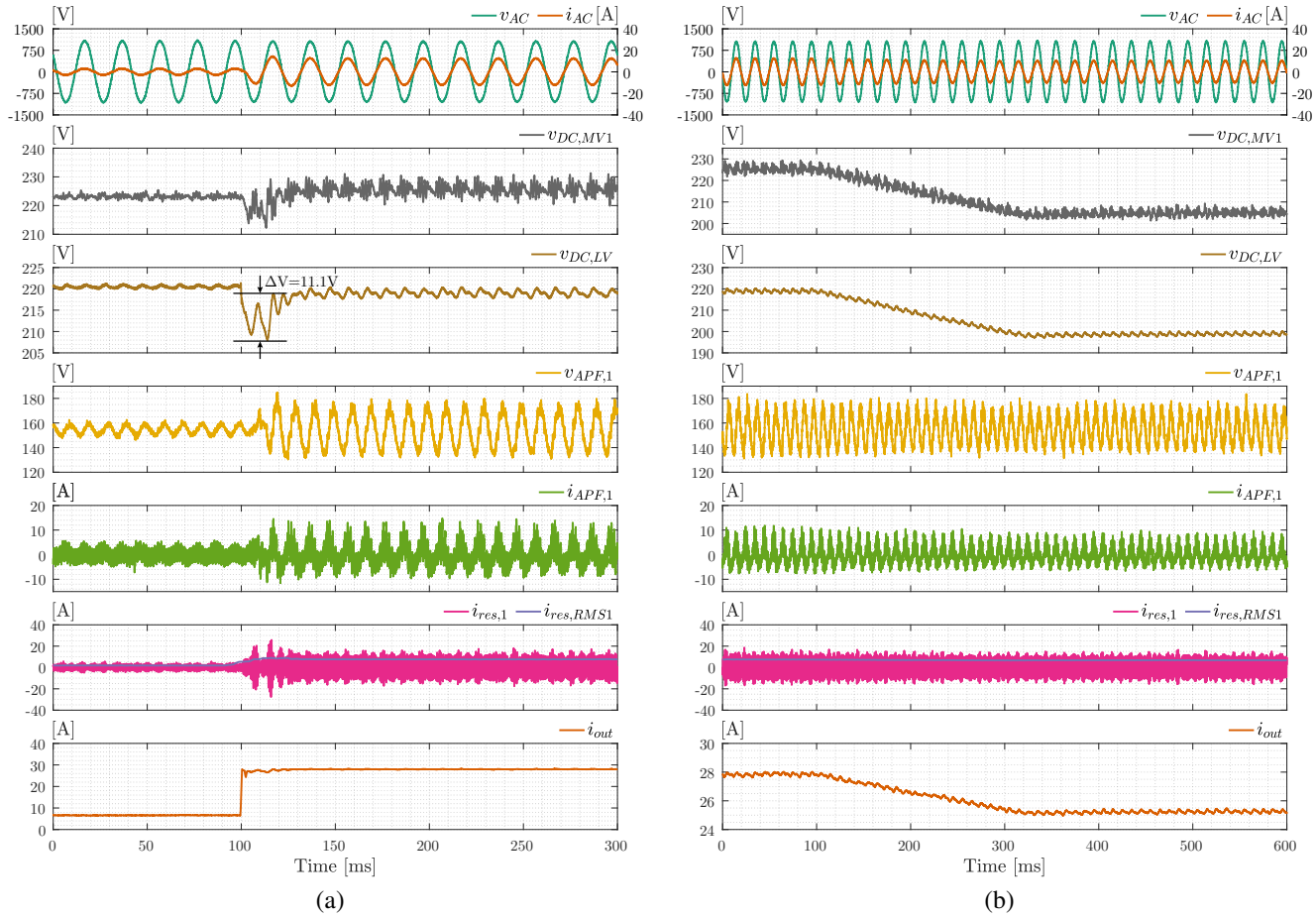


Fig. 17. Dynamic response of the SST with APF installed: a) load step change from 1.5kW to 6kW at $t = 100$ms b) reference voltage step change from 220V to 200V at $t = 100$ms.

can be observed on the LV side DC link voltage.

Fig. 17 shows the dynamic response of the SST with APF installed. The overall dynamic response is determined by the controller of the SST, while the APF acts faster and can always compensate for the pulsating power based on the line current measurement. In Fig. 17a, a load step change from 1.5kW to 6kW is applied to the SST, which results in a change of the line current and second harmonic ripple voltage. During the load change, $\Delta V_{DC,LV}$ increases up to 11.1V, but it is reduced to 2.1V after 40ms. In Fig. 17b, a reference voltage step change from 220V to 200V is applied. As this change is relatively moderate, the APF can always buffer the pulsating power and suppress the second harmonic ripple voltage.

C. Discussions

Table III gives the performance evaluation of the SST under three different conditions. The base case, which is the original configuration of the SST, achieved a relatively low DC link ripple voltage with bulky capacitors. By reducing the DC link capacitance, the power density of the SST increases while the

TABLE III
PERFORMANCE EVALUATION OF THE SST WITH APD

Parameters		**Original SST**	**SST with Reduced DC Link Capacitance**	**SST with APD and Reduced DC Link Capacitance**
MV side DC Link Ripple Voltage	$\Delta V_{DC,MV}$	5.4V	14.7V	10.5V
LV side DC Link Ripple Voltage	$\Delta V_{DC,LV}$	2.5V	10.8V	2.1V
MV side DC Link Capacitance	$C_{DC,MV}$	4mF	0.375mF	0.375mF
LV side DC Link Capacitance	$C_{DC,LV}$	2.2mF	0.55mF	0.55mF
Overall DC Link Capacitance	C_{total}	56mF	8.4mF	8.4mF
Volume of DC Link Capacitors	$V_{C_{DC}}$	33800cm^3	4130cm^3	10880cm^3 (with APF)
Influence on Overall Efficiency	$\Delta\eta$	0	-0.53%	-0.74%

second harmonic ripple voltage reaches an unacceptable level. With the help of the APD method, the SST can achieve both low DC link ripple voltage and high power density. Compared to the base case, the SST with APD can achieve an 85% reduction in the overall capacitance, a 67.8% reduction in the size of DC link capacitors, and a 16% reduction in the output ripple voltage. In practical SST demonstrators, the DC link capacitors may occupy around 30% of the total volume [7], [36], and the reduction of the DC link capacitance, thanks to the APD, may lead to a significant improvement in the power density.

Fig. 18 shows the efficiency plot of the SST with and without the APD method and reduced DC link capacitance. The efficiency of the original SST at 6kW is 92.92%. This is because the SST research platform in this paper is developed solely for the verification of control and topology rather than demonstrating the performance of SST. With reduced DC link capacitance, the transfer characteristic of the second harmonic pulsating power is changed [41], leading to higher current stress and a lower efficiency of 92.39%. The APFs introduce additional loss to the SST when they are active. However, they also reduce the current stress of the SST, which in return improves the efficiency of the SST. As shown in Fig. 14, the RMS value of i_{res} is reduced from 8.7A to 7.6A after the activation of APF. These two effects compensate for each other, and the overall efficiency is only reduced by 0.21% compared to the case with reduced DC link capacitance but APF disabled. It is worth noting that the benefit of APD also comes at the cost of two more active switches and the passive components of APF.

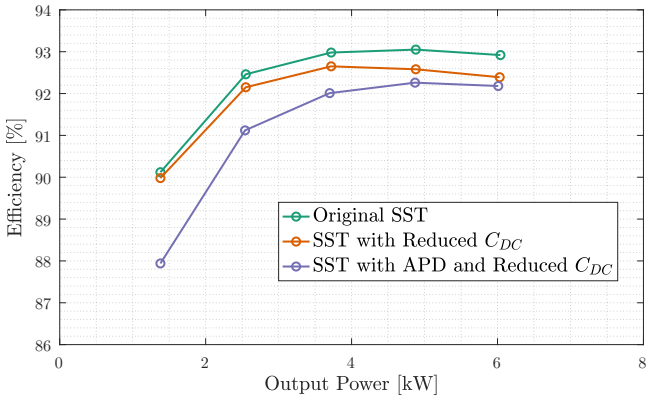


Fig. 18. Efficiency of the SST with and without the APD method and reduced DC link capacitance.

VI. CONCLUSION

Single-phase ISOP SST suffers from the second harmonic pulsating power from the AC grid. In this paper, the APD technology, where the bulky DC link capacitor is replaced by a much smaller capacitor and APF, is applied to ISOP SST to suppress the second harmonic ripple on the DC link voltage. The second harmonic pulsating power flow and the resulting ripple voltage in the ISOP SST are analyzed, and a modified ISOP SST cell with buck-type APF is proposed. The operating principle, parameter design, hardware implementation, and control method of the buck-type APF are demonstrated. Simulation results show that the APF can significantly reduce the SST's second harmonic ripple voltage and total DC link capacitance. Nine APFs are installed in each cell of an ISOP SST research platform, and the experimental results prove the feasibility and benefits of the proposed APD method. This paper provides a solution for ISOP SST where a high power density is required.

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