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Optimization of DC-Link Capacitance for Single-Phase ISOP SST Considering the Second Harmonic Pulsating Power in LLC Converter

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***Abstract*—In solid-state transformers with input-series output-parallel configuration, the LLC converter operating at a fixed switching frequency is one of the solutions for the isolated DC/DC conversion stage to provide a fixed voltage gain with galvanic isolation. However, in single-phase AC/DC conversion, the pulsating power at the double line frequency will propagate through the LLC converter, causing increased current stress and ripple voltages. This paper studies the pulsating power transfer behavior of LLC converters with a passive equivalent circuit model. The conclusion indicates that the primary and secondary side DC link capacitors can participate differently in buffering the pulsating power with different DC link designs. Furthermore, an inappropriate design may cause an excessive harmonic power transfer, discontinuities in resonant operation, and reduced overall efficiency. Simulations and measurements of a two-stage solid-state transformer verify the analysis. The guideline for DC link design of similar applications is provided.**

***Index Terms*—solid-state transformer, LLC converter, second harmonic current, passive equivalent circuit.**

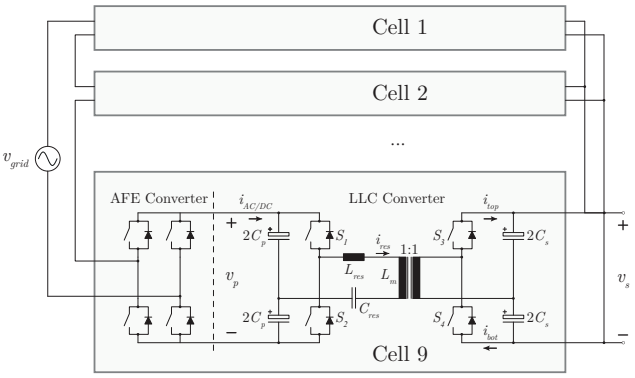

Fig. 1. Solid-state transformer with input-series output-parallel structure. The detailed circuit diagram of the SST cell is shown.

I. Introduction

The solid-state transformer (SST) is a technology that has potential in many fields, including traction systems, renewable energy, data centers, and smart grids [1]–[8]. MVAC to LVDC conversion is one of the typical SST applications. Due to the high input voltage, the input-series output-parallel (ISOP) structure is typically employed.

As shown in Fig. 1, the ISOP SST contains several cells that are connected in series at their MVAC terminals and in parallel at their LVDC terminals, which achieves the high step-down AC to DC conversion. The cells can be considered as independent two-stage AC/DC converters, which are composed of an active front end (AFE) converter for AC/DC conversion and a DC/DC converter that provides galvanic isolation and voltage matching [9]. In the ISOP structure, each cell's power rating is greatly reduced, and the input voltage rating can be easily expanded by increasing the number of cells.

The LLC resonant converter can provide DC/DC conversion with galvanic isolation. It also enables the zero-voltage switching of primary side active switches as well as zero-current switching of secondary side rectifier diodes [10]. When adopted as the isolated DC/DC converters in SST cells, the LLC converter is typically operated in open-loop modulation with a fixed 50% duty cycle. The switching frequency is fixed and slightly lower than the resonant frequency. In this scenario, the LLC converter offers a load-independent voltage transfer characteristic [11] and acts as a "DC transformer", while the AFE converter regulates the output voltage and power [12].

For single-phase ISOP SSTs, the instantaneous power from the grid contains pulsating components at the double line frequency [13]. Due to the open-loop operation, the pulsating power inevitably propagates through the LLC converter, which increases the current stress of components and causes second harmonic ripple voltages on both the primary and secondary side DC links. In typical single-stage AC/DC converters, a bulk DC link capacitor is typically installed to buffer the pulsating power and limit the ripple voltage. Considering that the DC link capacitor buffers all the pulsating power, the design of DC link capacitors follows a simple rule: the required capacitance is inversely proportional to ripple voltage amplitude. However, this rule cannot be adopted in ISOP SSTs with the LLC converter installed as a second stage, as the coupling of two DC link capacitors with the LLC converter should be considered.

So far, the research on the propagation of second harmonic pulsating power in LLC converters and the corresponding

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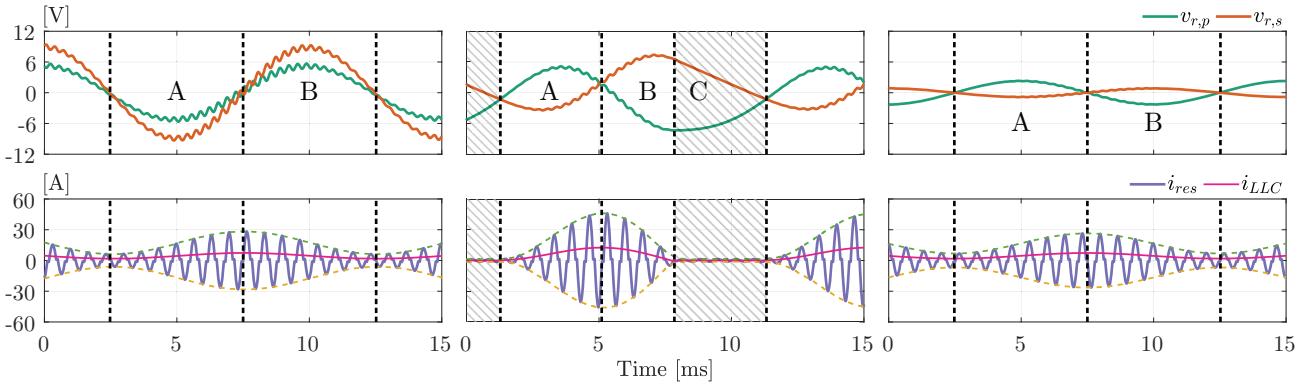


(a) $C_p = C_s = 0.5$mF, IPCRM (b) $C_p = C_s = 2$mF, DRM (c) $C_p = C_s = 5$mF, APCRM

Fig. 2. Simulation waveform of the LLC converter with different DC link capacitance.

design rules of DC link capacitors is very limited. The power flow of a three-phase solid-state transformer (SST) is analyzed in [14]. Although each SST cell processes single-phase power, the secondary side DC link capacitance can be approximated as being infinite as the pulsating power from three phases adds up to zero. Therefore, the conclusions of [14] cannot be generalized to the single-phase scenario. The small signal model of second harmonic components in LLC converters is provided in [15], and multiple DC link designs are compared in [16]. Yet, these two studies focus on control, efficiency, and reliability, while detailed modeling and analysis of the second harmonic components are still missing.

This paper analyzes the behavior of second harmonic components in LLC converters using a passive equivalent circuit. The equivalent inductance of the LLC converter and two DC link capacitors forms a CLC resonant circuit, of which the resonant frequency determines the pulsating power transfer. The primary and secondary side DC link capacitors can participate differently in buffering the pulsating power with different DC link designs. An inappropriate parameter design may cause an excessive power transfer and discontinuities in resonant operation, leading to a reduced SST efficiency. Simulations and measurements of a two-stage ISOP SST verify the analysis. This paper provides a guideline for the parameter design of similar applications where LLC converters interface an AC/DC converter.

II. Three Operating Modes of LLC Converters when Transferring Pulsating Power

In typical ISOP SSTs, the parameters and modulation index of different cells are identical, and the power flow of the SST is evenly distributed to all cells. Therefore, the analysis of the pulsating power on a single cell can be generalized to the entire SST. Fig. 2 shows the simulation waveform of an LLC converter connected to an AC/DC converter, which is identical to an SST cell. The parameters of the SST cell are provided in Table I. Three different values of the primary and secondary side DC link capacitors C_p and C_s are analyzed.

TABLE I
Parameters of the SST cell

DC Voltage V_{DC}	220V	Load Impedance Z_L	50Ω
Resonant Ind. L_{res}	135μH	Resonant Cap. C_{res}	60μF
Magnetizing Ind. L_m	13mH	Turns Ratio n	1
Switching Freq. f_s	1500Hz	Resonant Freq. f_{res}	1768Hz
DC Cap. C_p, C_s	0.5-6mF	Equivalent Ind. L_{eq}	1.85mH

With $C_p = C_s = 0.5$mF, the primary and secondary side DC link ripple voltage $v_{r,p}$ and $v_{r,s}$ are in-phase in Fig. 2a. Due to the propagation of pulsating power in the LLC converter, the waveform of the resonant current i_{res} is similar to a sinusoidal carrier wave at the switching frequency f_s with its amplitude modulated by a sinusoidal signal at the double line frequency $2f_g$. With C_p and C_s increased to 4mF in Fig. 2c, $v_{r,p}$ and $v_{r,s}$ are anti-phase. Based on the shape of i_{res} and the phase relationship between $v_{r,p}$ and $v_{r,s}$, the operating mode of the LLC converter in Fig. 2a is referred to as In-Phase Continuous Resonant Mode (IPCRM), while the case in Fig. 2c is referred to as Anti-Phase Continuous Resonant Mode (APCRM). Both two cases are collectively referred to as Continuous Resonant Mode (CRM).

However, with $C_p = C_s = 2$mF, the LLC converter exhibits a special working mode. As shown in Fig. 2b, there exist significant distortions in $v_{r,p}$ and $v_{r,s}$. In every cycle of the double line frequency, there exists a time interval, which is marked as shaded, where i_{res} is very low and dominated by the transformer's magnetizing current. As the secondary side current is zero, no power is transferred through the LLC converter. This phenomenon is referred to as the Discontinuous Resonant Mode (DRM) of LLC converters.

The three operating modes of the LLC converter are essentially determined by the transmission pattern of the second harmonic pulsating power. The ripple voltage and efficiency of the entire SST are closely related to the operating mode of LLC converter. The mathematical analysis of the three operating modes is given next.

III. Modeling of Second Harmonic Components in LLC Converters

By neglecting the losses and reactive power of the grid filter, the output current of the AFE converter i_{AFE} can be derived from the input AC voltage of each cell $v_{AC} = v_{grid}/N_{cells}$ and current i_{AC}:

$$\begin{aligned} i_{AFE} &= \frac{v_{AC} i_{AC}}{V_{DC}} = \frac{V_{AC} \sin(\omega t) I_{AC} \sin(\omega t - \phi)}{V_{DC}} \\ &= \frac{V_{AC} I_{AC}}{2V_{DC}} \cos\phi - \frac{V_{AC} I_{AC}}{2V_{DC}} \cos(2\omega t - \phi) \\ &= I_{DC} + i_r \end{aligned} \tag{1}$$

where V_{AC} and I_{AC} represent the amplitude of the input voltage and current, respectively. ϕ is the phase angle between the input voltage and current. ω is the angular frequency of the grid. I_{DC} is the DC component of i_{AFE}. i_r is the second harmonic ripple current from the grid, and its amplitude I_r is equal to I_{DC} at a unity power factor.

The LLC converter of the SST cell discussed in this paper is shown in Fig. 1. A half-bridge configuration with split DC link capacitors is adopted to reduce the number of devices. However, the following analysis can easily adapt to full-bridge or single-capacitor configurations. A passive equivalent model is introduced in [17] to describe the dynamic behavior of LLC converters. Fig. 3 shows the equivalent model of a simplified case where a 1:1 turns ratio is adopted, and all of the resistance and voltage drops in the current path are neglected.

In the equivalent circuit, the AFE converter is replaced by a current source i_{AFE}. The primary and secondary side voltages are $v_p \approx v_{r,p} + V_{DC}$ and $v_s \approx v_{r,s} + V_{DC}$. The equivalent capacitance C_p and C_s is equal to the total capacitance of two split capacitors. The second harmonic ripple currents flow through the DC link capacitors are $i_{r,p}$ and $i_{r,s}$. Z_L is the impedance of the load. This work considers a simplified case where Z_L is purely resistive. Therefore, the harmonic component of the load current $i_{r,L}$ is negligible.

The equivalent inductance L_{eq} is derived using the averaged piecewise sinusoidal current [17], which can be written as:

$$L_{eq} = L_{res} \left(\frac{\pi f_{res}}{f_s} \right)^2 \tag{2}$$

where $f_{res} = 1/\left(2\pi\sqrt{L_{res}C_{res}}\right)$ is the resonant frequency, L_{res} is the resonant inductance, and f_s is the switching

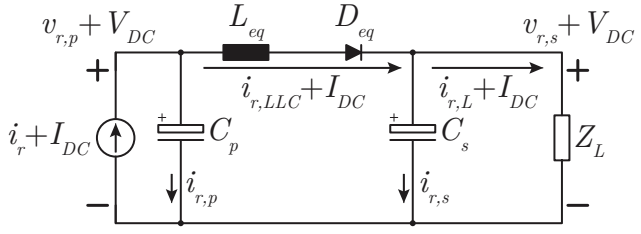


Fig. 3. Lossless passive equivalent model of the SST cell using LLC converter as the isolated DC/DC stage.

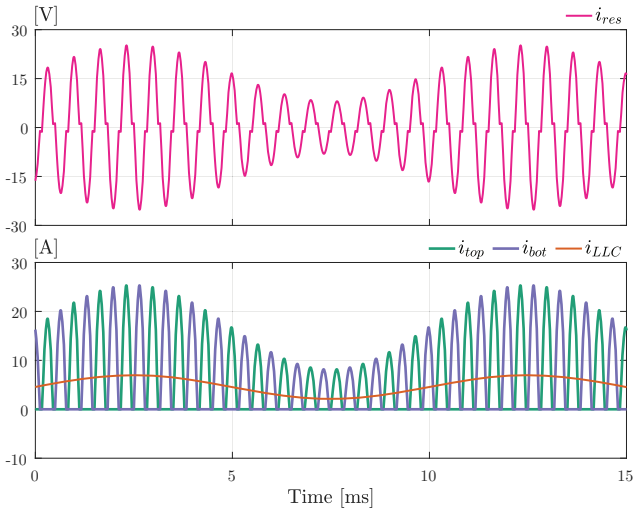


Fig. 4. The waveform of i_{res}, i_{top}, i_{bot}, and i_{LLC}.

frequency. For LLC converters without the split capacitor configuration, L_{eq} needs to be scaled down by a factor of 4, while the rest of the analysis remains the same.

The resonant current i_{res} is rectified by the anti-parallel diodes of S_3 and S_4 on the secondary side. The positive and negative parts of i_{res} are i_{top} and i_{bot}, respectively. i_{LLC} is the average value of i_{top} or i_{bot} in a switching cycle, which can be expressed as:

$$i_{LLC} = \bar{i}_{top} = \bar{i}_{bot} = I_{DC,LLC} + i_{r,LLC} \tag{3}$$

where $I_{DC,LLC}$ and $i_{r,LLC}$ are the DC component and second harmonic component of i_{LLC}. Considering a lossless power transfer, I_{DC} is equal to $I_{DC,LLC}$. Fig. 4 illustrates the waveform of i_{res}, i_{top}, i_{bot}, and i_{LLC}.

When f_s is close to f_{res}, the DC gain of the LLC converter is close to 1 [9], and $V_{DC} \approx V_p \approx V_s$, where V_p and V_s are the averaged primary and secondary side voltage. With large DC link capacitance, the DC link ripple voltage is very low. Therefore, the power transfer of the LLC converter can be approximated as:

$$p_{LLC} \approx V_{DC} i_{LLC} \tag{4}$$

Often, in LLC converters, only the switches on one side are active while the switches on the other side remain off, which realizes a unidirectional power transfer. In this paper, the power transfer direction remains unchanged in one AC cycle, and a power transfer from the primary side to the secondary side is considered. In the equivalent model proposed in [17], the diode D_{eq} only represents the voltage drop in the current path. In this paper, D_{eq} also denotes that the LLC converter can only transfer power in one direction. When the amplitude of the second harmonic ripple current $I_{r,LLC}$ is lower than $I_{DC,LLC}$:

$$I_{r,LLC} < I_{DC,LLC} \quad \text{and} \quad i_{LLC} > 0 \tag{5}$$

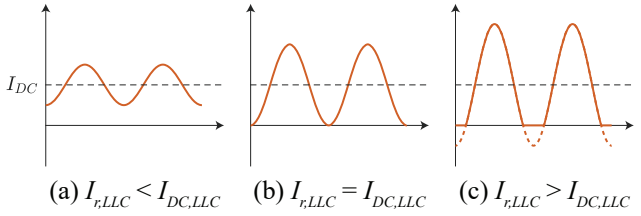


Fig. 5. The waveform of i_{LLC} with different relationship between $I_{r,LLC}$ and $I_{DC,LLC}$.

i_{LLC} is always above zero and D_{eq} remains conducting. This leads to the CRM of LLC converters. On the contrary, if (5) does not hold, there will be time intervals when D_{eq} is in the blocking state, leading to the DRM. Fig. 5 shows the waveform of i_{LLC} with different relationship between $I_{r,LLC}$ and $I_{DC,LLC}$.

IV. Propagation of the Second Harmonic Pulsating Power in LLC Converter

Suppose the relation in (5) holds, D_{eq} is always conducting, and the LLC converter with DC link capacitors can be simplified as a CLC circuit with a resonant frequency of $f_{CLC} = \sqrt{(C_p + C_s) / (L_{eq} C_p C_s)}/2\pi$. The transfer function between the input ripple current $i_r(s)$ and $i_{r,LLC}(s)$ is:

$$G_r(s) = \frac{i_{r,LLC}(s)}{i_r(s)} = \frac{1}{1 + \dfrac{sC_pZ_L}{1 + sC_sZ_L} + s^2 L_{eq} C_p} \tag{6}$$

Fig. 6 shows the Bode plot of $G_r(s)$ based on the parameters provided in Table I, with different DC link capacitance corresponds to the three cases in Fig. 2. C_p and C_s are the same in the following analysis.

The Bode plot shows that $G_r(s)$ contains two gain crossover frequencies at f_1 and f_2. In a 50Hz AC grid, the frequency of the second harmonic components $2f_g$ is 100Hz. By adjusting the capacitors C_p and C_s, the Bode plot can be shifted horizontally, and its relative position to $2f_g$ can be moved, leading to different behavior of second harmonic components in the system. When $2f_g < f_1$ or $2f_g > f_1$, the magnitude of the transfer function $|G_r(s)|$ at $2f_g$ is lower than 1, and the

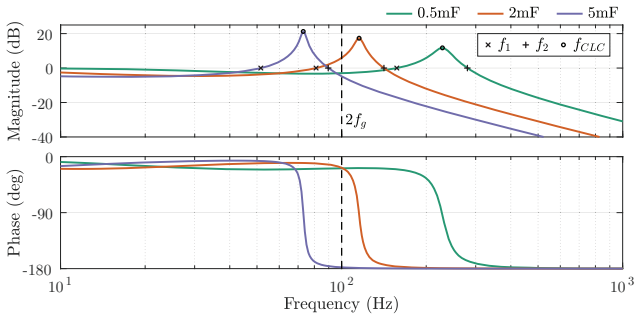


Fig. 6. Bode plot of the transfer function $G_r(s)$, with different DC link capacitance corresponds to the three cases in Fig. 2.

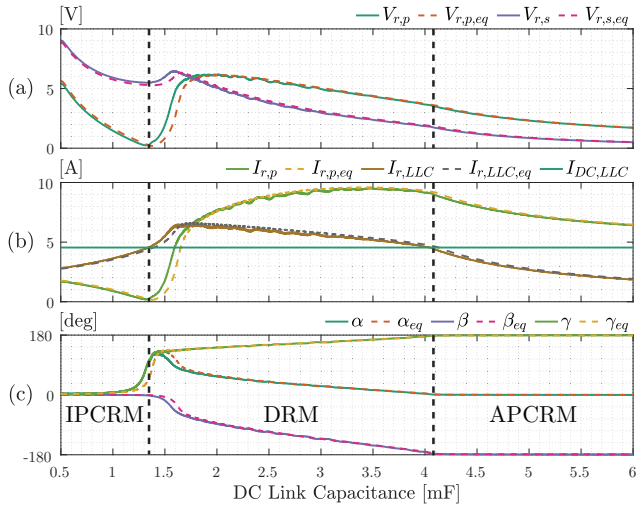


Fig. 7. The second harmonic components in the system with different DC link capacitance, obtained from the switched model simulations (solid lines) and equivalent model (dashed lines), respectively. a) Amplitude of second harmonic ripple voltages. b) Amplitude of the second harmonic ripple currents. c) The angle between phasor $\boldsymbol{I_{r,p}}$, $\boldsymbol{I_{r,LLC}}$ and $\boldsymbol{I_r}$.

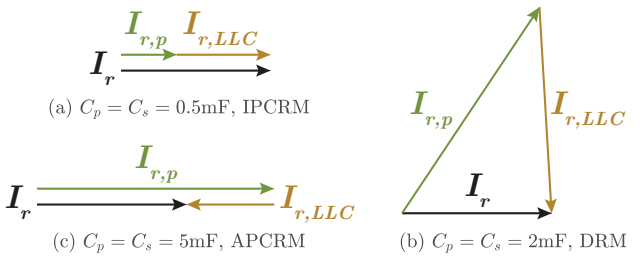


Fig. 8. Phasor diagram of $\boldsymbol{I_r}$, $\boldsymbol{I_{r,p}}$ and $\boldsymbol{I_{r,LLC}}$, with different DC link capacitance corresponds to the three cases in Fig. 2.

relation in (5) holds. However, if $2f_g$ is located between f_1 and f_2, $|G_r(s)|$ at $2f_g$ is higher than 1, and the relation in (5) no longer holds. $G_r(s)$ cannot be calculated with (6) because the reverse blocking of diode D_{eq} should be considered.

Fig. 7 shows the second harmonic components in the system with different DC link capacitance. The solid lines represent values obtained from the switched model simulations in PLECS, while the dashed lines represent values obtained from the equivalent model in Fig. 3. Results indicate that the equivalent model matches the simulation model closely. The amplitude of the DC link ripple voltage on both sides are $V_{r,p}$ and $V_{r,s}$. The ripple current amplitude of primary side DC link capacitors is $I_{r,p}$. The angle between phasor $\boldsymbol{I_{r,p}}$ and $\boldsymbol{I_r}$ is

TABLE II
Boundary Conditions of Different Operating Modes

Operating Mode	Condition	Characteristic
IPCRM	$2f_g < f_1$	$I_{r,LLC} < I_{DC,LLC}$ and $\gamma < 90°$
DRM	$f_1 < 2f_g < f_2$	$I_{r,LLC} > I_{DC,LLC}$
APCRM	$2f_g > f_2$	$I_{r,LLC} < I_{DC,LLC}$ and $\gamma > 90°$

α, while the angle between $\boldsymbol{I_{r,LLC}}$ and $\boldsymbol{I_r}$ is β. The angle between $\boldsymbol{I_{r,p}}$ and $\boldsymbol{I_{r,LLC}}$ is γ, which is almost equal to the angle between $\boldsymbol{V_{r,p}}$ and $\boldsymbol{V_{r,s}}$ when Z_L is resistive. Fig. 2 gives the detailed waveform with $C_p = C_s = (0.5, 2, 5)\,\mathrm{mF}$, while Fig. 8 gives the corresponding phasor diagram. The operating modes of LLC converters are divided into IPCRM, DRM, and APCRM, with boundary conditions given in Table II.

In IPCRM, the small DC link capacitance leads to $2f_g < f_1$. $i_{r,p}$, $i_{r,LLC}$ and i_r are almost in the same phase with $\beta \approx 0°$. The pulsating power is buffered by both DC link capacitors, that is $I_{r,p} + I_{r,LLC} \approx I_r$. In APCRM, the large DC link capacitance leads to $2f_g > f_2$. $i_{r,p}$ and i_r are still in the same phase with $\alpha \approx 0°$, while $i_{r,LLC}$ and i_r have opposite phases with $\beta \approx 180°$. The pulsating power is buffered by C_p only, while C_s generates additional pulsating power, which is $I_{r,p} - I_{r,LLC} \approx I_r$. In both cases, the LLC converter is operating at CRM where $I_{r,LLC} < I_r = I_{DC,LLC}$.

Fig. 2a and 2c give the waveform of IPCRM and APCRM. When $v_{r,p} > v_{r,s}$, which is the area A, i_{LLC} and the peak value of i_{res} increase, which represents an increased instantaneous power. On the contrary, the transferred power reduces in area B where $v_{r,p} < v_{r,s}$. As the waveform is symmetrical, the size of area A and B is the same.

In DRM, $2f_g$ is located between f_1 and f_2. Due to the resonant between DC link capacitors and LLC converter, an excessive ripple power transfer happens where $I_{r,LLC} > I_r = I_{DC,LLC}$. When considering the CLC resonant only, i_{LLC} may be less than zero. Yet, i_{LLC} is actually clamped above zero as the LLC converter cannot transfer a reversed power without changing active switches. The clamping effect is modeled through D_{eq}. Fig. 2b gives the waveform of DRM. Similar to the above analysis, i_{LLC} increases from zero to peak in area A, and reduces back to zero in area B. In area C, $v_{r,p}$ is still lower than $v_{r,s}$. However, i_{LLC} has already reached zero and cannot be further reduced. Although the primary side switches are still active, the operation of the LLC converter is suspended. i_{res} is dominated by the magnetizing inductance L_m, and no power is transferred to the secondary side.

In the above analysis, a unity power factor is considered. If the power factor is less than 1, the boundary of DRM is expanded as $I_r > I_{DC}$. Also, the location of f_1 and f_2 is determined by not only C_p, C_s and L_{eq}, but also Z_L, which indicates that the operating mode of the LLC converter is influenced by the load as well.

To optimize the utilization of DC link capacitors, the LLC converter preferably operates in IPCRM, where both C_p and C_s participate in buffering the second harmonic pulsating power. This can be achieved in practice by reducing C_p and C_s, which guarantees $2f_g < f_1$ for all possible operating conditions. According to (2), L_{res} should be minimized to expand the range of IPCRM.

If $2f_g < f_1$ cannot be guaranteed, the LLC converter can still be designed to operate in APCRM rather than DRM to achieve a higher efficiency. This requires large C_p and C_s to make sure $2f_g > f_2$.

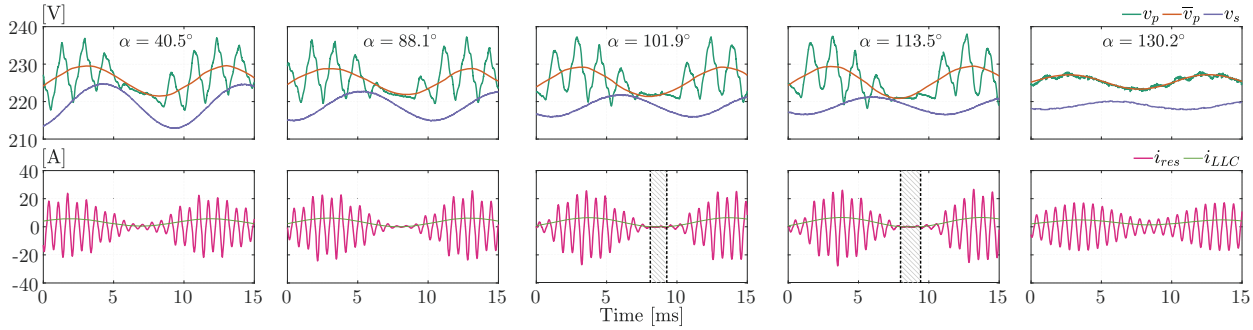
V. Experimental Verification

The analysis of this paper is verified by experiments on the low voltage prototype of the power electronic traction transformer (LV PETT), which is described in [5]. The LV PETT was originally developed by ABB as an analog simulator with modest power ratings for control hardware and software verification of a corresponding medium voltage prototype, named MV PETT [6]. It was generously donated to the Power Electronics Laboratory of EPFL by Hitachi Energy (former ABB) and now serves as an SST research platform.

Fig. 9 shows the LV PETT, while its topology is presented in Fig. 1. The parameters of SST cells are given in Table I. Fig. 10 shows the waveform of Cell 1 when LV PETT is connected to a 6kW resistive load with different C_{DC}. Due to the low switching frequency of AFE (317Hz), significant ripple can be observed in v_p, and a filtered waveform $\overline{v}_p$ is provided to highlight the second harmonic components. The switching frequency ripple in v_s is minor thanks to the phase-shift operation.

With the lowest capacitance in Fig. 10a, the LLC converter is in IPCRM. By increasing C_s in Fig. 10b, 10c and 10d, the LLC converter enters DRM, and the gap area of i_{res} increases. Fig. 10e shows the waveform with the highest capacitance. There is no interruption in i_{res}, while v_p and v_s are almost in anti-phase, indicating that the LLC converter is in APCRM. Compared to the simulation result, γ is not exactly $0°$ in IPCRM or $180°$ in APCRM due to the damping effect of loop resistance, which is not considered in the simulations. The efficiency plot of LV PETT with different C_p and C_s is provided in Fig. 11, which indicates that a lower $I_{r,LLC}$ can lead to a higher overall efficiency.

Fig. 9. The LV PETT prototype.



(a) $C_p = 0.4$mF, $C_s = 0.6$mF (b) $C_p = 0.4$mF, $C_s = 1.1$mF (c) $C_p = 0.4$mF, $C_s = 1.7$mF (d) $C_p = 0.4$mF, $C_s = 2.2$mF (e) $C_p = 4$mF, $C_s = 2.2$mF

Fig. 10. DC link voltages and resonant current of the Cell 1 in LV PETT with different DC link capacitors.

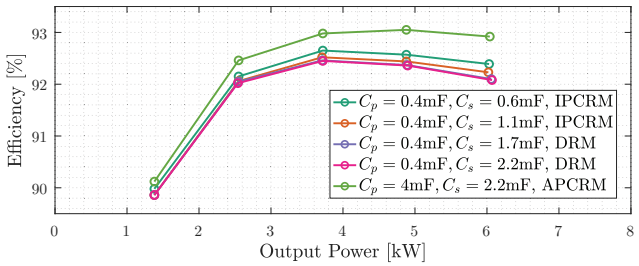


Fig. 11. Efficiency of the LV PETT with different C_p and C_s.

VI. Conclusion

LLC converters with a fixed switching frequency are suitable for the isolated DC/DC stage in ISOP SSTs. When applied in single-phase AC/DC conversion, the LLC converter transfers not only a constant power but also a pulsating power at the double line frequency. The pulsating power transfer behavior of the LLC converter can be modeled by a CLC resonant circuit with a diode. Depending on the CLC resonant frequency, the primary and secondary side DC link capacitors can participate differently in buffering the pulsating power, and the operation of LLC converters may be interrupted due to excessive ripple power transfer. Three different modes are introduced to describe the behavior of LLC converters. The conclusions of this paper are verified by both simulations and experiments, which provide a guideline for the parameter design of similar applications.

References

[1] E. R. Ronan, S. D. Sudhoff, S. F. Glover, and D. L. Galloway, "A power electronic-based distribution transformer," *IEEE Transactions on Power Delivery*, vol. 17, no. 2, pp. 537–543, 2002.

[2] M. Liserre, G. Buticchi, M. Andresen, G. De Carne, L. F. Costa, and Z.-X. Zou, "The smart transformer: Impact on the electric grid and technology challenges," *IEEE Industrial Electronics Magazine*, vol. 10, no. 2, pp. 46–58, 2016.

[3] Y. Xu, J. Zhang, W. Wang, A. Juneja, and S. Bhattacharya, "Energy router: Architectures and functionalities toward energy internet," in *2011 IEEE International Conference on Smart Grid Communications (SmartGridComm)*. IEEE, 2011, pp. 31–36.

[4] M. Steiner and H. Reinold, "Medium frequency topology in railway applications," in *2007 European Conference on Power Electronics and Applications*. IEEE, 2007, pp. 1–10.

[5] D. Dujic, C. Zhao, A. Mester, J. K. Steinke, M. Weiss, S. Lewdeni-Schmid, T. Chaudhuri, and P. Stefanutti, "Power electronic traction transformer-low voltage prototype," *IEEE Transactions on Power Electronics*, vol. 28, no. 12, pp. 5522–5534, 2013.

[6] C. Zhao, D. Dujic, A. Mester, J. K. Steinke, M. Weiss, S. Lewdeni-Schmid, T. Chaudhuri, and P. Stefanutti, "Power electronic traction transformer—medium voltage prototype," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 7, pp. 3257–3268, 2013.

[7] X. She, X. Yu, F. Wang, and A. Q. Huang, "Design and demonstration of a 3.6-kv–120-v/10-kva solid-state transformer for smart grid application," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 3982–3996, 2013.

[8] D. Wang, J. Tian, C. Mao, J. Lu, Y. Duan, J. Qiu, and H. Cai, "A 10-kv/400-v 500-kva electronic power transformer," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 11, pp. 6653–6663, 2016.

[9] J.-Y. Lee, Y.-S. Jeong, and B.-M. Han, "An isolated dc/dc converter using high-frequency unregulated *llc* resonant converter for fuel cell applications," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 7, pp. 2926–2934, 2010.

[10] B. Lu, W. Liu, Y. Liang, F. C. Lee, and J. D. Van Wyk, "Optimal design methodology for llc resonant converter," in *Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition, 2006. APEC'06.* IEEE, 2006, pp. 6–pp.

[11] F. Canales, P. Barbosa, and F. C. Lee, "A wide input voltage and load output variations fixed-frequency zvs dc/dc llc resonant converter for high-power applications," in *Conference Record of the 2002 IEEE Industry Applications Conference. 37th IAS Annual Meeting (Cat. No. 02CH37344)*, vol. 4. IEEE, 2002, pp. 2306–2313.

[12] S. Mukherjee, A. Kumar, and S. Chakraborty, "Comparison of dab and llc dc–dc converters in high-step-down fixed-conversion-ratio (dcx) applications," *IEEE Transactions on Power Electronics*, vol. 36, no. 4, pp. 4383–4398, 2020.

[13] D. Dong, I. Cvetkovic, D. Boroyevich, W. Zhang, R. Wang, and P. Mattavelli, "Grid-interface bidirectional converter for residential dc distribution systems—part one: High-density two-stage topology," *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 1655–1666, 2012.

[14] J. E. Huber and J. W. Kolar, "Analysis and design of fixed voltage transfer ratio dc/dc converter cells for phase-modular solid-state transformers," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*. IEEE, 2015, pp. 5021–5029.

[15] F. Liu, X. Ruan, X. Huang, and Y. Qiu, "Second harmonic current reduction for two-stage inverter with dcx-llc resonant converter in front-end dc–dc converter: Modeling and control," *IEEE Transactions on Power Electronics*, vol. 36, no. 4, pp. 4597–4609, 2020.

[16] J. Wei, H. Feng, and L. Ran, "Multi-dimensional design of dc-link for two-stage solid-state transformer cell considering secondorder harmonic current distribution," *IEEE Transactions on Power Electronics*, 2023.

[17] J. E. Huber, J. Miniböck, and J. W. Kolar, "Generic derivation of dynamic model for half-cycle dcm series resonant converters," *IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 4–7, 2017.